Low Voltage Differential Signaling (LVDS) Evaluation Module (EVM) for Quad Drivers and Receivers

User's Guide

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Introduction

In an effort to help system designers reduce design cycle time, TI offers a series of low-voltage differential signaling (LVDS) evaluation modules (EVMs) designed for analysis of the electrical characteristics of LVDS drivers and receivers. Four unique EVMs are available to evaluate the different classes of LVDS devices offered by TI. Flexibility has been designed into these EVMs so they can be setup in a point-to-point topology (one driver to one receiver), and a multidrop topology (one driver to various receivers). This user's guide identifies each EVM and establishes guidelines on their setup and procedures.

Table 1-1 identifies four EVMs covered by this user's guide.

Table 1-1. EVM Selection Guide

EVM NAME	EVM MARKING	DRIVER	RECEIVER	COMMENTS
SN65LVDS31–32EVM	SLLP101–1	SN65LVDS31	SN65LVDS32	Standard compliant devices
SN65LVDS31–32BEVM	SLLP101–2	SN65LVDS31	SN65LVDS32B	Wide common-mode receivers
SN65LVDM31–32BEVM	SLLP101–3	SN65LVDM31	SN65LVDS32B	Multipoint driver and wide common-mode
SN65LVDS31–33EVM	SLLP101–4	SN65LVDS31	SN65LVDS33	Enhanced wide common-mode receivers

As seen in Table 1-1, various combinations of drivers and receivers are supported by the different EVMs. Both drivers shown in Table 1 are pincompatible, as are the three receivers. The same printed-circuit board (PCB) has been used for all four EVMs, resulting in the same operating instructions included herein.

The SN65LVDS31–32EVM includes the SN65LVDS31 quad driver and SN65LVDS32 quad receiver. The SN65LVDS31 is a TIA/EIA-644 standard compliant LVDS driver. The SN65LVDS32 is a TIA/EIA-644 standard compliant LVDS receiver, which incorporates a passive open-circuit fail-safe detection circuit. The fail-safe circuit included in the SN65LVDS32 includes a pair of 300-kΩ pullup resistors on the bus pins.

The SN65LVDS31–32BEVM includes the SN65LVDS31 quad driver and SN65LVDS32B quad receiver. The SN65LVDS32B is a TIA/EIA-644 standard compliant LVDS receiver with extended common-mode capabilities and an active fail-safe circuit. The SN65LVDS32B receivers operate over a commonmode input voltage range of –2 V to 4.4 V, almost triple the operational rangerequired by the TIA/EIA–644 standard. The SN65LVDS32B's active-failsafe circuit includes a window comparator that provides operation over the entire input common-mode range. This allows for activation even when an external common-mode voltage is applied to the bus. A photograph of the SN65LVDS31–32BEVM is shown in Figure 1-1.

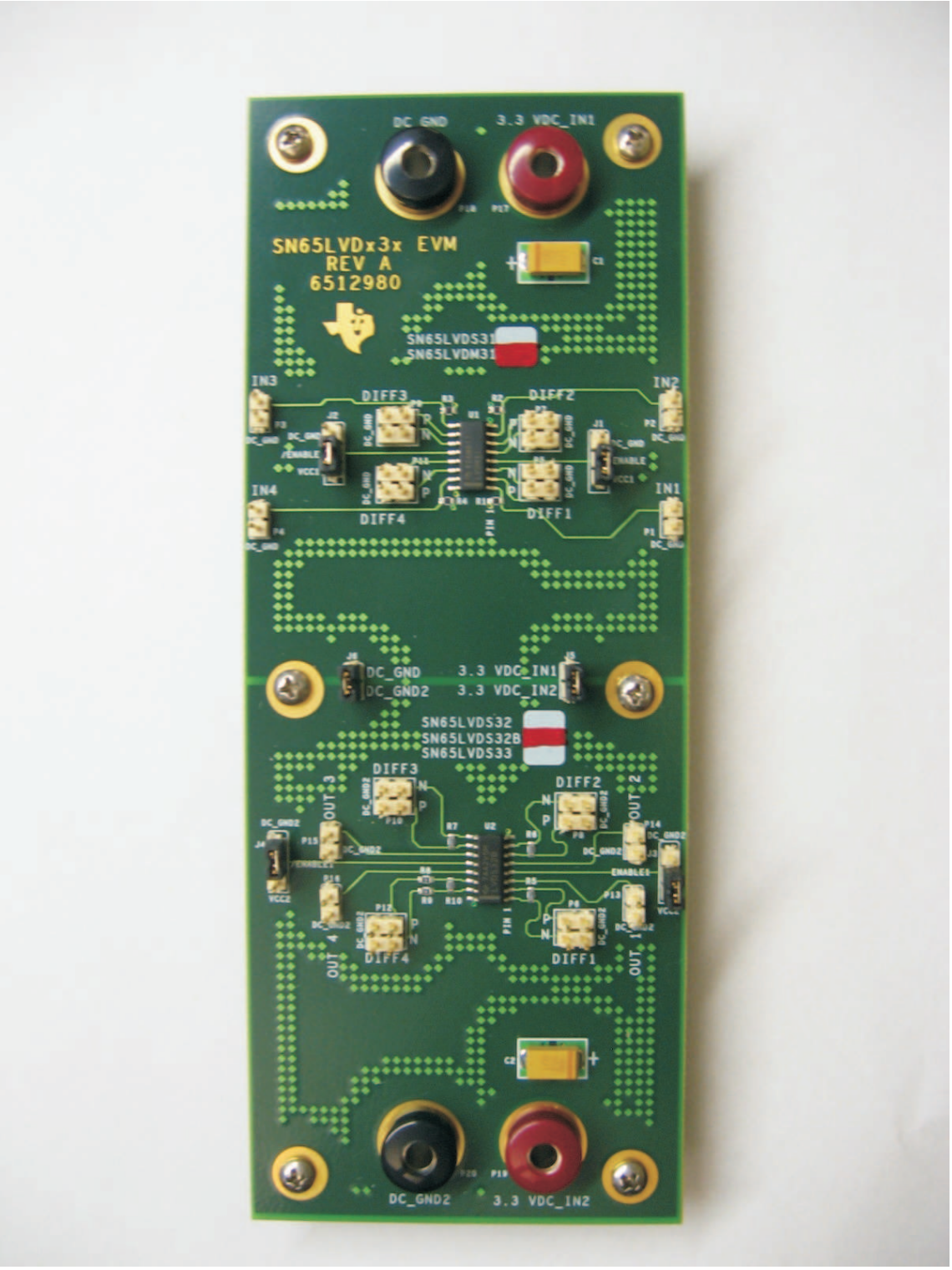


Figure 1-1. SN65LVDS31/32B EVM Printed-Circuit Board

Table 1-2. Jumper Functionality

JUMPER NUMBER	FUNCTION
JMP1, JMP3	Enable pin (active high) High= shunt center pin to pin “V” Low = shunt center pin to pin “G”
JMP2, JMP4	Enable pin (active low) High= shunt center pin to pin “V” Low = shunt center pin to pin “G”
JMP5, JMP6	Ground shifts Installed = common GND and V_{DC} Uninstalled = different GND and V_{DC}
P1, P2, P3, P4	Inputs to SN65LVDM31/SN65LVDS31 driver
P5, P7, P9, P11	Differential outputs of driver
P13, P14, P15, P16	Outputs from SN65LVDS32/SN65LVDS32B/SN65LVDS33 receiver
P6, P8, P10, P12	Differential inputs to receivers

The SN65LVDM31–32BEVM includes the SN65LVDM31 quad driver and SN65LVDS32B quad receiver. The SN65LVDM31 is a multipoint LVDS driver that provides twice the drive current of standard LVDS compliant drivers to allow operation in doubly-terminated (multipoint) topologies, heavily loaded bus lines, or situations where increased noise margin is desired in a design. The SN65LVDM31 complies with the driver requirements of the TIA/EIA–644 standard, except for this doubling of the output current.

The SN65LVDS31-33EVM includes the SN65LVDS31 quad driver and the SN65LVDS33 quad receiver. The SN65LVDS33 is a TIA/EIA-644 standard compliant LVDS receiver. The SN65LVDS33 receiver incorporates the widest common-mode input voltage range of –4 V to 5 V, as well as an active-failsafe circuit that provides operation over the entire input common-mode range. The receiver also provides an input voltage range specification compatible with a 5-V PECL signal. Precise control of the differential input voltage threshold allows for inclusion of 50 mV of input voltage hysteresis to improve noise rejection on slowly changing input signals.

TI also offers a family of LVDS receivers incorporating integrated terminations. This family of devices is recognized by the LVDT string in their part numbers (e.g. SN65LVDT32B and SN65LVDTS33). The SN65LVDT32B and SN65LVDT33B are pin compatible with the SN65LVDS32, the SN65LVDS32B, and the SN65LVDS33. Although not offered on a separate EVM, user evaluation of the SN65LVDT32B and the SN65LVDT33 is possible by user replacement of the receivers included on any of these EVMs. Special EVM operating instructions are included below if evaluations of the SN65LVDT32B and SN65LVDT33 are desired.

Reference will be made throughout the rest of this document to the SN65LVDS31 and the SN65LVDS32. Recalling that the same PCB has been used for all four EVMs, and that EVM operation is identical for all four modules, please read these as a reference to either of the drivers (SN65LVDS31 and SN65LVDM31) and either of the receivers (SN65LVDS32, SN65LVDS32B, and SN65LVDS33). When special instructions are necessary for any of the devices, explicit device references will be included. Likewise, future references to the EVM should be understood to apply to any of the four available evaluation modules.

The EVM has been designed with the driver section on the top half of the board and the receiver section on the bottom half. The installed quad driver is designated U1, while the quad receiver is designated U2. The EVM, as delivered, incorporates 100-Ω termination resistors at the inputs to the four receivers (R5, R6, R7, and R10). If the user desires to evaluate an SN65LVDT32B or an SN65LVDT33, these four termination resistors must be removed.

Jumpers J5 and J6 are included to allow the driver and receiver portions of the board to either share the same power and ground source, or be powered separately for independent device analysis. Removal of these jumpers allows for the introduction of ground shifts between the driver and receiver, demonstrating the wide common-mode operation of the SN65LVDS32B and the SN65LVDS33. Refer to Chapter 5 of this user’s guide for guidelines on operating the EVM with forced ground shifts.

Equipment Required

This chapter provides a list of equipment required for the analysis of low-voltage differential signaling. It also provides a schematic diagram and parts list.

- 3.3-V_{DC} power supply (TEK-PS280 or equivalent)
- A transmission medium from the driver to the receiver (cable or wire)
- A function generator capable of supplying TTL level signaling rates of up to 400 Mbps. Note: 50-Ω source impedance.
- A high-bandwidth oscilloscope, preferably in the 4-GHz range.
- Differential and single-ended oscilloscope probes.

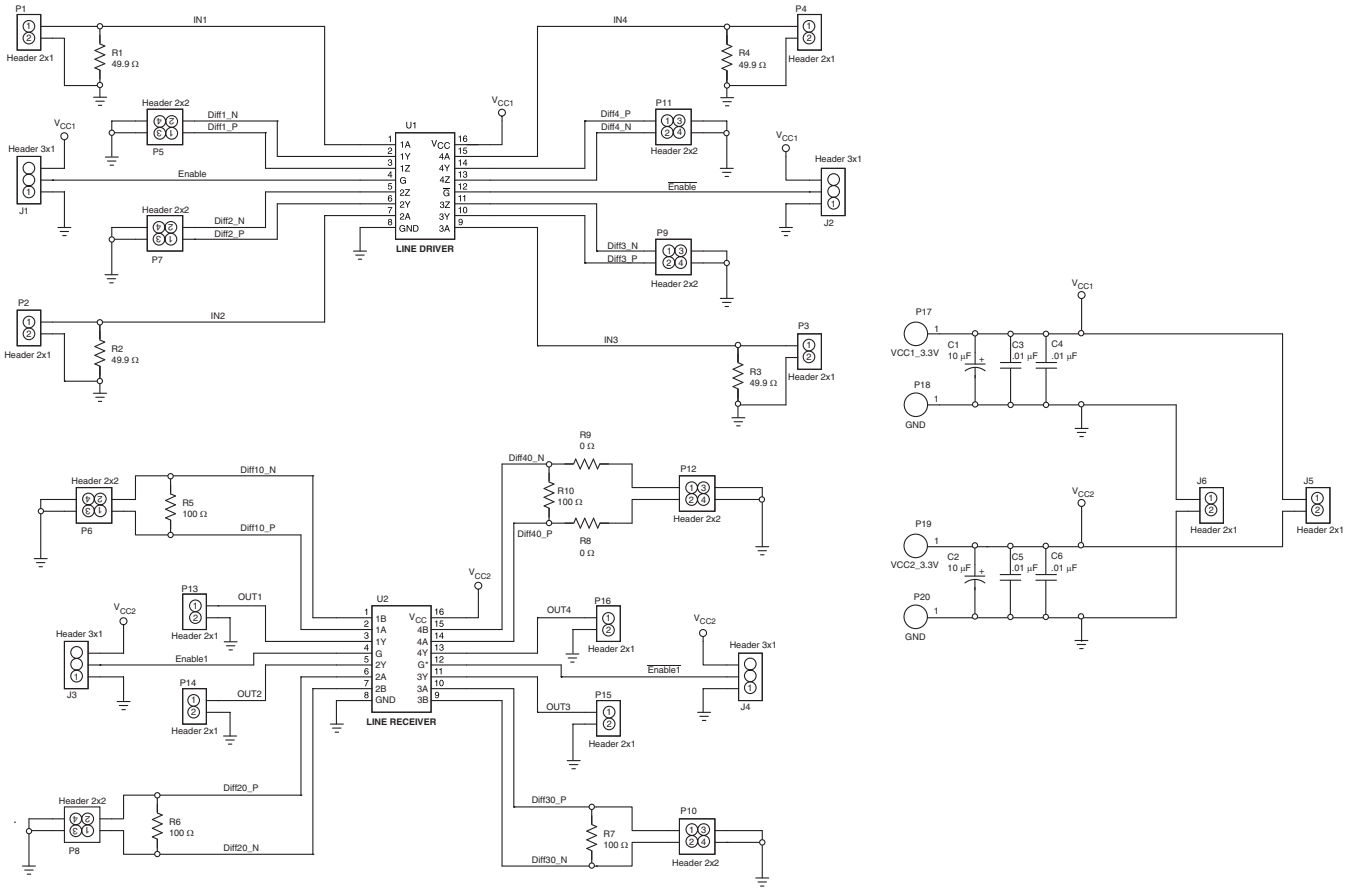


Figure 2-1. EVM Schematic Diagram

	QUAD DRIVERS (U1)		QUAD RECEIVERS (U2)		
EVM PCB	SN65LVDS31	SN65LVDM31	SN65LVDS32	SN65LVDS32B	SN65LVDS33
SLLP101–1	X		X		
SLLP101–2	X			X	
SLLP101–3		X		X	
SLLP101–4	X				X

Table 2-1. Parts List (SLLP101–1, SLLP101–2, SLLP101–3, and SLLP101–4)

ITEM NO.	101-1 QTY.	101-2 QTY.	101-2 QTY.	101-4 QTY.	REF. DES.	DESCRIPTION	PART NUMBER	MFG.
1	2	2	2	2	C1, C2	Capacitor, 10.0 µF, tantalum	PCT3106TR–ND	Digi-Key
2	4	4	4	4	C3.C6	Capacitor, 0.01 µF	C0805C103K5RAC	Mallory
3	4	4	4	4	J1.J4	3-Position male post with shorting jumpers	68001–236/65474–010	Berg Elec
4	2	2	2	2	J5, J6	2-Position male post with shorting jumpers	68001–236/65474–010	Berg Elec
5	4	4	4	4	P1–P4	Connectors, SMA, edgemount	528–S0101	Allied
6	8	8	8	8	P5–P12	2-Position female post, SIP	905–3090	Allied
7	4	4	4	4	P13–P16	2-Position male post	518–1052	Allied
8	4	4	4	4	P17–P20	Banana jack connectors, female	528–0172	Allied
9	4	4	4	4	R1–R4	Resistors, 51 Ω, 805 PK	P51GCT–ND	Digi-Key
10	3	3	3	3	R5–R7	Resistors, 100 Ω, 603 PK	P100GCT–ND	Digi-Key
11	2	2	2	2	R8–R9	Resistors, 0 Ω, 603 (optional: 45.3 Ω)	P0.0GCT–ND	Digi-Key
12	1	1	1	1	R10	Resistors, 100 Ω, 603 (optional: 10.22 Ω)	P100GCT–ND	Digi-Key
13	1	0	1	1	U1	IC, Quad driver	SN65LVDS31D	TI
14	0	1	0	0	U1	IC, Quad driver	SN65LVDM31D	TI
15	0	0	0	1	U2	IC, Quad receiver	SN65LVDS32D	TI
16	0	1	1	0	U2	IC, Quad receiver	SN65LVDS32BD	TI
17	1	0	0	0	U2	IC, Quad receiver	SN65LVDS33D	TI
18	6	6	6	6	J1–J6	Jumper short, (use with items 3 and 4)	65474–010	Allied

Point-to-Point Transmission

This chapter shows the setup for point-to-point transmission.

The point-to-point configuration with one driver transmitting to one receiver is a typical transmission scheme. The transmission quality is superior, since there are no stubs and few discontinuities on the bus to degrade the signal. Note that the required 100-Ω termination resistor (R5) is already in place across the differential pair at the input of the receiver (U2).

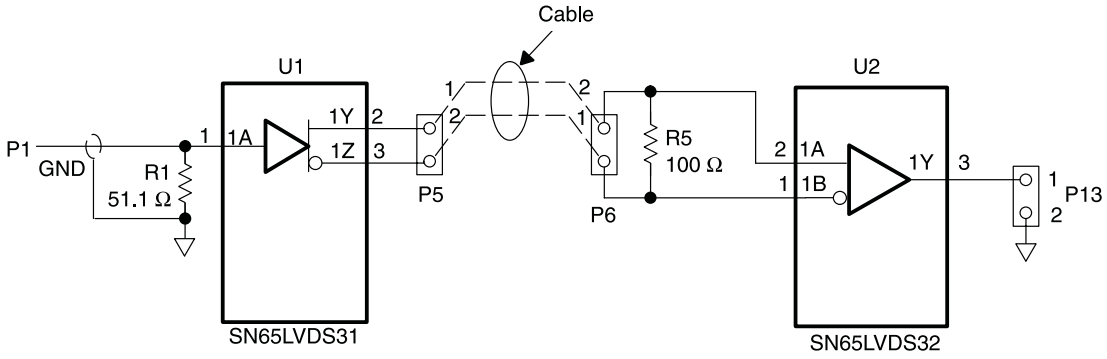


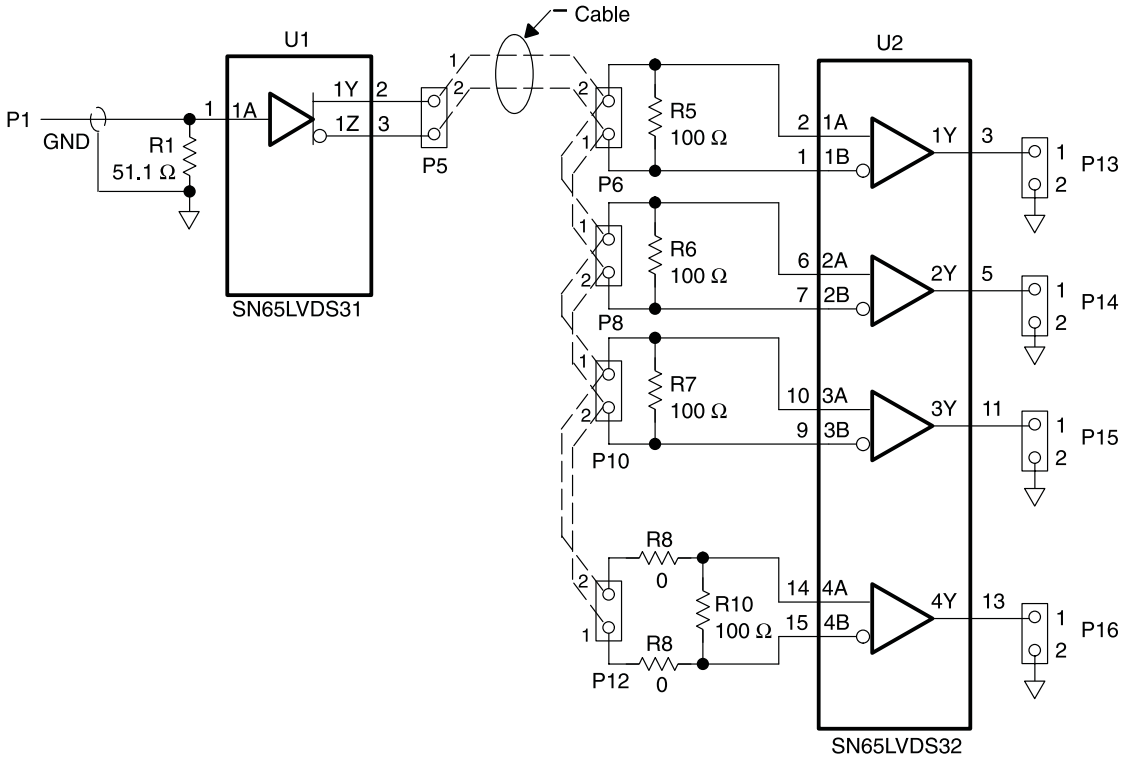
Figure 3-1. Point-to-Point Schematic Diagram

Multidrop Transmission

This chapter shows the setup for multidrop transmission.

The multidrop configuration with one driver transmitting to several receivers may be implemented as shown in Figure 4-1. In this application, only a single 100-Ω termination resistor is required across the differential pair at the inputs of the last receiver. Termination resistors at the inputs of the middle receivers in the configuration must be removed. To minimize reflections, line length between receivers should be kept as short as possible. Stub length should also be kept to a minimum. On the EVM, stub length is approximately 3 cm.

For a complete discussion of this configuration with up to 36 receivers, consult the TI application note, *LVDS Multidrop Connections*, literature number SLLA054.



Termination resistors R5, R6, and R7 must be removed.

Figure 4-1. Multidrop Schematic Diagram

Evaluation of Receiver Operation During Ground Shifts

This chapter explains how to introduce ground shifts between the driver and the receiver to test the receiver operation over its full common-mode voltage input range.

LVDS driver outputs have an offset voltage of approximately 1.2 V. The SN65LVDS32 receiver complies with the TIA/EIA–644 standard. It correctly detects the logic level of the input signal when 100 mV of differential signal is present at its input, and the input common-mode voltage is between 0 V and 2.4 V. (The actual input common-mode range is also dependent upon the differential input voltage; see recommended operating condition in the data sheet for dependency.) The SN65LVDS32B provides operation over an input common-mode voltage range of –2 V to 4.4 V, whereas the SN65LVDS33 extends the operation to an input common-mode voltage range of –4 V to 5 V. Both the above mentioned receivers are equipped to correctly detect the input state with a 50-mV differential signal at its input.

input state with a 50-mV differential signal at its input. All EVMs can be used to evaluate the receiver operation in the presence of ground shifts between the driver and receiver. Testing of EVMs that host a SN65LVDS32B or a SN65LVDS33 will demonstrate the extended range operation of these devices.

Perform the following steps to demonstrate operation during ground shifts.

1. Remove the jumper shorts on jumpers J5 and J6.
   Three dc power supplies will be used for this test.
2. Using the first power supply (PS1), apply 3.3-V power to the driver section of the EVM (via connectors P17 and P18).
3. Using the second power supply (PS2), apply 3.3-V power to the receiver section of the EVM (via connectors P19 and P20).
4. Tie the third power supply (PS3) between the grounds of PS1 and PS2.
5. Initially set PS3 to 0 V.
6. Input a test signal to the driver while monitoring the output of a receiver (refer to Chapter 3, Point-to-Point Transmission).
7. Vary the ground shift between the driver and the receiver via adjustments to PS3.

A test setup is shown in Figure 5-1.

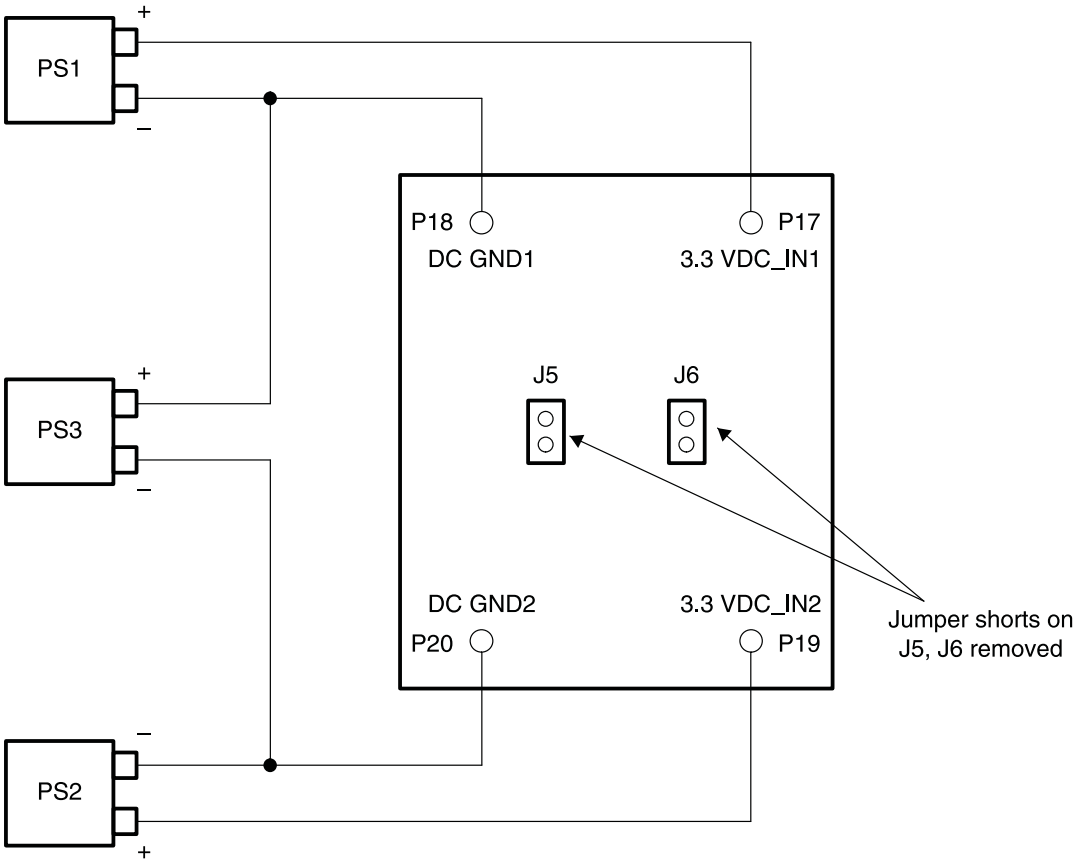


Figure 5-1. Test Setup

The Application of TIA/EIA-422 Data to an LVDS Receiver

This chapter explains the application of TIA/EIA-422 data into an LVDS receiver.

The fourth channel of the receiver (4A and 4B) configured with the resistor divider network of R8, R9, and R10 may be used for the evaluation of TIA/EIA-422 data applied to an LVDS receiver. TIA/EIA-422 signaling voltage levels are adjusted to appropriate LVDS input voltage levels by installing 45-Ω resistors in the spaces provided for R8 and R9 on the evaluation board. The 100-Ω resistor (R10) must then be removed and replaced with a 10-Ω resistor as shown in Figure 6-1. This resistor divider network now comprises a total differential load of 100 Ω to match the characteristic impedance of a common transmission line, and reduces the TIA/EIA-422 maximum differential signal amplitude from 6 V to an appropriate 600 mV.

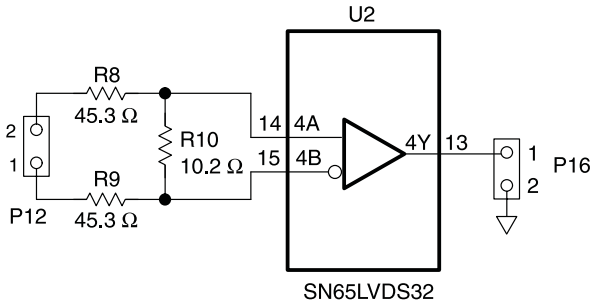


Figure 6-1. TIA/EIA-422 Data to an LVDS Receiver Schematic

References

This chapter contains a list of LVDS literature available.

There is a wide selection of the LVDS devices and related applications materials available to assist in the design and development of LVDS interfaces. This information is located at www.ti.com/sc/datatran. Input LVDS into the search tool or enter the part number of a specific device to obtain additional information.

1. LVDS Designer's Notes (literature number SLLA014A)
2. Reducing EMI With Low Voltage Differential Signaling (literature number SLLA030)
3. The Active Fail-Safe Feature of the SN65LVDS32B (literature number SLLA082)
4. A statistical Survey of Common-Mode Noise (literature number SLLA057)
5. Measuring Crosstalk in LVDS Systems (literature number SLLA064)
6. Interface Circuits for TIA/EIA–644 (LVDS) (literature number SLLA038)
7. Transmission at 200 Mbps in VME Card Cage Using LVDM (literature number SLLA088)
8. Performance of LVDS With Different Cables (literature number SLLA053)
9. LVDS Multidrop Connections (literature number SLLA054)

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