TLK6002 Dual-Channel, 0.47-Gbps to 6.25-Gbps, Multi-Rate Transceiver Evaluation Module

This user's guide describes the usage and construction of the TLK6002 evaluation module (EVM). This document provides guidance on proper use of the EVM by showing some device configurations and test modes. In addition, design, layout, and schematic information is provided to the user. Users can use information in this guide to choose the optimal design methods and materials when designing a complete system.

WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case, users at their expense are required to take whatever measures may be required to correct this interference.

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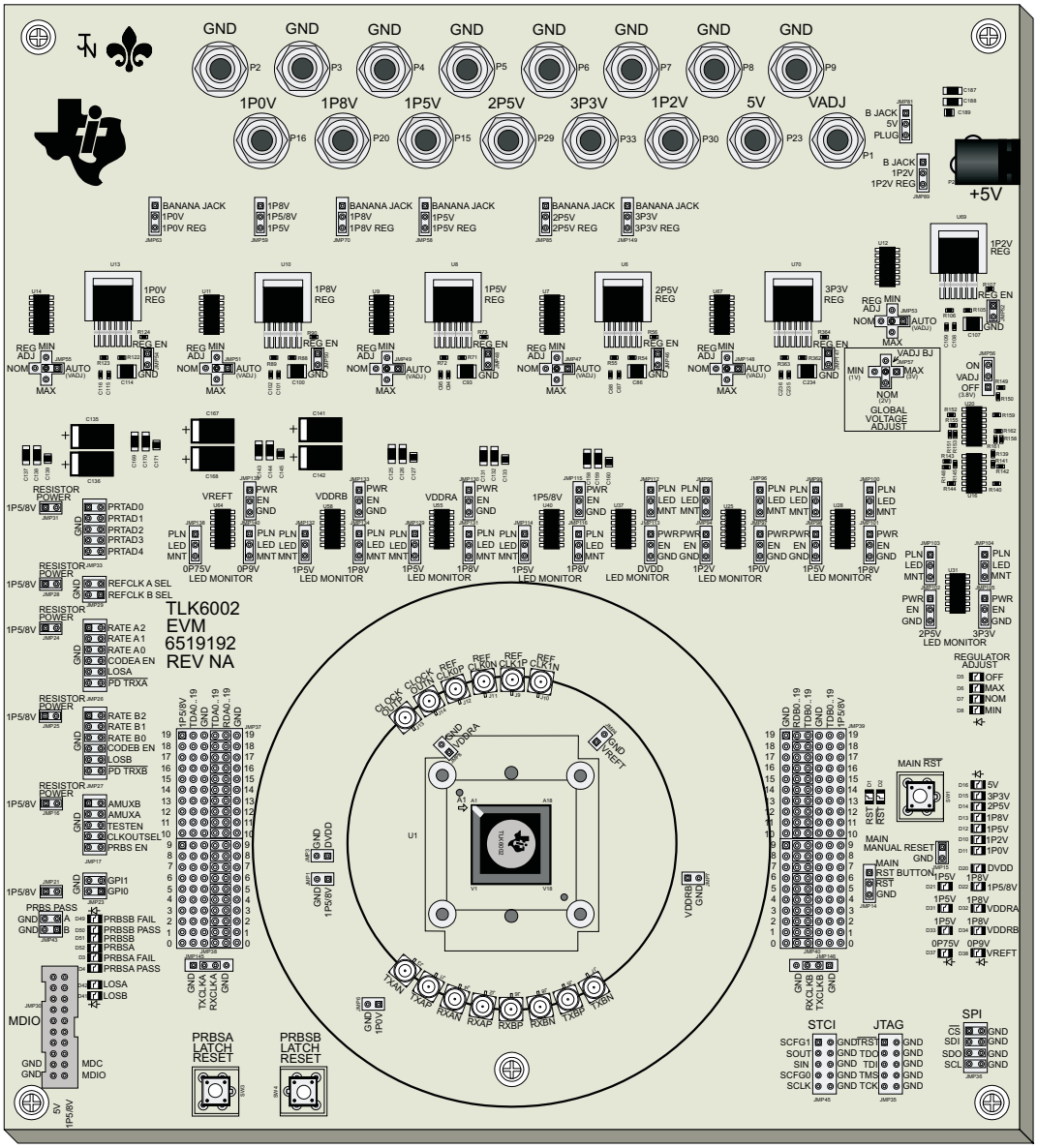
1 Introduction



The Texas Instruments TLK6002 SERDES evaluation module (EVM) board is used to evaluate the functionality and the performance of the TLK6002 Dual-Channel, Multi-Rate Transceiver device in a 324-ball PBGA package. The TLK6002 is a multi-gigabit transceiver intended for use in ultra-high-speed bidirectional point-to-point data transmission systems such as base station RRH (Remote Radio Head) applications as well as any other high-speed application. All CPRI and OBSAI data rates of 0.6144, 0.768, 1.2288, 1.536, 2.4576, 3.072, 4.9152, and 6.144 Gbps are supported using a single, fixed-reference clock frequency of either 122.88 MHz or 153.6 MHz. Non-CPRI or OBSAI serial data rates between 0.470 Gbps and 6.25 Gbps are also supported. Each channel of the TLK6002 can be operated from a single, shared-reference clock or independently from separate reference clocks at different frequencies. A CIPRI/OBSAI Automated Rate Sense (ARS) Function has been included to help facilitate the determination of the incoming CPRI/OBSAI serial link rate per channel.

Other features of the TLK6002 include an integrated Latency Measurement function, PRBS (2^7-1), (2^{23}-1), (2^{31}-1), and High, Low, and Mixed CRPAT Generation and Verification for self-test, system-level support. Programmable Serial Side output swing and Serial Side Dual Tap Transmit De-emphasis as well as Receive Adaptive Equalization allow extended backplane reach and transmission line optimization.

SERDES operation and 8B/10B Encoding and Decoding for 20-bit and 16-bit plus control bits are supported allowing use of a lower cost FPGA solution compared to a FPGA with integrated high-speed transceivers and built-in SERDES functionality. Latency/depth configurable transmit and receive FIFOs and loss of signal (LOS) detection of ≤ 75 mVdfpp are just a few of the other features supported in this device.

Configuration of the TLK6002 on a per-channel basis is available by way of accessing a register space of control bits available through a two-wire access port called the Management Data Input/Output (MDIO) interface as defined in Clause 22 of the IEEE 802.3 Ethernet Specification.(1)

The TLK6002EVM board can be run from a single, 5-V power supply or 5-Vdc transformer. All voltages needed are regulated down through onboard LDO regulators which can be adjusted to the appropriate minimum, nominal, and maximum values through a single jumper location.

Voltage monitor circuits with LEDs are included on all voltage rails for easy debugging and identification of valid power rails.

All data I/O signals are broken out to connectors for easy and rapid prototyping. All control signals are easily controlled through shunts on header blocks.

PRBS latch circuits have been added to aid in PRBS BER tests.

The EVM board functionality can be easily expanded through the use of the three peripheral ports. Optical modules, clock oscillator generators, and FPGAs are just a few possible uses for these ports.

2 EVM PCB and High-Speed Design Considerations

The board can be used to evaluate device parameters in addition to acting as a guide for high-speed board layout. As the frequency of operation increases, the board designer must take special care to ensure that the highest signal integrity is maintained. To achieve this, the board's impedance is controlled to 50 Ω for both the high-speed differential serial and low-speed parallel data and clock connections. Vias are minimized and, when necessary, are designed to minimize impedance discontinuities along the transmission line. Because the board contains both serial and parallel transmission lines, care was taken also to control trace length mismatch (board skew) to less than ±0.5 mil.

Overall, the board layout is designed and optimized to support high-speed operation. Thus, understanding impedance control and transmission line effects are crucial when designing high-speed boards. Some of the advanced features offered by this board include:

- PCB (printed-circuit board) is designed for optimal high-speed signal integrity.
- SMP and parallel header fixtures are easily connected to test equipment.
- All input/output signals are accessible for rapid prototyping.
- The entire board can be powered from a single, 5-V power supply where the power planes can be supplied through onboard regulators or through separate banana jacks for isolation.
- Onboard capacitors provide ac coupling of high-speed transmit and receive signals.
- External parallel loop-back function can be achieved easily using simple 0.1-inch jumpers.
- Entire board can operate from a single 5-V power supply or from individual power supplies.
- Voltage monitoring LED circuits provide quick indication that the voltage is within specification.

(1) The MDIO register map is located within the *TLK6002, Dual-Channel 0.47Gbps to 6.25Gbps Multi-Rate Transceiver* data sheet.

3 TLK6002 EVM Kit Contents

The TLK6002 EVM kit contains the following:

- TLK6002 EVM board
- TLK6002 EVM User's Guide (this document)
- *TLK6002, Dual-Channel 0.47-Gbps to 6.25-Gbps Multi-Rate Transceiver* data sheet
- MDIO Interface EVM
- MDIO Interface EVM documentation
- RS-232 cable
- 20-conductor MDIO ribbon cable
- CD-ROM containing MDIO Sonic Software and User Guides
- 14 3-foot SMA-to-SMP cables
- 4 1-foot SMP-to-SMP cables
- 5-Vdc transformer power supply

4 Power

The TLK6002EVM can be operated off of a single 5-V power supply using the onboard linear dropout voltage regulators to generate the voltages required to correctly operate the TLK6002, 1-V, 1.5-V, and 1.8-V power rails. Additional 1.2-V, 2.5-V, and 3.3-V supplies have been added to support additional circuitry on the EVM board and to provide voltage to the peripheral ports to minimize the amount of power circuitry needed on those boards. Banana jacks and selection headers allow external laboratory power supplies to be used instead of the onboard LDO regulators. The LDO regulators used on the EVM are TI's TPS74401 (or TPS74201 depending on available stock at the PCB assembly shop) and are adjustable using a resistor divider between the output and a feedback pin. Each regulator has been set to provide the appropriate minimum, nominal, or maximum voltage per the data sheet limits at its output when appropriately set. However, no sense lines are connected to the plane near the DUT to compensate for resistive loss through the board. This loss must be less than 5 mV to 10 mV and not affect the operation of the TLK6002 device. If more information on the use of these regulators is desired, consult the regulator data sheets found at www.ti.com.

To modify your power supply configuration between either all individual supplies, all onboard regulators, or a combination of both, simply change the jumper position on the appropriate power supply headers (JMP58, JMP63, JMP70, JMP85, JMP89, and JMP149) selecting either the BANANA JACK or the REG pin in combination with the center pin. The following figure shows how to use the onboard regulators for the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V supply rails, and an individual power supply connected to the 1-V banana jack (P16) and 2.5-V banana jack (P29). The 5-V power supply is required for operation of the LEDs on this board even if you are not using the onboard voltage regulators and can be provided from a laboratory power supply through the banana jack (P1) or through the supplied 5-Vdc transformer. Moving the jumper location on JMP81 changes the 5-V power supply source from the banana jack or supplied 5-Vdc transformer.

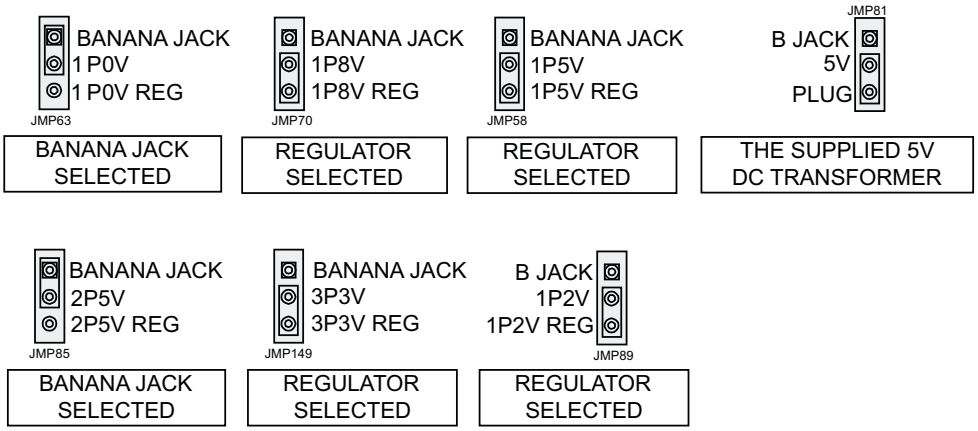


Figure 1. TLK6002 EVM Power Source Selection Example

Several power supplies such as VDDQA, VDDQB, VDDRA, VDDRB, VDDO1, VDDO2, and VDDO3 can be operated off of either 1.5 V or 1.8 V depending on your specific setup. The EVM is designed to allow either of these voltages to be selected for use with the previously mentioned TLK6002 supply rails, but only allow either 1.5 V or 1.8 V to be selected at a time without some board modifications. Selection between 1.5 V and 1.8 V is performed by moving the jumper between the center pin and the respective 1p5V and 1p8V pins of JMP59.

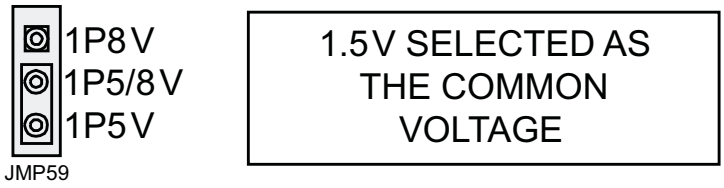


Figure 2. TLK6002 EVM 1p5/8V Voltage Source Selection

Each TPS74x01 LDO has a voltage margin adjust circuit connected to the voltage adjustment feedback path to select among the minimum, nominal, and maximum output voltage for that particular voltage node. To adjust the voltage margin, place the shunt between the center pin of the jumper shaped like a "+" located next to the regulator and the desired MIN, NOM, or MAX value. A common voltage margin control circuit is also added that adjusts all the regulators to their minimum, nominal, or maximum values through a single jumper selection. In order to have the regulator respond to these common control signals, the selection on the regulator's margin control header needs to have the center pin and the AUTO pin selected.

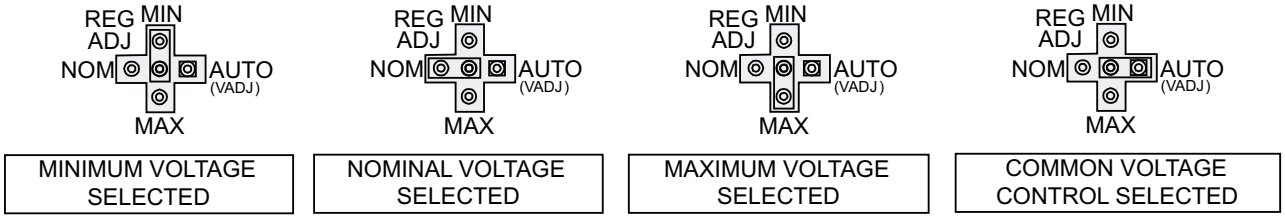


Figure 3. TLK6002 EVM Regulator Voltage Margin Selection

The TLK6002EVM comes configured to allow for common voltage margin selection via JMP57, which is set to a Nominal setting. To globally control the margin of all regulators, place the shunt between the center pin and the appropriate MIN, NOM, or MAX pins. The adjustment circuit consists of a several resistor dividers and some voltage window comparator circuits. When the minimum voltage is selected, 1 V is input to the comparator circuit. When the nominal voltage is selected, 2 V is input to the comparator circuit. When the maximum voltage is selected, 3 V is input to the comparator circuit. The output of the comparator circuits feeds some digital logic and engages the appropriate FETs located in each of the LDO feedback adjustment circuits. This output places additional resistors in parallel with the defaulted minimum value resistors creating the Thevenin equivalent resistance in the feedback voltage divider needed to adjust the output voltage. Precision 0.1% resistors have been used in these circuits to provide accurate output voltages, but due to manufacturing tolerances the actual output voltage may be less than 10 mV off the theoretical and calculated value.

Using this voltage window approach eliminates the need for a programmable device such as a microcontroller to adjust the LDO margins and allows for easy sweeps using a single shunt or an external power supply.

A fourth selection on JMP57 labeled VADJ BJ has been added that places the voltage input to the window comparator circuit that feeds the voltage supplied on the VADJ banana jack (P1) and allows for easy automated testing sweeps to be performed by controlling this voltage to 1 V, 2 V, and 3 V. The voltage window limits are set to ±0.25 V with respect to the mentioned control voltages. For example, the minimum voltage window is 0.75 V to 1.25 V, the nominal voltage window is set to 1.75 V to 2.25 V, and the maximum voltage window is set to 2.75 V to 3.25 V. If the voltage on the VADJ line does not fall between one of these valid windows, no FETs is selected in the regulator's feedback circuit and the regulator defaults to the minimum output voltage.

The regulators can also be disabled using this voltage window detect circuit by placing the shunt between the center pin and the OFF pin of JMP56. This places 3.8 V on the input to the voltage window comparator circuit which is set for 3.75 to 4.0V and turn on a FET connected to the Enable pin of the regulators. 3.8V is used because it is within the window and the voltage reference chip used produces a 4.096-V voltage and 4 V may be too close to the high limits established by this reference chip. The placement of the shunt on JMP57 is irrelevant if the OFF position on JMP56 is selected because it overrides any min, nom, max setting. See the Power Regulator Min/Nom/Max Adjustment page 16 of the TLK6002EVM schematics for more information on how this circuitry is connected.

Any combination of local regulator control, global regulator control, and external power supplies can be implemented through the appropriate configuration of the various headers.

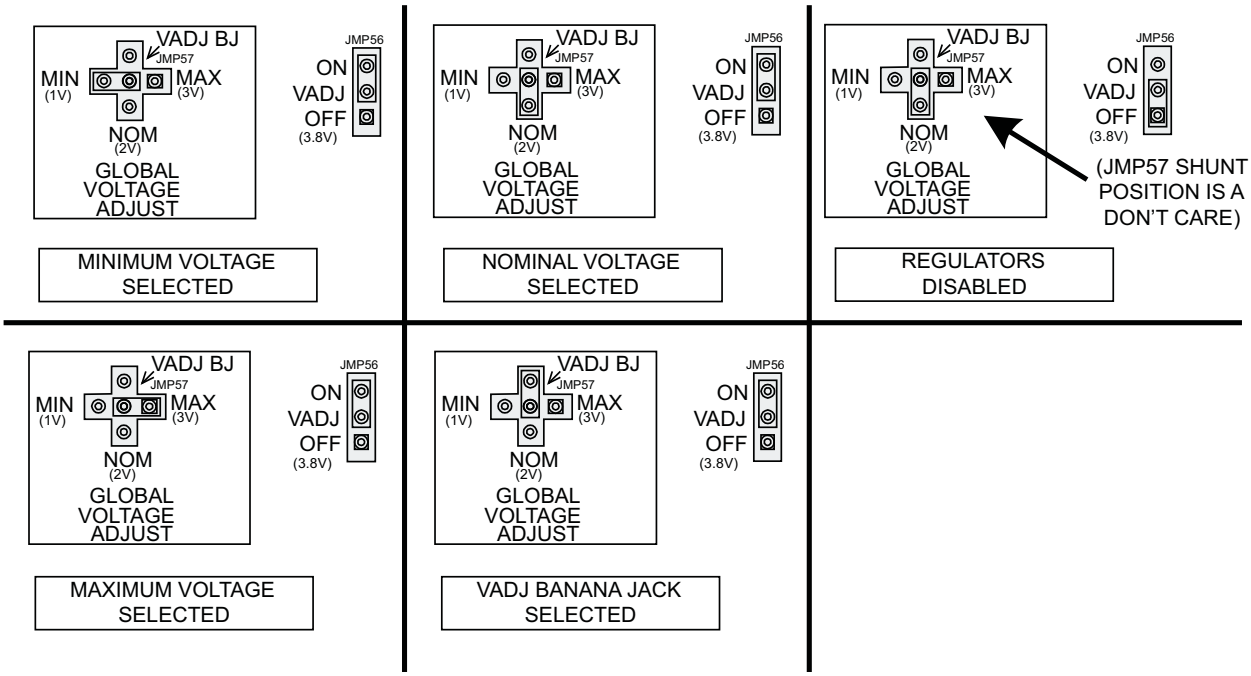


Figure 4. TLK6002 EVM Global Regulator Margin Selection

A large 1210 0-Ω resistor has been installed at the voltage entrance point of each power plane and can be replaced with a ferrite bead of an appropriate value depending upon the desired data rate if desired. See the Power Distribution page 18 of the TLK6002EVM schematics for more specific information on how all the power planes are connected and sourced from either the banana jacks or regulators.

The VREFT plane is sourced through a voltage divider providing half of the voltage on the 1p5/8V plane. The VDDQA/B, VDDRA/B, and VDDO1/2/3 power pins of the TLK6002 can be operated off of either 1.5 V or 1.8 V with VREFTA/B being half of whatever voltage is on the VDDQA/B pins which is on the 1p5/8V plane. The VREFT plane can be powered through the plane monitoring header (JMP4) and removing the 0-Ω resistor (R181), although this is not recommended. A separate VDDRA and VDDRB plane has been added as no relationship exists between the VDDRA/B pin and the VDDQA/B pins; however, the VDDRA/B planes are sourced through 0-Ω resistor (R176 and R177) from the voltage on the 1p5/8V plane that provides power to the VDDQA/B and VDDO1/2/3 pins. These resistors can be replaced with a ferrite bead or removed completely and an external supply can be connected to the VDDRA header (JMP8) and VDDRB header (JMP7) in the case different voltages are desired on the two planes.

Furthermore, for more accurate current readings, the PULLUP_EN jumpers on all control pin headers can be removed, quickly disconnecting the pullup resistors from the voltage plane. However, the removal of the PULLUP_EN jumpers also requires manual high/low control of every control pins.

5 Power Monitoring LEDs

Each plane of the TLK6002EVM has been equipped with a voltage monitoring circuit that monitors the voltage on the plane and lights the LEDs when the voltage is within the minimum/maximum data sheet limits for that power supply. A precision TI voltage reference chip is used along with 0.1% precision resistors setting minimum and maximum reference levels providing a detection circuit that is accurate to approximately ±10 mV. The LEDs serve as a basic indication that the status of power on the board is within the acceptable minimum/maximum limits given in the data sheet, and not as a precise measurement tool as some LED circuits may turn off at slightly different voltages when approaching the limits due to the manufacturing tolerances and available component values.

The voltage monitor circuits can also be bypassed, and the LEDs driven directly from the voltage on the individual planes such as when performing voltage tolerance tests. Instead of being lit only when the voltage on the plane is within the minimum/maximum range, the LED is lit when the voltage is greater than the voltage needed to turn on the LED drive circuit's NPN transistor, allowing current to flow, and the LED to be lit from the 5-V source. In the Direct Connect mode, the base resistors have been given extra margin to allow the LEDs to light when the voltage on the plane is a little below the minimum limit of that supply in order to provide a LED indicator of power on the plane during voltage tolerance tests near the lower supply limits.

Placing the jumper on the PWR side of the Voltage Monitor Enable/Disable header connects the power plane to the input of the voltage monitoring circuit. This input is high impedance and does not load down the power source providing the voltage to the plane.

Placing the header on the MNT side of the LED Monitor/Direct Connect selection header connects the LED drive circuit to the output of the voltage monitor circuit causing the LED to be lit only when the voltage is within the acceptable range.

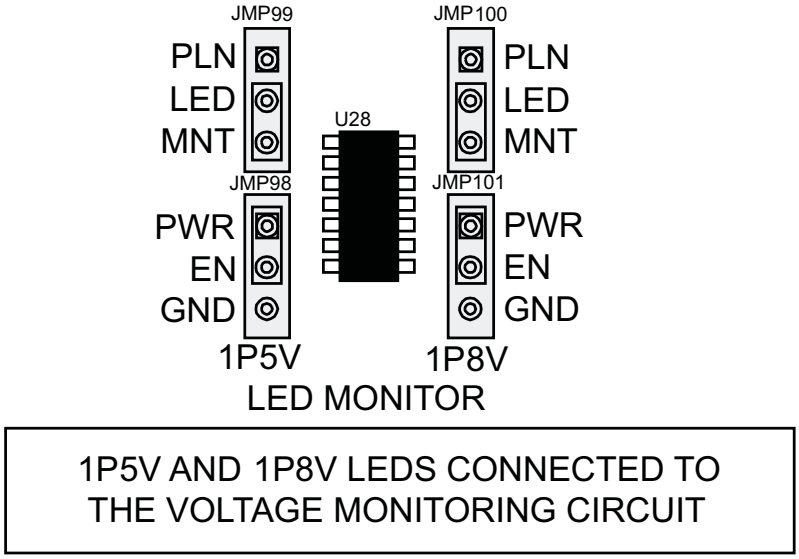


Figure 5. TLK6002 EVM Voltage Monitor LED Enabled Example

Placing the jumper on the GND side of the Voltage Monitor Enable/Disable header disconnects the power plane to the input of the voltage monitoring circuit and instead ties the input to GND. This prevents the output of the voltage monitoring circuit from floating and possibly causing the LED to flicker during contact with the board.

Placing the jumper on the MNT side of the LED Monitor/Direct Connect selection header connects the LED drive circuit to the output of the voltage monitor circuit causing the LED to be off because the voltage monitor circuit senses that the plane voltage is GND, which is less than the acceptable plane voltage.

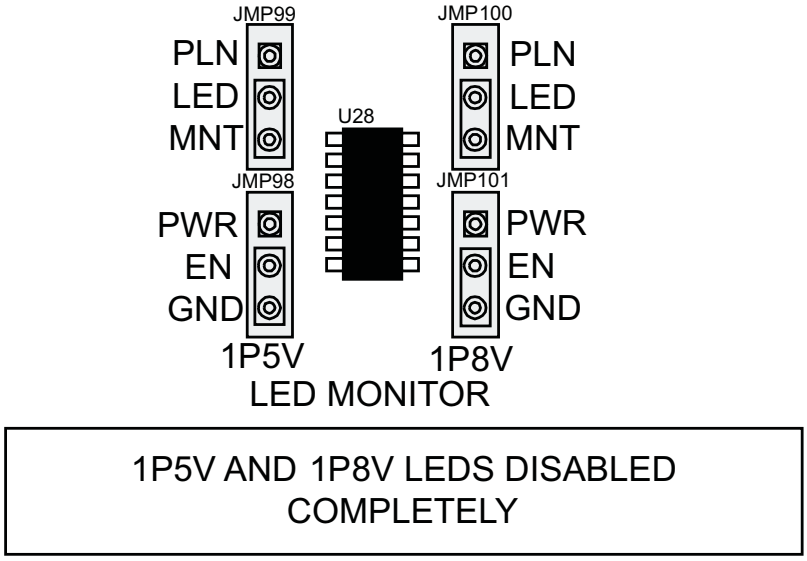


Figure 6. TLK6002 EVM Voltage Monitor LED Disabled Example

Placing the jumper on the DIRECT side of the LED Monitor/Direct Connect selection header connects the LED drive circuit to the power plane itself, causing the LED to be lit when the voltage is great enough to cause current to flow through the LED drive circuit. This LED configuration has been designed to be used when pushing the lower limits of the acceptable voltage range to continue to provide an indicator that power is on the plane, however, without regards to what that voltage may actually be.

The jumper on the Voltage Monitor Enable/Disable header does not matter as this is only the input to the voltage monitor circuit, which has been bypassed when the LED drive circuit is connected directly to the power plane itself.

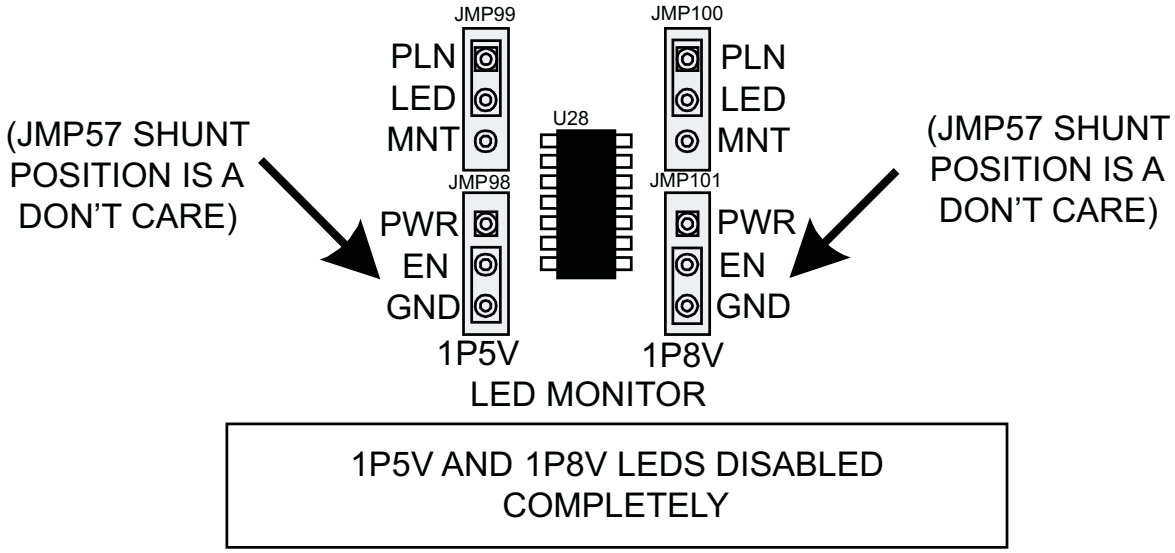


Figure 7. TLK6002 EVM Voltage Monitor LED Connected Directly to Plane Example

6 Control and Output Status Signals

All of the external control and status pins on the TLK6002EVM have been consolidated to a single location on the board and broken out into several header blocks for easier reference. LEDs have been added to the LOSA, LOSB, PRBS_PASSA, and PRBS_PASSB lines in addition to the headers for scope probes, to allow easy monitoring of the High/Low value on the line. The LED is ON when the line is a Logic High, and the LED is OFF when the line is a logic low. If the line is toggling, a dimming of the LED may be observed as the LED is pulsing on and off relative to the activity on the line.

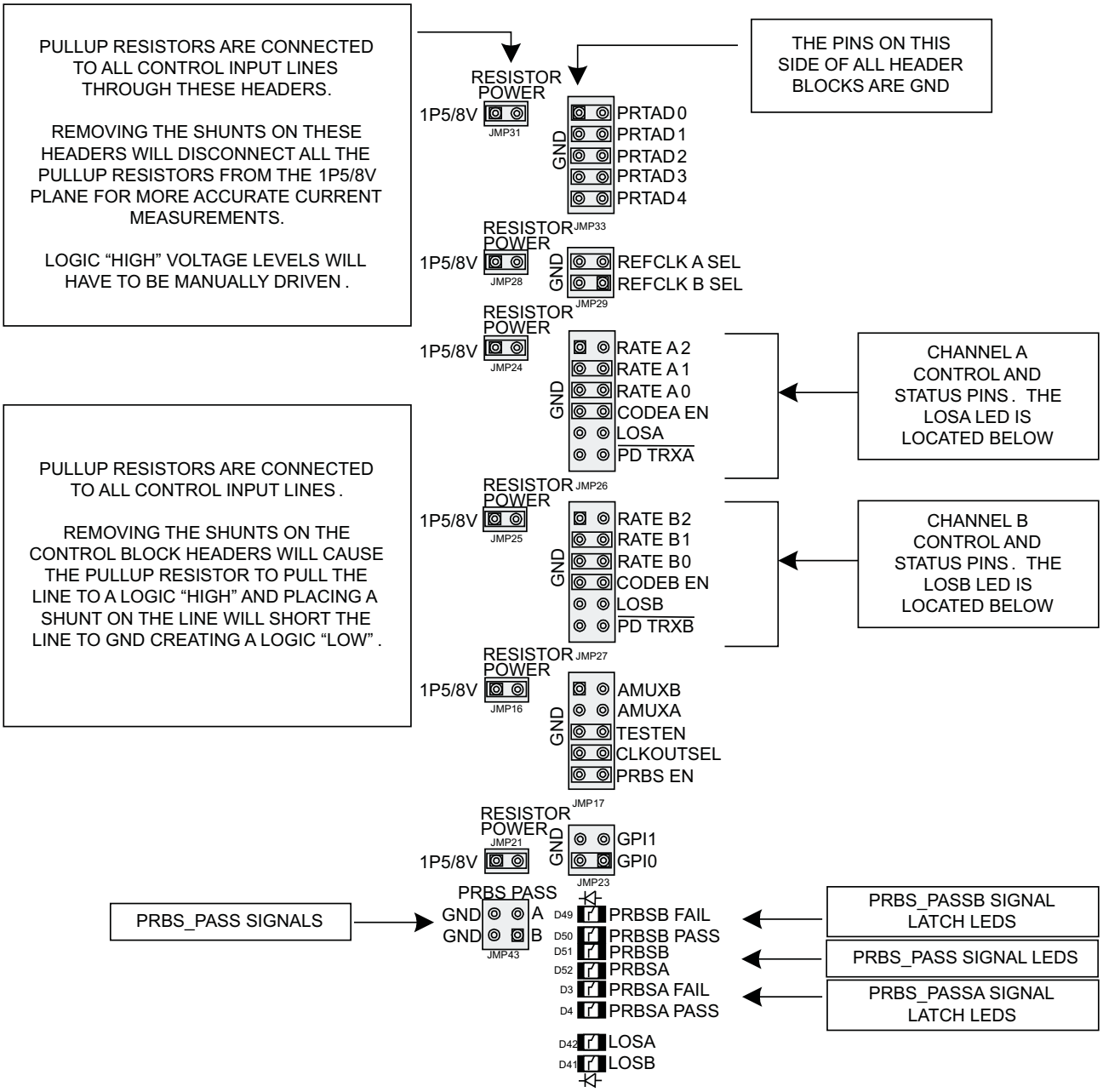


Figure 8. Control Connectors (JMP17, JMP23, JMP26, JMP27, JMP29, JMP33, JMP43)

6.1 Control Signal and Status Pin Descriptions:

PRTAD[4:0]: Port Address. Used to select the Port ID.

PRTAD[4:1] selects the device port address. TLK6002 has two different PHY addresses (ports). Selecting a unique PRTAD[4:1] per TLK6002 device allows 16 TLK6002 devices per MDIO bus. Each channel can be accessed by setting the appropriate port address field within the serial interface protocol transaction.

TLK6002 responds if the four MSBs of the inband PHY address field on MDIO protocol (PA[4:1]) matches PRTAD[4:1]. The LSB of PHY address field (PA[0]) determines which channel/port within TLK6002 to respond to.

PRTAD[0] is not used functionally, but is present for device testability and compatibility with other devices in the family of products.

Channel A responds to port address 0 within the block of two port addresses.

Channel B responds to port address 1 within the block of two port addresses.

PRTAD[0] must be grounded on the application board.

The PRTAD[3] pin in application mode must be biased with a pullup or pulldown resistor (or allow for an isolation mechanism from the onboard driver) and not connected directly to a power or ground plane. The application board allows the flexibility of easily reworking the PRTAD[3] signal to a high level if the device debug is necessary (by including an uninstalled resistor to VDDO1).

REFCLK_A_SEL: Reference Clock Select Channel A. This input, when low, selects REFCLK_0_P/N as the clock reference to Channel A SERDES macro. When high, REFCLK_1_P/N is selected as the clock reference to Channel A SERDES macro. If software control is desired (register bit 0.1), this input signal must be tied low. See Figure 4, “TLK6002 Reference Clock/Output Clock Architecture” of the *TLK6002, Dual-Channel 0.47Gbps to 6.25Gbps Multi-Rate Transceiver* data sheet (SLLSE34) for more detail.

REFCLK_B_SEL: Reference Clock Select Channel B. This input, when low, selects REFCLK_0_P/N as the clock reference to Channel B SERDES macro. When high, REFCLK_1_P/N is selected as the clock reference to Channel B SERDES macro. If software control is desired (register bit 0.1), this input signal must be tied low. See Figure 4, “TLK6002 Reference Clock/Output Clock Architecture” of the TLK6002 data sheet (SLLSE34) for more detail.

RATE_A[2:0]: Channel A Rate select pins. These pins put channel A into one of the four supported (full/half/quarter/eighth) channel operation rates, enable software control, or enable Auto Rate Sense (ARS):

000 – Full Rate mode

001 – Half Rate mode

010 – Quarter Rate mode

011 – Eighth Rate mode

100 – Software Selectable Rate

101 – Channel A Auto Rate Sense (ARS) Function Enabled.

Channel A SERDES settings are determined by Channel A ARS machine. CLK_OUT_P/N selected by CLK_OUT_SEL. See Table 9 of the TLK6002 data sheet (SLLSE34) for additional details on CLK_OUT_P/N.

110 – Channel A Auto Rate Sense (ARS) Function Enabled.

Channel A SERDES settings are determined by Channel A ARS machine. CLK_OUT_P/N is not selected by CLK_OUT_SEL. Channel B may not be simultaneously configured with RATE_B = 110 with respect to CLK_OUT_P/N, this setting has the highest priority. See Table 9 of the TLK6002 data sheet (SLLSE34) for additional details on CLK_OUT_P/N.

111 – Channel A Auto Rate Sense (ARS) Function Enabled – Slave Mode.

If Channel B ARS is enabled (Rate B = 101 or 110 only):

Channel A SERDES settings are determined by Channel B ARS machine. CLK_OUT_P/N is not selected by CLK_OUT_SEL. See Table 9 of the TLK6002 data sheet (SLLSE34) for additional details on CLK_OUT_P/N.

If Channel B ARS is not enabled (Rate B = 000/001/010/011/111):

Channel A SERDES settings are determined by Channel A MDIO registers. CLK_OUT_P/N is selected by CLK_OUT_SEL. See Table 9 of the TLK6002 data sheet (SLLSE34) for additional details on CLK_OUT_P/N.

Channel A and B must not be in slave mode simultaneously. Both directions of Channel A are controlled by these input signals.

The RATE_A[2] pin must be routed to an uninstalled header so that it can be driven externally in the event that device debug is required. In application mode, it must be biased with a pullup or pulldown resistor and not connected directly to a power or ground plane.

CODEA_EN: Encoder/Decoder Channel A Enable: When this pin is asserted high, the internal 8b/10b encoder/decoder is enabled. This signal is ORed with MDIO register bits and must be pulled low through a resistor if software control is desired. This pin must be routed to an uninstalled header so that it can be driven externally in the even that device debug is required. In application mode, it must be biased with a pullup or pulldown resistor and not connected directly to a power or ground plane.

LOSA: Channel A Receive Loss Of Signal (LOS) Indicator.

LOSA = 0, signal detected.

LOSA = 1, loss of signal.

Loss of signal detection is based on the input signal level. When RXAP/N has an input signal of ≤75mVdfpp, LOSA is asserted (if enabled). The input signal must be greater than or equal to 150mVdfpp for this function to operate reliably.

Other functions can be observed on LOSA real time, configured via MDIO.

During device reset (RESET_N asserted low), this pin is driven low. During pin-based power down (PD_TRXA_N asserted low), this pin is floating. During register-based power down (1.15 asserted high), this pin is floating.

It is highly recommended that LOSA be brought to an easily accessible point on the application board (header) in the event that debug is required.

PD_TRXA_N: Transceiver Power Down. When this pin is held low (asserted), Channel A is placed in power-down mode. When de-asserted, Channel A operated normally. After de-assertion, a software data path reset must be issued through the MDIO interface.

RATE_B[2:0]: Channel B Rate select pins. These pins put channel B into one of the four supported (full/half/quarter/eighth) channel operation rates, enable software control, or enable Auto Rate Sense (ARS):

000 – Full Rate mode

001 – Half Rate mode

010 – Quarter Rate mode

011 – Eighth Rate mode

100 – Software Selectable Rate

101 – Channel A Auto Rate Sense (ARS) Function Enabled.

Channel B SERDES settings are determined by Channel B ARS machine. CLK_OUT_P/N is selected by CLK_OUT_SEL. See Table 9 of the TLK6002 data sheet (SLLSE34) for additional details on CLK_OUT_P/N.

110 – Channel B Auto Rate Sense (ARS) Function Enabled.

Channel B SERDES settings are determined by Channel B ARS machine. CLK_OUT_P/N is not selected by CLK_OUT_SEL. Channel A may not be simultaneously configured with RATE_A = 110 with respect to CLK_OUT_P/N; this setting has the highest priority. See Table 9 of the TLK6002 data sheet (SLLSE34) for additional details on CLK_OUT_P/N.

111 – Channel B Auto Rate Sense (ARS) Function Enabled – Slave Mode

If Channel B ARS is enabled (Rate B = 101 or 110 only):

Channel B SERDES settings are determined by Channel B ARS machine. CLK_OUT_P/N is not selected by CLK_OUT_SEL. See Table 9 of the TLK6002 data sheet (SLLSE34) for additional details on CLK_OUT_P/N.

If Channel B ARS is not enabled (Rate B = 000/001/010/011/111):

Channel B SERDES settings are determined by Channel B MDIO registers. CLK_OUT_P/N is selected by CLK_OUT_SEL. See Table 9 of the TLK6002 data sheet (SLLSE34) for additional details on CLK_OUT_P/N.

Channel A and B must not be in slave mode simultaneously. Both directions of Channel A are controlled by these input signals.

The RATE_B2 pin must be routed to an uninstalled header so that it can be driven externally in the event that device debug is required. In application mode, it must be biased with a pullup or pulldown resistor and not connected directly to a power or ground plane.

CODEB_EN: Encoder/Decoder Channel B Enable: When this pin is asserted high, the internal 8b/10b encoder/decoder is enabled. This signal is ORed with MDIO register bits, and must be pulled low through a resistor if software control is desired. This pin must be routed to an uninstalled header so that it can be driven externally in the event that device debug is required. In application mode, it must be biased with a pullup or pulldown resistor and not connected directly to a power or ground plane.

LOSB: Channel B Receive Loss Of Signal (LOS) Indicator.

LOSB = 0, signal detected.

LOSB = 1, loss of signal.

Loss of signal detection is based on the input signal level. When RXBP/N has an input signal of ≤75 mVdfpp, LOSB is asserted (if enabled). The input signal must be greater than or equal to 150mVdfpp for this function to operate reliably.

Other functions can be observed on LOSB real time, configured via MDIO.

During device reset (RESET_N asserted low), this pin is driven low. During pin-based power down (PD_TRXB_N asserted low), this pin is floating. During register-based power down (1.15 asserted high), this pin is floating.

It is highly recommended that LOSB be brought to an easily accessible point on the application board (header) in the event that debug is required.

PD_TRXB_N: Transceiver Power Down. When this pin is held low (asserted), Channel B is placed in power-down mode. When de-asserted, Channel B operated normally. After de-assertion, a software data path reset must be issued through the MDIO interface.

AMUXB: SERDES Channel B Analog Testability I/O. This signal is used during the device manufacturing process. It must be left unconnected in the device application.

AMUXA: SERDES Channel A Analog Testability I/O. This signal is used during the device manufacturing process. It must be left unconnected in the device application.

TESTEN: Test Enable. This signal is used during the device manufacturing process. It must be grounded through a resistor in the device application board. The application board must allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO2).

PRBS_EN: Enable PRBS: When this pin is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths of both channels. This signal is logically ORed with an MDIO register bit. PRBS 2^{31}-1 is selected by default, and can be changed in MDIO register 7.10:8. Note that PRBS is not possible in eighth rate mode.

The PRBS_EN pin must be routed to an uninstalled header so that it can be driven externally in the event that device debug is required. In application mode, it must be biased with a pullup or pulldown resistor (or allow for an isolation mechanism from the onboard driver) and not connected directly to a power or ground plane.

CLK_OUT_SEL: Output Clock Selection. If ARS is not enabled and CLK_OUT_SEL is low, Channel A recovered byte clock is output onto CLK_OUT_P/N. If ARS is not enabled and CLK_OUT_SEL is high, Channel B recovered byte clock is output onto CLK_OUT_P/N. If software control is desired, (registered bit 0.6), this input signal must be tied low. See Figure 4, “TLK6002 Reference Clock/Output Clock Architecture” of the TLK6002 data sheet (SLLSE34) for more detail. If ARS is enabled, the function of CLK_OUT_SEL is shown in Table 9 of the TLK6002 data sheet.

GPI0: General Purpose Input Zero. This signal is used during the device manufacturing process. It must be grounded through a resistor in the device application board. The application board must allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO2).

GPI1: General Purpose Input One. This signal can be used to logically combine an external status condition with LOSA or LOSB if enabled in an MDIO register. Note that if GPI1 is low, LOSA/B is asserted if a logical combination in enabled. Similarly, if GPI1 is high, LOSA/B is de-asserted. If unused, this input must be grounded in the device application (not floating).

7 PRBS PASS Latch Circuits

The TLK6002EVM has a Pass/Fail Latch circuit to aid in PRBS testing. The PRBS_PASSA and PRBS_PASSB status signals have been routed out to Header JMP43 for monitoring with an oscilloscope. Additionally, these signals are routed to the base of an NPN transistor that drives an LED on or off depending on whether the PRBS_PASSA/B signals are High or Low. The blue LEDs D51 and D52 are a good indication of general passing or general failing depending on whether the LED is on or off. However, it is not a good method to easily monitor individual bit failures. An error counter can be read through the MDIO register interface that contains the actual error count should the counter not have overflowed; however, it requires the counter to be read in order to determine whether an error has occurred. With proper setup and operation, the PRBS_PASS Latch circuits can quickly indicate whether an error has occurred or not.

To properly operate the PRBS_PASS latches, configure the TLK6002 for PRBS operation either by pulling the PRBS_EN line high or through the appropriate MDIO register settings. PRBS data is generated and output on the Serial Transmit and the Serial Receive monitors for valid PRBS data and counts the number of errors received. In addition to counting the errors, the PRBS_PASS line is high if the line is error free, and transitions low for the duration of time that an error, or errors, are detected. Once the PRBS link is established and running error free, pushing the PRBS_PASS RESET button resets the latch circuit, which consists of a J/K flip-flop and a red and green LED to indicate the state of the flip-flop. When the J/K flip-flop is reset, the green LED is lit until a high-to-low transition on the PRBS_PASS signal is observed. Because the PRBS_PASS signal is connected to the clock input of the J/K flip-flop, a high-to-low transition causes the flip-flop to toggle to the next state which turns OFF the green LED and turns ON the red LED. The circuit remains in this state until the RESET button is pushed again, which resets the flip-flop to its initial state.

NOTE: If the PRBS_PASS lines are low, indicating constant PRBS failure and the PRBS_PASS RESET buttons are pushed, the green LEDs lights and remain lit, which might be falsely interpreted as a passing result. This is incorrect as the line was not ever passing and as long as it is failing the PRBS_PASS line will be low and never have the high-to-low transition required to toggle the state and light the red LED. This is not the intended operation of the circuit, and this latch circuit must ONLY be used on a passing and correctly established channel with valid PRBS data. An easy indication of whether the PRBS Latch may be used is whether the blue PRBSA/B LEDs are on as well, because they can only be on if the PRBS_PASS signals are high indicating a passing status. If the blue LEDs are not on, then the green and red PRBS_PASS/Fail LEDs are not a valid indication of the status of the test.

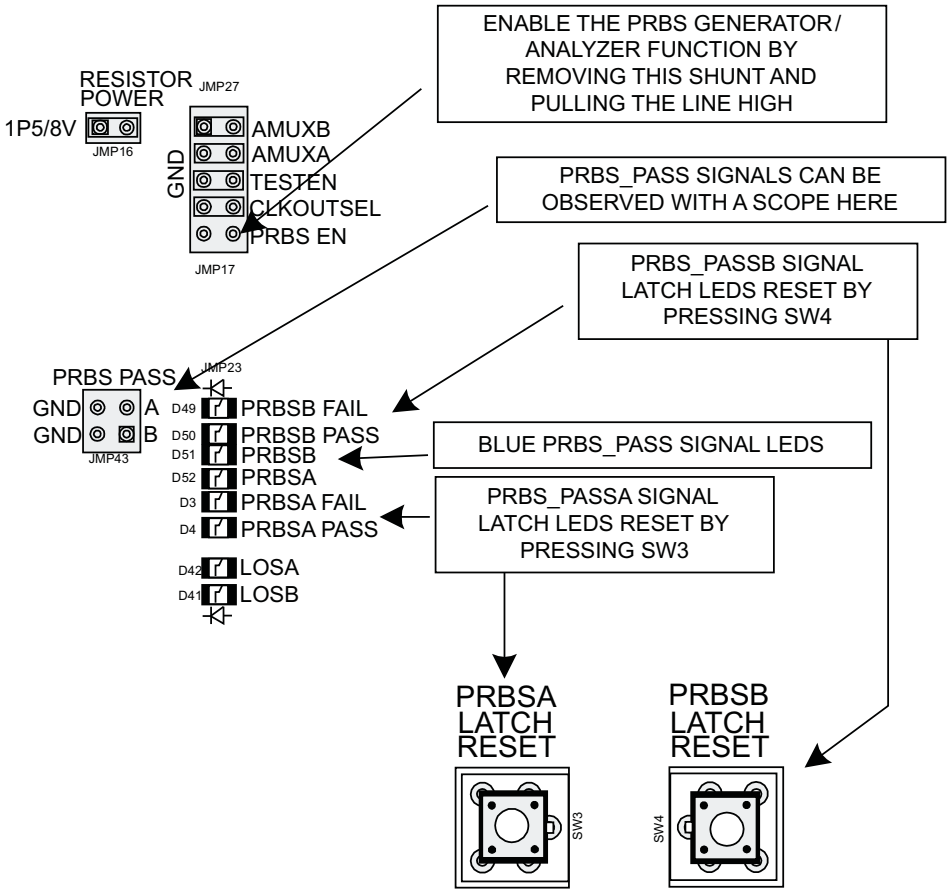


Figure 9. TLK6002 EVM MDIO Connector (JMP30)

8 MDIO

The TLK6002 supports the Management Data Input/Output (MDIO) Interface as defined in Clause 22 of the IEEE 802.3 Ethernet Specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK6002 is possible without the use of this interface; however, some additional features are accessible only through the MDIO interface.

The MDIO Management Interface consists of a bidirectional data path (MDIO) and a clock reference (MDC). The port address is determined by control pins PRTAD[4:0

In Clause 22, the top four control pins PRTAD[4:1] determine the device port address. In this mode, the two individual channels in TLK6002 are classified as two different ports. Therefore, any PRTAD[4:1] value has two ports per TLK6002. The TLK6002 responds if the four MSBs of PHY address field on MDIO protocol (PA[4:1]) matches PRTAD[4:1]. The LSB of PHY address field (PA[0]) determines which channel/port within the TLK6002 to respond to.

If PA[0] = 1'b0, TLK6002's Channel A responds.

If PA[0] = 1'b1, TLK6002's Channel B responds.

Write transactions which address an invalid register or read-only registers are ignored. Read transactions of invalid registers return a 0.

The bidirectional MDIO pin must be externally pulled up to 1.5 V or 1.8 V (VDDO) with an appropriate resistor value as per the IEEE802.3 Clause 22/45 MDIO Standard.

The supplied MDIO EVM uses an FPGA with 2.5-V I/O signal levels whereas the TLK6002 requires either 1.5-V or 1.8-V I/O levels on these signals. Therefore, bidirectional level shifters have been provided on board that level shift the 2.5-V MDIO and MDC signals to the appropriate 1p5/8V levels. If a different MDIO controller id used that already has 1.5-V or 1.8-V signal levels, resistors R530, R531, R532, and R533 can be removed; thus, disconnecting the level shifters and resistors R469 and R470 can be installed which connects the TLK6002 MDIO and MDC signal pins directly to the pins of JMP30. A third option of using NFETs as level shifters has also been provided, if this option is desired in the end application. Removing resistors R530, R531, R532, and R533, as well R469 and R470 if they were installed, and installing an appropriate NFET such as Fairchild's FDV301N allows for this third option of level shifting to be evaluated.

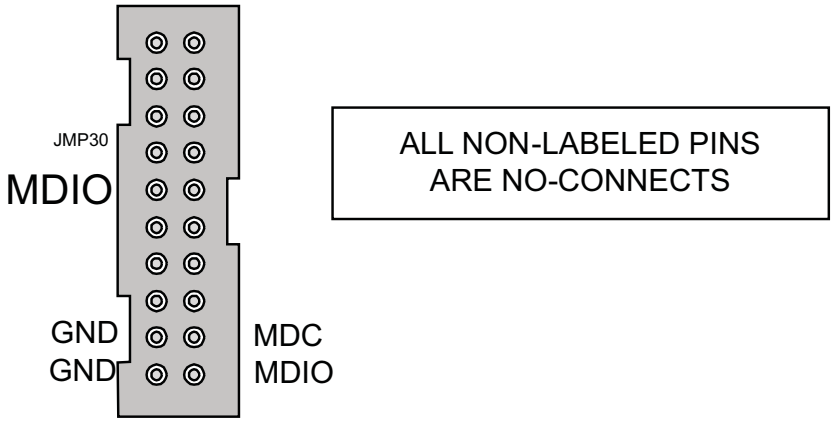


Figure 10. TLK6002 EVM MDIO Connector (JMP30)

9 JTAG

The EVM also provides a separate connector to support the full five-pin JTAG interface of the TLK6002 with onboard level shifters to be compatible with most standard JTAG Control Interfaces to be used for manufacturing tests. Pullup resistors on the 3.3-V (header) side of the level shifter are not installed by TI but can be installed if an open-drain type of controller is used which requires the use of external pullup resistors.

TDI: JTAG Input Data. TDI is used to serially shift test data and test instructions into the device during the operation of the test port. In system applications where JTAG is not implemented, this input signal can be left floating. During pin-based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is not pulled up. During register-based power down (1.15 asserted high for both channels), this pin is pulled up normally.

TDO: JTAG Output Data. TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high-impedance state. During device reset (RESET_N asserted low), this pin is floating. During pin-based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is floating. During register-based power down (1.15 asserted high on both channels), this pin is floating.

TMS: JTAG Mode Select. TMS is used to control the state of the internal test-port controller. In system applications where JTAG is not implemented, this input signal can be left unconnected. During pin-based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is not pulled up. During register-based power down (1.15 asserted high both channels), this pin is pulled up normally.

TCK: JTAG Clock. TCK is used to clock state information and test data into and out of the device during boundary scan operation. In system applications where JTAG is not implemented, this input signal must be grounded.

TRST_N: JTAG Test Reset. TRST_N is used to reset the JTAG logic into system operational mode. This input can be left unconnected in the application and is pulled down internally, disabling the JTAG circuitry. If JTAG is implemented on the application board, this signal must be de-asserted (high) during JTAG system testing, and otherwise asserted (low) during normal operation mode. During pin-based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is not pulled down. During register-based power down (1.15 asserted high on both channels), this pin is pulled down normally.

NOTE: TRST_N must be tied low when the JTAG port is not in use and during normal operation of the port as shown in Figure 11 because an external pullup resistor is provided. If you have no need to use the JTAG port, removing resistor R423 allows the internal pulldown to disable the circuitry and installing resistor R426 provides an external pulldown on this pin.

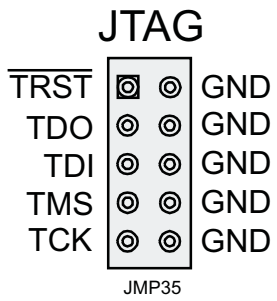


Figure 11. TLK6002 EVM JTAG Connector (JMP35)

10 Reset

The TLK6002EVM comes configured for Manual Reset operations involving the Pushbutton Reset Switch (SW1). When switch SW1 is pressed, the TLK6002 device RESET pin (RST_N) goes LOW and the entire TLK6002 device is reinitialized. A TI TPS3125J18 Ultra Low Voltage Processor Supervisory Circuit is used to control the Reset line. During power on, $\overline{\text{RESET}}$ pin of U2 is asserted when the supply voltage becomes higher than 0.75 V. Thereafter, the supply voltage supervisor monitors the voltage and keeps $\overline{\text{RESET}}$ output active as long as the voltage remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_d = 180 ms, starts after the voltage has risen above the threshold voltage (V_{IT}).

A manual reset input to the supervisory circuit, $\overline{\text{MR}}$, accepts the input from the pushbutton switch SW1. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active, thus resetting the TLK6002 device whenever the pushbutton RESET is pressed. By placing a jumper on JMP15, the Manual Reset ($\overline{\text{MR}}$) is tied hard to ground causing the TLK6002 to be held in a constant state of Reset without the need to continually hold the Reset Pushbutton SW1. The Supervisory circuit released the Reset line to a HIGH 180 ms (t_d) from the time the $\overline{\text{MR}}$ line becomes greater than the threshold voltage (V_{IT}).

By removing the jumper from JMP14, the Supervised Reset Circuit is disconnected from the RST_N line. Reset control from an external controller or piece of equipment can be connected directly to pin 2 (RST_N) of JMP14 and a ground pin GND has been added to the JMP14 header next to the RST_N pin to allow easy access for the return current on that cable.

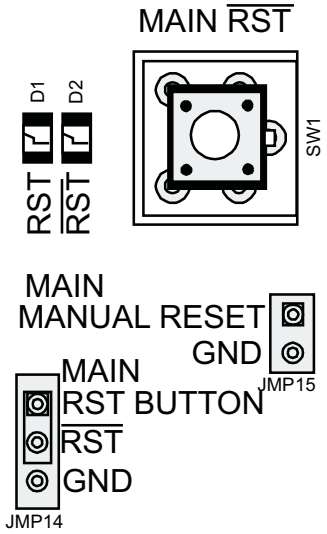


Figure 12. RESET Switch – SW1, JMP14, or JMP15

NOTE: The Jumper on JMP14 connecting RESET SW to RST_N must be connected as shown in order to cause the TLK6002 to be reset and reinitialized If switch SW1 is pressed, the device RESET pin (RST_N) goes LOW, the entire TLK6002 device is reinitialized.

11 Parallel Signals

The parallel signals on the TLK6002EVM have been routed to a 0.1-in. header block that is configured like Figure 13. All RD pins on header blocks RDA/B[7:0], RDA/B[15:8], as well as all TDA/B pins on header blocks TDA/B[7:0], TDA/B[15:8], have matched trace lengths to themselves ±0.5 mil.

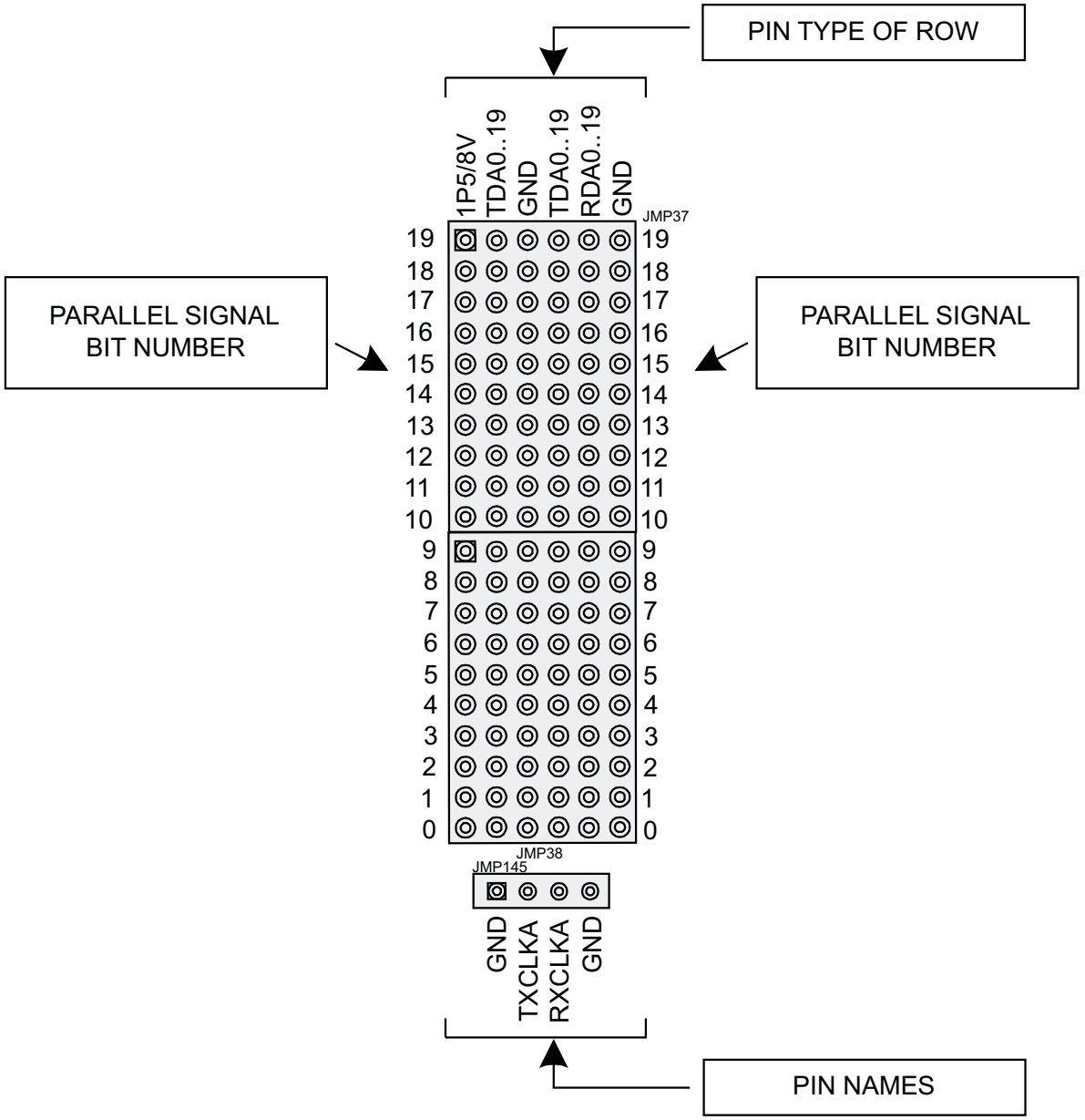


Figure 13. Parallel Signal Header Block Diagram

Parallel Loopback, shown in Figure 14, can be easily implemented by placing jumpers on the RDx/TDx pins of the header. For example, placing a jumper on pins 4 and 5 of JMP37 loops back TDA19 to RDA19.

The Transmit Data Clocks and Receive Data Clocks are located in header blocks JMP145 and JMP146 with the clock pins next to each other. These signals are the parallel side input and output clocks per channel. During Parallel Loopback, the clocks can be shorted together as shown in Figure 14.

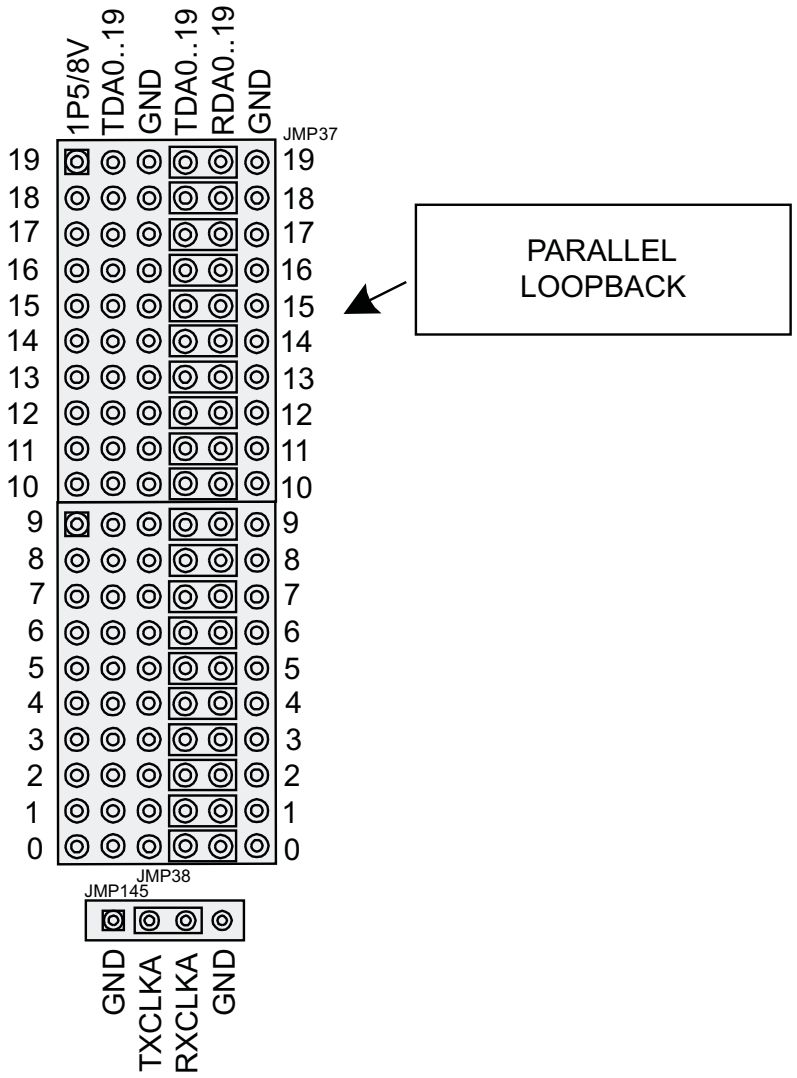


Figure 14. Parallel Loopback Example

Additional GND and VDD pins have been added into the header block for several reasons. The GND pins next to the RDA/B and TDA/B pins provide a convenient ground reference for a scope probe or coaxial cables. The additional TDA/B row and VDD pins allow a static pattern to be driven into the TDA/B bus by placing jumpers across either the TDA and 1p5/8V pins for a HIGH, or TDA/B and GND pins for a LOW eliminating the need for cables during quick tests. The extra row of TDA/B can also be used to monitor the signals on the TDA/B pins. Figure 15 shows a clock pattern (01010101010101010101) on TDA[19:0].

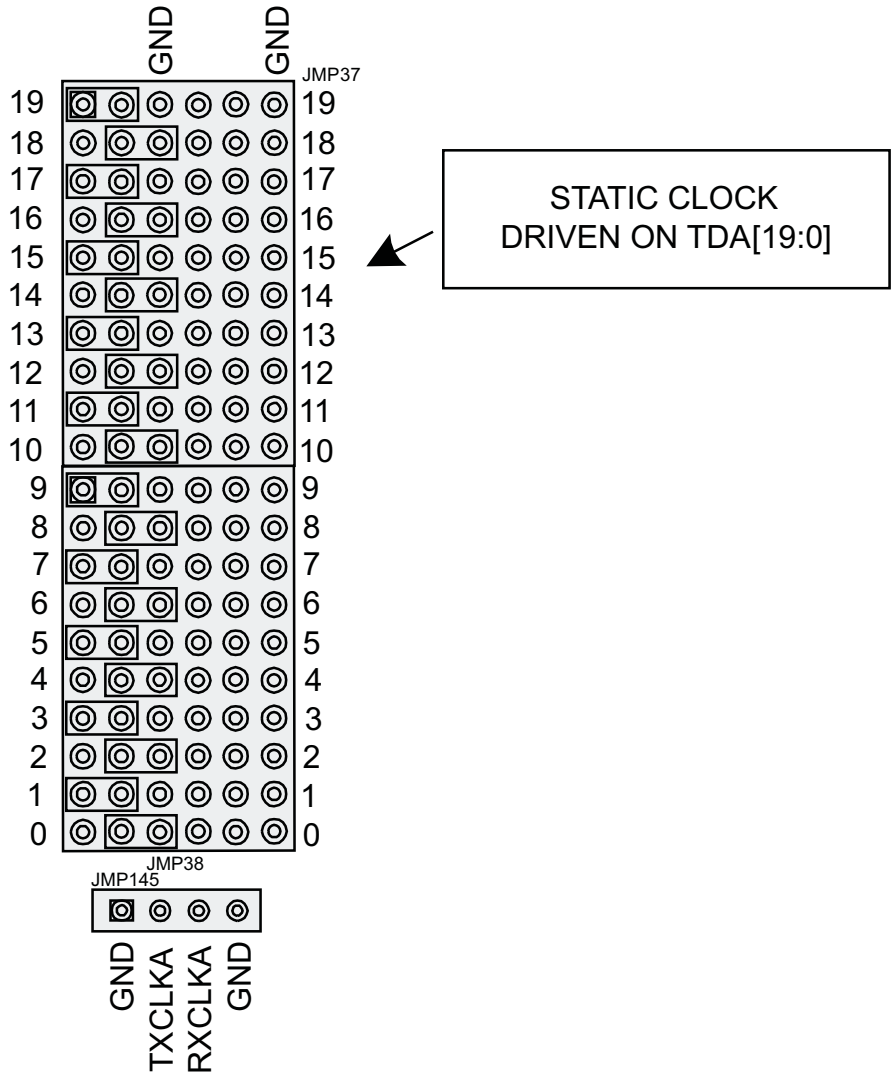


Figure 15. TDA[19:0] Static Clock Data Pattern Example

12 Peripheral Ports

The TLK6002EVM can support three small peripheral boards which can contain any sort of additional circuitry required for effective evaluation of the TLK6002 device. Examples of additional circuitry that can be implemented include a clock source such as an oscillator with multiplier/divider chip, FPGA, CPLD, or even an optical module to name a few. All of the power rails (1.2 V, 1.5/8 V, 2.5 V, 3.3 V and 5 V) have been provided to allow for minimal power circuitry on the peripheral board itself as well as the global reset signal which is connected to the TLK6002 Reset pin. TI is developing an optical module peripheral board and a clock multiplier and divider peripheral board specifically for use with the TLK6002EVM which will be capable of providing practically any clock frequency needed for operation of the TLK6002 device. However, these boards are not complete and ready for distribution with the TLK6002EVM. See sheet 28 of the TLK6002EVM schematic located in Section 14 as well as the line item in the bill of materials for connector part number information.

13 Test and Setup Configurations

The device reset requirements and setup procedure to configure the TLK3132 can be found in the latest version of the TLK6002 data sheet (SLLSE34). Always refer to the latest release of the data sheet for the latest reset, setup, and initialization procedures.

The following figures show some generic test setups using the TLK6002EVM.

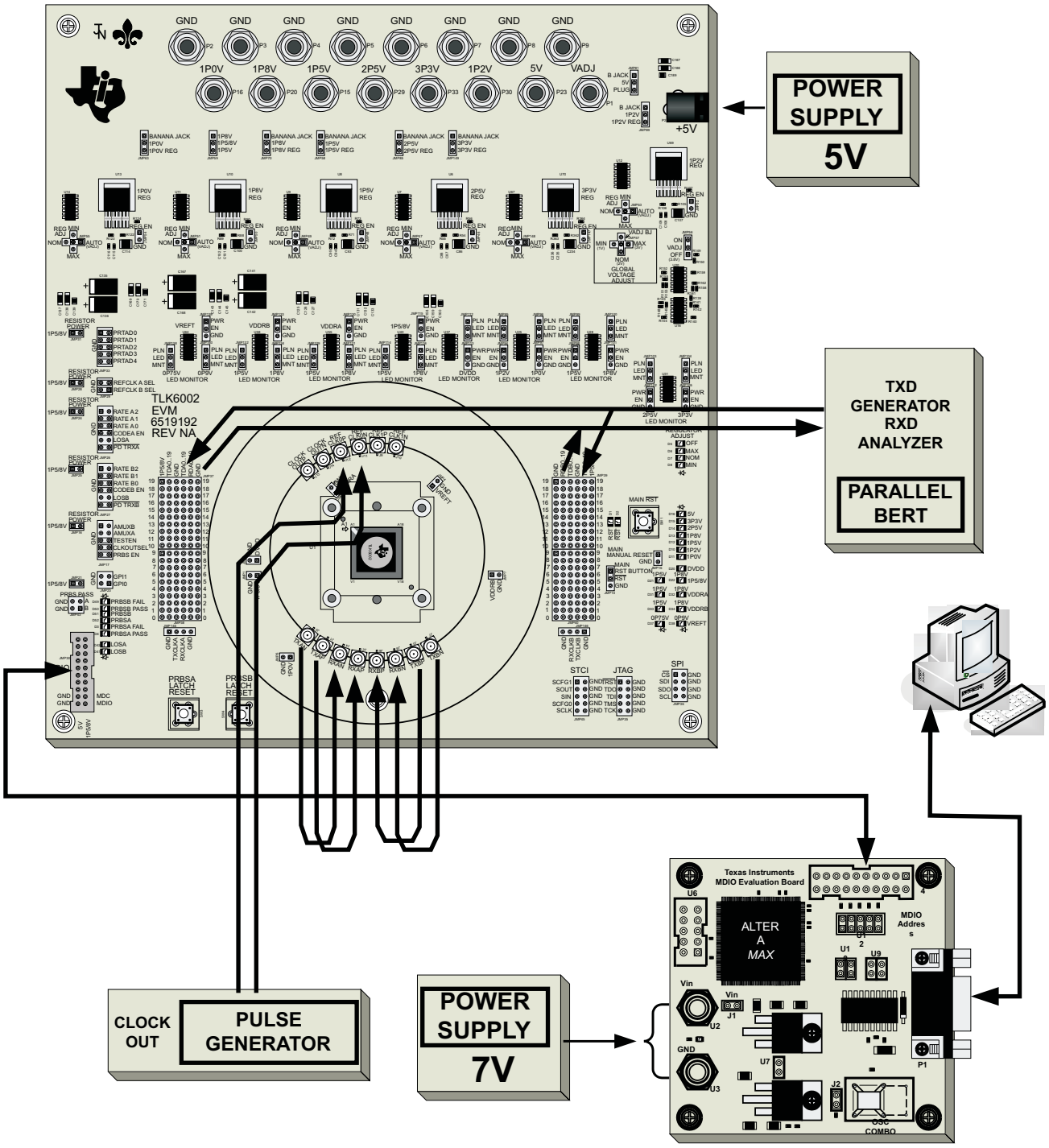


Figure 16. Example TLK6002EVM Test Configuration – Serial Loopback

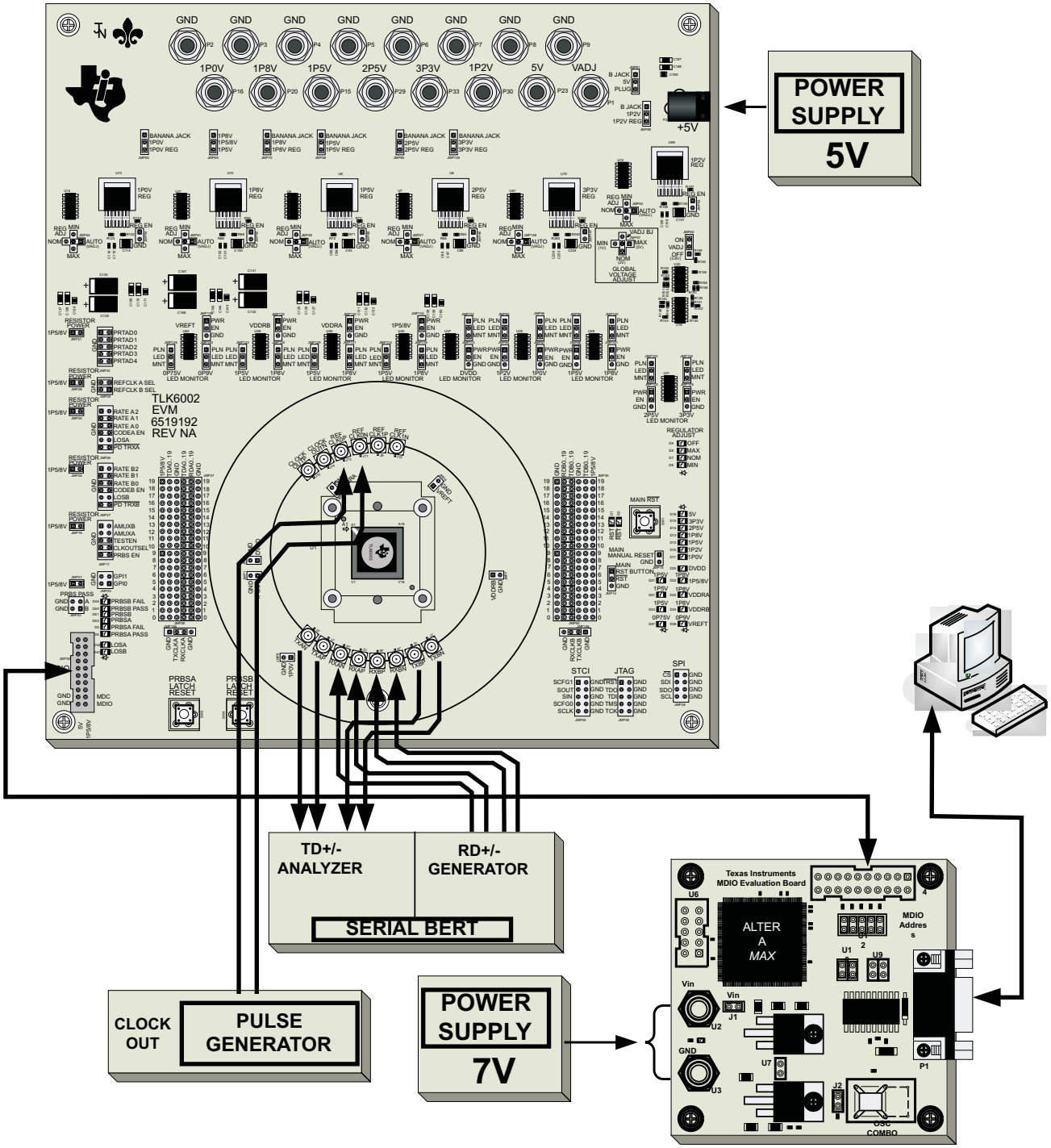


Figure 17. Example TLK6002 EVM Test Configuration – Parallel Loopback

14 TLK6002EVM Schematics

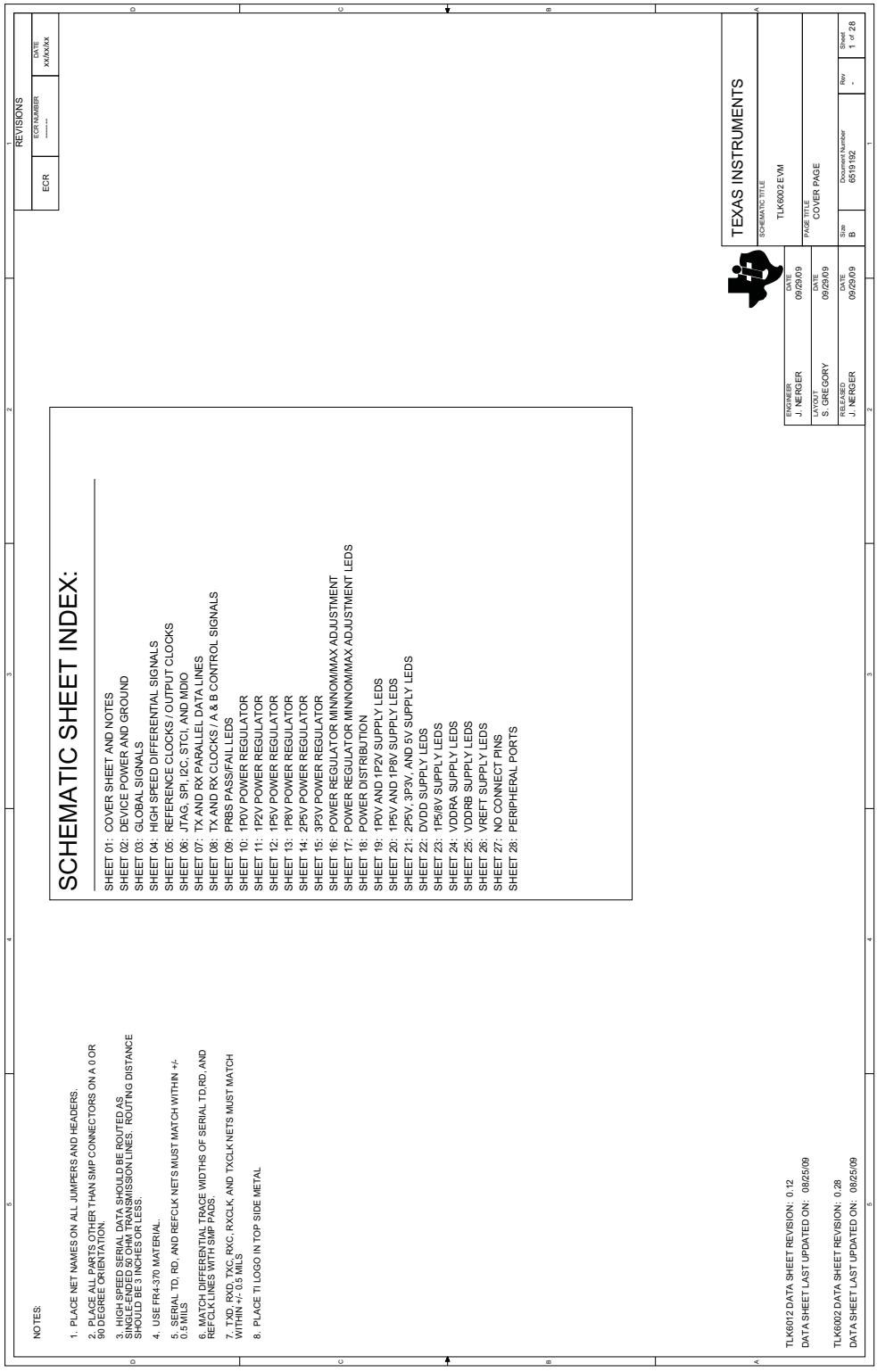


Figure 18. Cover Page and Index, Sheet 1

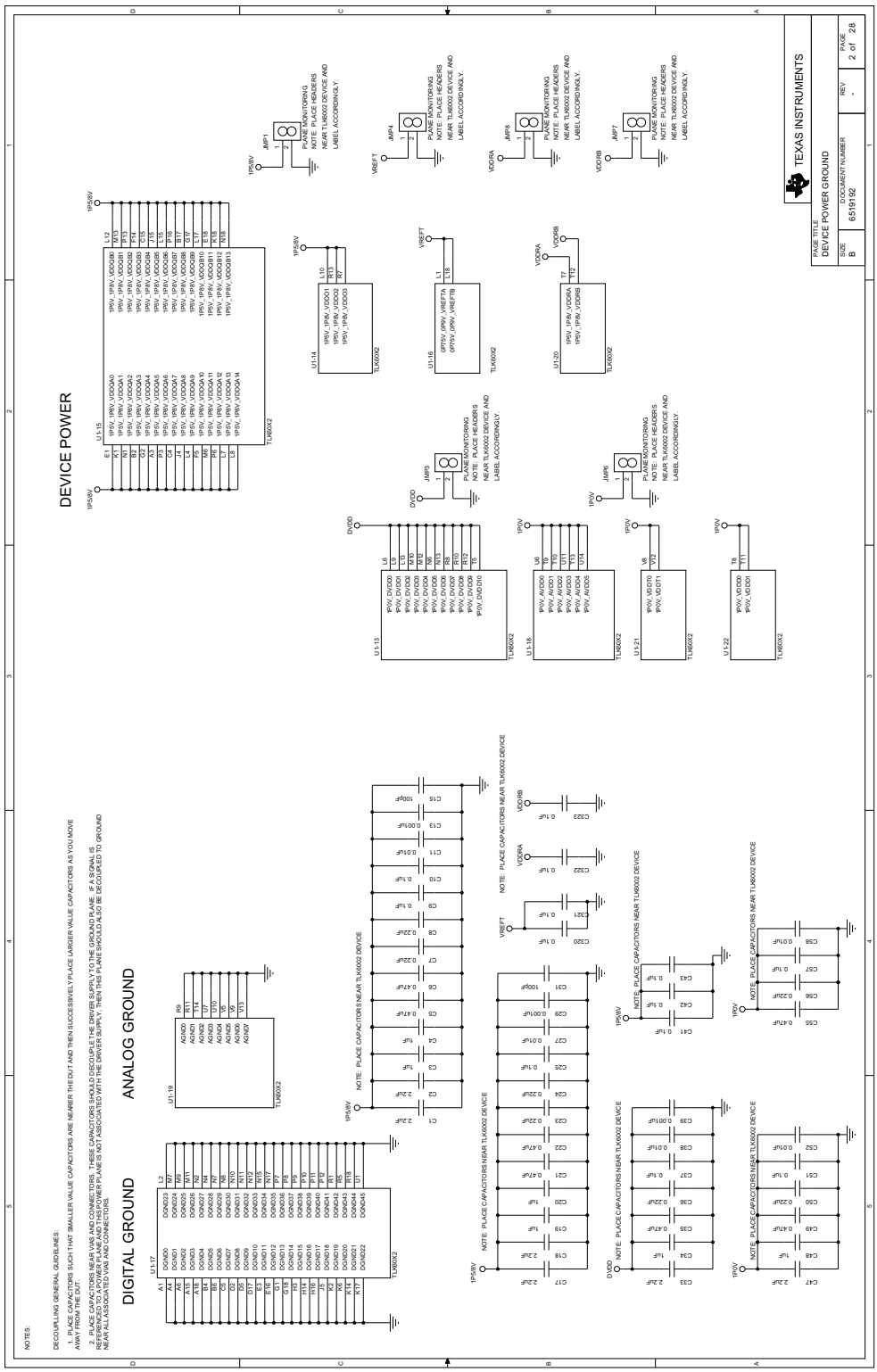


Figure 19. Device Power and Ground, Sheet 2

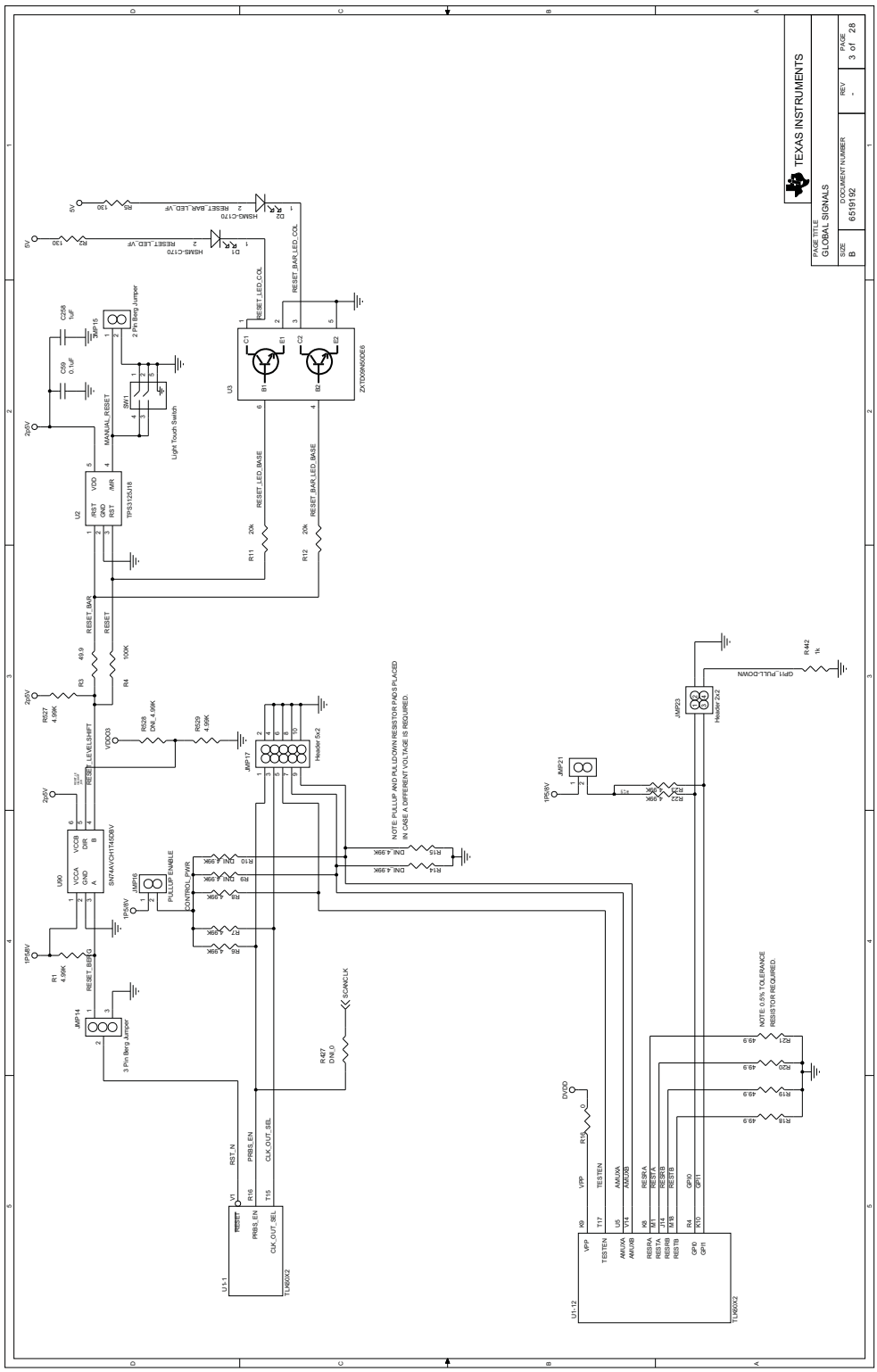


Figure 20. Global Signals, Sheet 3

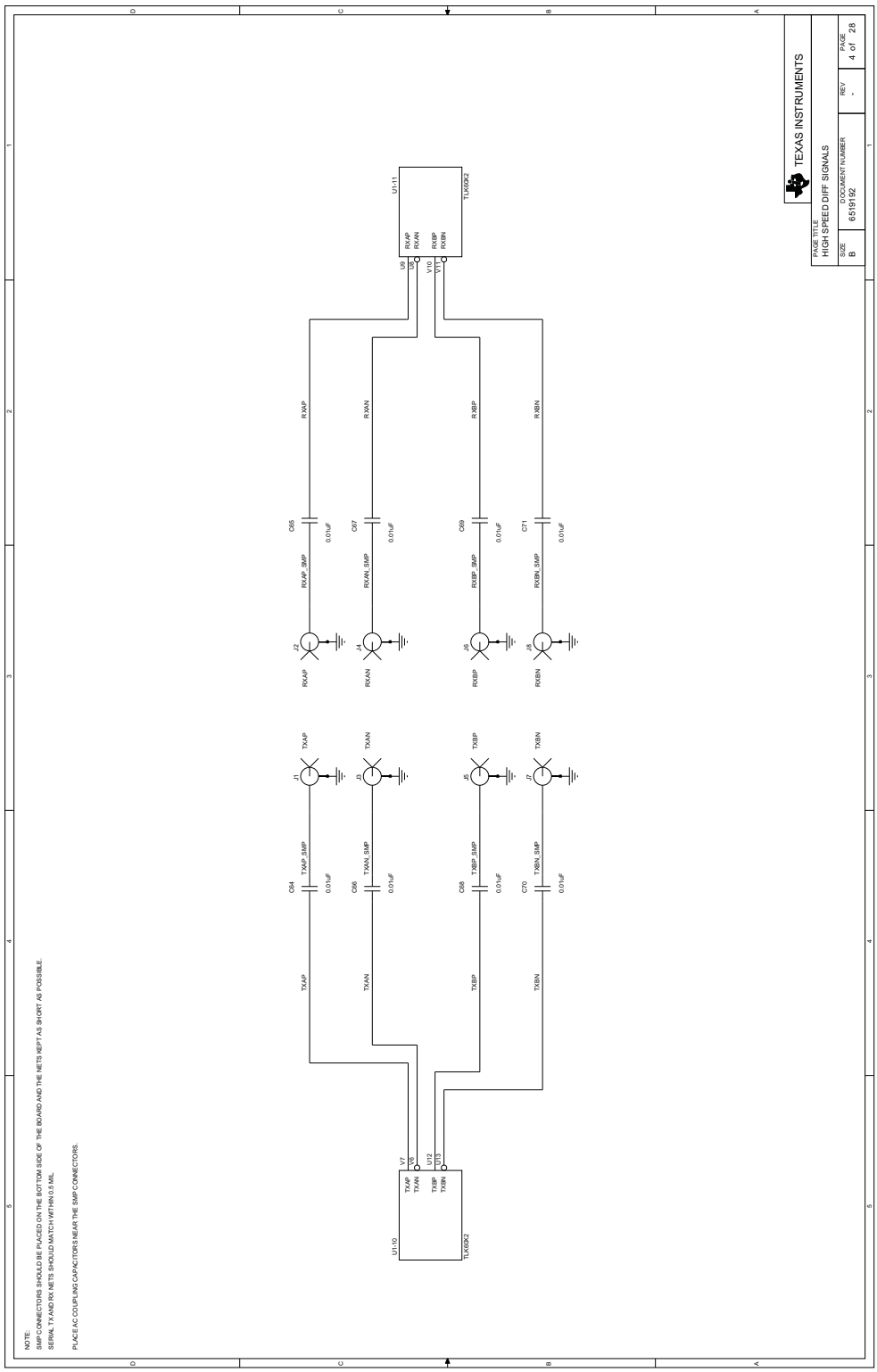


Figure 21. High-Speed Differential, Sheet 4

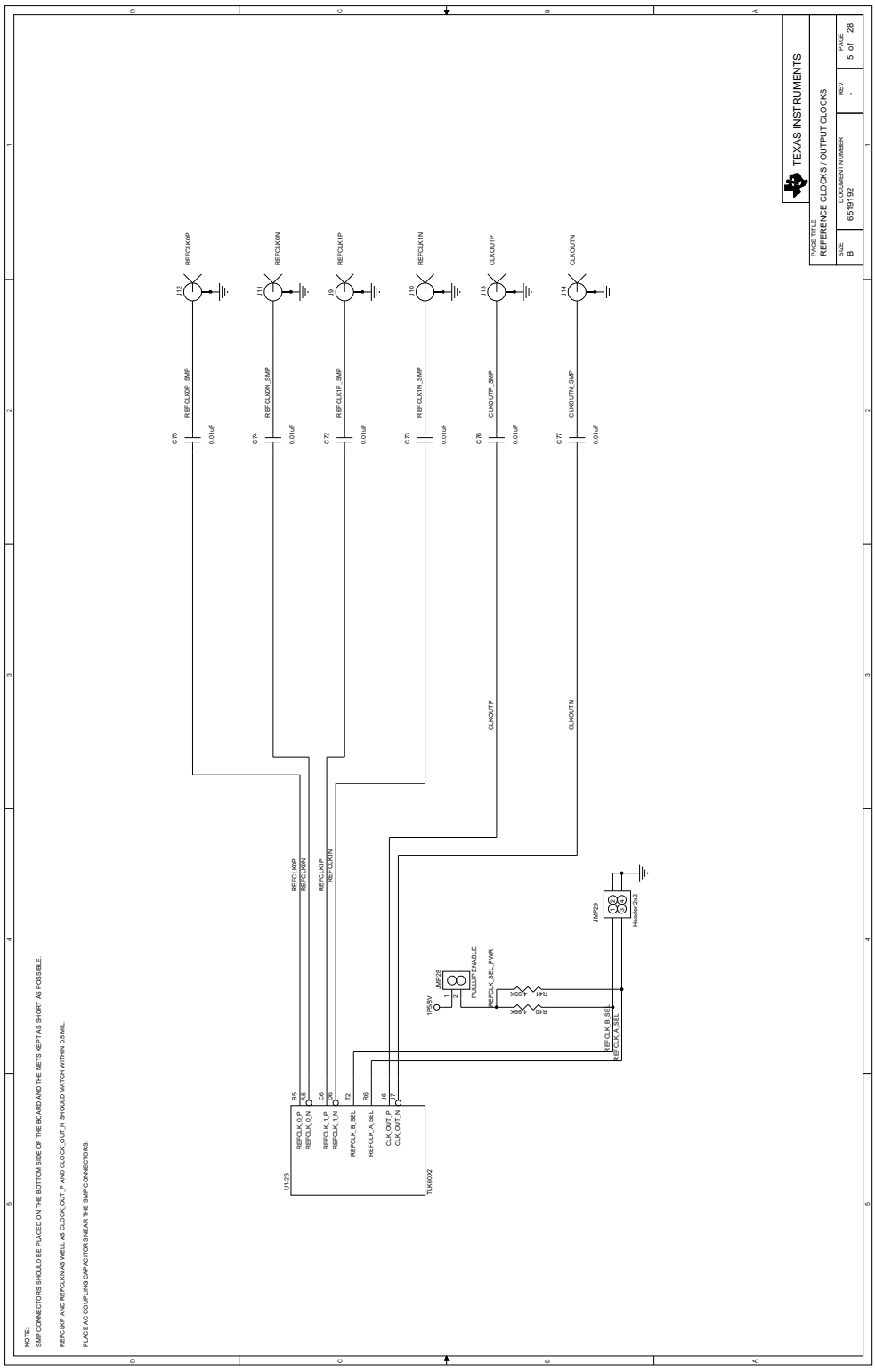


Figure 22. Reference and Output Clocks, Sheet 5

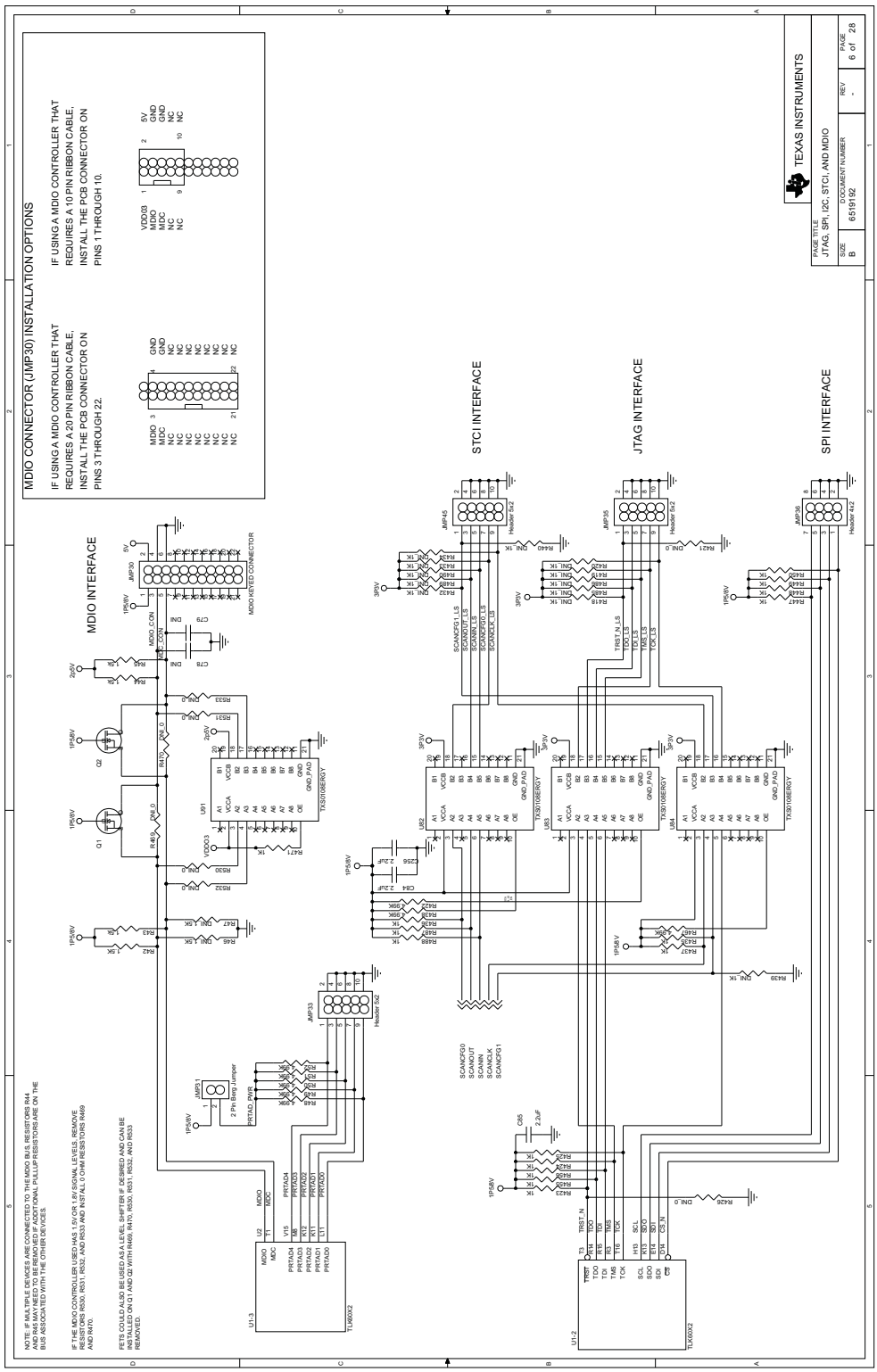


Figure 23. JTAG, SPI, I2C, STCI, and MDIO, Sheet 6

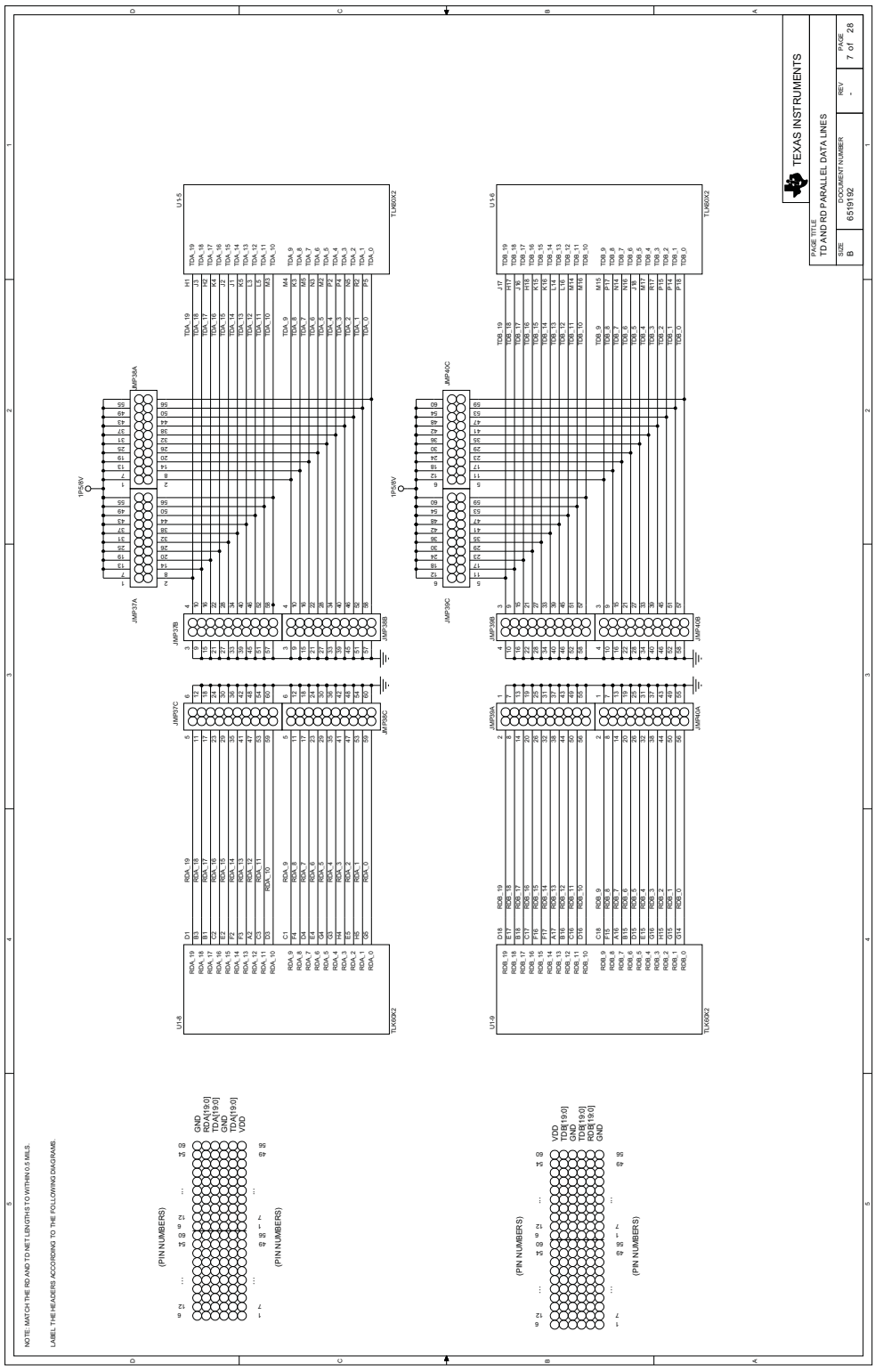


Figure 24. TD and RD Parallel Data Lines, Sheet 7

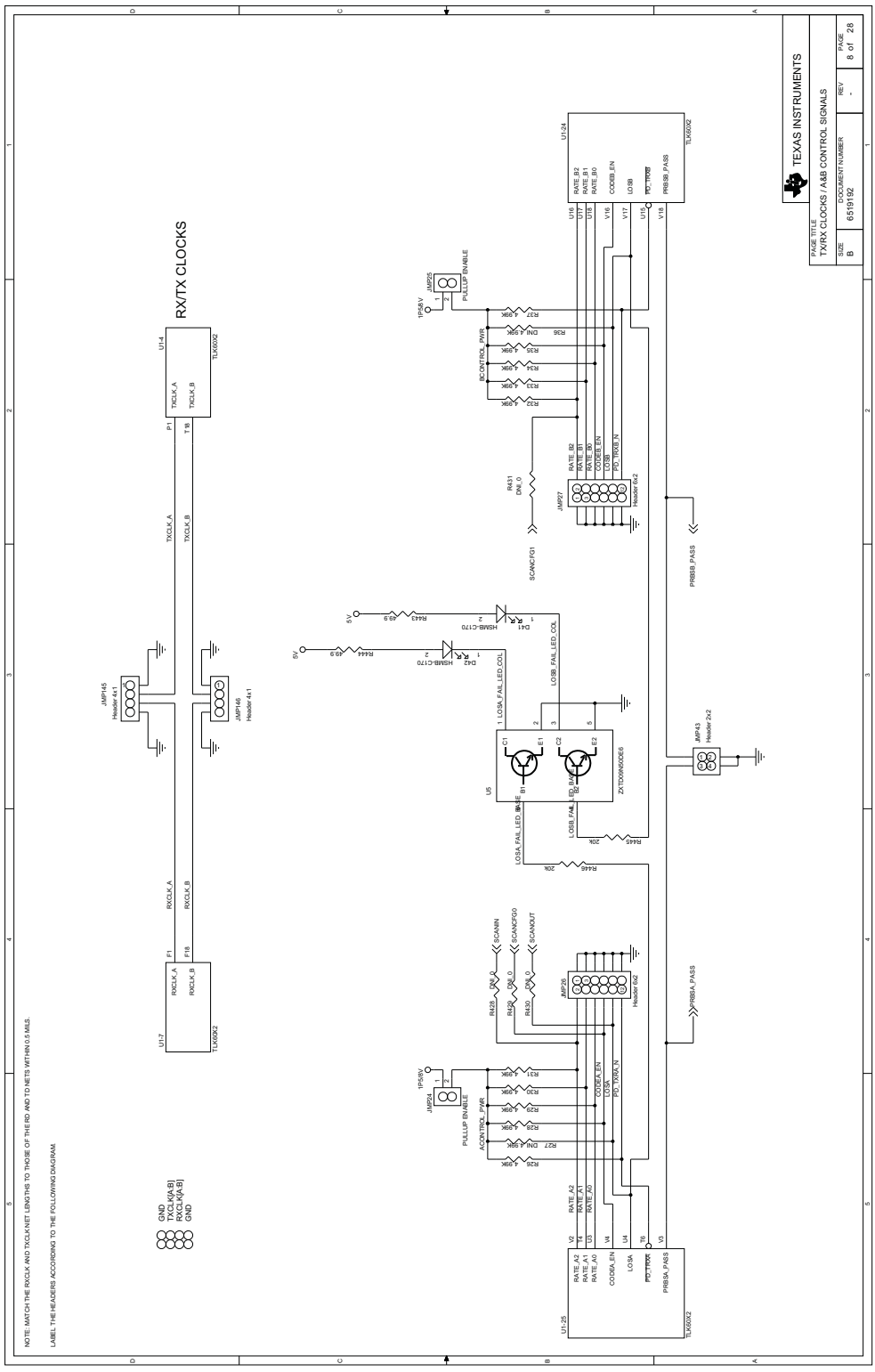


Figure 25. TX/RX Clocks and A and B Control, Sheet 8

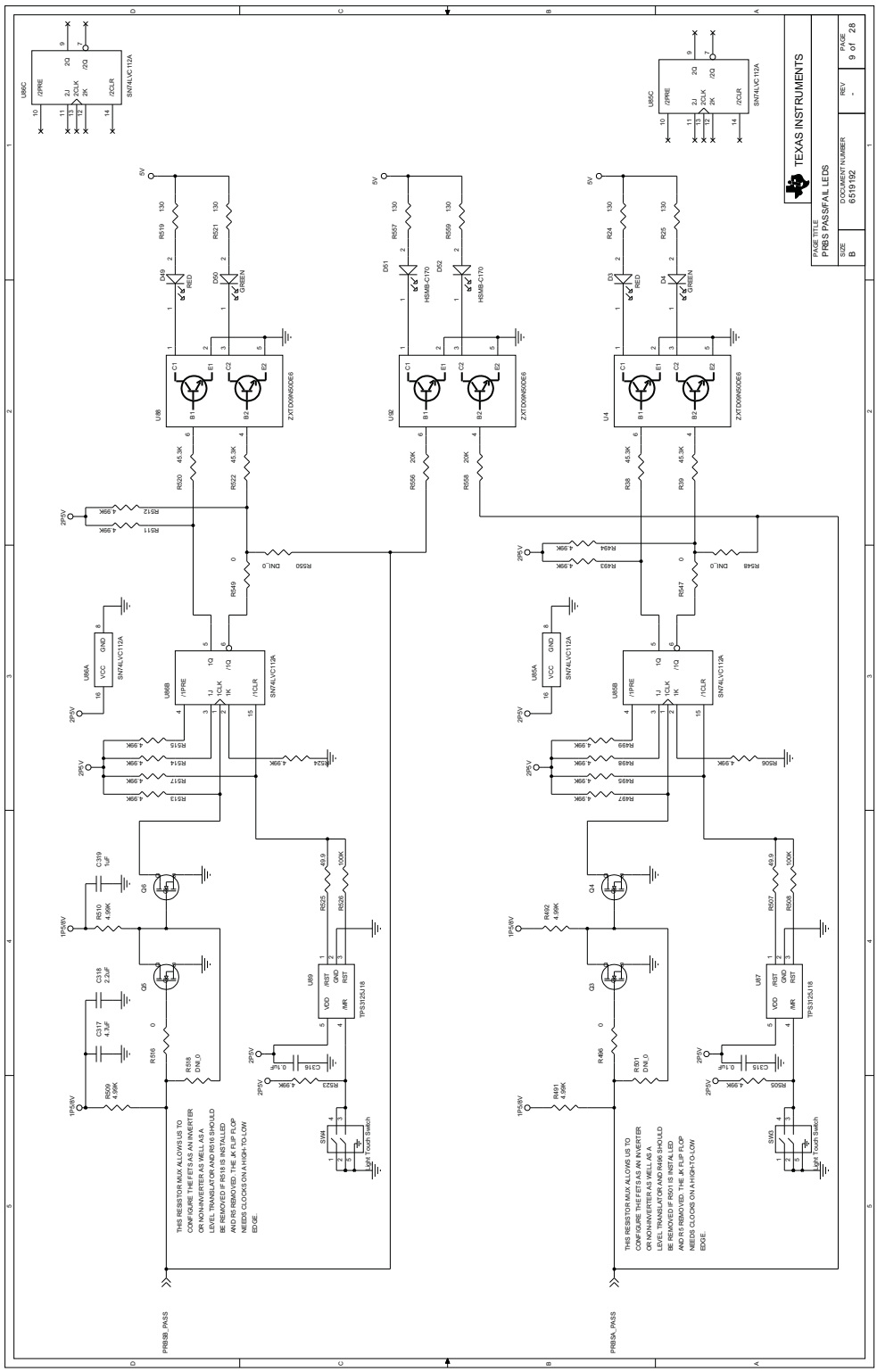


Figure 26. PRBS Pass/Fail LEDs, Sheet 9

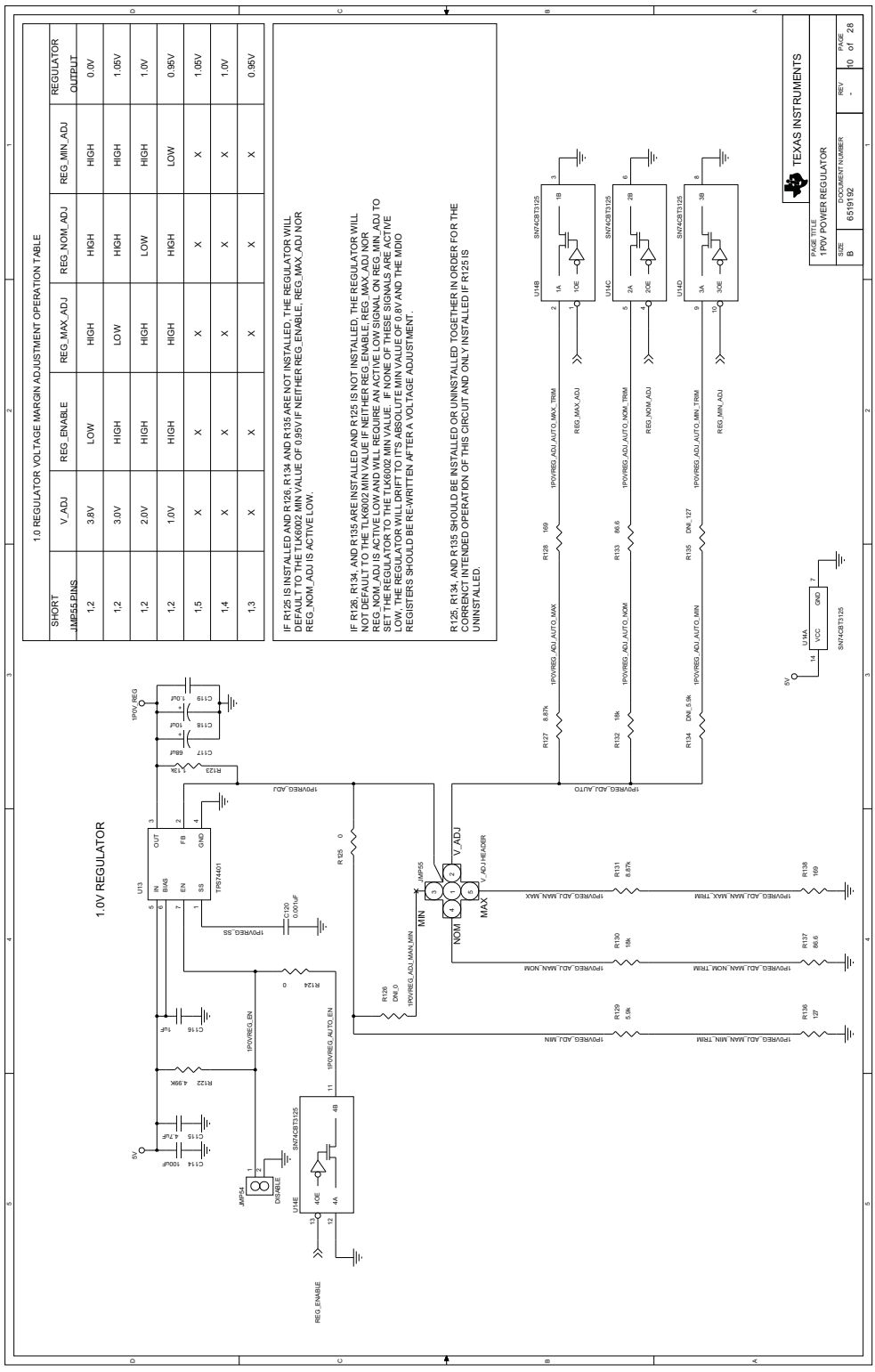


Figure 27. 1p0V Power Regulator, Sheet 10

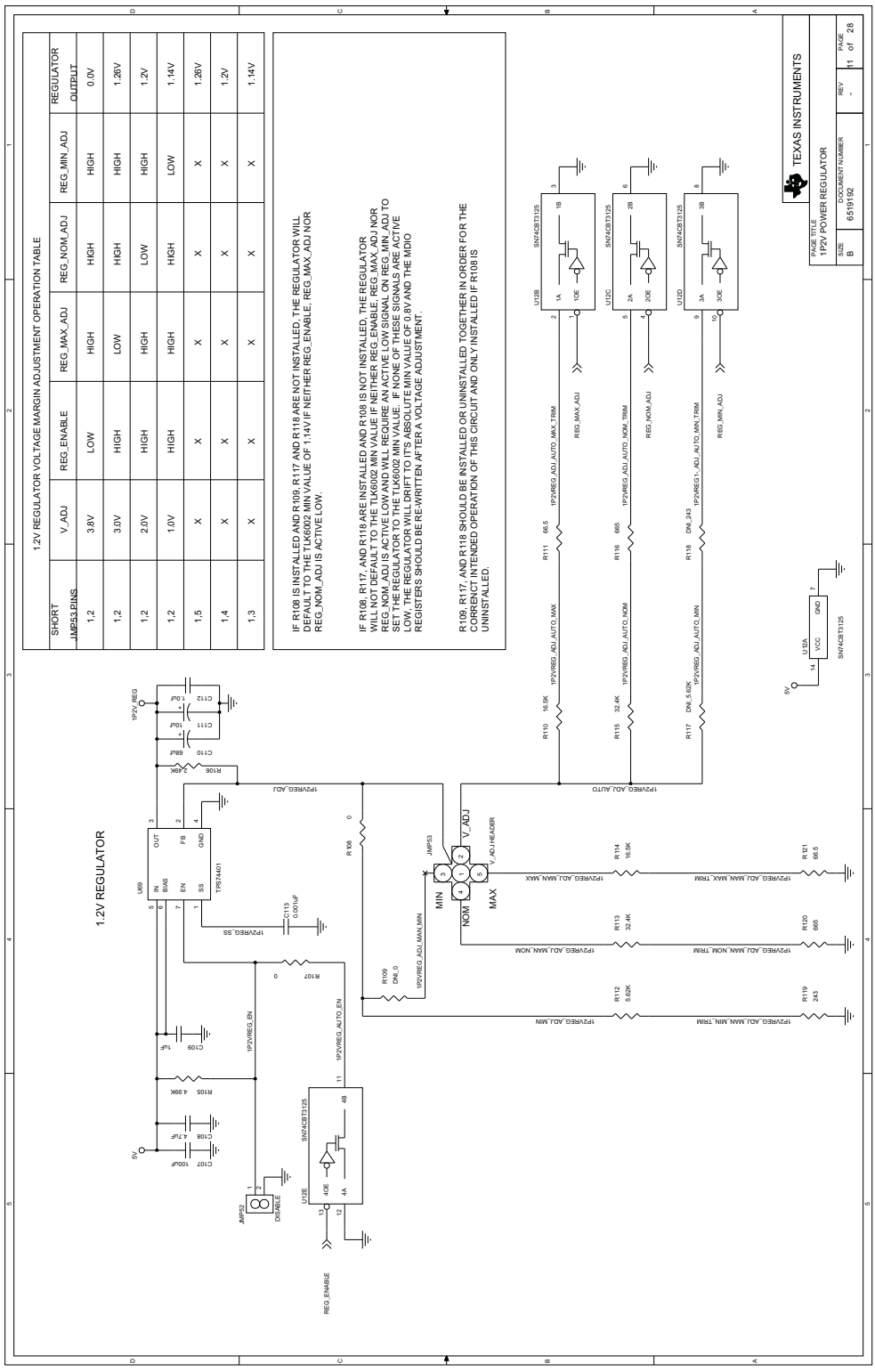


Figure 28. 1p2V Power Regulator, Sheet 11

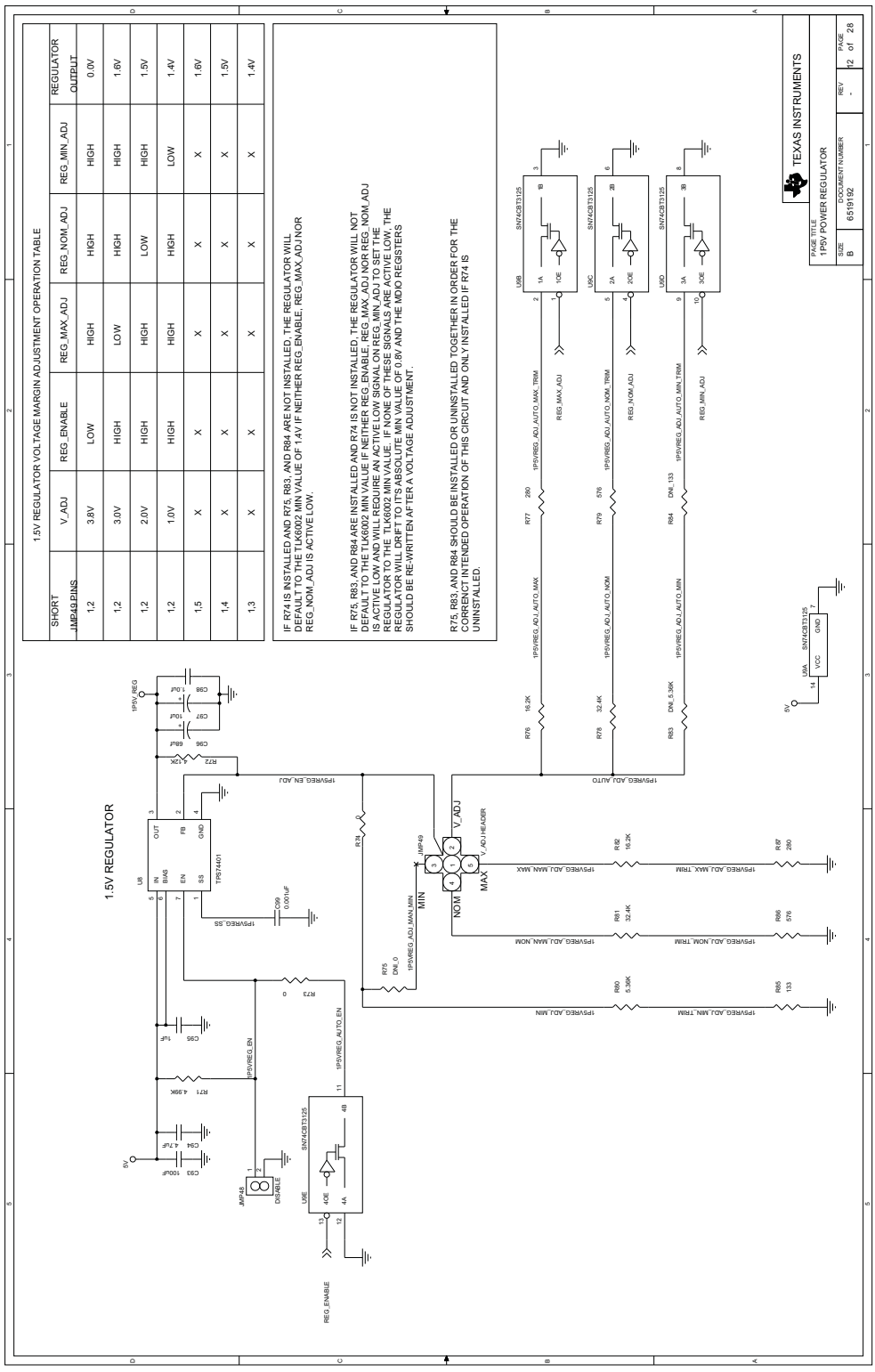


Figure 29. 1p5V Power Regulator, Sheet 12

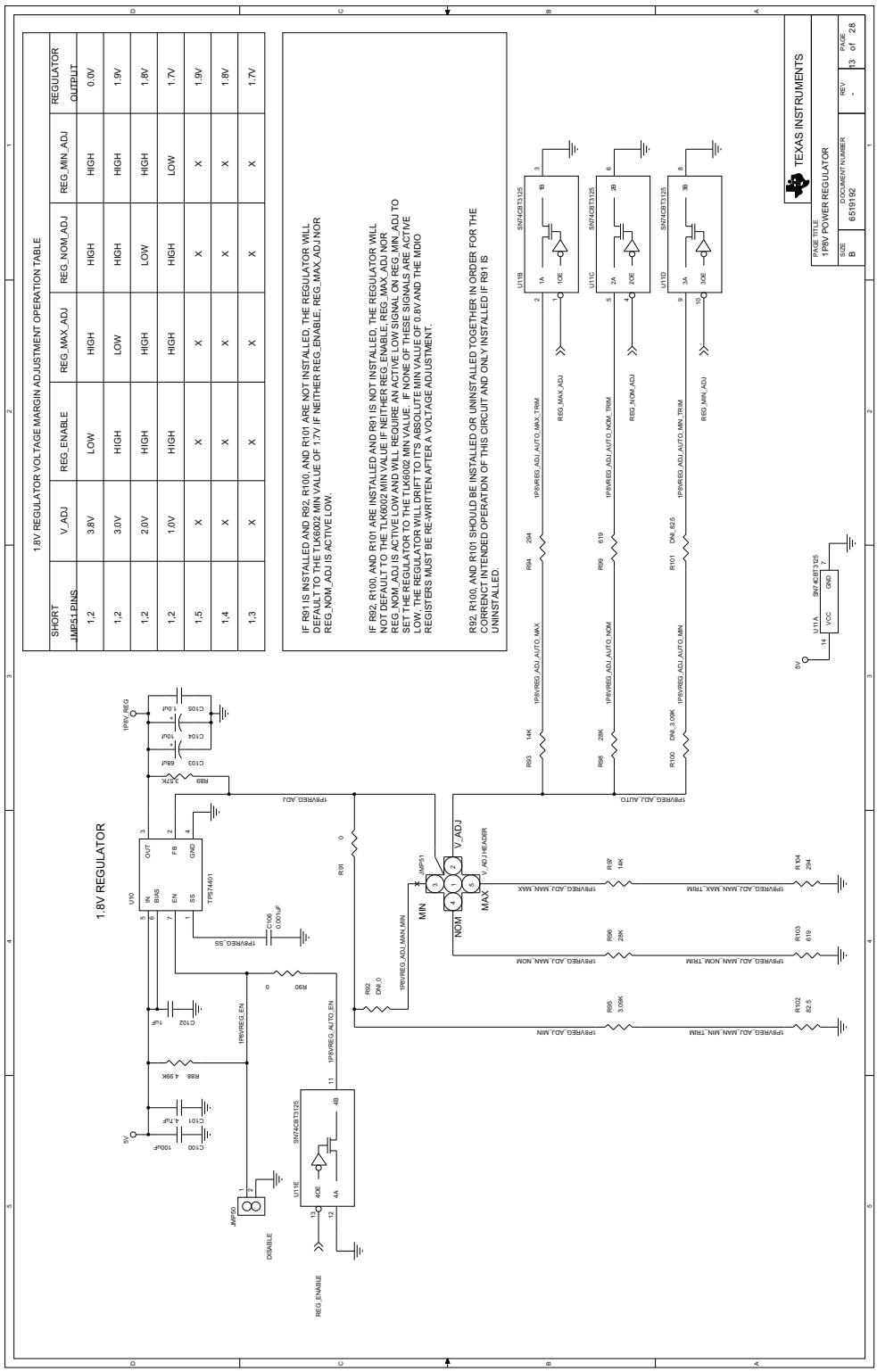


Figure 30. 1p8V Power Regulator, Sheet 13

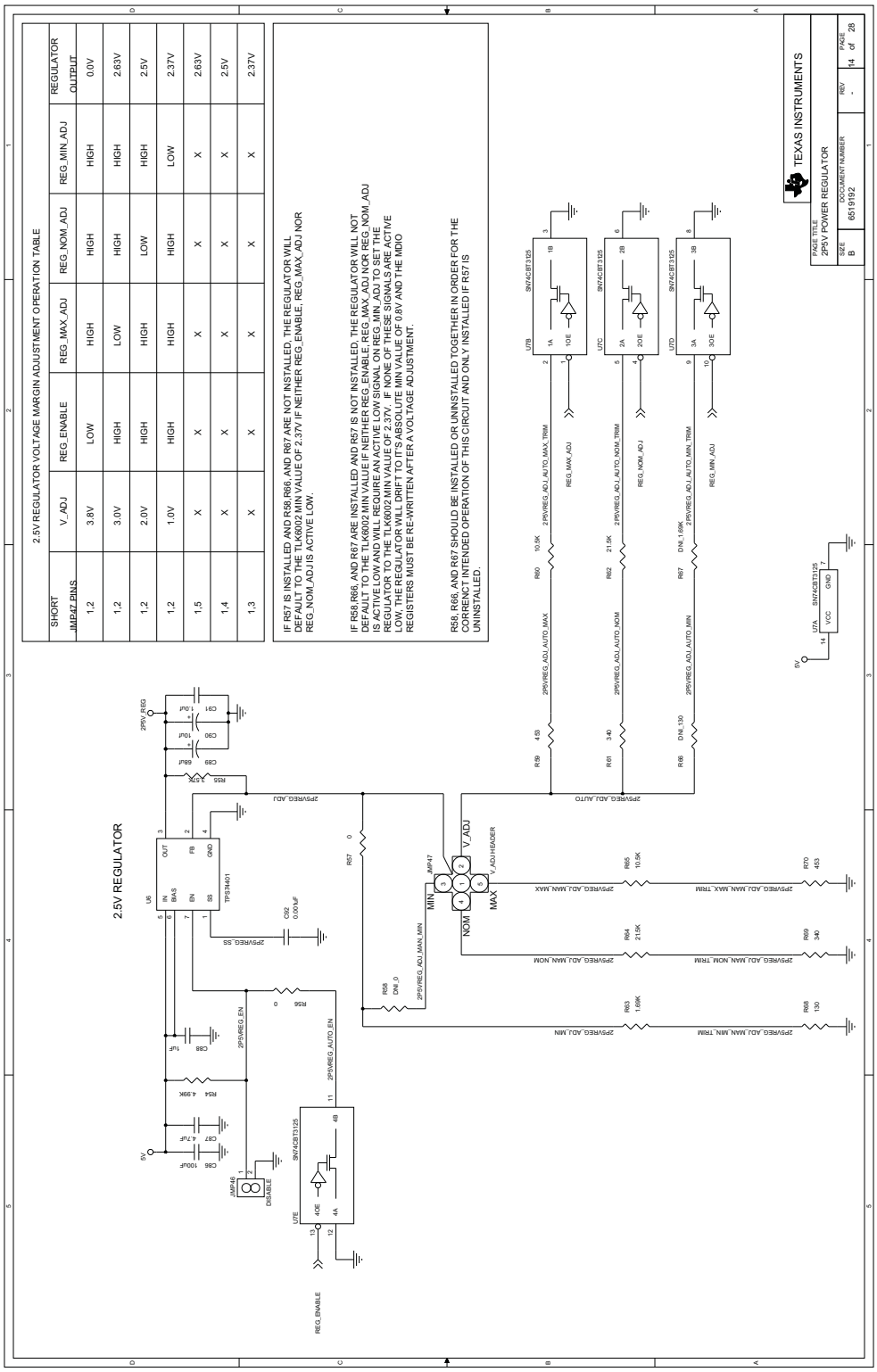


Figure 31. 2p5V Power Regulator, Sheet 14

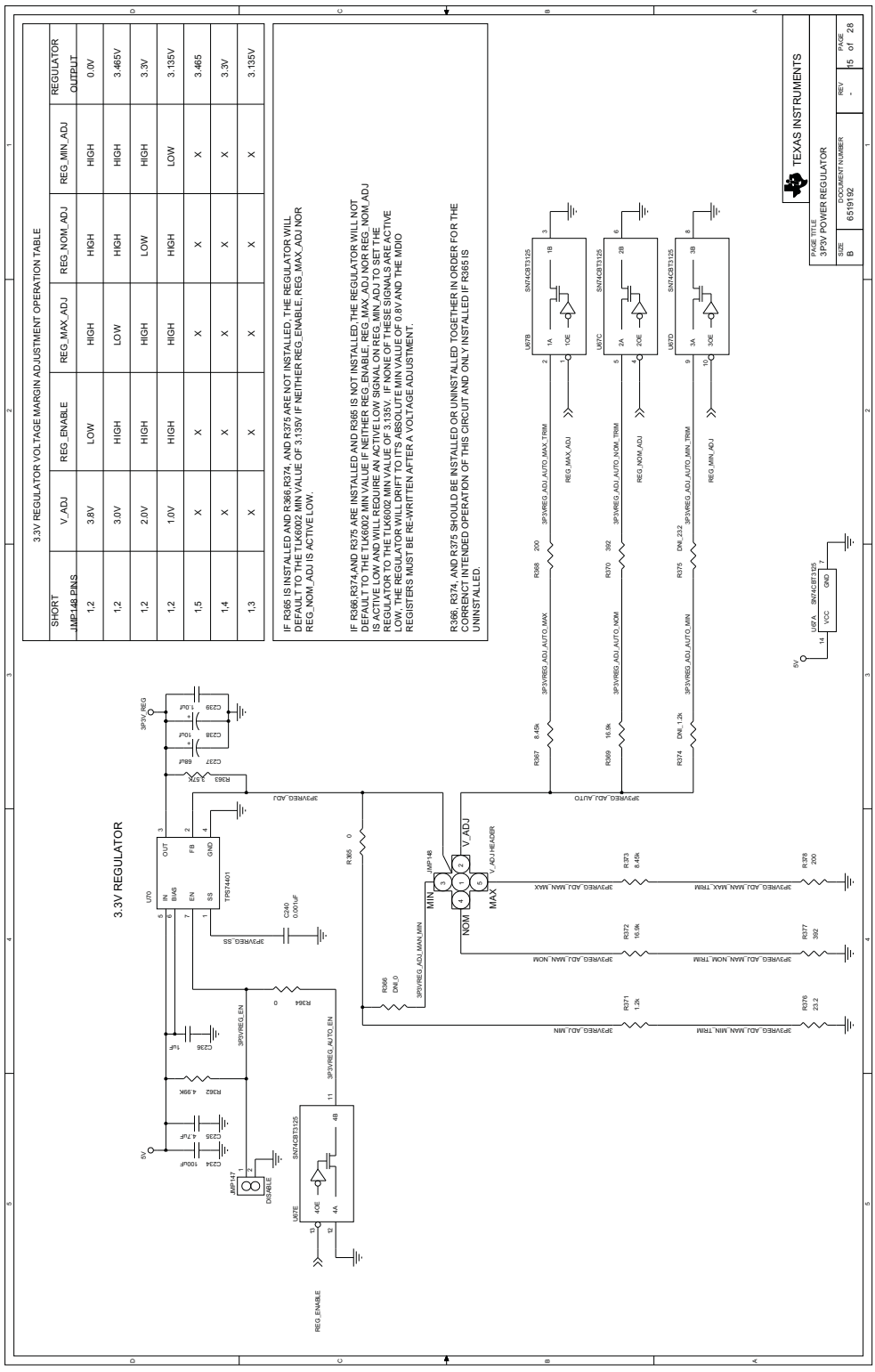


Figure 32. 3p3V Power Regulator, Sheet 15

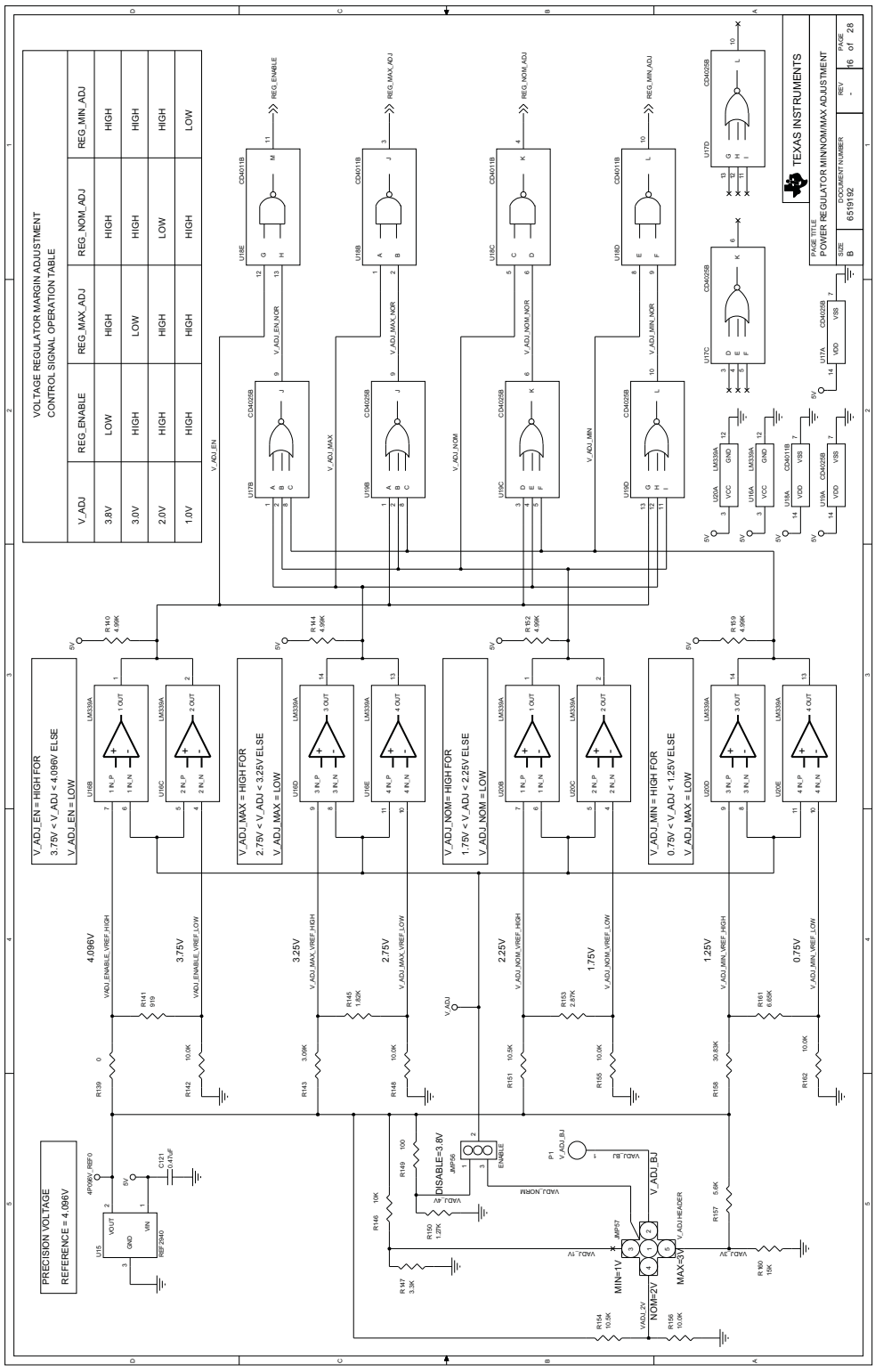


Figure 33. Power Regulator Min/Nom/Max Adjustment, Sheet 16

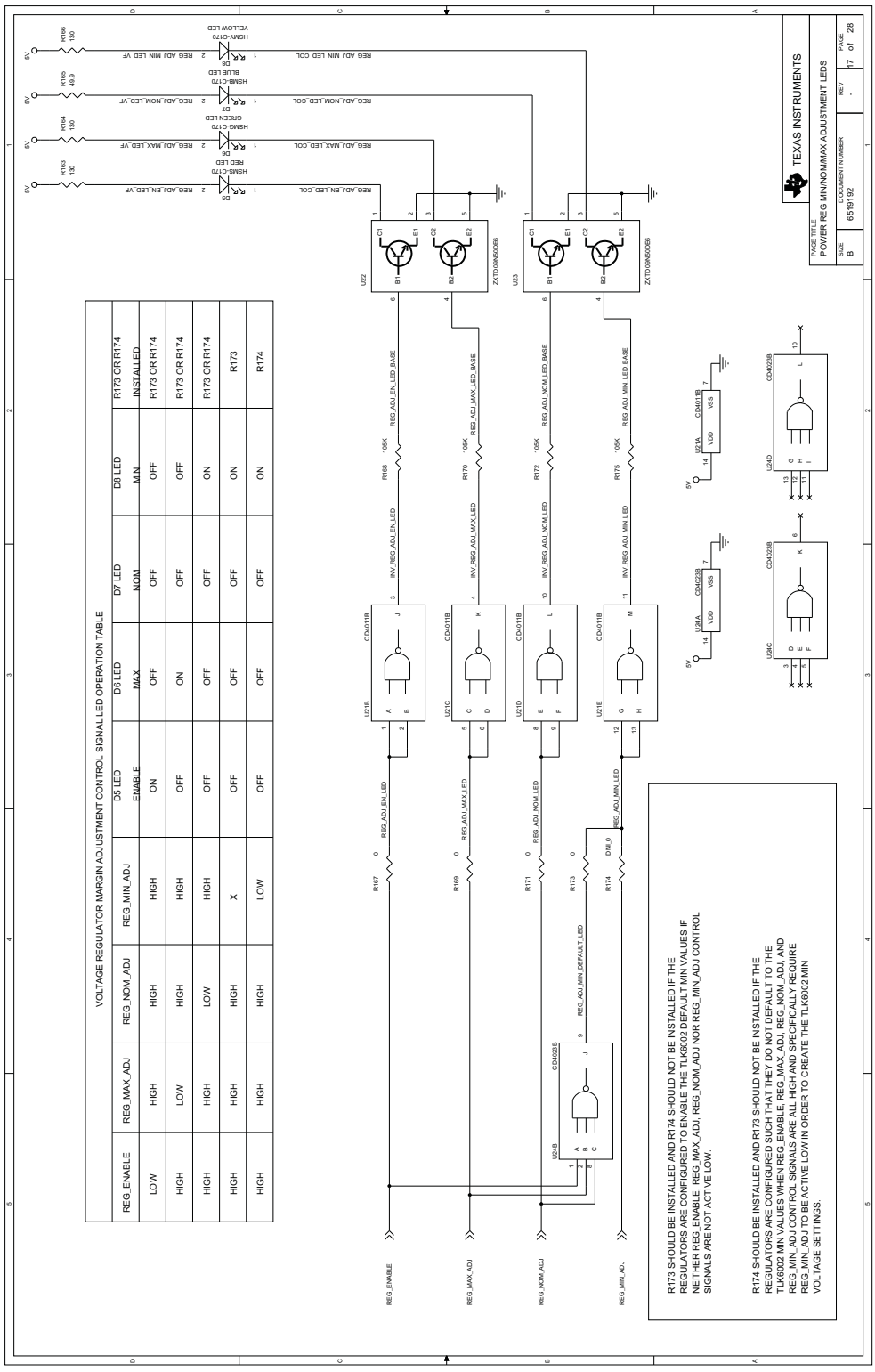


Figure 34. Power Regulator Min/Nom/Max Adjustment LEDs, Sheet 17

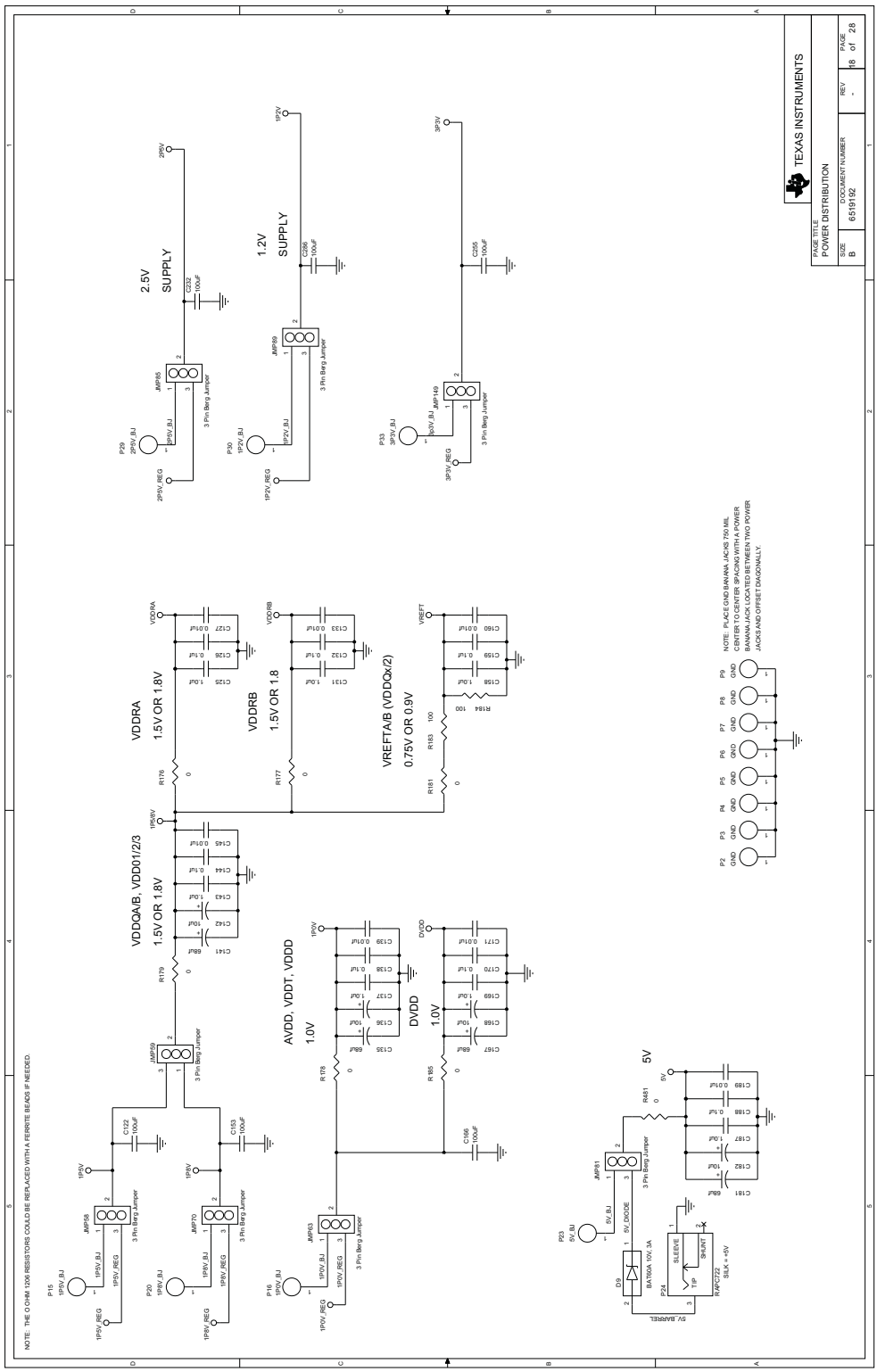


Figure 35. Power Distribution, Sheet 18

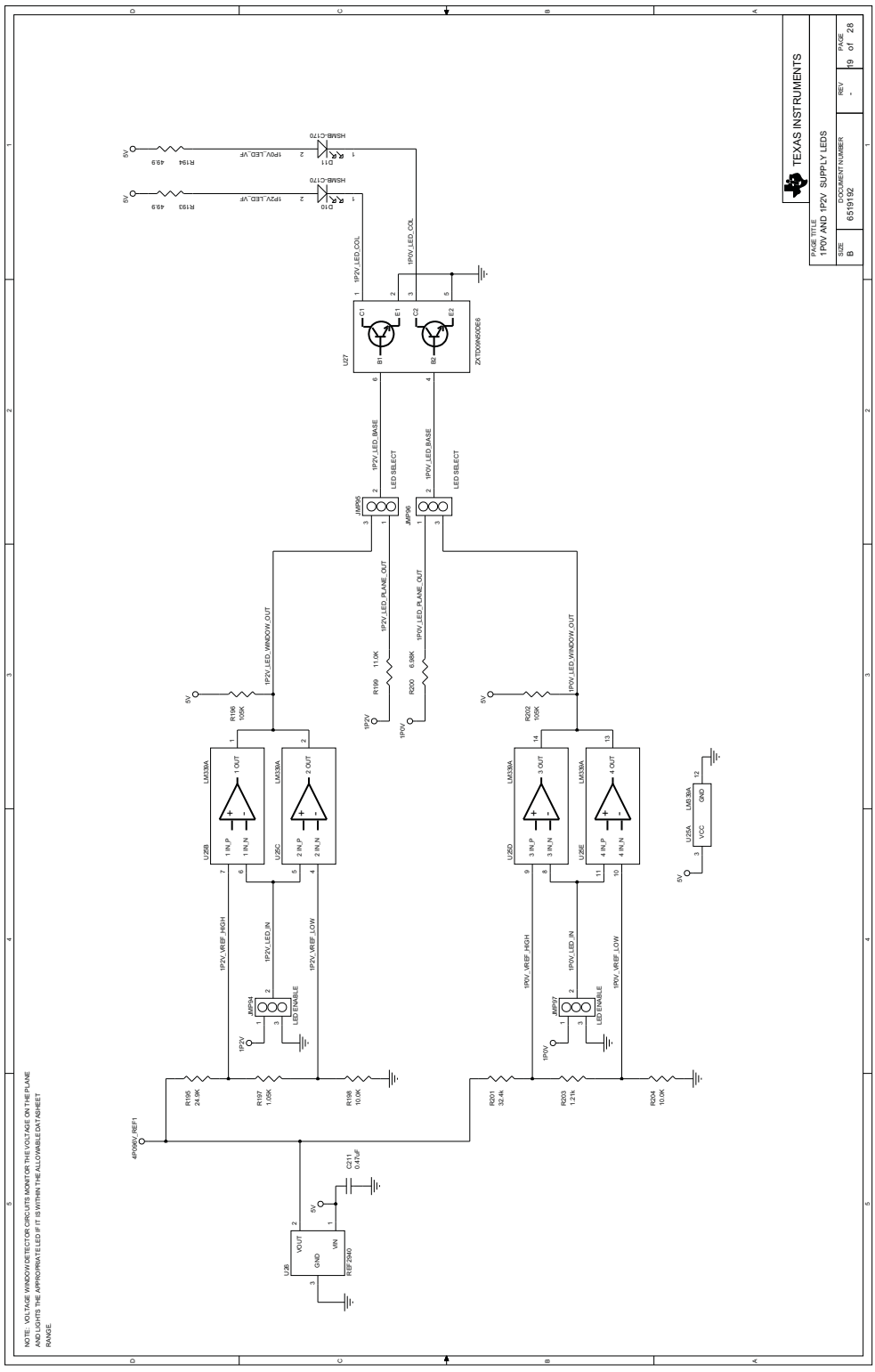


Figure 36. 1p0V and 1p2V Supply LEDs, Sheet 19

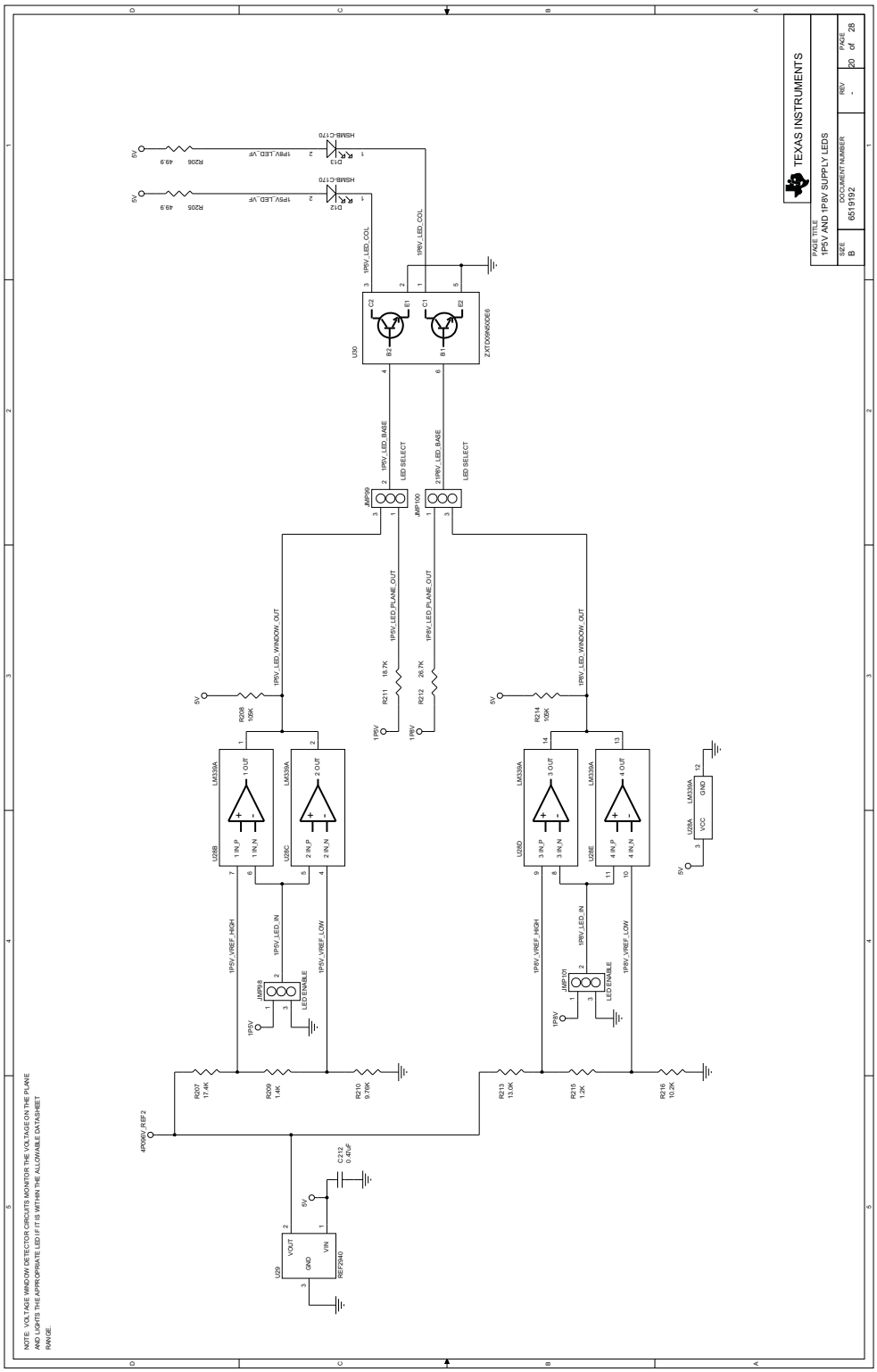


Figure 37. 1p5V and 1p8V Supply LEDs, Sheet 20

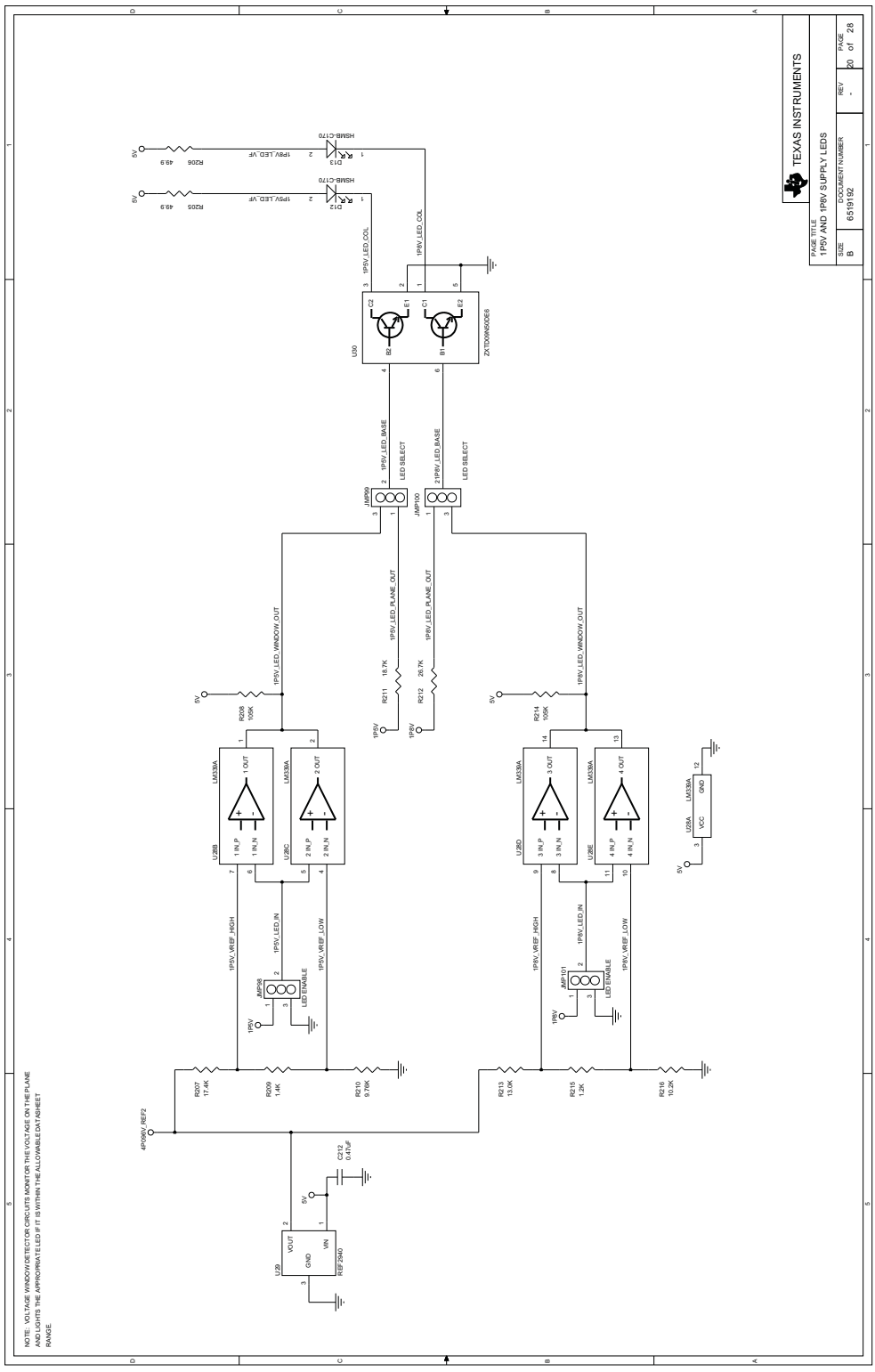


Figure 38. 2p5V, 3p3V, and 5V Supply LEDs, Sheet 21

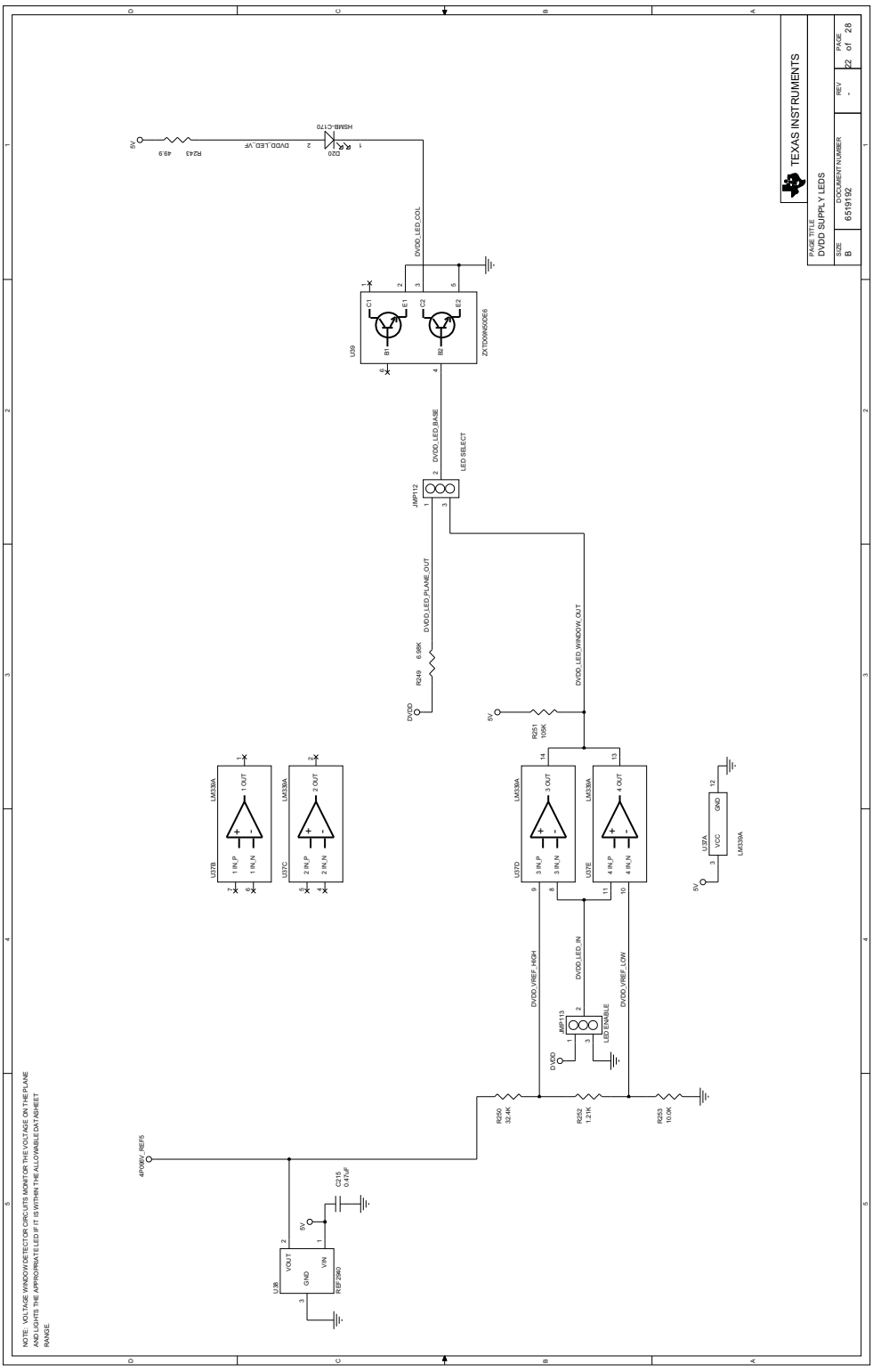


Figure 39. DVDD Supply LEDs, Sheet 22

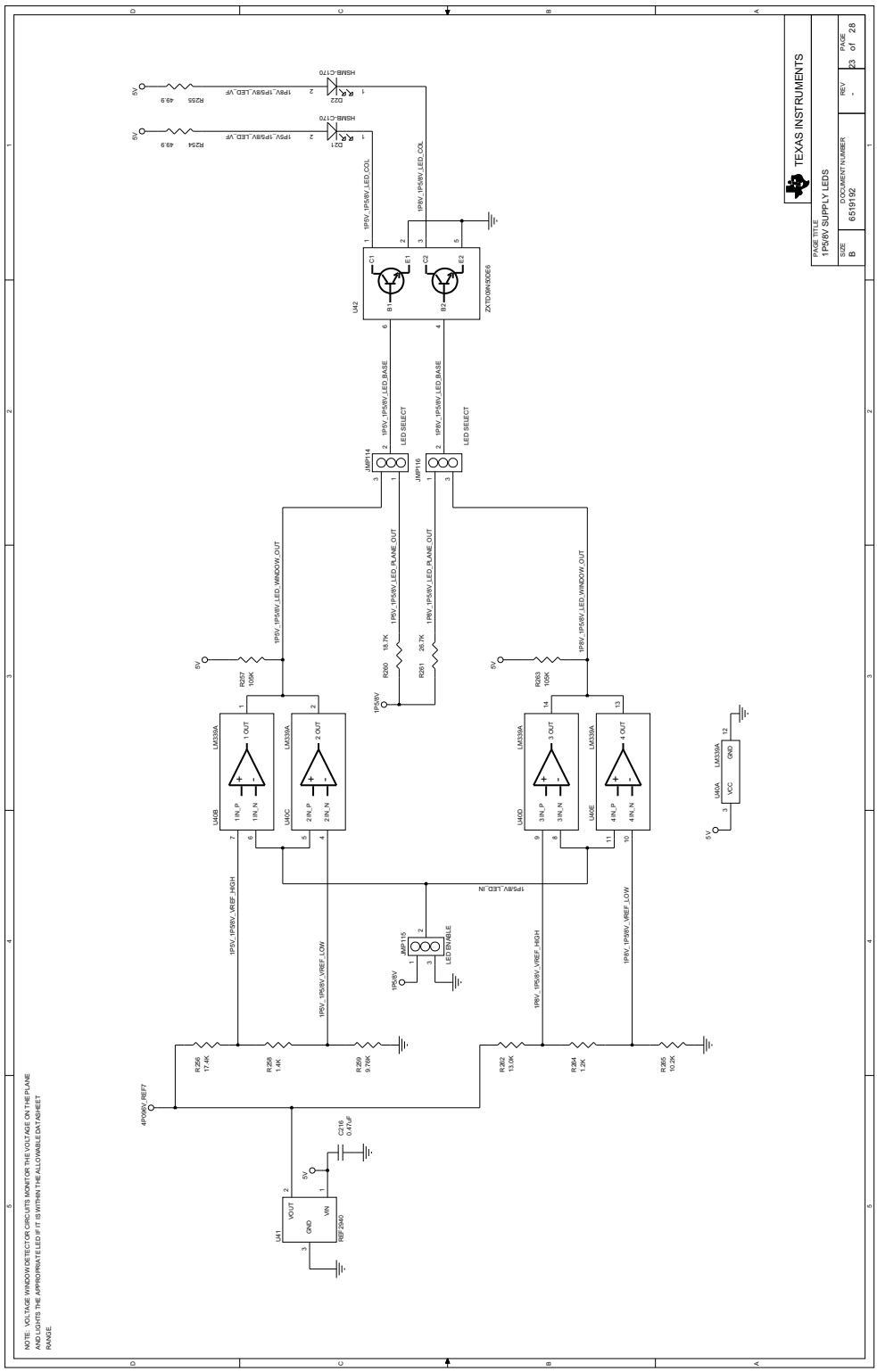


Figure 40. 1p5/8V Supply LEDs, Sheet 23

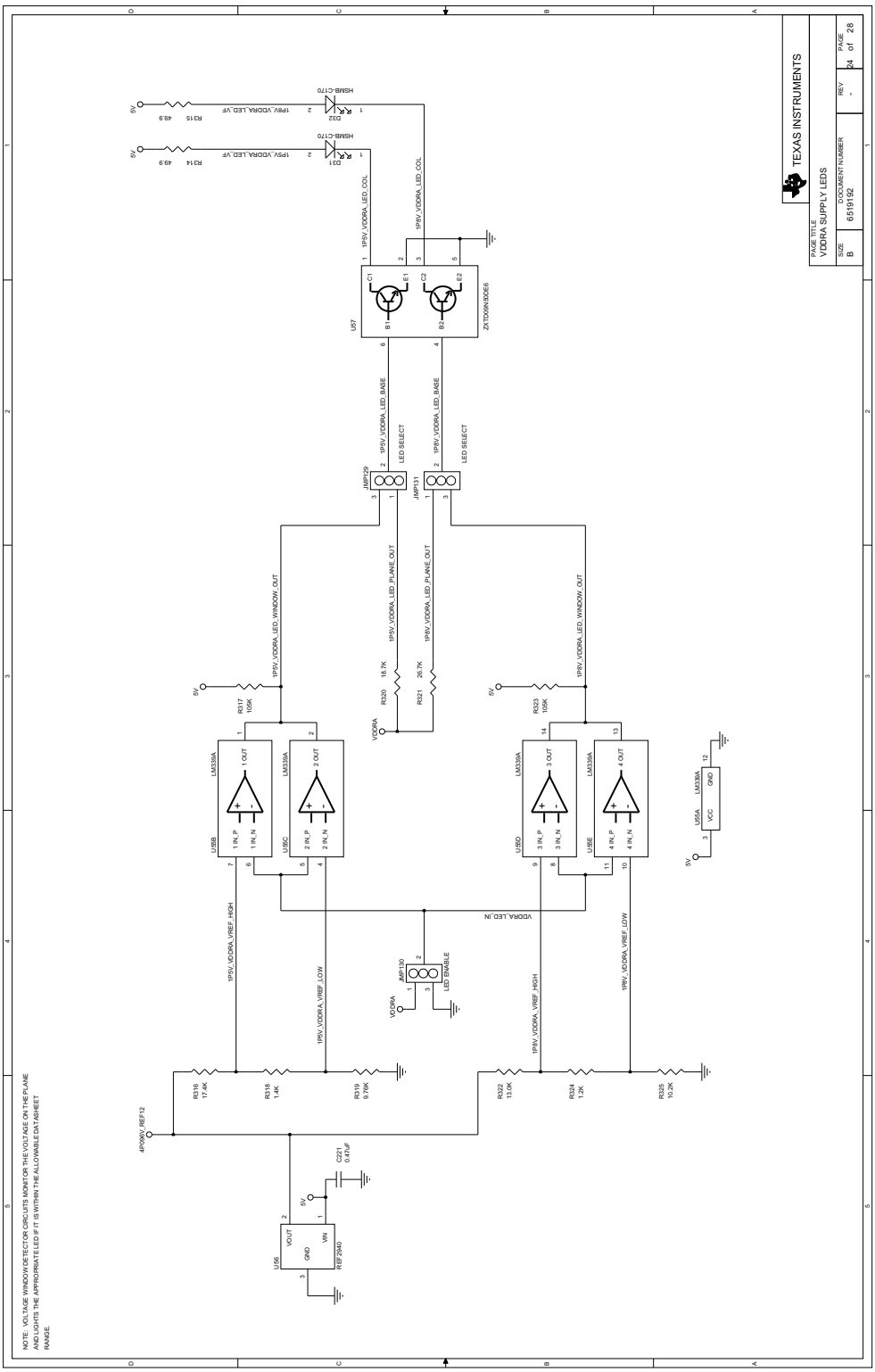


Figure 41. VDDRA Supply LEDs, Sheet 24

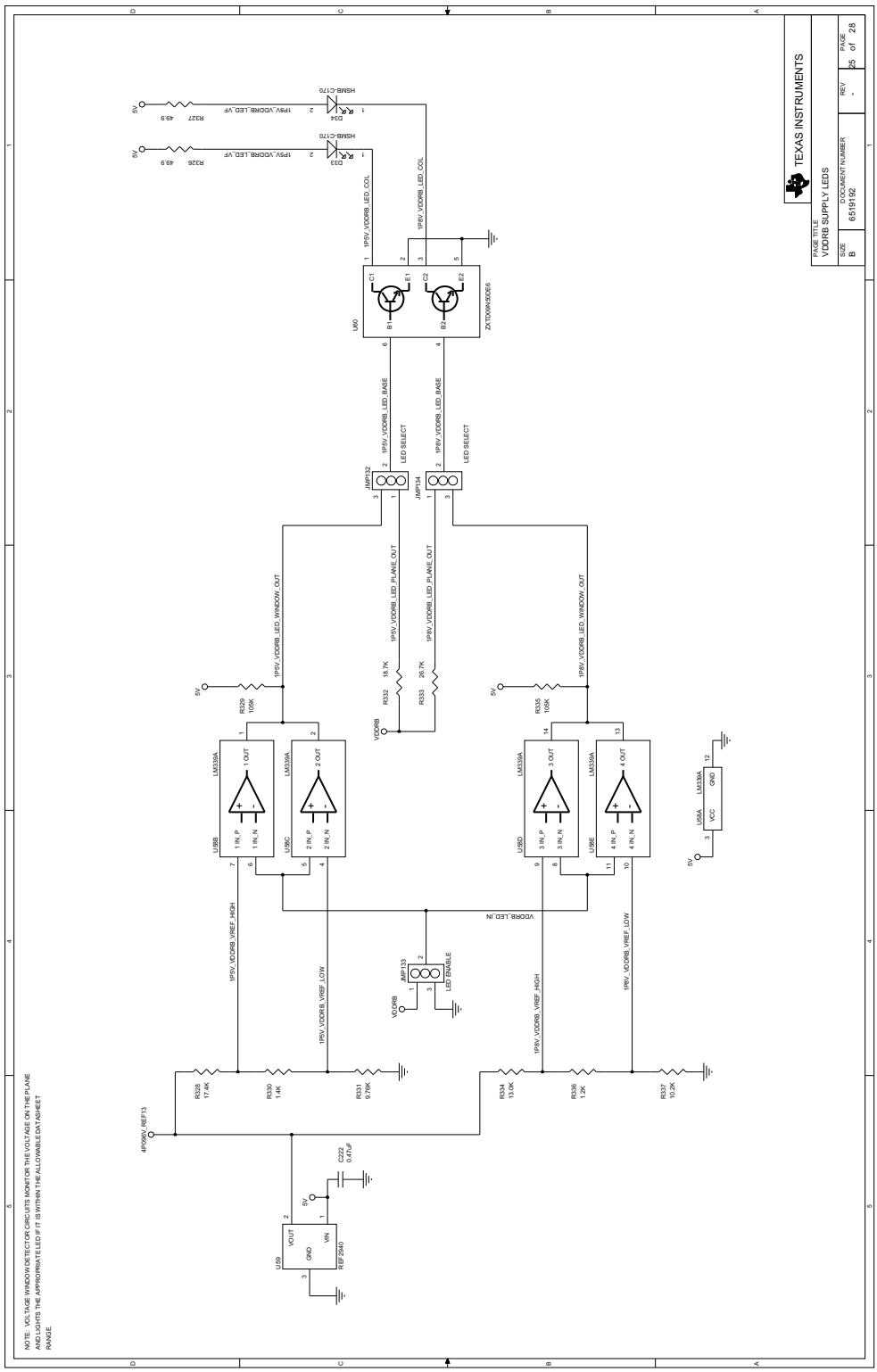


Figure 42. VDDRB Supply LEDs, Sheet 25

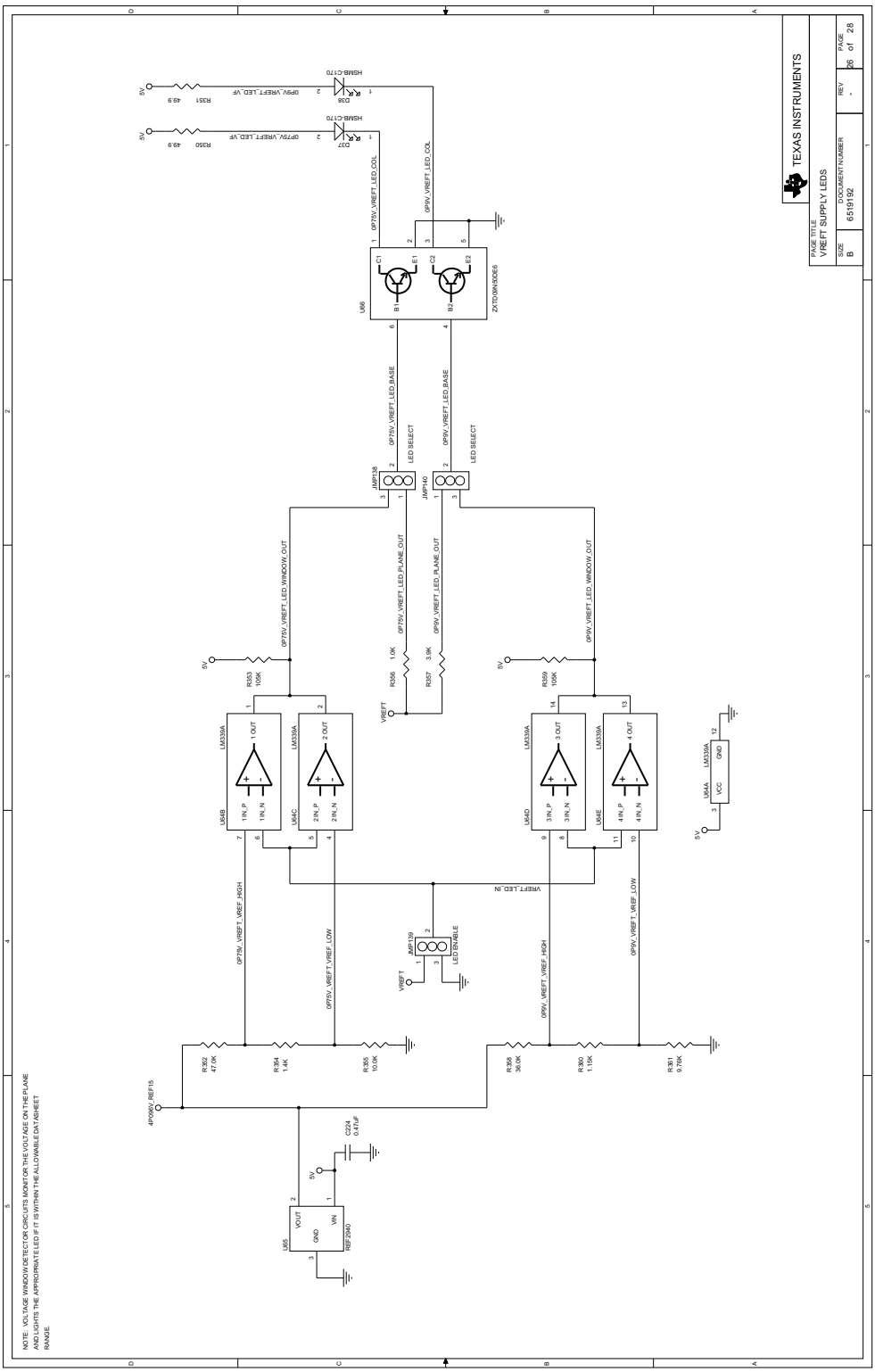


Figure 43. VREFT Supply LEDs, Sheet 26

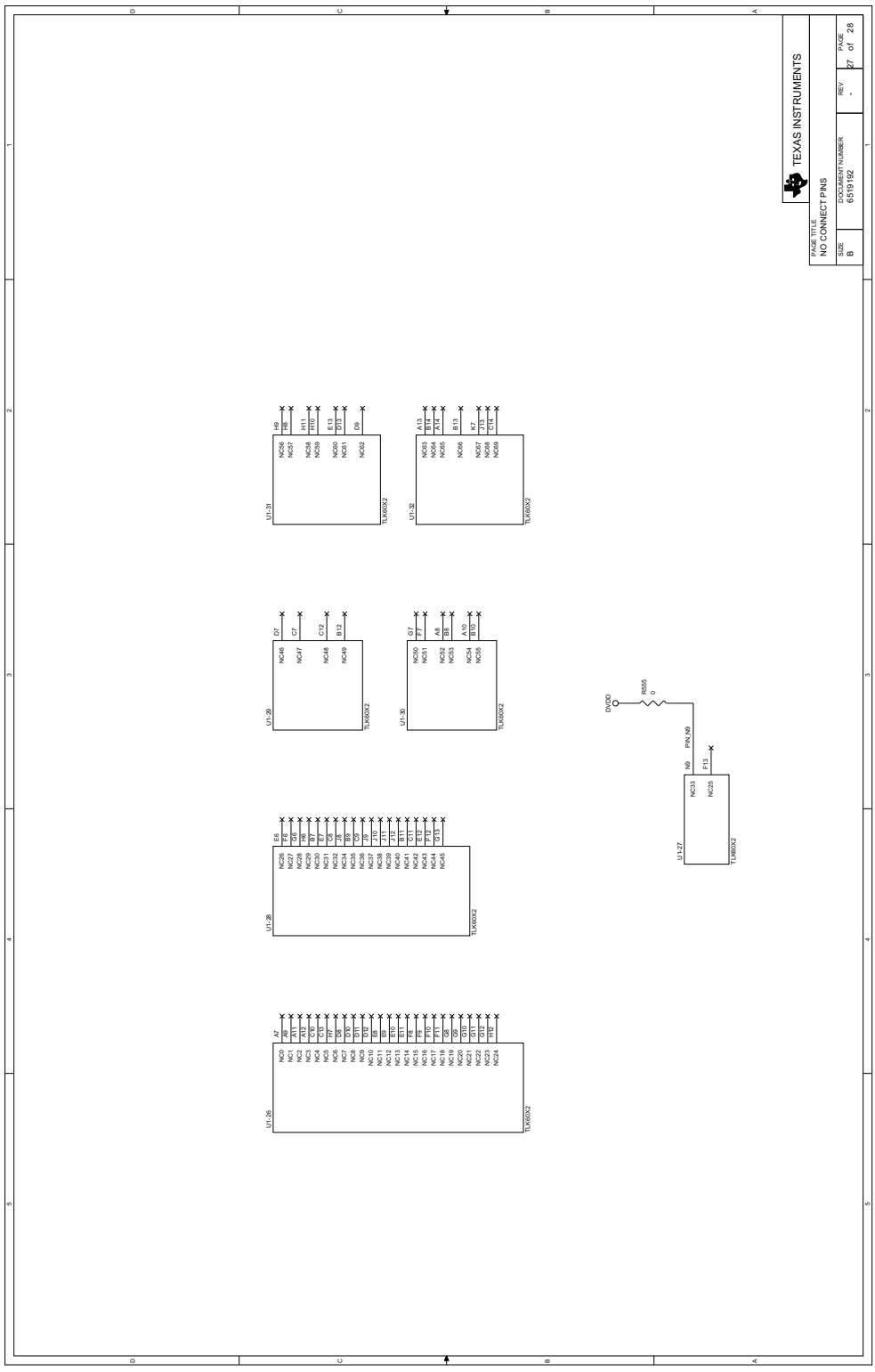


Figure 44. No Connect Pins, Sheet 27

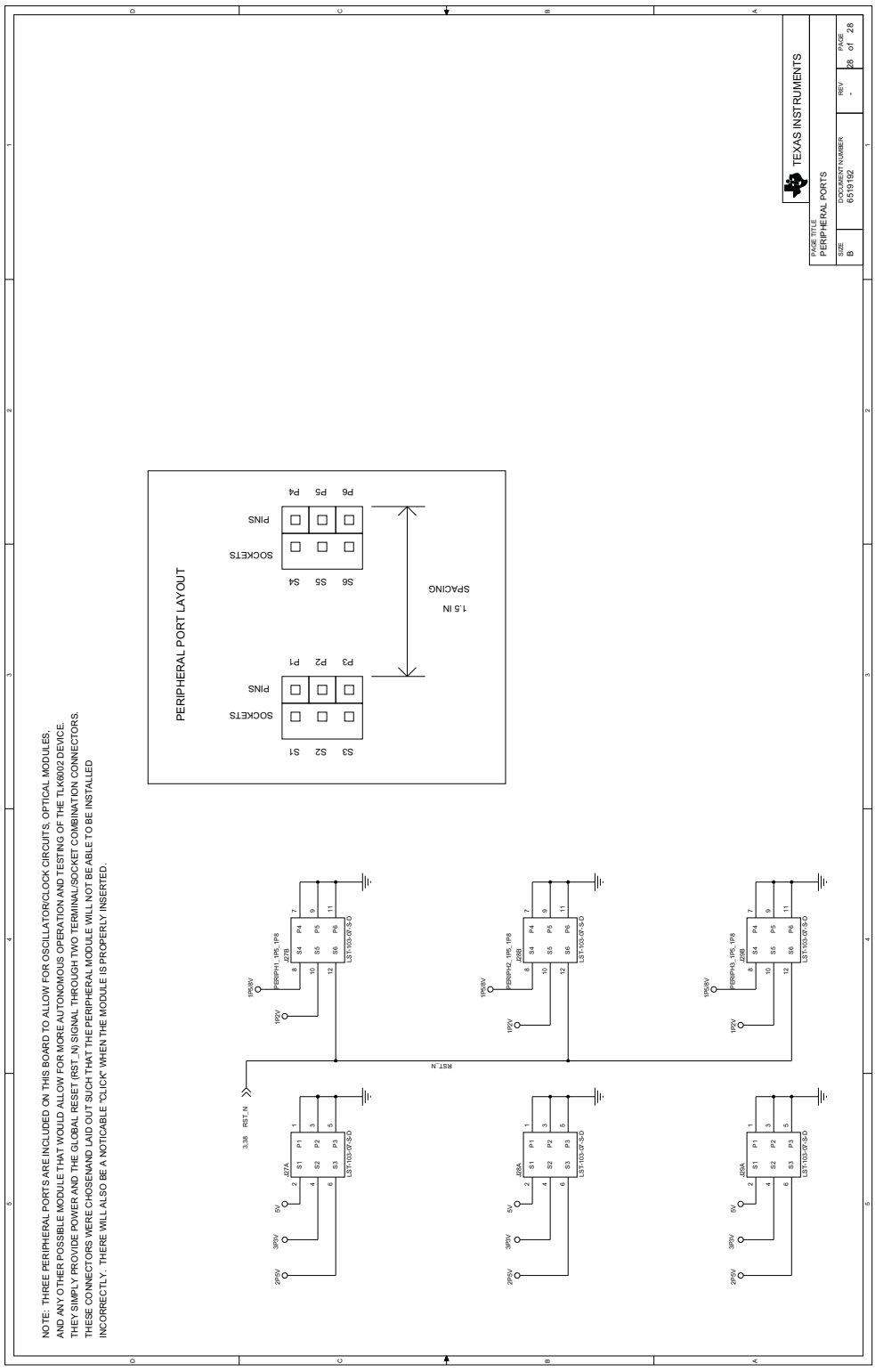


Figure 45. Peripheral Ports, Sheet 28

15 TLK6002EVM Bill of Materials

Table 1. Bill of Materials

Item	Qty	Reference	Value	Part	Part_Number	Manufacturer
1	3	C51, C322, C323	0.1μF	0201 CAP	C0201X5R6R3-104KNE	Venkel
2	15	C52, C64, C65, C66, C67, C68, C69, C70,C71, C72, C73, C74, C75, C76, C77	10000pF	0201 CAP	GRM033R71A103KA01D	Murata Electronics
3	4	C11, C27, C38, C58	0.01μF	0402 CAP	C0402X7R500-103KNE	Venkel
4	12	C9, C10, C25, C37, C41, C42, C43, C57,C315, C316, C320, C321	0.1μF	0402 CAP	C0402X7R160-104KNE	Venkel
5	7	C7, C8, C23, C24, C36, C50, C56	0.22μF	0402 CAP	EMK105BJ224KV-F	Taiyo Yuden
6	7	C5, C6, C21, C22, C35, C49, C55	0.47μF	0402 CAP	C0402X5R6R3-474KNE	Venkel
7	7	C3, C4, C19, C20, C34, C48, C319	1.0μF	0402 CAP	GRM155R61A105KE15D	Murata Electronics
8	3	C13, C29, C39	1000pF	0402 CAP	C0402COG500-102JNE	Venkel
9	2	C15, C31	100pF	0402 CAP	C0402COG500-101JNE	Venkel
10	6	C1, C2, C17, C18, C33, C47	2.2μF	0402 CAP	GRM155R60J225ME15D	Murata Electronics
11	1	C59	0.1μF	0603 CAP	06033C104JAT2A	Avx Corporation
12	9	C121, C211, C212, C213, C215, C216, C221, C222, C224	0.47μF	0603 CAP	C0603X7R160-474KNE	Venkel
13	7	C88, C95, C102, C109, C116, C236, C258	1.0μF	0603 CAP	C1608X7R1C105K	Tdk Corporation
14	6	C92, C99, C106, C113, C120, C240	1000pF	0603 CAP	C0603COG500-102JNE	Venkel
15	4	C84, C85, C256, C318	2.2μF	0603 CAP	GRM188R71A225KE15D	Murata Electronics
16	7	C87, C94, C101, C108, C115, C235, C317	4.7μF	0603 CAP	C0603X5R6R3-475KNE	Venkel
17	7	C127, C133, C139, C145, C160, C171, C189	0.01μF	0805 CAP	GRM21BR72A103KA01L	Murata Electronics
18	7	C126, C132, C138, C144, C159, C170, C188	0.1μF	1206 CAP	C1206C104J5RACTU	Kemet
19	13	C91, C98, C105, C112, C119, C125, C131, C137, C143, C158, C169, C187, C239	1.0μF	1206 CAP	C1206X7R500-105KNE	Murata Electronics
20	12	C86, C93, C100, C107, C114, C122, C153, C166, C232, C234, C255, C286	100μF	1812 CAP	GRM43SR60J107ME20L	Murata Electronics
21	10	C90, C97, C104, C111, C118, C136, C142, C168, C182, C238	10μF	7343-43 (EIA)	B45197A7106K509	Kemet
22	10	C89, C96, C103, C110, C117, C135, C141, C167, C181, C237	68μF - LESR	7361-38 (EIA)	B45197A4686K409	Kemet
23	11	R16, R139, R167, R169, R171, R173, R496, R516, R547, R549, R555	0.0 (Zero Ω)	0402 RES	ERJ-2GE0R00X	Panasonic - Ecg
24	1	R145	1.82K	0402 RES	ERJ-2RKF1821X	Panasonic - Ecg
25	4	R142, R148, R155, R162	10.0K	0402 RES	RG1005P-103-B-T5	Susumu Co Ltd

Table 1. Bill of Materials (continued)

Item	Qty	Reference	Value	Part	Part_Number	Manufacturer
26	1	R151	10.5K	0402 RES	RG1005P-1052-B-T5	Susumu Co Ltd
27	2	R508, R526	100K	0402 RES	RC0402FR-07100KL	Yageo America
28	4	R168, R170, R172, R175	105K	0402 RES	ERJ-2RKF1053X	Panasonic - Ecg
29	3	R163, R164, R166	130	0402 RES	RG1005P-131-B-T5	Susumu Co Ltd
30	1	R153	2.87K	0402 RES	RR0510P-2871-D	Susumu Co Ltd
31	6	R11, R12, R445, R446, R556, R558	20K	0402 RES	ERJ-2RKF2002X	Panasonic - Ecg
32	1	R143	3.09K	0402 RES	ERJ-2RKF3091X	Panasonic - Ecg
33	1	R158	30.9K	0402 RES	ERJ-2RKF3092X	Panasonic - Ecg
34	21	R491, R492, R493, R494, R495, R497, R498, R499, R505, R506, R509, R510, R511, R512, R513, R514, R515, R517, R523, R524, R529	4.99K	0402 RES	CR0402-16W-4991FT	Venkel
35	4	R38, R39, R520, R522	45.3K	0402 RES	ERJ-2RKF4532X	Panasonic - Ecg
36	3	R165, R507, R525	49.9	0402 RES	RG1005P-49R9-B-T5	Susumu Co Ltd
37	4	R18, R19, R20, R21	49.9	0402 RES	RR0510R-49R9-D	Susumu Co Ltd
38	1	R161	6.65K	0402 RES	ERJ-2RKF6651X	Panasonic - Ecg
39	1	R141	910	0402 RES	RG1005P-911-B-T5	Susumu Co Ltd
40	12	R56, R57, R73, R74, R90, R91, R107, R108, R124, R125, R364, R365	0.0 (Zero Ω)	0603 RES	ERJ-3GEY0R00V	Panasonic - Ecg
41	17	R356, R423, R424, R425, R435, R436, R437, R442, R447, R448, R449, R450, R455, R456, R471, R487, R488	1.00K	0603 RES	RR0816P-102-B-T5	Susumu Co Ltd
42	1	R228	1.02K	0603 RES	TNPW06031K02BEEA	Vishay/Dale
43	1	R197	1.05K	0603 RES	RR0816P-1051-B-T5-03H	Susumu Co Ltd
44	1	R221	1.10K	0603 RES	RG1608P-112-B-T5	Susumu Co Ltd
45	1	R123	1.13K	0603 RES	RR0816P-1131-D-06H	Susumu Co Ltd
46	1	R360	1.15K	0603 RES	RG1608P-1151-B-T5	Susumu Co Ltd
47	5	R215, R264, R324, R336, R371	1.20K	0603 RES	RG1608P-122-B-T5	Susumu Co Ltd
48	2	R203, R252	1.21K	0603 RES	RG1608P-1211-B-T5	Susumu Co Ltd
49	1	R150	1.27K	0603 RES	RR0816P-1271-D-11H	Susumu Co Ltd
50	5	R209, R258, R318, R330, R354	1.40K	0603 RES	RG1608P-1401-B-T5	Susumu Co Ltd
51	4	R42, R43, R44, R45	1.50K	0603 RES	RG1608P-152-B-T5	Susumu Co Ltd
52	1	R63	1.69K	0603 RES	RG1608P-1691-B-T5	Susumu Co Ltd
53	1	R225	1.96K	0603 RES	RN731JTTD1961B25	Koa Speer
54	7	R146, R156, R198, R204, R222, R253, R355	10.0K	0603 RES	ERA-3AEB103V	Panasonic - Ecg

Table 1. Bill of Materials (continued)

Item	Qty	Reference	Value	Part	Part_Number	Manufacturer
55	4	R216, R265, R325, R337	10.2K	0603 RES	RG1608P-1022-B-T5	Susumu Co Ltd
56	3	R60, R65, R154	10.5K	0603 RES	RG1608P-1052-B-T5	Susumu Co Ltd
57	1	R149	100	0603 RES	RG1608P-101-B-T5	Susumu Co Ltd
58	1	R4	100K	0603 RES	TNPW06031003BT9	Vishay/Dale
59	15	R196, R202, R208, R214, R220, R227, R251, R257, R263, R317, R323, R329, R335, R353, R359	105K	0603 RES	RR0816P-1053-B-T5-03D	Susumu Co Ltd
60	1	R199	11K	0603 RES	RG1608P-113-B-T5	Susumu Co Ltd
61	1	R136	127	0603 RES	ERJ-3EKF1270V	Panasonic - Ecg
62	4	R213, R262, R322, R334	13.0K	0603 RES	RG1608P-133-B-T5	Susumu Co Ltd
63	9	R2, R5, R24, R25, R68, R519, R521, R557, R559	130	0603 RES	RG1608P-131-B-T5	Susumu Co Ltd
64	1	R85	133	0603 RES	RG1608P-1330-B-T5	Susumu Co Ltd
65	2	R93, R97	14.0K	0603 RES	TNPW060314K0BEEA	Vishay/Dale
66	1	R160	15.0K	0603 RES	RG1608P-153-B-T5	Susumu Co Ltd
67	2	R76, R82	16.2K	0603 RES	RR0816P-1622-D-21C	Susumu Co Ltd
68	2	R110, R114	16.5K	0603 RES	RG1608P-1652-B-T5	Susumu Co Ltd
69	2	R369, R372	16.9K	0603 RES	TNPW060316K9BEEA	Vishay/Dale
70	2	R128, R138	169	0603 RES	TNPW0603169RBEEN	Vishay/Dale
71	4	R207, R256, R316, R328	17.4K	0603 RES	RR0816P-1742-B-T5-24C	Susumu Co Ltd
72	2	R130, R132	18.0K	0603 RES	RG1608P-183-B-T5	Susumu Co Ltd
73	4	R211, R260, R320, R332	18.7K	0603 RES	RG1608P-1872-B-T5	Susumu Co Ltd
74	1	R106	2.49K	0603 RES	RG1608P-2491-B-T5	Susumu Co Ltd
75	2	R368, R378	200	0603 RES	RG1608P-201-B-T5	Susumu Co Ltd
76	2	R62, R64	21.5K	0603 RES	RN731JTTD2152B25	Koa Speer
77	1	R376	23.2	0603 RES	ERJ-3EKF23R2V	Panasonic - Ecg
78	1	R195	24.9K	0603 RES	RG1608P-2492-B-T5	Susumu Co Ltd
79	1	R119	243	0603 RES	288-0603-243-RC	Xicon
80	4	R212, R261, R321, R333	26.7K	0603 RES	RR0816P-2672-B-T5-42C	Susumu Co Ltd
81	2	R96, R98	28.0K	0603 RES	RNCF 16 T9 28K .1% I	Stackpole Electronics Inc
82	2	R77, R87	280	0603 RES	TNPW0603280RBEEA	Vishay/Dale
83	2	R94, R104	294	0603 RES	MCR03EZPFX2940	Rohm
84	1	R95	3.09K	0603 RES	RN731JTTD3091B25	Koa Speer
85	1	R147	3.30K	0603 RES	RG1608P-332-B-T5	Susumu Co Ltd
86	3	R55, R89, R363	3.57K	0603 RES	RG1608P-3571-B-T5	Susumu Co Ltd

Table 1. Bill of Materials (continued)

Item	Qty	Reference	Value	Part	Part_Number	Manufacturer
87	1	R357	3.90K	0603 RES	RG1608P-392-B-T5	Susumu Co Ltd
88	6	R78, R81, R113, R115, R201, R250	32.4K	0603 RES	RG1608P-3242-B-T5	Susumu Co Ltd
89	2	R61, R69	340	0603 RES	288-0603-340-RC	Xicon
90	1	R358	36.0K	0603 RES	RR0816P-363-B-T5	Susumu Co Ltd
91	2	R370, R377	392	0603 RES	TNPW0603392RBEEN	Vishay/Dale
92	1	R72	4.12K	0603 RES	RG1608P-4121-B-T5	Susumu Co Ltd
93	37	R1, R6, R7, R8, R22, R23, R26, R28, R29, R30, R31, R32, R33, R34, R35, R37, R40, R41, R48, R49, R50, R51, R52, R54, R71, R88, R105, R122, R140, R144, R152, R159, R362, R422, R438, R467, R527	4.99K	0603 RES	RG1608P-4991-B-T5	Susumu Co Ltd
94	1	R223	41.2K	0603 RES	RG1608P-4122-B-T5	Susumu Co Ltd
95	2	R59, R70	453	0603 RES	RG1608P-4530-B-T5	Susumu Co Ltd
96	1	R352	47.0K	0603 RES	RG1608P-473-B-T5	Susumu Co Ltd
97	19	R3, R193, R194, R205, R206, R217, R218, R226, R243, R254, R255, R314, R315, R326, R327, R350, R351, R443, R444	49.9	0603 RES	RG1608P-49R9-B-T1	Susumu Co Ltd
98	1	R80	5.36K	0603 RES	TNPW06035K36BEEA	Vishay/Dale
99	1	R157	5.60K	0603 RES	RG1608P-562-B-T5	Susumu Co Ltd
100	1	R112	5.62K	0603 RES	RG1608P-5621-B-T5	Susumu Co Ltd
101	1	R129	5.90K	0603 RES	RG1608P-5901-B-T5	Susumu Co Ltd
102	2	R79, R86	576	0603 RES	ERJ-3EKF5760V	Panasonic - Ecg
103	1	R219	6.19K	0603 RES	RR0816P-6191-B-T5-77H	Susumu Co Ltd
104	2	R200, R249	6.98K	0603 RES	CR0603-10W-6981FT	Venkel
105	1	R224	60.4K	0603 RES	ERJ-3EKF6042V	Panasonic - Ecg
106	2	R99, R103	619	0603 RES	RR0816P-6190-D-77A	Susumu Co Ltd
107	2	R111, R121	66.5	0603 RES	MCR03EZPFX66R5	Rohm
108	2	R116, R120	665	0603 RES	TNPW0603665RBEEN	Vishay/Dale
109	2	R367, R373	8.45K	0603 RES	RG1608P-8451-B-T5	Susumu Co Ltd
110	2	R127, R131	8.87K	0603 RES	TNPW06038K87BEEN	Vishay/Dale
111	1	R102	82.5	0603 RES	RR0816Q-82R5-D-89R	Susumu Co Ltd
112	2	R133, R137	86.6	0603 RES	ERJ-3EKF86R6V	Panasonic - Ecg
113	6	R210, R229, R259, R319, R331, R361	9.76K	0603 RES	RG1608P-9761-B-T5	Susumu Co Ltd
114	2	R183, R184	100	0805 RES	RG2012P-101-B-T5	Susumu Co Ltd
115	7	R176, R177, R178, R179, R181, R185, R481	0.0 (Zero Ω)	1210 RES	RK73Z2ETTE	Koa Speer

Table 1. Bill of Materials (continued)

Item	Qty	Reference	Value	Part	Part_Number	Manufacturer
116	1	D9	Zener Diode	SOD-323	BAT 60A E6327	Infineon Technologies
117	6	Q1, Q2, Q3, Q4, Q5, Q6	NFET	SOT-23	FDV301N	Fairchild Semiconductor
118	15	U3, U4, U5, U22, U23, U27, U30, U33, U39, U42, U57, U60, U66, U88, U92	Dual NPN	SOT-23-6	ZXTD09N50DE6TA	Zetex Inc
119	1	U24	3-Input NAND	14-SOIC	CD4023BME4	Texas Instruments
120	10	U16, U20, U25, U28, U31, U37, U40, U55, U58, U64	Differential Comparator	14-SOIC	LM339AD	Texas Instruments
121	2	U18, U21	2-Input NAND	14-SOIC (3.9mm Width)	CD4011BM	Texas Instruments
122	2	U17, U19	3-Input NOR	14-SOIC (3.9mm Width)	CD4025BM96	Texas Instruments
123	6	U7, U9, U11, U12, U14, U67	Quadruple FET Bus Switch	14-SOIC (3.9mm Width)	SN74CBT3125D	Texas Instruments
124	2	U85, U86	J/K Flip-Flop	14-TSSOP	SN74LVC112APWR	Texas Instruments
125	4	U82, U83, U84, U91	Bi-Directional Level Shifter	20-QFN	TXS0108ERGYR	Texas Instruments
126	6	U6, U8, U10, U13, U69, U70	Adjustable LDO	7-DD	TPS74201KTWT	Texas Instruments
127	9	U15, U26, U29, U32, U38, U41, U56, U59, U65	Precision Voltage Reference	SOT-23	REF2940AIDBZT	Texas Instruments
128	3	U2, U87, U89	Voltage Supervisor with Manual Reset	SOT-23-5	TPS3125J18DBVR	Texas Instruments
129	1	U90	Bi-Directional Level Shifter	SOT-23-6	SN74AVCH1T45DCKR	Texas Instruments
130	1	U1	6.25Gbps SerDes	324 PBGA	TLK6002	Texas Instruments
131	21	D7, D10, D11, D12, D13, D14, D15, D16, D20, D21, D22, D31, D32, D33, D34, D37, D38, D41, D42, D51, D52	LED - Blue Diffused	C170	HSMB-C170	Avago Technologies Us Inc
132	4	D2, D6, D4, D50	LED - Green Diffused	C170	HSMG-C170	Avago Technologies Us Inc
133	4	D1, D5, D3, D49	LED - Red Diffused	C170	SML-LXT0805IW-TR	Lumex Opto/Components Inc
134	1	D8	LED - Yellow Diffused	C170	HSMY-C170	Avago Technologies Us Inc
135	3	SW1, SW3, SW4	Push Button	6mm	EVQ-PBE05R	Panasonic - Ecg
136	6	J27, J28, J29	Connector	0.1x0.1”	LST-103-07-S-D	Samtec
137	1	JMP30	20 Pin - Shrouded	0.1" SP	5103308-5	Tyco Electronics/Amp
138	19	JMP1, JMP3, JMP4, JMP6, JMP7, JMP8,JMP15, JMP31, JMP16, JMP24, JMP25, JMP28, JMP21, JMP46, JMP48, JMP50, JMP52, JMP54, JMP147	1 X 2	0.1"	HTSW-150-08-G-S	Samtec

Table 1. Bill of Materials (continued)

Item	Qty	Reference	Value	Part	Part_Number	Manufacturer
139	36	JMP14, JMP58, JMP59, JMP63, JMP70, JMP81, JMP85, JMP89, JMP149, JMP56, JMP94, JMP97, JMP98, JMP101, JMP102, JMP105, JMP113, JMP115, JMP130, JMP133, JMP139, JMP95, JMP96, JMP99, JMP100, JMP103, JMP104, JMP112, JMP114, JMP116, JMP129, JMP131, JMP132, JMP134, JMP138, JMP140	1 X 3	0.1"	HTSW-150-08-G-S	Samtec
140	2	JMP145, JMP146	1 X 4	0.1"	HTSW-150-08-G-S	Samtec
141	7	JMP47, JMP49, JMP51, JMP53, JMP55, JMP57, JMP148	1 X 5 +	0.1"	HTSW-150-08-G-S	Samtec
142	3	JMP23, JMP29, JMP43	2 X 2	0.1x0.1”	HTSW-150-08-G-D	Samtec
143	1	JMP36	2 X 4	0.1x0.1"	HTSW-150-08-G-D	Samtec
144	4	JMP17, JMP33, JMP35, JMP45	2 X 5	0.1x0.1"	HTSW-150-08-G-D	Samtec
145	2	JMP26, JMP27	2 X 6	0.1x0.1"	HTSW-150-08-G-D	Samtec
146	8	JMP37, JMP38, JMP39, JMP40	20 X 3	0.1x0.1"	HTSW-150-08-G-T	Samtec
147	1	P24	Power Jack	2.1mm	PJ-002AH	Cui Inc
148	16	P1, P2, P3, P4, P5, P6, P7, P8, P9, P15, P16, P20, P23, P29, P30, P33	Banana Plug - Metal	4mm	108-0740-001	Emerson Network Power Co
149	14	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14	Connector	SMP	19S101-40ML5	Rosenberger
150			Shunt	0.1"	151-8000-E	Kobiconn
151	5	Screws	4-40/0.25"	Round	PMSSS 440 0025 PH	Building Fasteners
152	5	Standoff	0.75"	Round Threaded	2029	Keystone Electronics
153	2	C78, C79	Capacitors	DNI		
154	42	R9, R10, R14, R15, R27, R36, R46, R47, R58, R75, R92, R109, R126, R366, R421, R426, R469, R470, R66, R67, R83, R84, R100, R101, R117, R118, R134, R135, R420, R432, R433, R434, R485, R486, R489, R490	0603 Resistors	DNI		
155	11	R174, R427, R428, R429, R430, R431, R501, R518, R548, R550, R528	0402 Resistors	DNI		
156	4	R530, R531, R532, R533	0402 Resistors	DNI		

16 TLK6002EVM Board Layouts

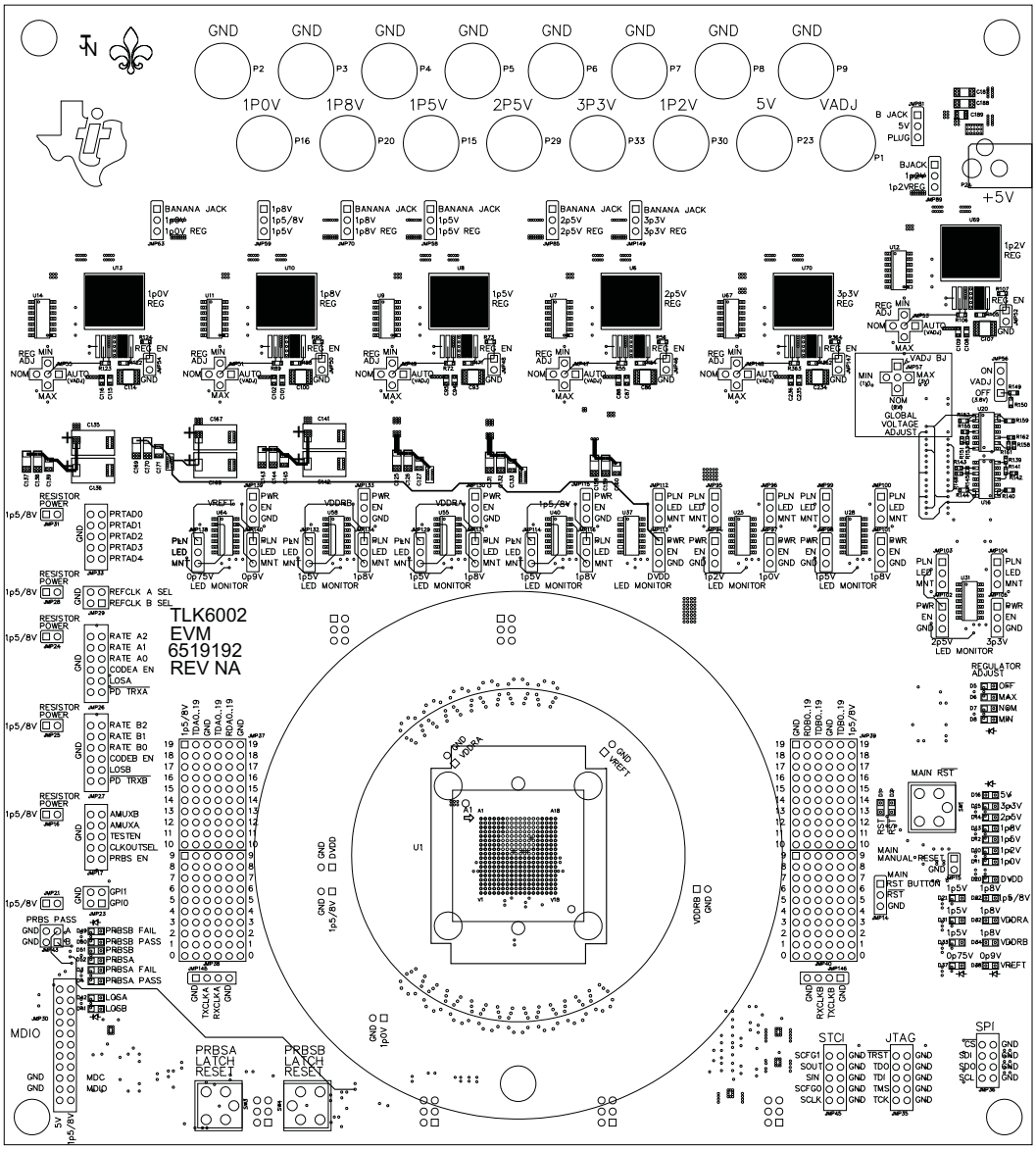


Figure 46. Top Signal, Layer 1

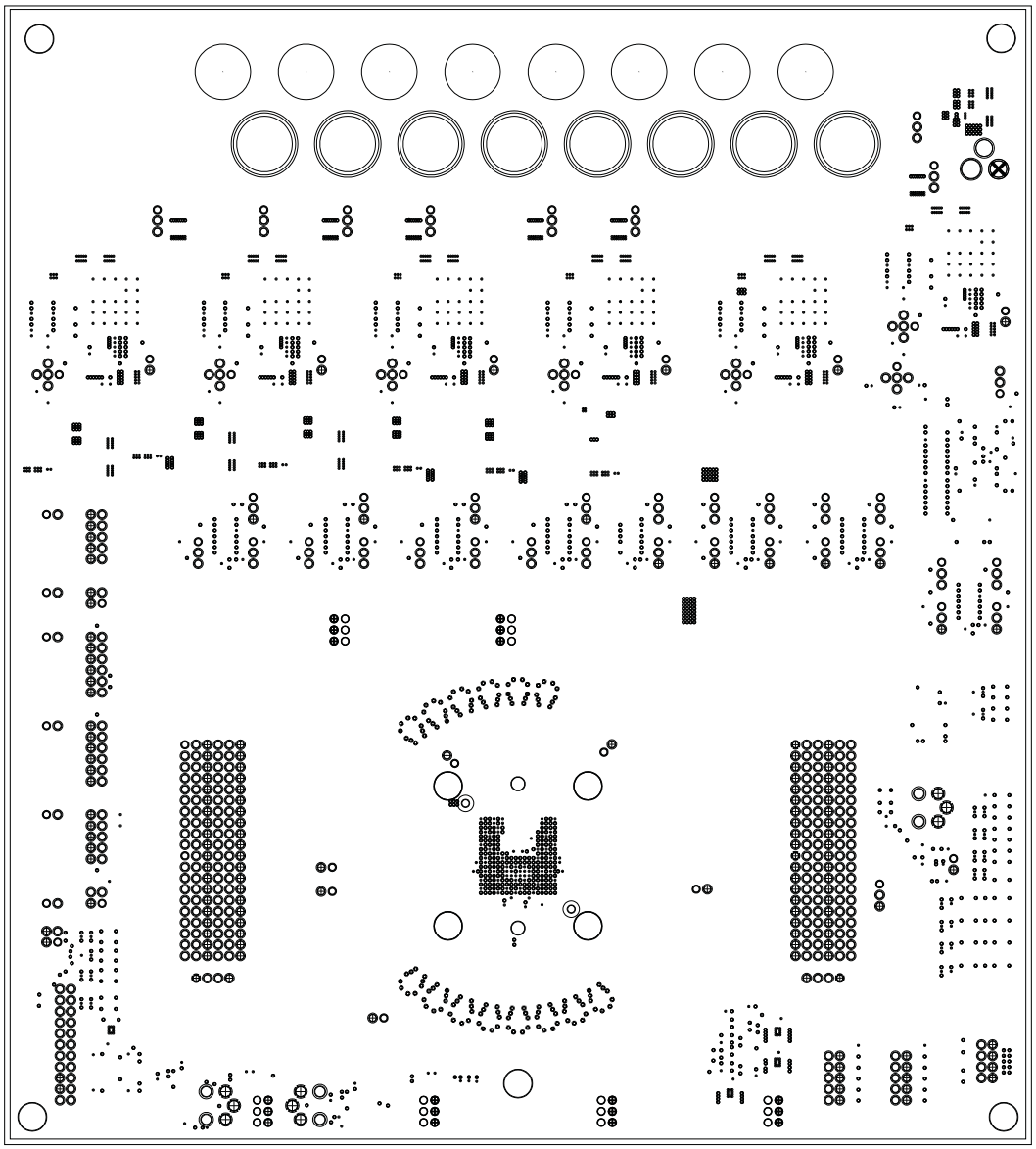


Figure 47. Internal Ground, Layers 2,4,6,8,10

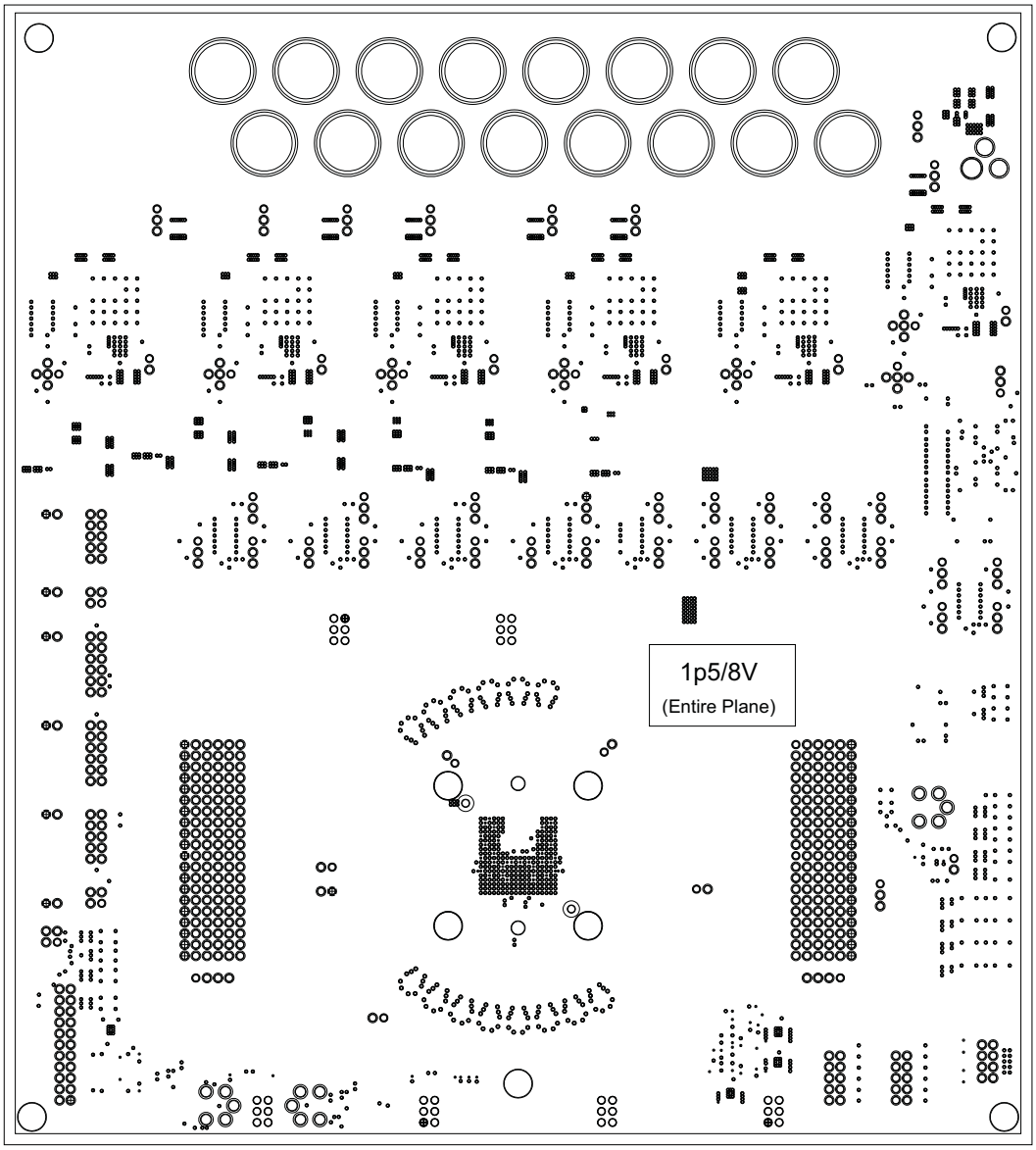


Figure 48. Internal Power, Layer 3

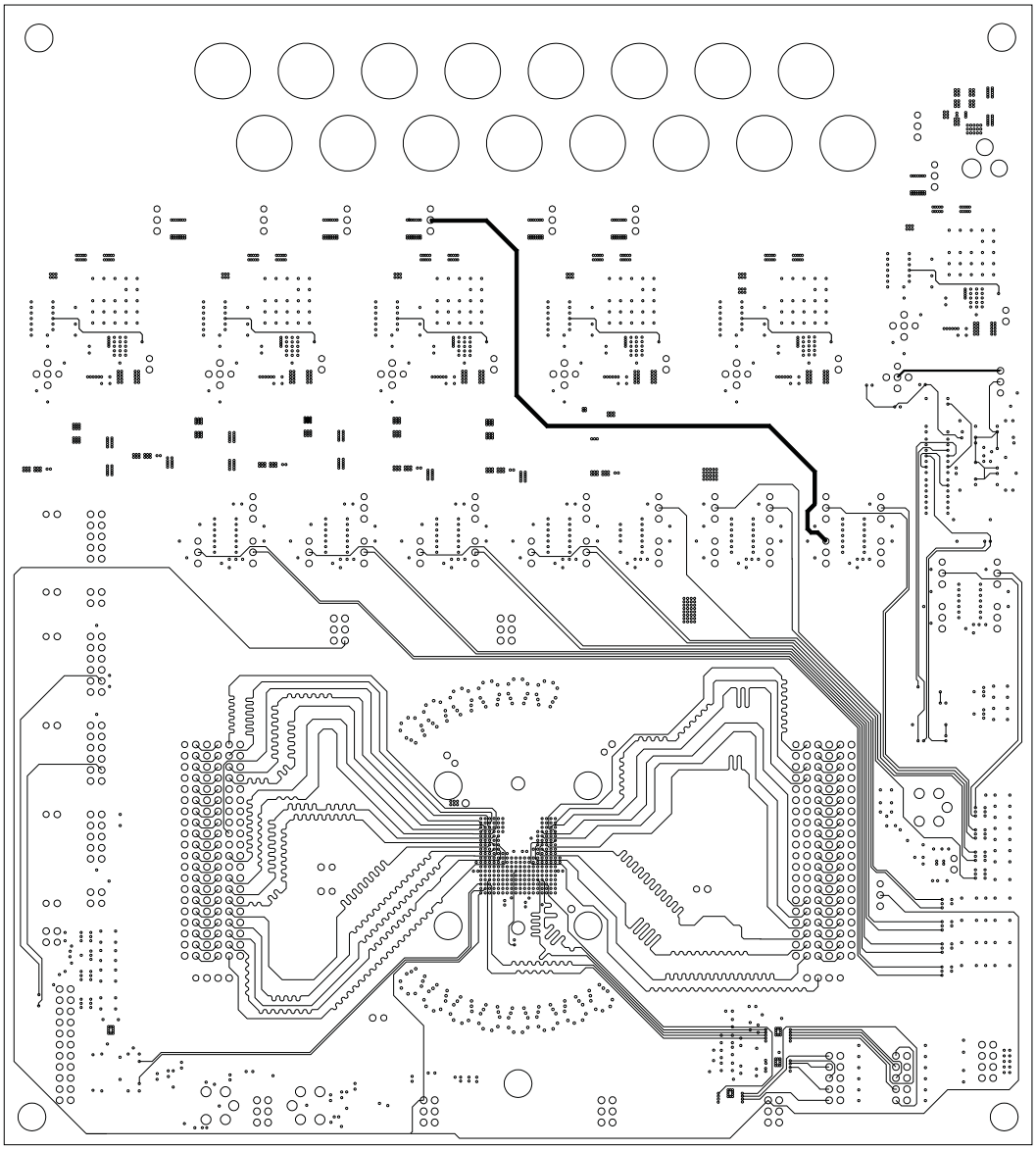


Figure 49. Internal Signal, Layer 5

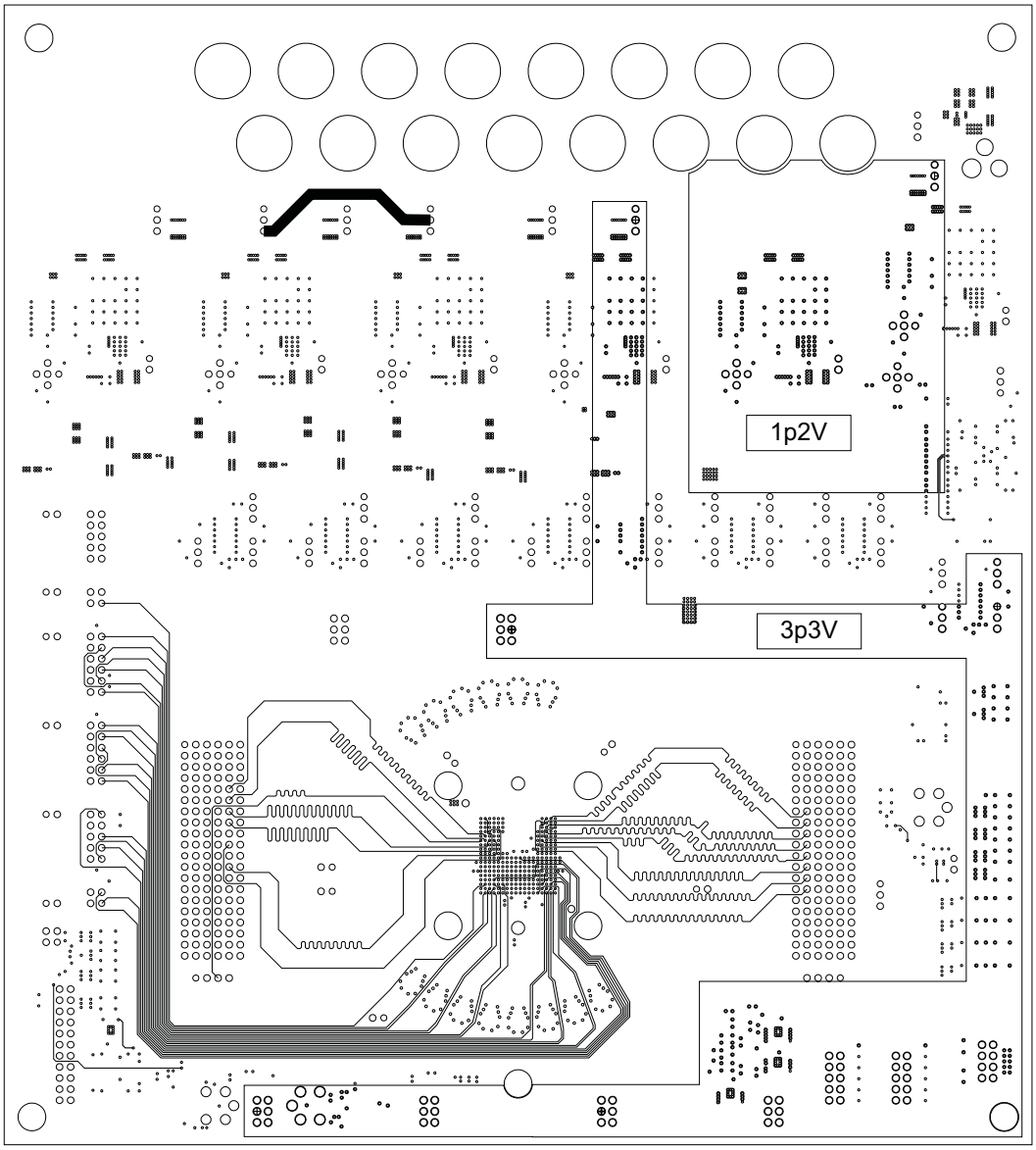


Figure 50. Internal Signal, Layer 7

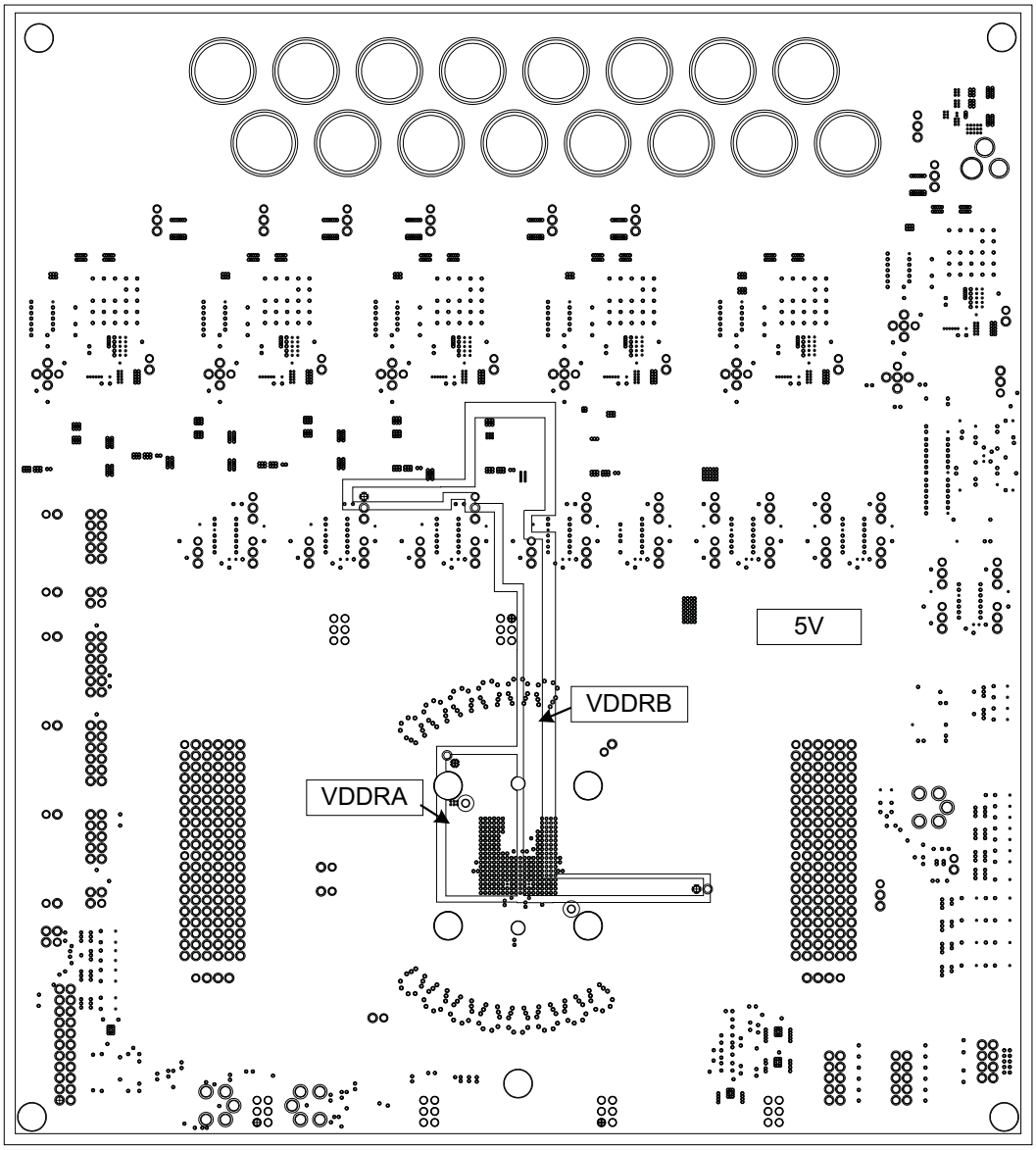


Figure 51. Internal Power, Layer 9

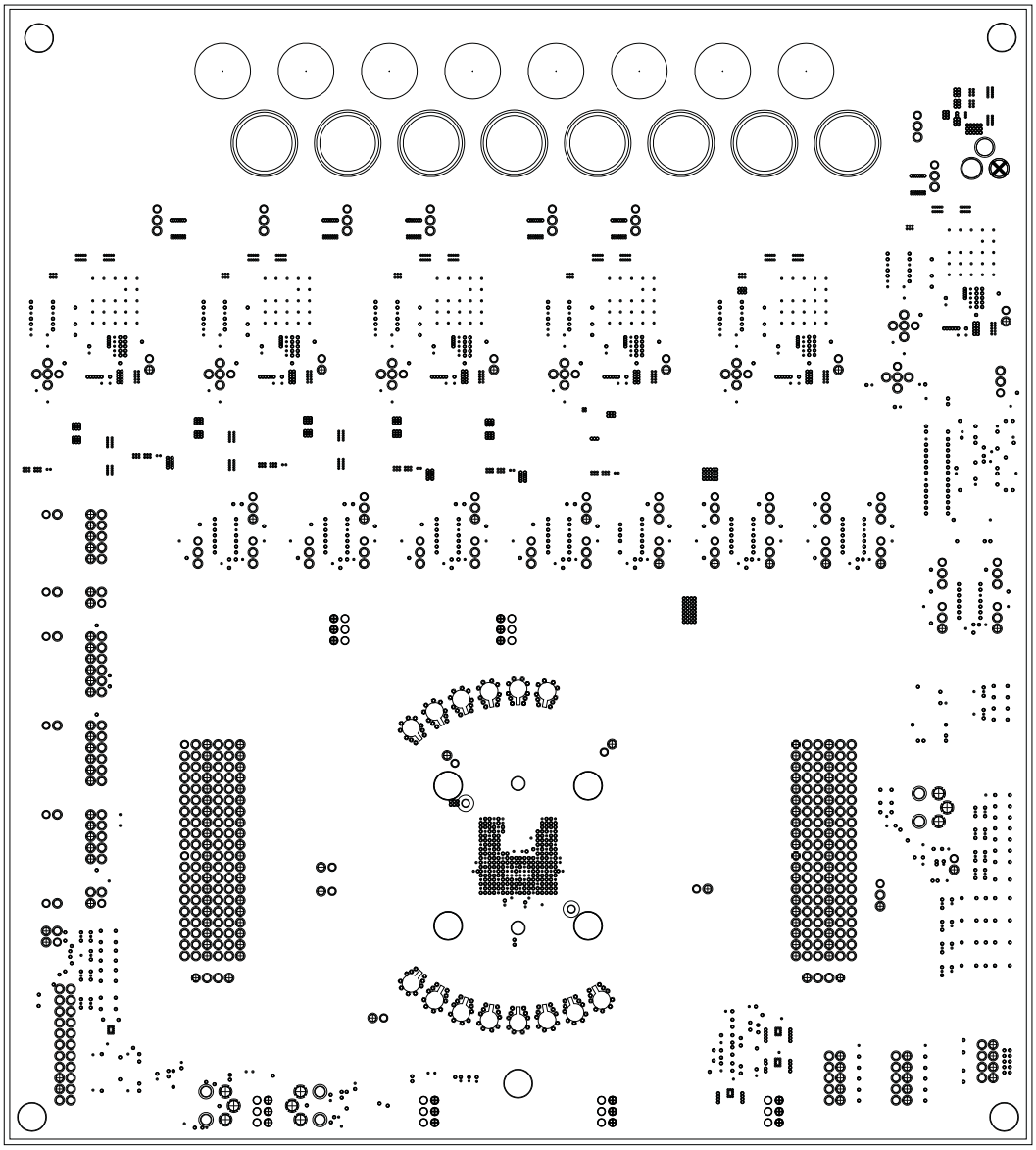


Figure 52. Internal Ground and Power, Layers 11,13,15,17

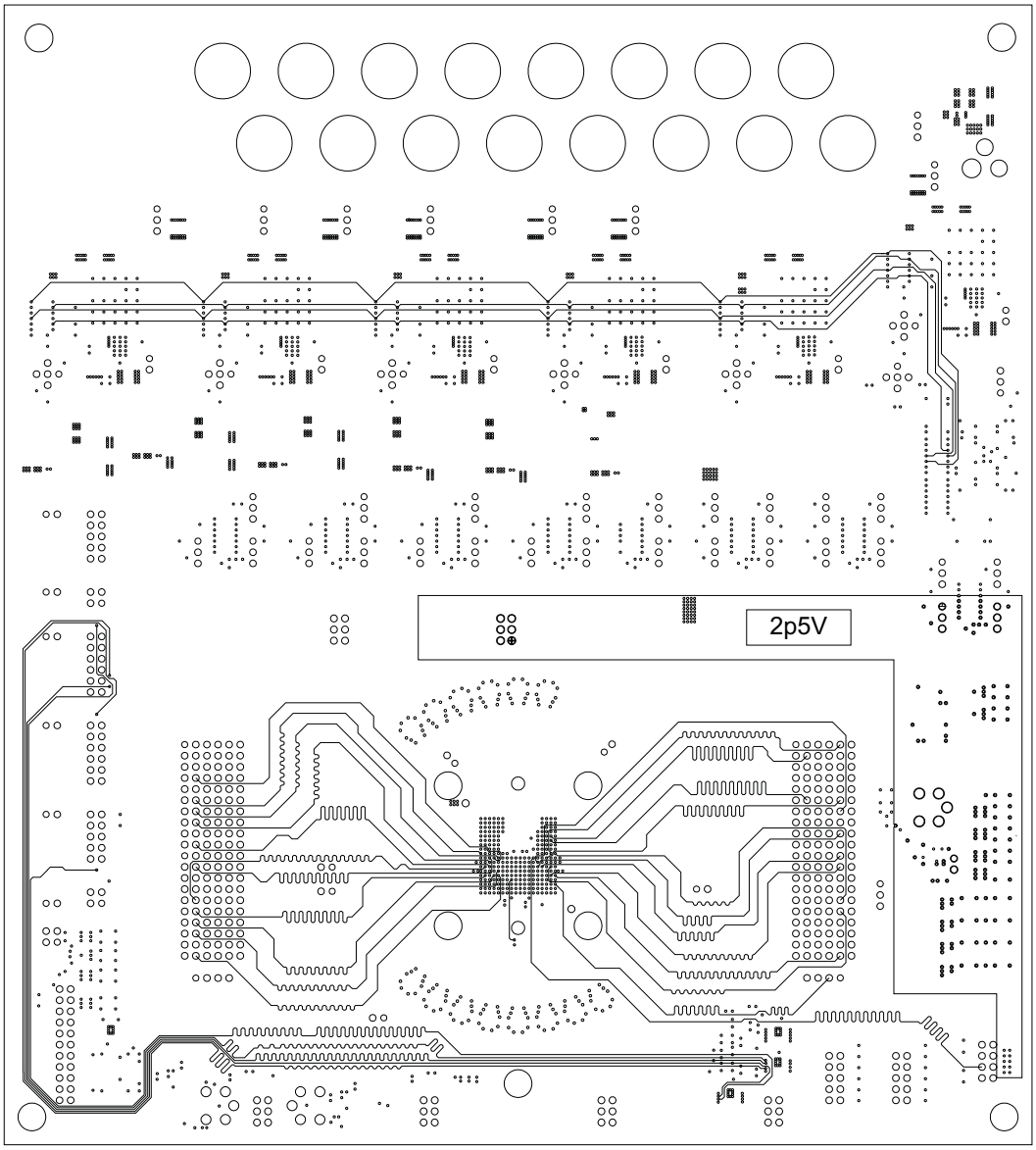


Figure 53. Internal Signal, Layer 12

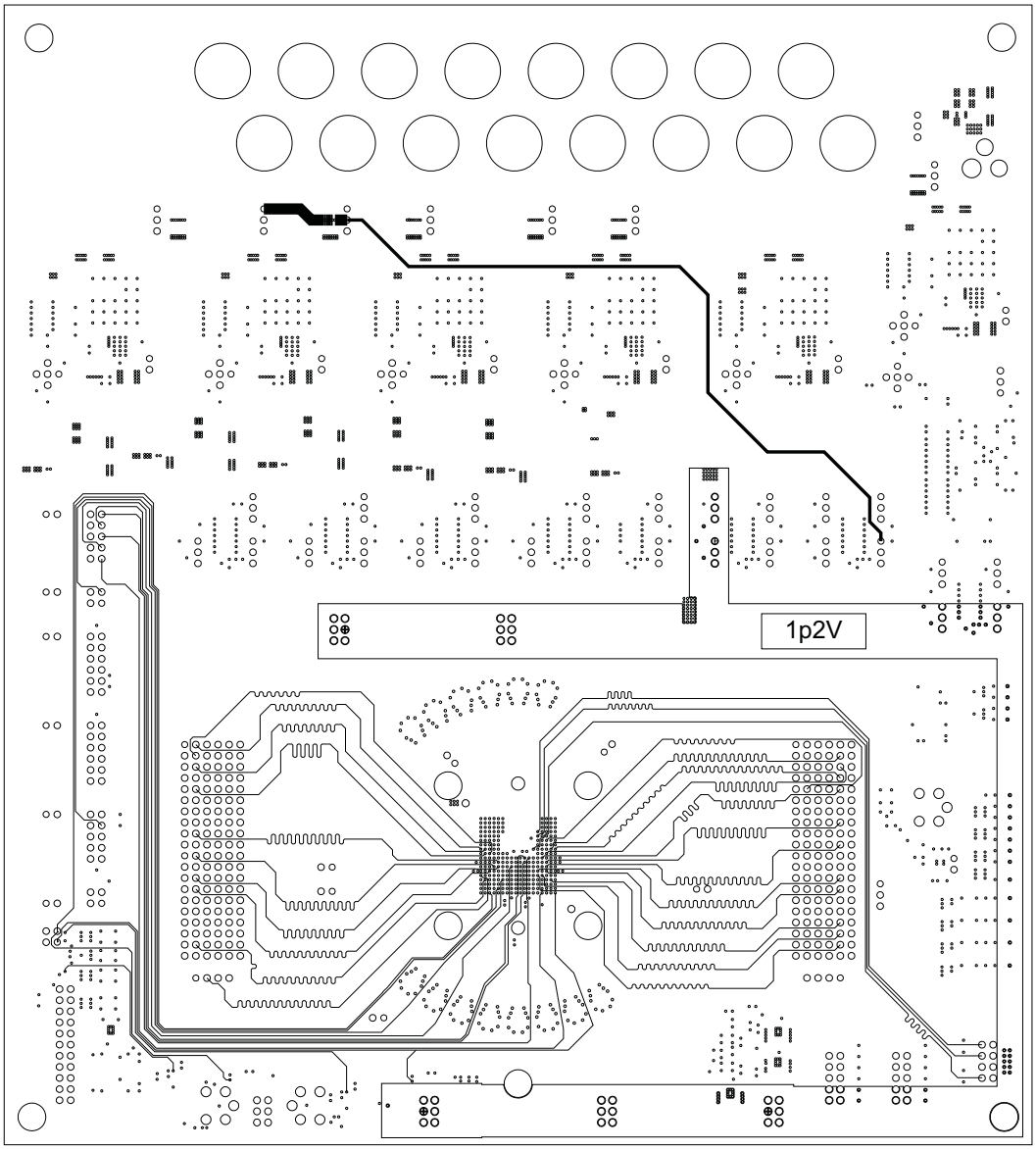


Figure 54. Internal Signal, Layer 14

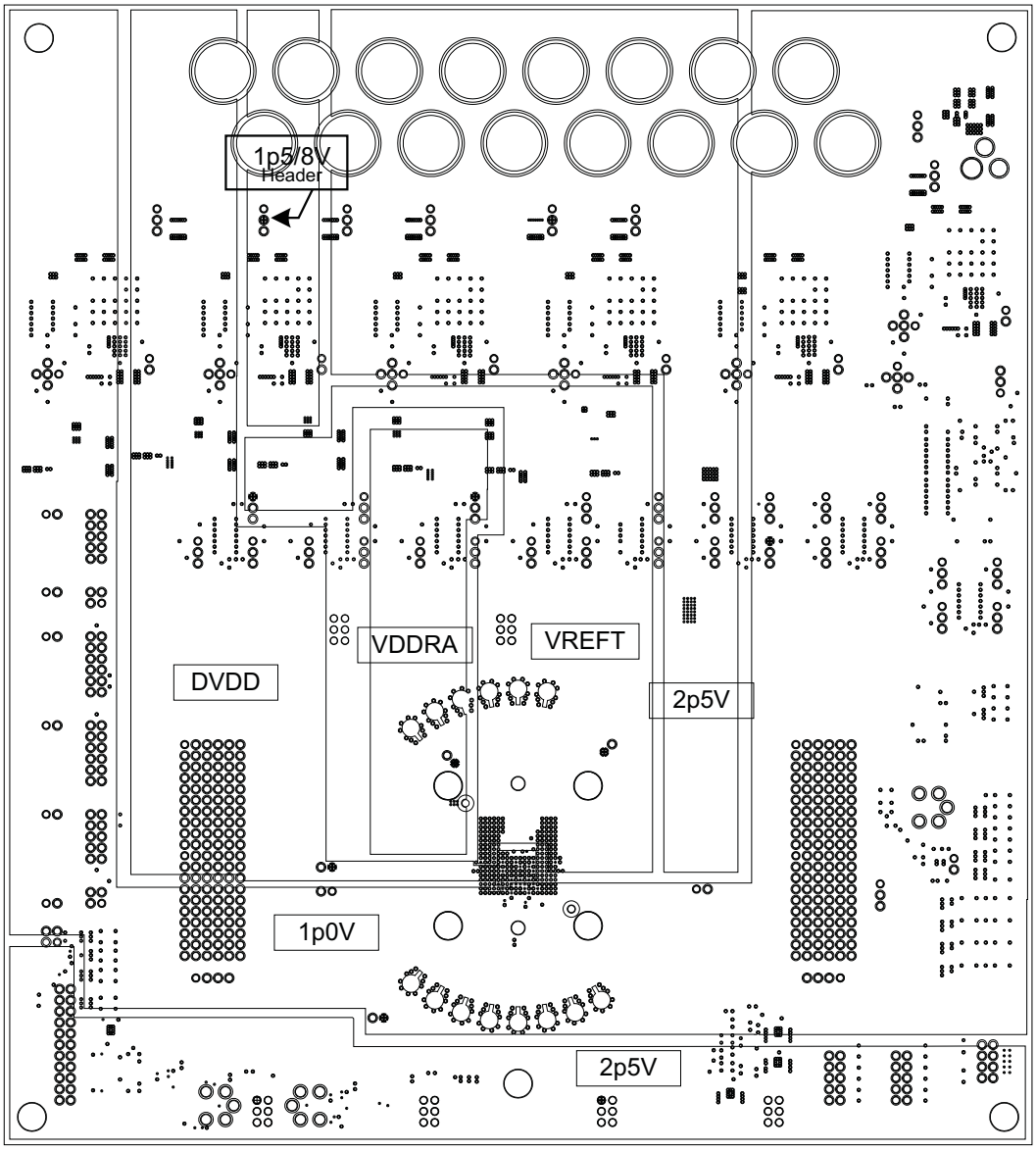


Figure 55. Internal Power, Layer 16

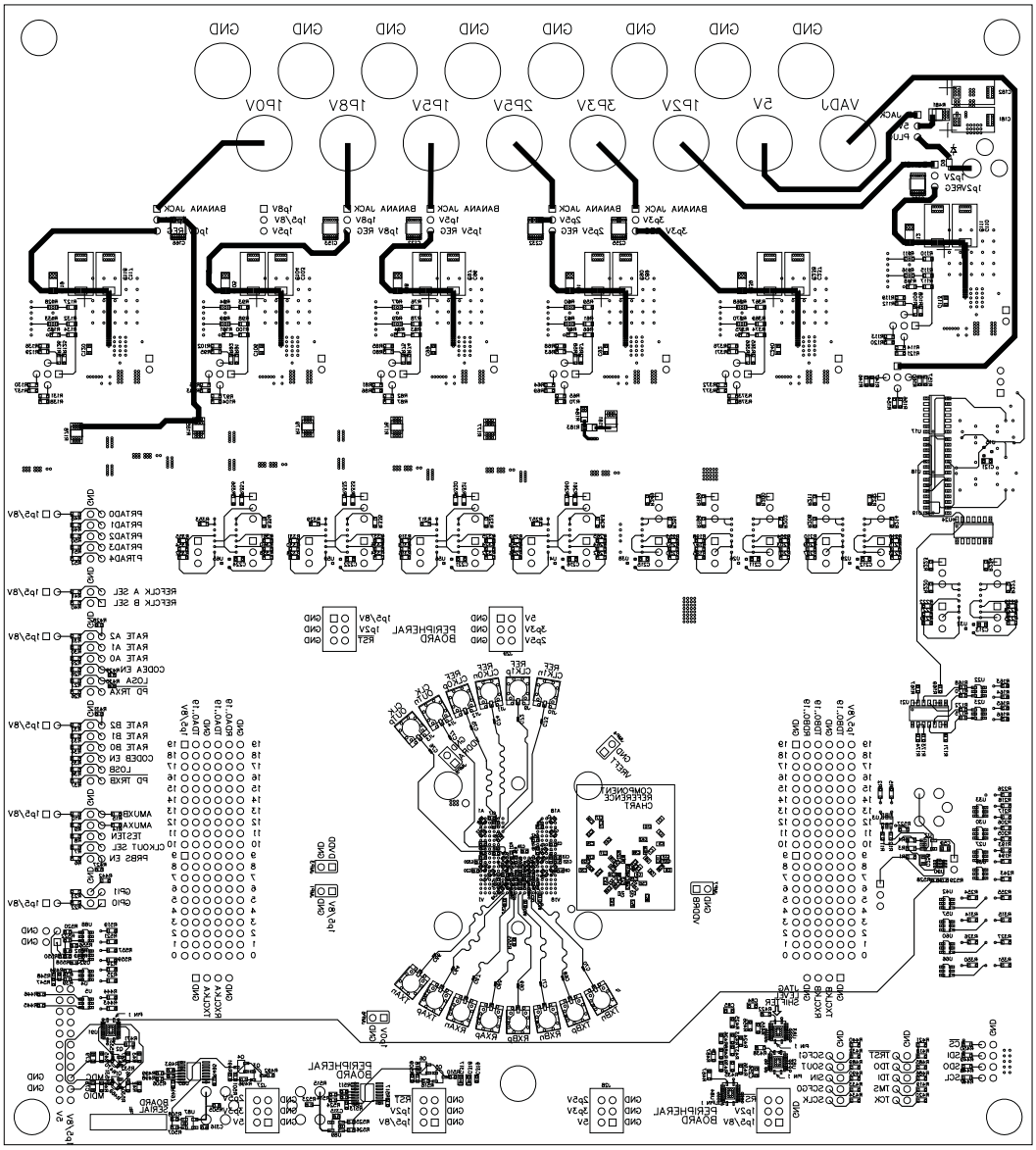


Figure 56. Bottom Signal, Layer 18

Table 2. TLK6002EVM Layer Construction

Subclass Name	Type	Material	Thickness (mil)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Width (mil)	Impedance (1) (Ω)
	SURFACE	AIR						
TOP	CONDUCTOR	COPPER	2.4	595900	1	0	9.5	47.903
	DIELECTRIC	FR-4	5	0	4.1	0.035		
L2_GND	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	5	0	4.1	0.035		
L3_PWR	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	5	0	4.1	0.035		
L4_GND	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	7	0	4.1	0.035		
L5_SIG	CONDUCTOR	COPPER	1.2	595900	1	0	6.0	50.337
	DIELECTRIC	FR-4	7	0	4.1	0.035		
L6_GND	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	7	0	4.1	0.035		
L7_SIG	CONDUCTOR	COPPER	1.2	595900	1	0	6.0	50.337
	DIELECTRIC	FR-4	7	0	4.1	0.035		
L8_GND	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	4	0	4.1	0.035		
L9_PWR	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	4	0	4.1	0.035		
L10_GND	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	4	0	4.1	0.035		
L11_GND	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	7	0	4.1	0.035		
L12_SIG	CONDUCTOR	COPPER	1.2	595900	1	0	6.0	50.337
	DIELECTRIC	FR-4	7	0	4.1	0.035		
L13_GND	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	7	0	4.1	0.035		
L14_SIG	CONDUCTOR	COPPER	1.2	595900	1	0	6.0	50.337
	DIELECTRIC	FR-4	7	0	4.1	0.035		
L15_GND	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	5	0	4.1	0.035		
L16_PWR	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	5	0	4.1	0.035		
L17_GND	PLANE	COPPER	1.2	595900	1	0		
	DIELECTRIC	FR-4	5	0	4.1	0.035		
BOTTOM	CONDUCTOR	COPPER	2.4	595900	1	0	9.5	47.903
	SURFACE	AIR						

(1) The Impedance is set to be slightly less than 50 Ω on the traces in order to compensate for slight over-etching during the manufacturing process. The end impedance after etching should result in a 50-Ω Impedance. Always consult with your board manufacturer for their process/design requirements to ensure the desired impedance is achieved.

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During normal operation, some circuit components may have case temperatures greater than 50° C. The EVM is designed to operate properly with certain components above 25° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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