Application Report
SLOA038 - October 1999

THS3001 SPICE Model Performance

Jim Karki *Mixed Signal Products*

ABSTRACT

This application report outlines the SPICE model of the THS3001 high-speed monolithic operational amplifier. General information about the model file structure, performance comparison, model listing, and a brief comment about symbols are included. The listing can be copied and pasted into an ASCII editor, or it can be down loaded by visiting the THS3001 product folder at http://www.ti.com/sc/docs/products/analog/THS3001.html.

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1 Introduction

SPICE modeling has become commonplace today, especially with the advent of affordable PCs with more computing power than main frames of a few years ago.

A big concern in SPICE modeling is the accuracy of the models. Without a good model, simulation results are little more than verification of rudimentary circuit operation. The Boyle operational amplifier (op amp) model introduced during the mid ‘70s came from the need for a model that did not use a lot of computing resources, and gave reasonable results for the µA741. In the years since, people have enhanced the Boyle model to add more accuracy.

Today, full-transistor models simulate with speed and accuracy on modest home systems. The goal, when creating the SPICE model of the THS3001 high-speed monolithic operational amplifier, is to provide a model that will accurately simulate the actual device in a circuit. The model is derived from the full-transistor model used internally by TI design. Simplifications are made to speed simulation time, and various performance parameters are adjusted to match the model to measured device performance.

2 File Structure

The THS3001 SPICE model file, THS3001.lib, is written in ASCII file format and is compatible with a wide variety of computing platforms. The model is written in subcircuit format and has been tested with MicroSim® PSpice® release 8 and OrCAD® PSpice® version 9. It should be compatible with most SPICE2- and SPICE3-based simulation programs.

The THS3001.lib file contains the subcircuit definition for the THS3001. The model begins with a .SUBCKT statement and ends with a .ENDS statement.

3 Performance

Typical performance parameters are modeled, and normal part-to-part variations experienced in real life cannot be expected. At frequencies above a few hundred MHz, performance becomes increasingly dependent on parasitic devices associated with the circuit, and modeling suffers. So, even though the model is very accurate, always verify circuit performance with lab testing. An EVM is available upon request.

The following graphs compare simulation results to measured device data. In all graphs, the simulation results are dashed lines and the measured data are solid lines. Device performance is measured using the THS3001 EVM, or is taken from the data sheet. SPICE simulation was done using MicroSim® PSpice® release 8. Most of the parameters are measured using Vcc=±15 V, and performance follows at lower voltages.

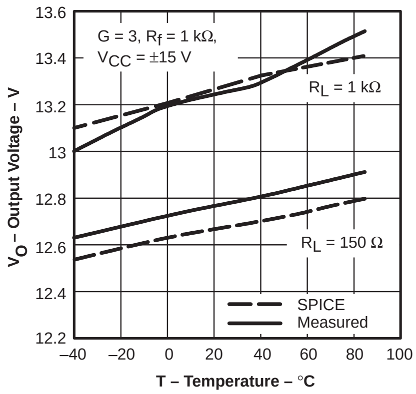

Figure 1. Output Voltage (pk) vs Temperature

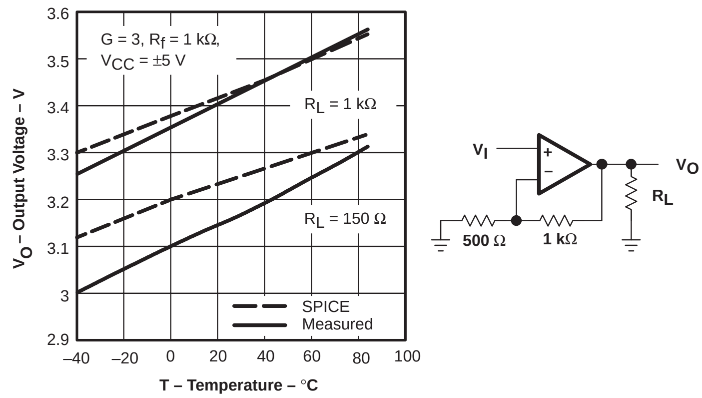

Figure 2. Output Voltage (pk) vs Temperature

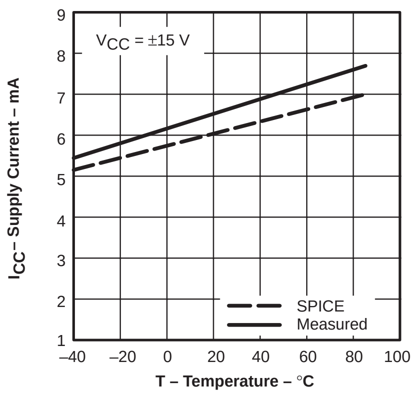

Figure 3. Supply Current vs Temperature

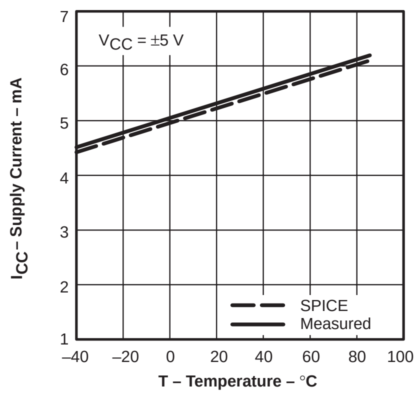

Figure 4. Supply Current vs Temperature

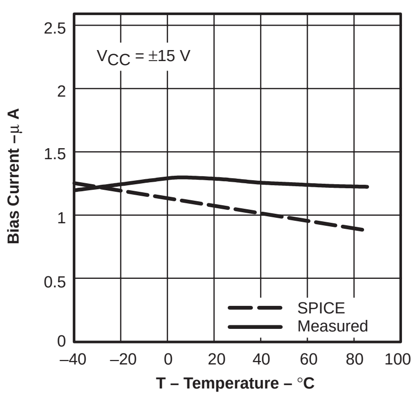

Figure 5. Bias Current vs Temperature

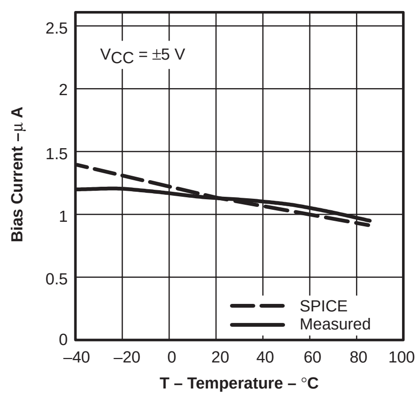

Figure 6. Bias Curent vs Temperature

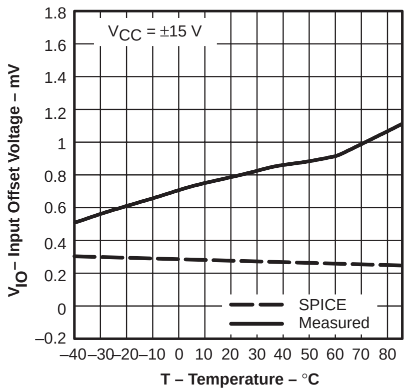

Figure 7. Input Offset Voltage vs Temperature

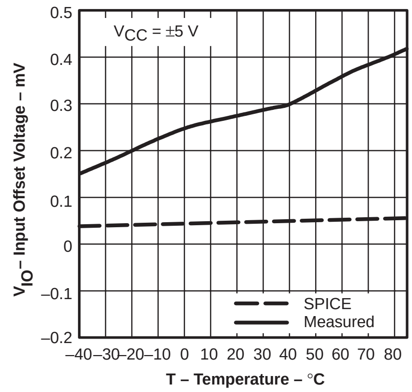

Figure 8. Input Offset Voltage vs Temperature

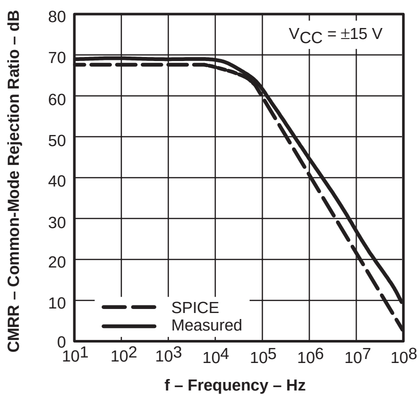

Figure 9. Common-Mode Rejection Ratio vs Frequency

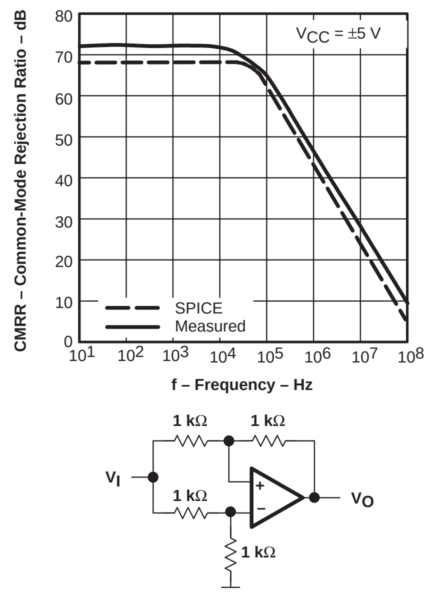

Figure 10. Common-Mode Rejection Ratio vs Frequency

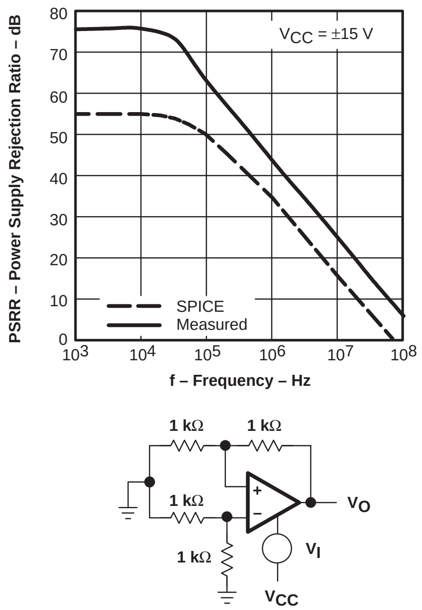

Figure 11. Power Supply Rejection Ratio vs Frequency

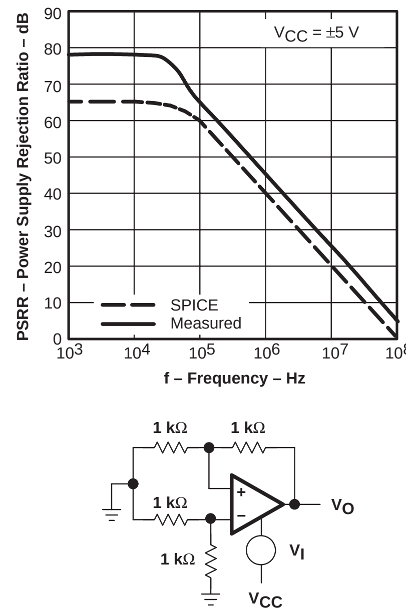

Figure 12. Power Supply Rejection Ratio vs Frequency

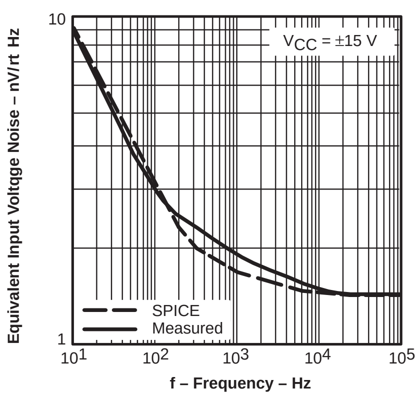

Figure 13. Equivalent Input Voltage Noise vs Frequency

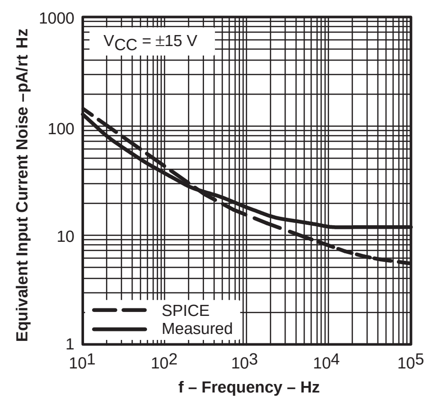

Figure 14. Equivalent Input Current Noise vs Frequency

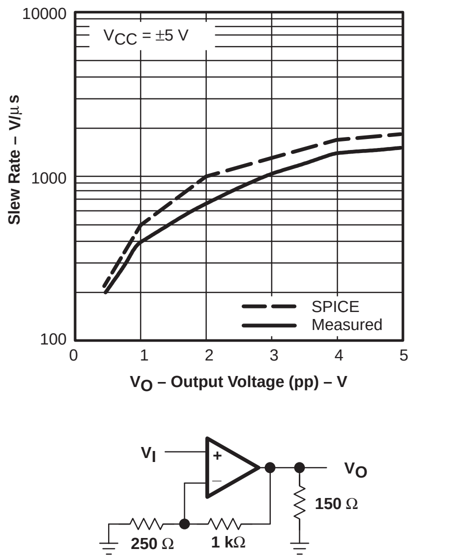

Figure 15. Slew Rate vs Output Voltage (pp)

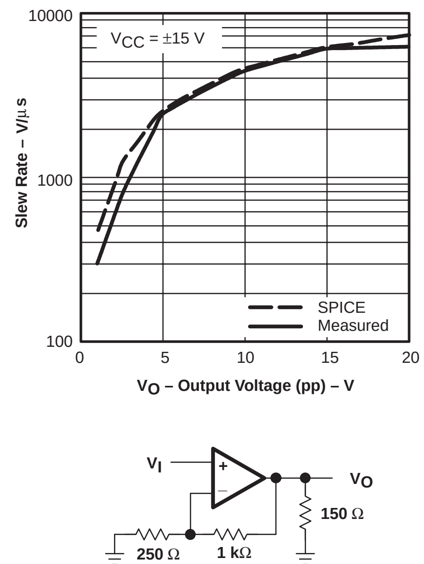

Figure 16. Slew Rate vs Output Voltage (pp)

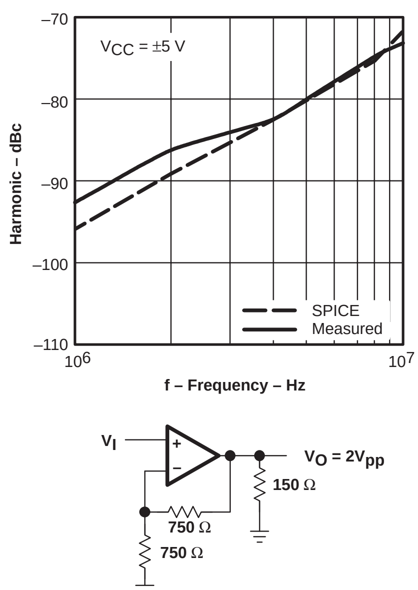

Figure 17. 2nd Harmonic vs Frequency

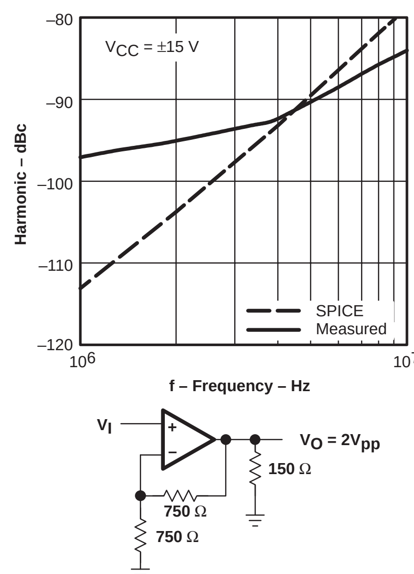

Figure 18. 2nd Harmonic vs Frequency

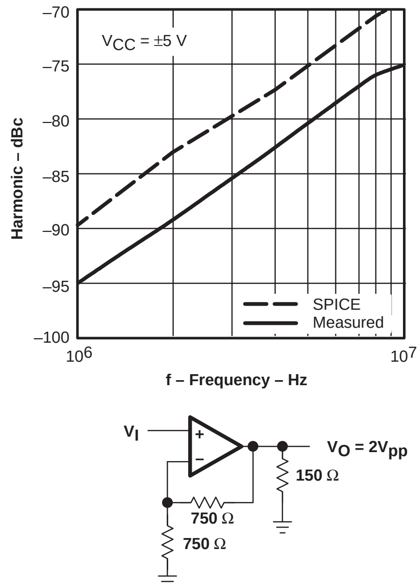

Figure 19. 3rd Harmonic vs Frequency

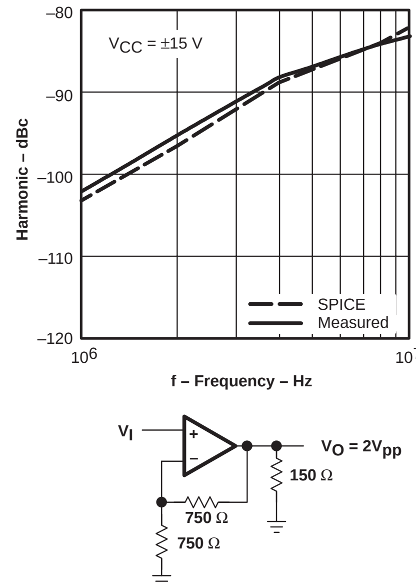

Figure 20. 3rd Harmonic vs Frequency

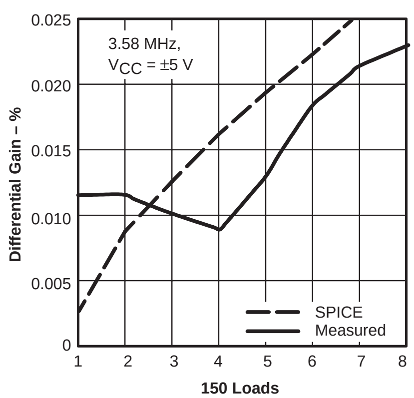

Figure 21. Differential Gain vs Loads

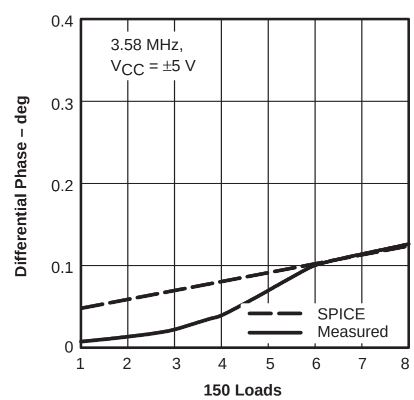

Figure 22. Differential Phase vs Loads

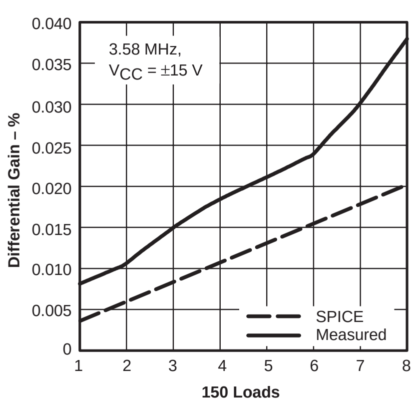

Figure 23. Differential Gain vs Loads

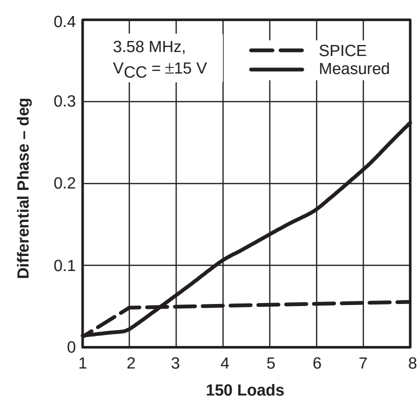

Figure 24. Differential Phase vs Loads

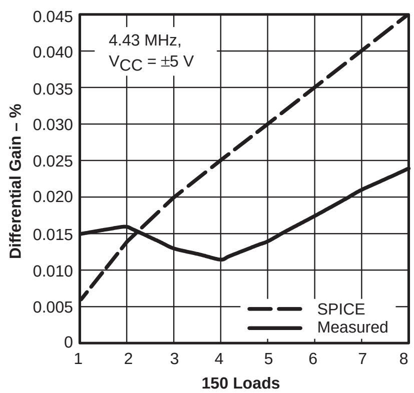

Figure 25. Differential Gain vs Loads

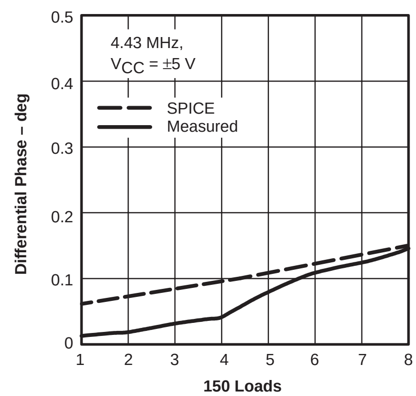

Figure 26. Differential Phase vs Loads

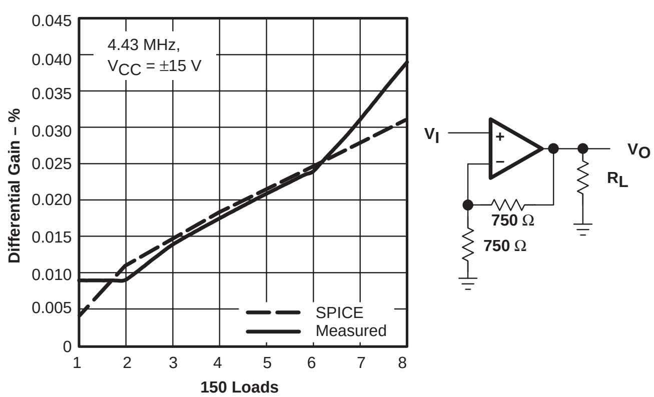

Figure 27. Differential Gain vs Loads

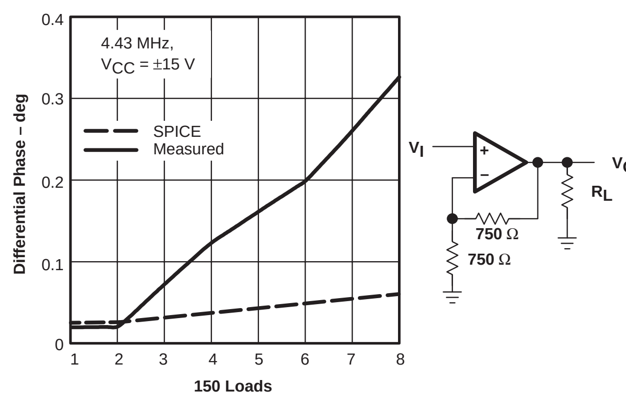

Figure 28. Differential Phase vs Loads

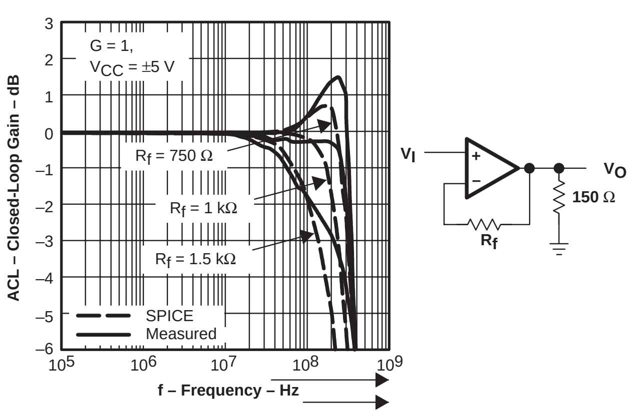

Figure 29. Closed-Loop Gain vs Frequency

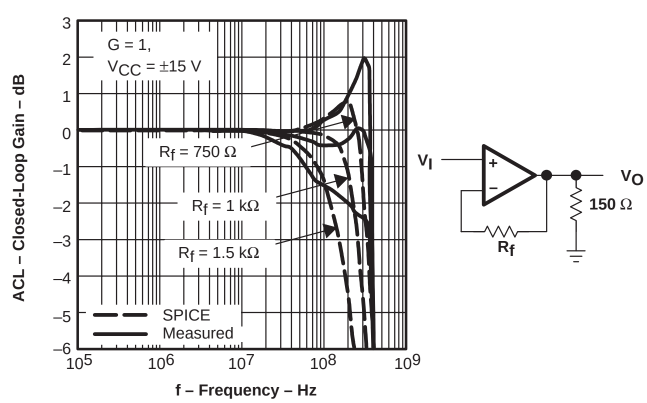

Figure 30. Closed-Loop Gain vs Frequency

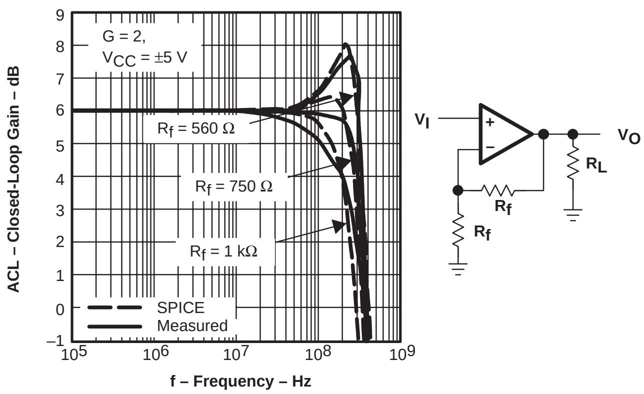

Figure 31. Closed-Loop Gain vs Frequency

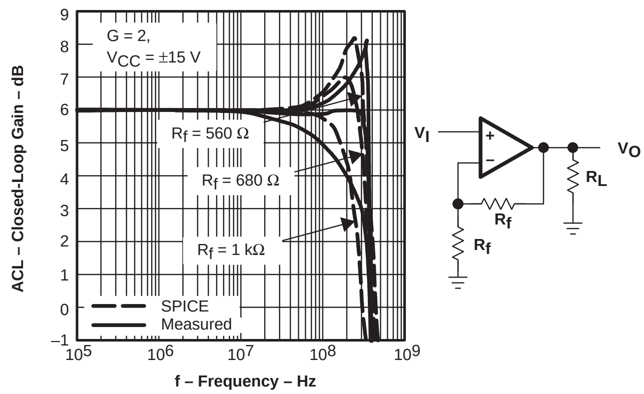

Figure 32. Closed-Loop Gain vs Frequency

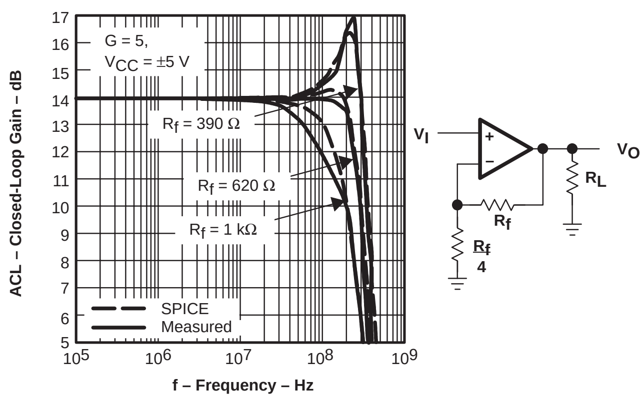

Figure 33. Closed-Loop Gain vs Frequency

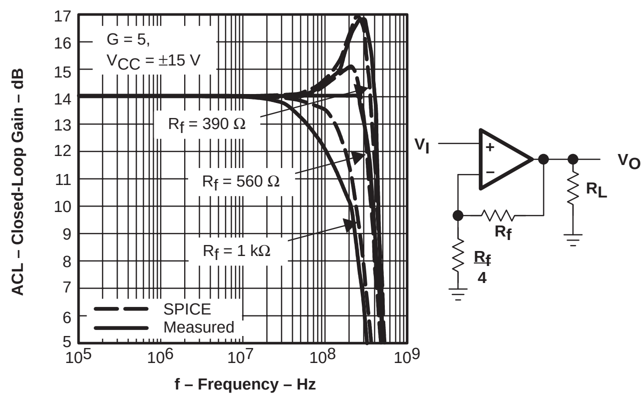

Figure 34. Closed-Loop Gain vs Frequency

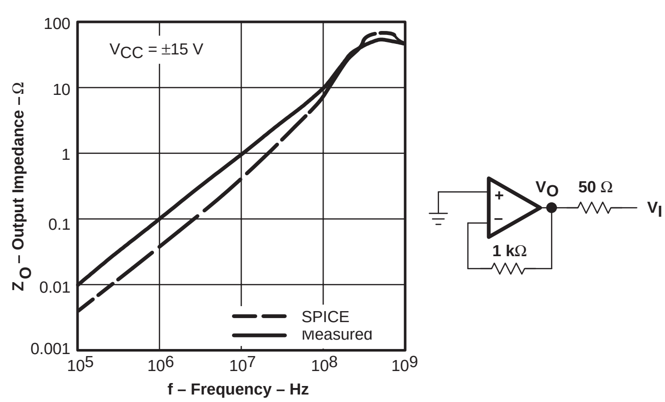

Figure 35. Output Impedance vs Frequency

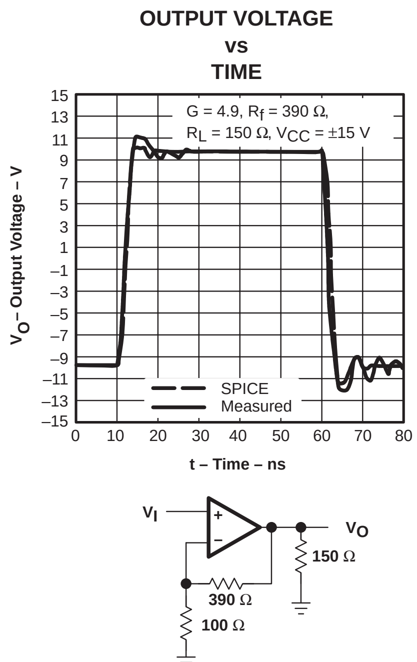

Figure 36. Output Voltage vs Time

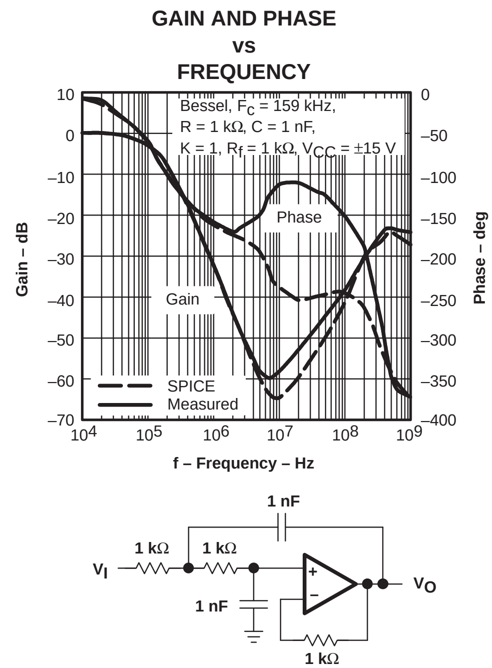

Figure 37. Gain and Phase vs Frequency

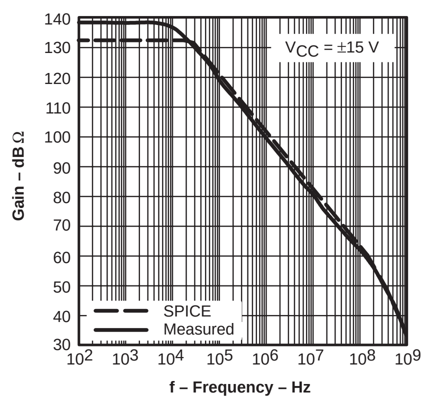

Figure 38. Open Loop Transimpedance Gain vs Frequency

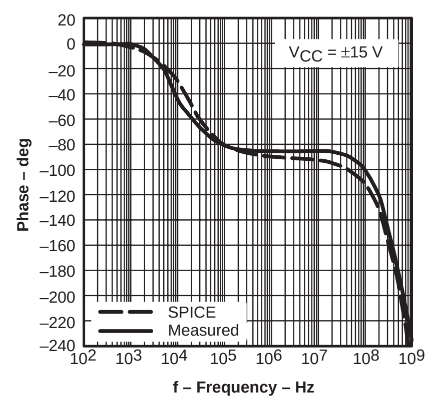

Figure 39. Open Loop Transimpedance Gain vs Frequency

4 Schematic and Subcircuit Listing

The schematic representation of the model and the subcircuit listing follow.

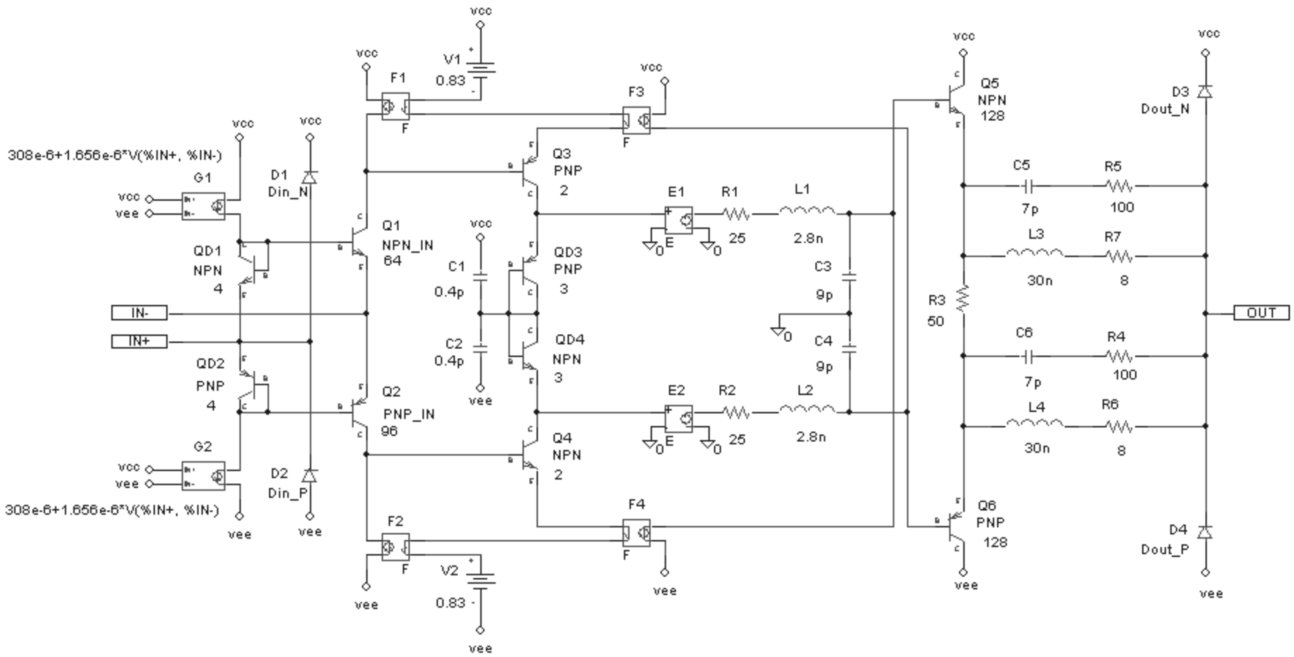

Figure 40. THS3001 SPICE Model Schematic

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* EXEMPLARY, OR PUNITIVE DAMAGES ARISING OUT OF THE USE OR APPLICATION OF THE SPICE
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* discontinue or make changes without notice to any product herein to improve reliability,
* function, or design. Texas Instruments does not convey any license under patent rights or
* any other intellectual property rights, including those of third parties.
*
* THS3001 SUBCIRCUIT
* HIGH SPEED, CURRENT FEEDBACK, OPERATIONAL AMPLIFIER
* WRITTEN 8/10/99
* TEMPLATE=X^@REFDES %IN+ %IN– %Vcc+ %Vcc– %OUT @MODEL
* CONNECTIONS:      NON–INVERTING INPUT
*                   | INVERTING INPUT
*                   | | POSITIVE POWER SUPPLY
*                   | | | NEGATIVE POWER SUPPLY
*                   | | | | OUTPUT
*                   | | | | |
*                   | | | | |
*                   | | | | |
.SUBCKT THS3001     1 2 3 4 5
*
* INPUT *
Q1  31 32 2 NPN_IN 4
QD1 32 32 1 NPN 4
Q2  7 15 2 PNP_IN 4
QD2 15 15 1 PNP 4
* PROTECTION DIODES *
D1  1 3 Din_N
D2  4 1 Din_P
D3  5 3 Dout_N
D4  4 5 Dout_P
* SECOND STAGE *
Q3  17 31 11 PNP 2
Q4  16 7 13 NPN 2
QD3 30 30 17 PNP 3
```

```
QD4 30 30 16 NPN 3
C1  30 3  0.4p
C2  4 30  0.4p
F1  3 31 VF1 1
VF1 33 34 0V
F2  7 4 VF2 1
VF2 35 6 0V
F3  3 12 VF3 1
VF3 34 11 0V
F4  14 4 VF4 1
VF4 13 35 0V
* FREQUENCY SHAPING *
E1  18 0 17 0 1
E2  19 0 16 0 1
R1  44 18 25
R2  19 42 25
C3  0 14  9p
C4  0 12  9p
L1  44 14 2.8n
L2  42 12 2.8n
* OUTPUT *
Q5  3 14 28 NPN 128
Q6  4 12 29 PNP 128
C5  28 9  7p
R5  9 5  100
L3  28 10  30n
R7  10 5  8
Re  28 29 Rt 50
C6  29 21  7p
R4  21 5  100
L4  29 22  30n
R6  22 5  8
* BIAS SOURCES *
G1  3 32 VALUE = { 308e-6+1.656e-6*V(3, 4) }
G2  15 4 VALUE = { 307e-6+1.656e-6*V(3, 4) }
V1  3 33 0.83
V2  6 4 0.83
.MODEL Rt RES TC1=-0.006
* DIODE MODELS *
.MODEL Din_N D  IS=10E-21 N=1.836 ISR=1.565e-9 IKF=1e-4 BV=30 IBV=100E-6 RS=105 TT=11.54E-9
 CJO=2E-12 VJ=.5 M=.3333
.MODEL Din_P D  IS=10E-21 N=1.836 ISR=1.565e-9 IKF=1e-4 BV=30 IBV=100E-6 RS=160 TT=11.54E-9
 CJO=2E-12 VJ=.5 M=.3333
.MODEL Dout_N D IS=10E-21 N=1.836 ISR=1.565e-9 IKF=1e-4 BV=30 IBV=100E-6 RS=60  TT=11.54E-9
 CJO=2E-12 VJ=.5 M=.3333
.MODEL Dout_P D IS=10E-21 N=1.836 ISR=1.565e-9 IKF=1e-4 BV=30 IBV=100E-6 RS=105 TT=11.54E-9
 CJO=2E-12 VJ=.5 M=.3333
* TRANSISTOR MODELS *
.MODEL NPN_IN NPN
+ IS=170E-18 BF=100 NF=1 VAF=100 IKF=0.0389 ISE=7.6E-18
```

```
+ NE=1.13489 BR=1.11868 NR=1 VAR=4.46837 IKR=8 ISC=8E–15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E–15 VJE=1.0888 MJE=0.381406
+ VJC=0.589703 MJC=0.265838 FC=0.1 CJC=133.8E–15 XTF=272.204 TF=12.13E–12
+ VTF=10 ITF=0.294 TR=3E–09 XTB=1 XTI=5 KF=25E–15
.MODEL NPN NPN
+ IS=170E–18 BF=100 NF=1 VAF=100 IKF=0.0389 ISE=7.6E–18
+ NE=1.13489 BR=1.11868 NR=1 VAR=4.46837 IKR=8 ISC=8E–15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E–15 VJE=1.0888 MJE=0.381406
+ VJC=0.589703 MJC=0.265838 FC=0.1 CJC=133.8E–15 XTF=272.204 TF=12.13E–12
+ VTF=10 ITF=0.147 TR=3E–09 XTB=1 XTI=5
.MODEL PNP_IN PNP
+ IS=296E–18 BF=100 NF=1 VAF=100 IKF=0.021 ISE=494E–18
+ NE=1.49168 BR=0.491925 NR=1 VAR=2.35634 IKR=8 ISC=8E–15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E–15 VJE=0.940007 MJE=0.55
+  VJC=0.588526 MJC=0.55 FC=0.1 CJC=133.8E–15 XTF=141.135 TF=12.13E–12
+ VTF=6.82756 ITF=0.267 TR=3E–09 XTB=1 XTI=5 KF=25E–15
.MODEL PNP PNP
+ IS=296E–18 BF=100 NF=1 VAF=100 IKF=0.021 ISE=494E–18
+ NE=1.49168 BR=0.491925 NR=1 VAR=2.35634 IKR=8 ISC=8E–15
+ NC=1.8 RB=251.6 RE=0.1220 RC=197 CJE=120.2E–15 VJE=0.940007 MJE=0.55
+  VJC=0.588526 MJC=0.55 FC=0.1 CJC=133.8E–15 XTF=141.135 TF=12.13E–12
+ VTF=6.82756 ITF=0.267 TR=3E–09 XTB=1 XTI=5
.ENDS
*$
```

5 About Building a Symbol

The first line of the subcircuit definition – .SUBCKT THS3001_NN 1 2 3 4 5 – defines the name of the model and the subcircuit nodes available for external connection. When creating a symbol in PSpice®, the subcircuit node assignments need to match the TEMPLATE device property, and the MODEL value must equal the model name. The comment line in the file * TEMPLATE = X^@REFDES %IN+ %IN– %VCC+ %VCC– %OUT @MODEL gives the proper value for the TEMPLATE property. This associates the symbol pin names with subcircuit nodes available for external connections. The symbol pin numbers are used for packaging purposes and are not used for simulation. Using the forgoing results in the following associations:

Table 1. Subcircuit Node to Symbol Pin Summary

Subcircuit Node	THS3001 Symbol Pin Name
2	IN–
3	Vcc+
4	Vcc–
5	OUT

IMPORTANT NOTICE

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