AFE5832 32-Channel Analog Front-End Evaluation Module (EVM Rev. A)

This user's guide gives a general overview of the AFE5832 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the AFE5832 analog front-end, and to the Rev. A version of the EVM hardware. The AFE5832 EVM provides a platform for evaluating the AFE under various signal, clock, reference, and ADC output formats. In addition, the EVM supports the testing of the low-voltage differential signaling (LVDS) interface using the TSW1400EVM capture card.

This user's guide refers to software AFE5832 GUI v.1.0.0 or higher, and *High-Speed Data Converter Pro* (HSDC Pro) Software v.4.7 and requires Microsoft Windows 7® or Windows 10® to function.

For any further questions regarding the EVM, GUI or device, contact TI support.

Contents

1 EVM Hardware Overview 4
2 GUI Software Installation 5
3 Quick Views of Evaluation Setups for LVDS Interface 6
3.1 Equipment Setup Overview 6
4 Testing the EVM Data Capture with LVDS Interface 8
4.1 EVM Hardware Setup 8
4.2 Capturing an Analog Input Signal With the LVDS Interface 10
5 Testing the EVM in Digital Time Gain Compensation (DTGC) Mode 15
6 Using the EVM in CW Mode 17
Appendix A Software Installation 19
Appendix B Overview of the AFE5832 EVM GUI Features 34
Appendix C Hardware Configuration 49
Appendix D Triggering Options 54
Appendix E Common Hardware Modifications 57
Appendix F Hardware Reference 58
Appendix G FAQ and Troubleshooting 82

List of Figures

1 AFE5832 EVM Hardware Overview 4
2 Provided Power Cable for J1 Connector 5
3 Evaluation Setup Overview 6
4 TSW1400EVM and AFE5832 EVM Hardware Setup for LVDS Capture 8
5 Connect to TSW EVM (TSW1400 Shown) 10
6 Choose Firmware 10
7 TSW1400 EVM LEDs Turn On After Firmware Download 11
8 AFE5832 GUI Launches 11
9 Clock Configuration on AFE EVM for LVDS Capture 12
10 Software Reset and Initialize Buttons on AFE5832 EVM GUI 12
11 AFE_RST Hardware Reset Button 12
12 AFE5832 EVM GUI Data Format and Analog Configuration (LVDS) 13
13 LED D5 on the TSW1400 EVM Turns On When ADC is Ready 14

14 Analog Input Capture for LVDS 14
15 DTGC Mode Test: AFE5832 EVM Switches (S5) 15
16 DTGC Mode Test: Change GUI Configuration 15
17 DTGC Mode Test: Trigger Options 16
18 DTGC Mode Test: HSDC Pro Test Parameter Settings 16
19 DTGC Mode Test: Waveform 16
20 CW Mode Preset 17
21 CW Output 18
22 HSDC Pro Install (Begin) 19
23 HSDC Pro Install (TI License Agreement) 20
24 HSDC Pro Install (TI License Agreement) 20
25 HSDC Pro Install (Install Directory) 21
26 HSDC Pro Install (Installation Ready) 21
27 HSDC Pro Install (Cypress Driver Install) 22
28 HSDC Pro Install (Continue Installation) 22
29 HSDC Pro Install (Continue Driver Installation) 23
30 HSDC Pro Install (Finish Installation) 23
31 AFE5832 GUI Install (Begin Installation) 24
32 AFE5832 GUI Install (TI License Agreement) 25
33 AFE5832 GUI Install (National Instruments® License Agreement) 26
34 AFE5832 GUI Install (PSF License Agreement) 27
35 AFE5832 GUI Install (Install Directory) 28
36 AFE5832 GUI Install (Select Components) 28
37 AFE5832 GUI Install (Installation Ready) 29
38 AFE5832 GUI Install (Installation Progress) 29
39 AFE5832 GUI Install (Installation for Users) 30
40 AFE5832 GUI Install (Python® is Already Installed) 30
41 AFE5832 GUI Install (Destination Directory) 31
42 AFE5832 GUI Install (Customize Python®) 31
43 AFE5832 GUI Install (Python® Installation Progress) 32
44 AFE5832 GUI Install: (Python® Finished) 32
45 AFE5832 GUI Install (Finished) 33
46 AFE5832: Hovering Over Controls 34
47 AFE5832: Quick Setup Tab 36
48 AFE5832: Quick Setup: HSDC Pro Related Parameters 37
49 AFE5832: VCA: VCA and CW Mixer 38
50 AFE5832: VCA: DTGC 39
51 AFE5832: ADC: Top Level 40
52 AFE5832: ADC: Test Pattern 41
53 AFE5832: ADC: Digital Signal Processing 42
54 Clicking on Register and Field Names 43
55 AFE5832: Register Map Configuration: Update Modes 44
56 AFE5832: Register Map Configuration: Immediate Update Mode 45
57 AFE5832: Register Map Configuration: Deferred Update Mode 46
58 AFE5832: Register Map Configuration: Changing Register Value 47
59 AFE5832: Register Map Configuration: Manual Data Entry 48
60 Default Jumper Positions 49
61 EVM ADC Clock Source Configuration 51
62 AFE EVM ADC Clock Source Configuration Schematic 52

63 EVM ADC Clock Source Configuration Examples 52
64 CPLD Switches and LEDs 53
65 HSDC Pro Trigger Configuration for SW 54
66 HSDC Pro Trigger Configuration for SW Trigger 55
67 HSDC Pro Trigger Configuration for HW 55
68 HSDC Pro Trigger Configuration for HW External Trigger 56
69 AFE5832 EVM Block Diagram 58
70 AFE5832 Rev. A EVM Schematic 1 of 12 59
71 AFE5832 Rev. A EVM Schematic 2 of 12 60
72 AFE5832 Rev. A EVM Schematic 3 of 12 61
73 AFE5832 Rev. A EVM Schematic 4 of 12 62
74 AFE5832 Rev. A EVM Schematic 5 of 12 63
75 AFE5832 Rev. A EVM Schematic 6 of 12 64
76 AFE5832 Rev. A EVM Schematic 7 of 12 65
77 AFE5832 Rev. A EVM Schematic 8 of 12 66
78 AFE5832 Rev. A EVM Schematic 9 of 12 67
79 AFE5832 Rev. A EVM Schematic 10 of 12 68
80 AFE5832 Rev. A EVM Schematic 11 of 12 69
81 AFE5832 Rev. A EVM Schematic 12 of 12 70
82 Read DDR Error for No Capture 82

List of Tables

1 Default Header Configuration Table Rev. A 50
2 EVM Rev. A Testpoints 50
3 AFE5832 EVM Bill of Materials 71

Trademarks

1 EVM Hardware Overview

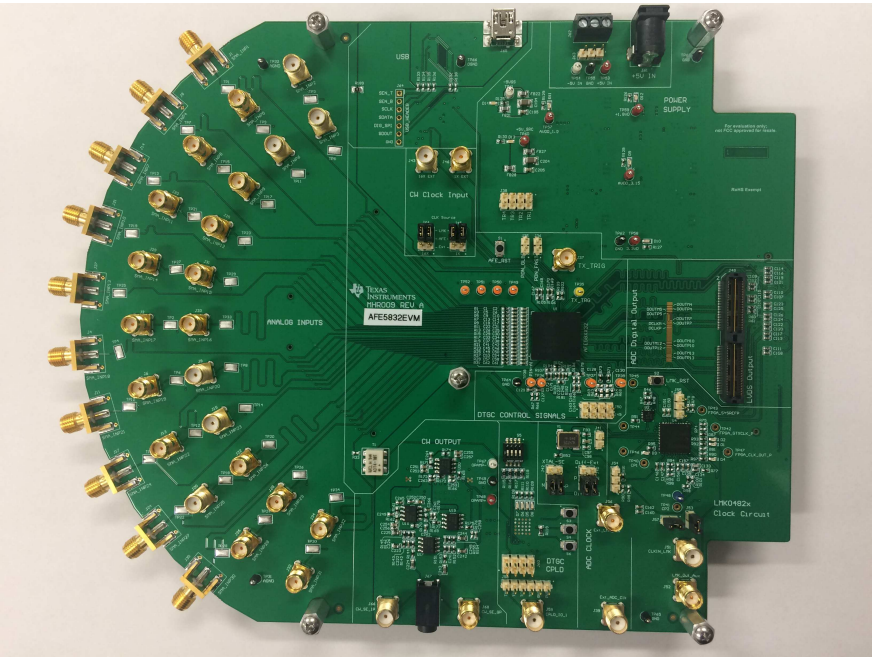


Figure 1. AFE5832 EVM Hardware Overview

The EVM received should resemble Figure 1. For more hardware details and the default jumper map, see Appendix C.

The AFE5832 EVM kit contains the following items:

1. AFE5832 EVM
2. 1 mini-USB cable
3. Power cable with barrel connector

Figure 2. Provided Power Cable for J1 Connector

2 GUI Software Installation

The AFE5832 EVM and the TSW capture card EVM have individual software and both require software installations. Ensure that no USB connections are made to the EVMs until after the installations are complete. This user's guide refers to software AFE5832 GUI v.1.0.0, and HSDC Pro Software v.4.7.

See the *HSDCPro Installation* section for information on the installation of the TSW EVM Software GUI (HSDC Pro). For information on the installation of the AFE5832 EVM Software GUI, see the *AFE5832 EVM GUI Installation* section.

3 Quick Views of Evaluation Setups for LVDS Interface

The AFE5832 EVM is tested using the TSW1400EVM for LVDS data interface.

3.1 Equipment Setup Overview

As shown in Figure 3, mating the AFE5832 EVM with a TSW EVM allows for testing using the data interface.

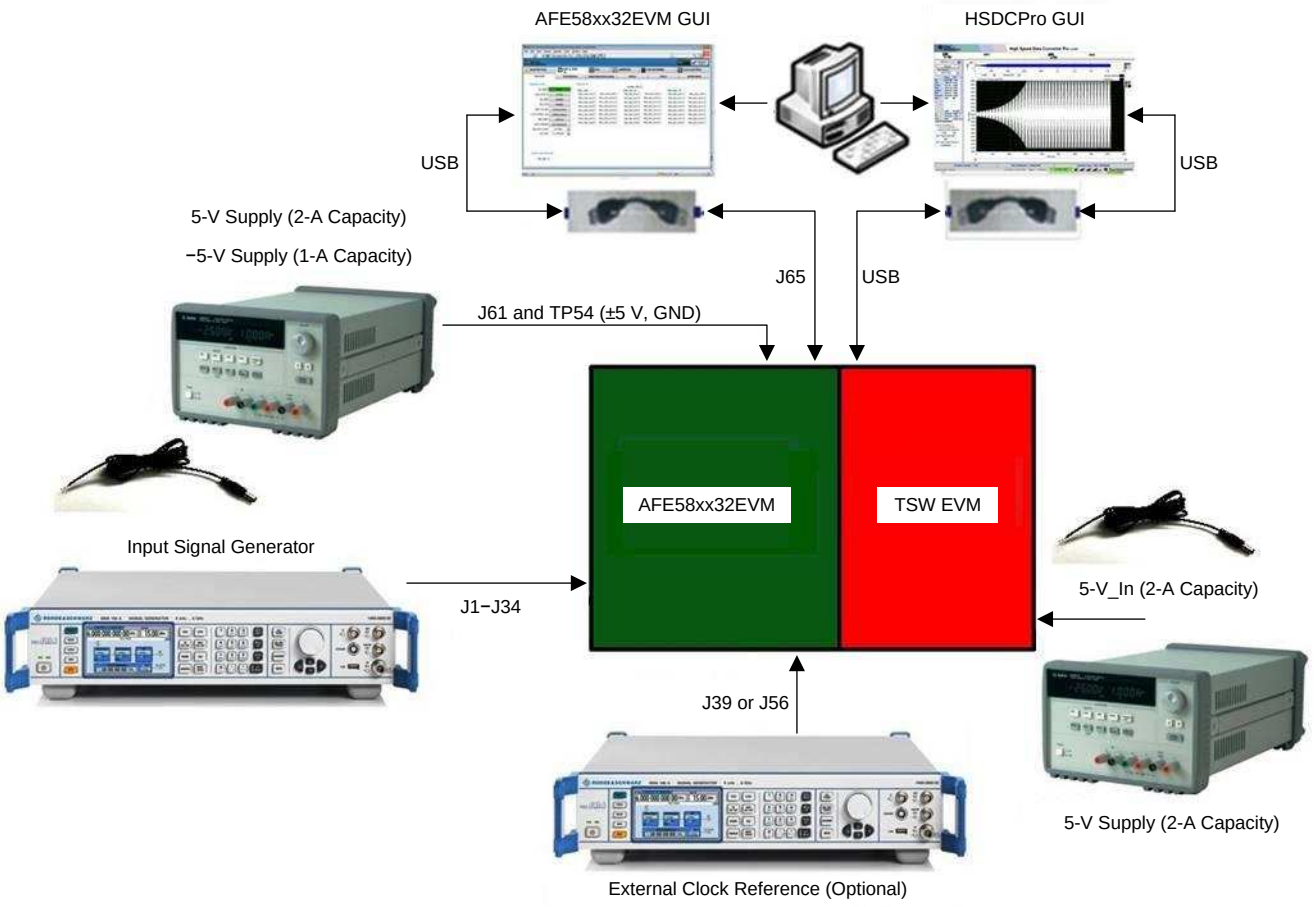


Figure 3. Evaluation Setup Overview

TSW Capture Card EVM: The TSW1400 EVM is required for capturing data from the AFE5832 EVM and its analysis using the graphical user interface (GUI), called High Speed Data Converter Pro (HSDC Pro).

For more information on the TSW1400EVM, see: TSW1400EVM.

Power Supply: A barrel connector power cable is provided with the EVM and is connected at J61, but does not support the –5 V needed for the CW mode. This requires an additional cable, not provided.

This 5-V power supply must be able to source up to 2 A, and –5-V supply must provide up to 1 A. The –5-V supply is used for the negative supply of amplifiers in the CW output external circuitry. The TSW1400 EVM is powered through a power cable similar to Figure 2 that is provided with its own EVM kit.

USB Interface to PC: The USB connections from the AFE5832 EVM and TSW EVM to the PC are used for communication from the GUIs to the boards. USB 2.0 or 3.0 ports are both acceptable.

Equipment: Signal generators (with low-phase noise) must be used as source of the input signal for optimal performance. An onboard crystal oscillator option is provided so that an external clock source is not needed for basic capture. Additionally, for best performance a band-pass filter (BPF) is recommended on the analog input signal to attenuate the harmonics and noise from the signal. For coherent sampling or custom sample rate, an external clock is provided to J39 or J56 (GUI configuration is required for the external clock configuration). For more information on clock configuration, see Section C.1.3.

4 Testing the EVM Data Capture with LVDS Interface

This section outlines (1) the external connections required to test the AFE5832 EVM using the LVDS interface, (2) how to setup the GUIs for testing, and (3) how to capture an analog input signal.

4.1 EVM Hardware Setup

Make the connections shown in Figure 4 for proper hardware setup.

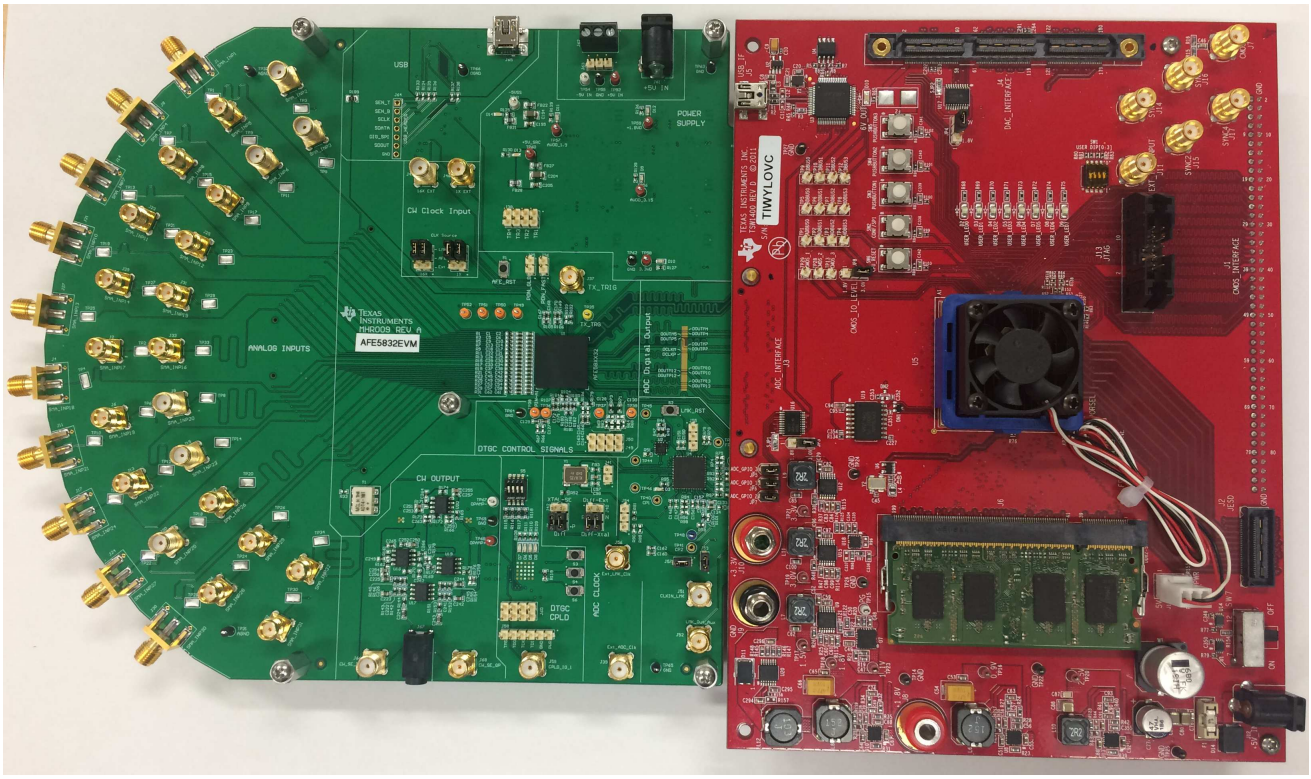


Figure 4. TSW1400EVM and AFE5832 EVM Hardware Setup for LVDS Capture

1. **Board Mating:** For LVDS data, mate the TSW1400 EVM at connector **J3** to the AFE5832 EVM at connector **J48** through the high-speed ADC interface connector.
2. **Power Supply:** Connect a 5-V (2-A) power supply using the provided power cable to **J12 (+5V_IN)** of the TSW1400 EVM or **J11 (+5V_IN)** of the TSW14J50 EVM . See the TSW manual for more information, if needed.

   Next, connect a 5-V (2-A) power supply using the provided power cable to **J61** of the AFE5832 EVM. **Connect the white-striped side of this cable to the positive side of the 5-V power supply.** Optionally, connect a –5-V (1-A) supply at **J63** or TP54 if using the CW circuit. No cable is provided for this.

   Turn on the TSW1400 at the SW7 switch.
3. **USB:** After installing the GUIs as shown in Appendix A, connect the USB cable from the PC to **J65 (USB)** located on the top side of the AFE5832 EVM. Connect the USB cable from PC to **J5 (USB_IF)** of the TSW1400 EVM.

   NOTE: TI recommends that the PC USB port be able to support USB2.0. If unsure, always choose the USB ports at the back of the PC chassis over ones located on the front or sides.
4. **Equipment:** Connect a sine wave generator to SMA **J1, INP1**. Set the frequency to 5 MHz and the amplitude to –20 dBm. For best performance, a 5-MHz band-pass filter (BPF) is recommended on the analog input signal to attenuate the harmonics and noise from the signal.
5. **CPLD Switches:** Ensure that all 4 switches in **S5** are in the 'off' position. LEDs D5–D8 should be lit up.

S4 should be 'off' immediately after powering up the board for LVDS capture, but can be manipulated for other modes. For more information on the Complex Programmable Logic Device (CPLD), refer to Section C.1.4.

4.2 Capturing an Analog Input Signal With the LVDS Interface

This section describes the software setup for capturing an analog input using the AFE5832 EVM. If there is any issue with a data capture, refer to the troubleshooting section.

Data capture is confirmed by using only the *Quick Setup* page of the AFE5832 GUI. Assuming the hardware is connected correctly as in Section 4.1, follow these steps to acquire data:

4.2.1 HSDC Pro Actions

1. Connect both EVMs to the PC using two USB cables as instructed in Section 4.1.
2. Open the HSDC Pro GUI using *Run as Administrator*. **Do not open the AFE5832 GUI before this step because it opens automatically. If it is already open, close it.**
3. If the TSW Hardware is already connected to the USB, then a pop-up window should appear to connect the HSDC Pro GUI to the EVM Hardware.

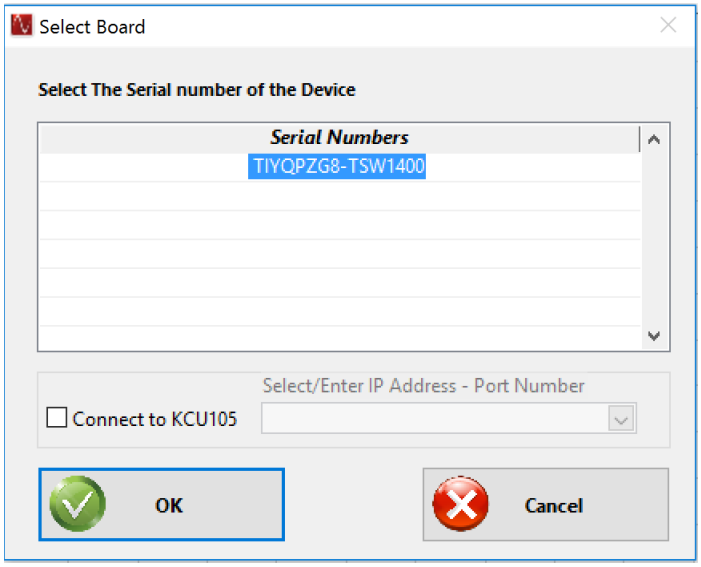


Figure 5. Connect to TSW EVM (TSW1400 Shown)

4. A pop-up window prompts the user to choose a firmware to download to the TSW EVM FPGA.
5. Select firmware: In the upper left-hand corner "Select ADC" box, type the name of your device and the drop-down list will automatically filter based on your input. Then, from the drop-down, choose your desired format. **Be sure to choose the correct device to match the AFE5832 EVM hardware or the AFE5832 GUI will show an error when launching.**

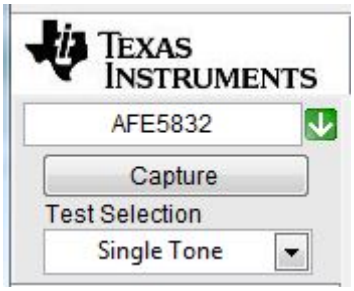


Figure 6. Choose Firmware

6. When prompted to update the firmware, click the *Yes* button.
7. The firmware begins downloading to the FPGA on the TSW EVM.
8. When the firmware has finished downloading, several Green LEDs are lit on the TSW EVM. For the TSW1400, D5 (USER_LED3) is usually off when the EVM is not configured, and D6 is off.

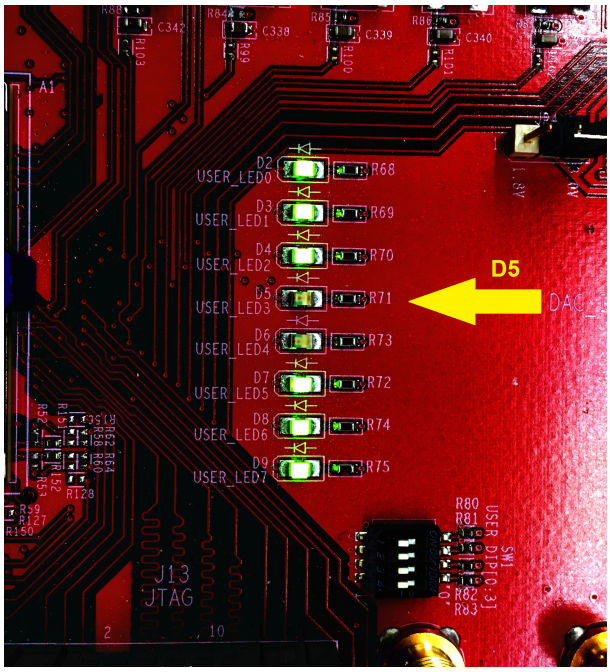


Figure 7. TSW1400 EVM LEDs Turn On After Firmware Download

9. The AFE5832 EVM GUI opens automatically. Wait until this is finished before continuing. If any errors arise at this time, contact TI support.

Figure 8. AFE5832 GUI Launches

4.2.2 AFE5832 GUI Actions

1. Verify the clock configuration by matching J42, J40, and J54 to Figure 9. Provide a 160-MHz, +13-dBm clock to J56.

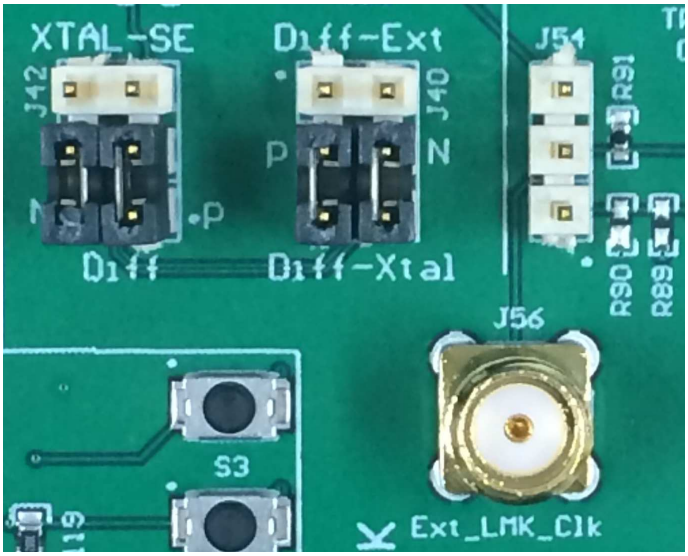


Figure 9. Clock Configuration on AFE EVM for LVDS Capture

2. Press the *DUT RESET* button on the AFE5832 GUI.
3. Press the *Initialize Device* button on the AFE5832 EVM GUI (Figure 10). These buttons are located close to the upper left-hand corner of the GUI window.
   - Alternatively, there is an option to use the hardware reset. Press the AFE_RST button on the AFE EVM, located above the AFE device (S1), as shown in Figure 11. Hold for 1 second. Then, press the *Initialize Device* button on the AFE5832 EVM GUI.

Figure 10. Software Reset and Initialize Buttons on AFE5832 EVM GUI

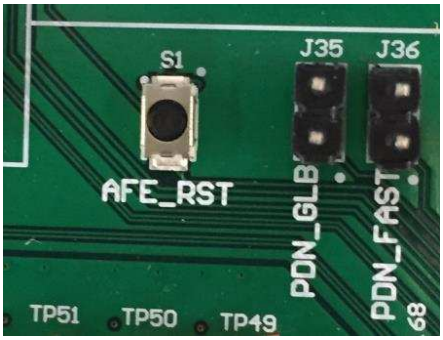


Figure 11. AFE_RST Hardware Reset Button

4. Ensure there is no SMA cable connected to J37 TX_Trig on the AFE5832EVM.
5. Turn switch 4 contained in **S5** on the AFE EVM 'off' for LVDS only. The red LED, D8 should light up. For more information on the *Complex Programmable Logic Device* (CPLD), refer to Section C.1.4.
6. Choose the *Data Formats* and the *Analog Configuration* for each category as shown in Figure 12:
   - OUTPUT FORMAT: Select ‘LVDS: 12x 12b’
   - ADC FORMAT: Select ‘Analog Input’
   - VCA GAIN: Select ‘Mid Gain’
   - DTGC Modes: Select ‘Programmable Fixed-Gain Mode’

NOTE: Ensure the right CPLD switches are configured on S5 as detailed for each capture mode.

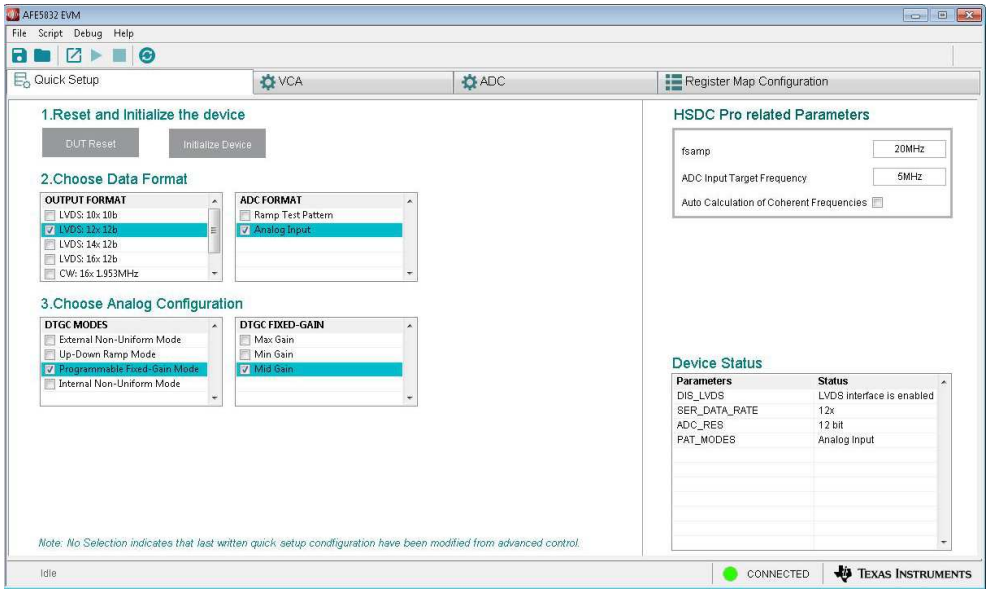


Figure 12. AFE5832 EVM GUI Data Format and Analog Configuration (LVDS)

7. At this point, D5 on the TSW1400 EVM should turn on. If this is not the case, consult Appendix G. There is most likely an ADC clock issue.

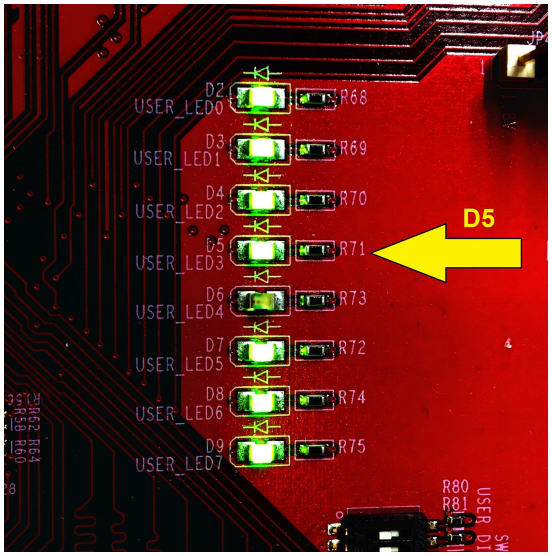


Figure 13. LED D5 on the TSW1400 EVM Turns On When ADC is Ready

8. Return to HSDC Pro, and press the *Capture* button in the upper left-hand corner (as shown in Figure 14). A capture similar to that shown in Figure 14 appears for a successful capture. The quality of the output spectrum depends heavily on the coherency and the purity of the input signal and clock.

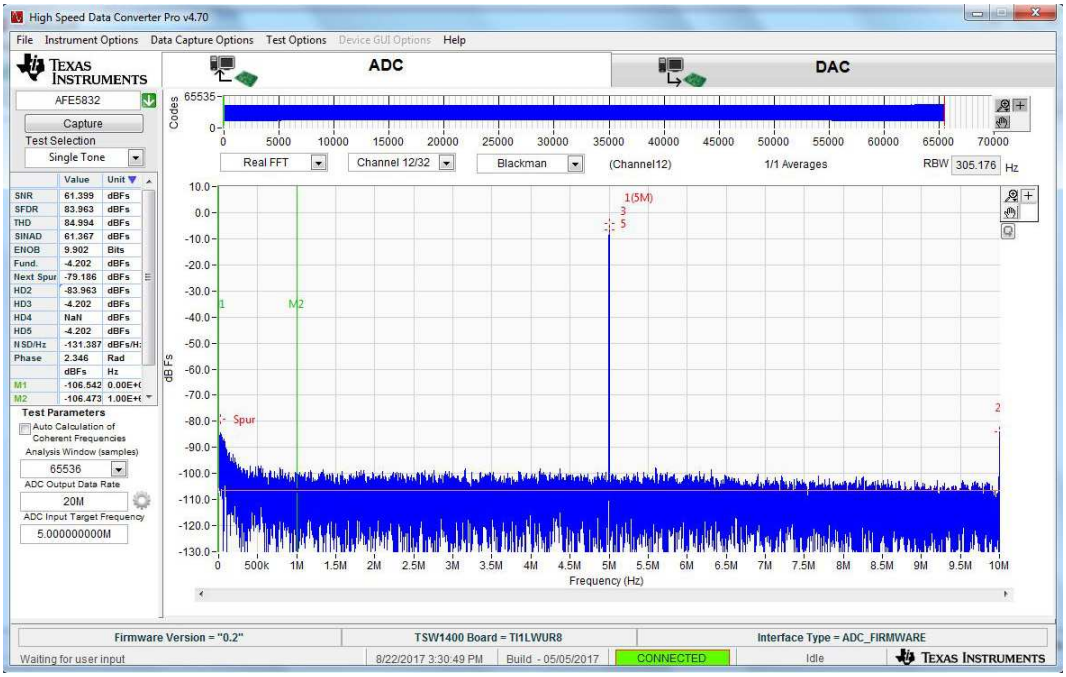


Figure 14. Analog Input Capture for LVDS

5 Testing the EVM in Digital Time Gain Compensation (DTGC) Mode

Use the following steps to test the EVM in DTGC mode:

a. Input a 5-MHz, –20-dBm signal to any SMA input on the AFE EVM. Connect a 5-MHz filter to the input signal. Connect a single SMA-SMA cable from J11 (TSW EVM) to J37 (AFE EVM).

b. Change the jumper configurations as outlined in Section C.1.3 and apply a 160-MHz, 10-dBm external LMK input clock to J56 or clock at 4× the desired ADC sample rate.

c. Set the switches of the AFE5832 EVM at S5 for 'Up-Down Ramp Mode' as Figure 15 illustrates. LEDs D6-D8 should be lit and LED D5 should be off.

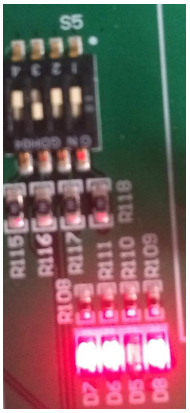


Figure 15. DTGC Mode Test: AFE5832 EVM Switches (S5)

d. Choose *AFE5832.ini* as firmware on HSDC Pro.

e. Change the DTGC Mode on the AFE5832 EVM GUI to ‘Up-Down Ramp Mode’ and configure the other formats as shown in Figure 16:

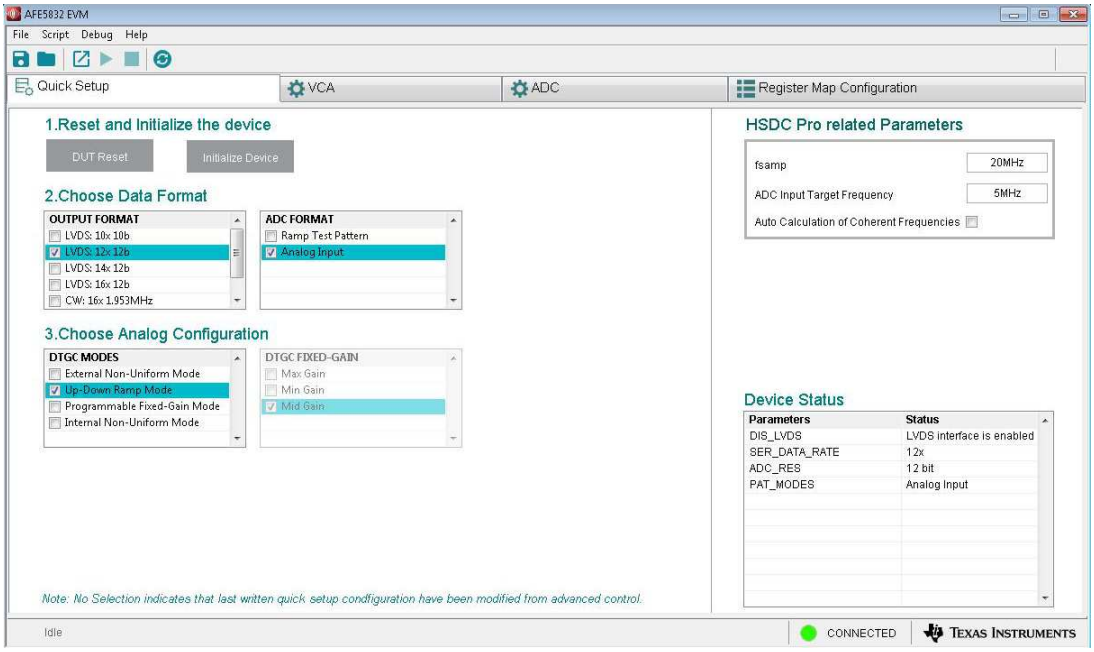


Figure 16. DTGC Mode Test: Change GUI Configuration

f. In HSDC Pro, navigate to the *Trigger Option* menu. Choose “Trigger mode enable” and “Arm on next capture button press” as shown in Figure 17.

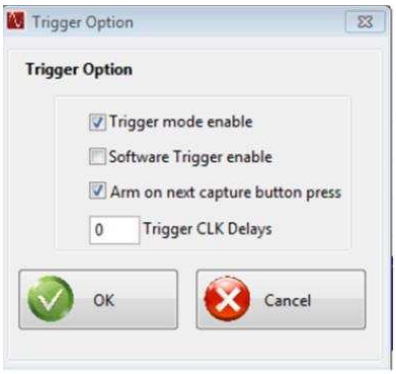


Figure 17. DTGC Mode Test: Trigger Options

g. Change the *ADC Output Data Rate* to '20M' and the *ADC Input Target Frequency* to '5M'. Set the view display to 'Codes'.

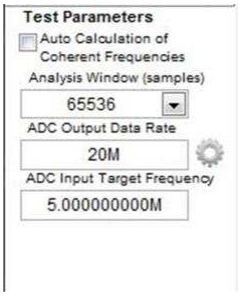


Figure 18. DTGC Mode Test: HSDC Pro Test Parameter Settings

h. Press the *Capture* button on HSDC Pro.

i. The Up-Down Ramp DTGC waveform should appear similar to Figure 19.

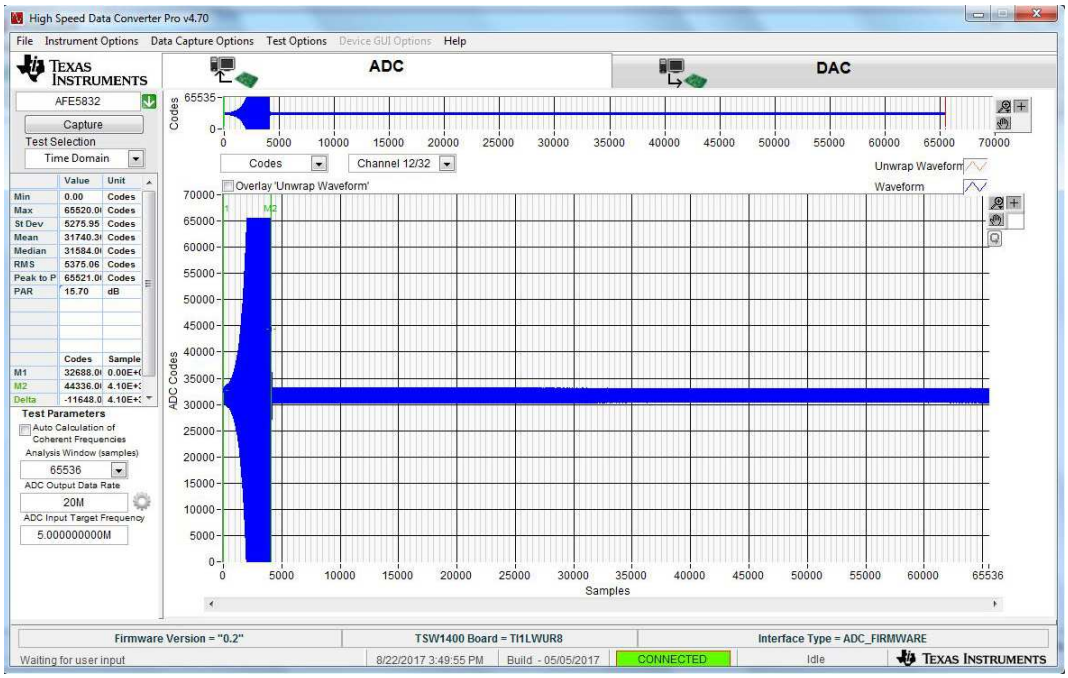


Figure 19. DTGC Mode Test: Waveform

6 Using the EVM in CW Mode

Demonstrating the CW mixer in the AFE is done by following these steps:

1. In the AFE5832 GUI, reset and initialize the device by referring to Figure 10 and Figure 11. Remember to connect a –5-V and a 5-V source to the device.
2. Connect a sine wave generator to any SMA channel. Set the frequency to 1.963125 MHz and the amplitude to –23 dBm.
3. Provide a 125-MHz, +10-dBm clock input to J56 of the AFE EVM (LMK external clock). Refer to Section C.1.3 for jumper configurations.
4. Turn *Switch 4* contained in **S5** on the AFE EVM to 'on'. The red LED, D8 should not light up. For more information on the CPLD, refer to Section C.1.4.
5. Connect two cables to an oscilloscope with timebase of 40 µs and 500 mV / div. Input resistance should be 1 MΩ on each scope channel. DC couple the oscilloscope.
6. Connect those two cables to SMAs, J66 and J68 on the AFE EVM.
7. Choose the following data format on the AFE5832 EVM GUI:

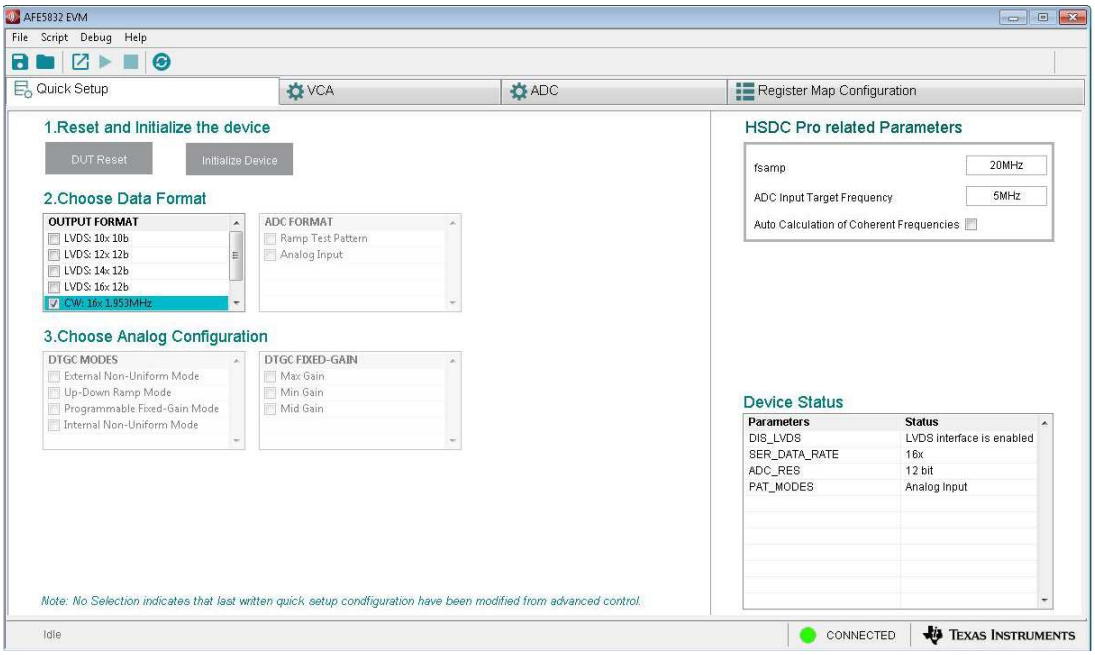


Figure 20. CW Mode Preset

8. Trigger the oscilloscope on either channel.
9. The oscilloscope displays the frequency I and Q signals at 10 kHz as shown in Figure 21. The amplitude should be around 1.5 Vpp ±300 mVpp, though this amplitude may change. The frequency should be 10 kHz and the I and Q signals should be 90 degrees out of phase.

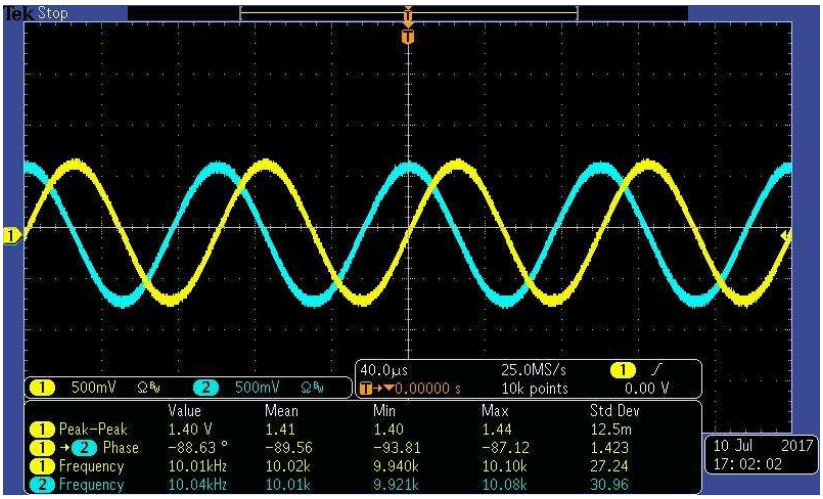


Figure 21. CW Output

Software Installation

Section A.1 provides detailed procedures for installing High Speed Data Converter Pro (HSDC Pro), the software GUI used to control a suite of FPGA capture solutions including the TSW1400. Section A.2 provides details for installing the AFE5832 EVM GUI.

A.1 High Speed Data Converter Pro (HSDC Pro) GUI Installation

Download HSDC Pro v.4.7 from the mySecureSoftware folder at https://www.ti.com/securesoftware/docs/securesoftwarehome.tsp.

1. Unzip the saved file and run the installer executable (*Run as Administrator*) to obtain the menu shown in Figure 22.
2. Click the *Next* button.

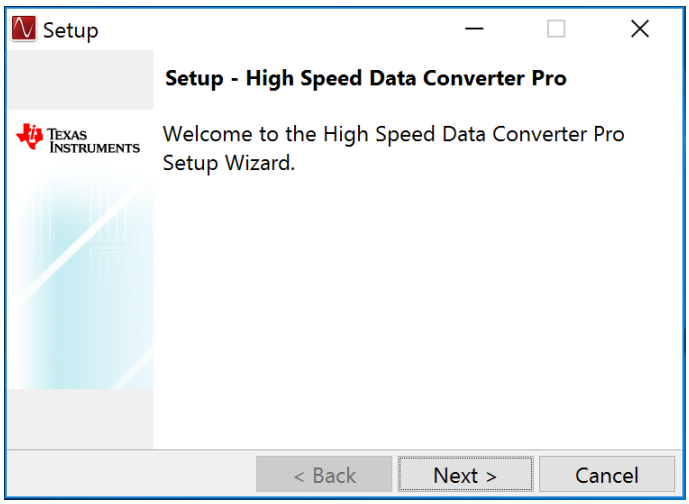


Figure 22. HSDC Pro Install (Begin)

3. Read the License Agreement from Texas Instruments and select *I accept the License Agreement*, then press the *Next* button as shown in Figure 23.

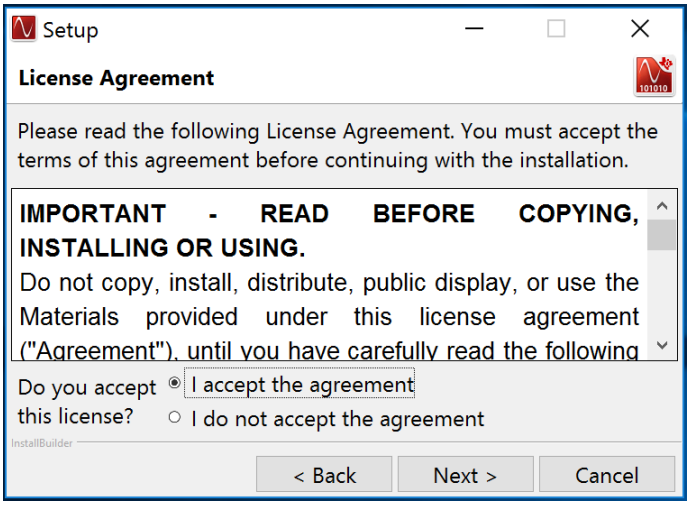


Figure 23. HSDC Pro Install (TI License Agreement)

4. Read the License Agreement from Texas Instruments and select *I accept the agreement*, then press the *Next* button as shown in Figure 24.

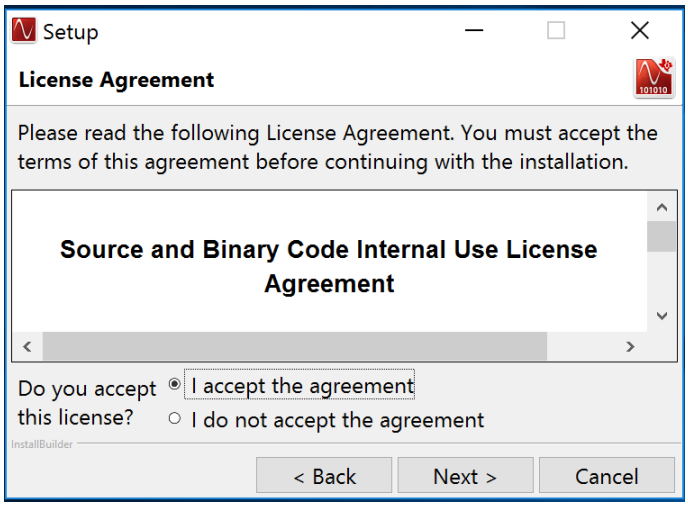


Figure 24. HSDC Pro Install (TI License Agreement)

5. Allow the installation to be placed in the default directory by clicking *Next*, as in Figure 25.

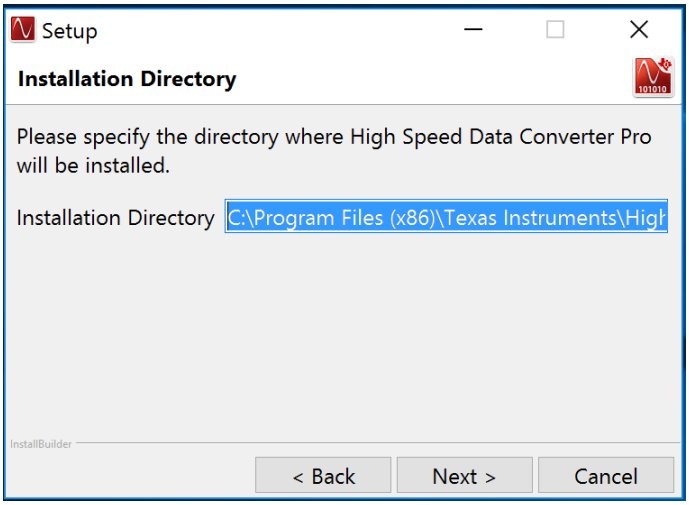


Figure 25. HSDC Pro Install (Install Directory)

6. Click *Next* to begin the installation, as in Figure 26.

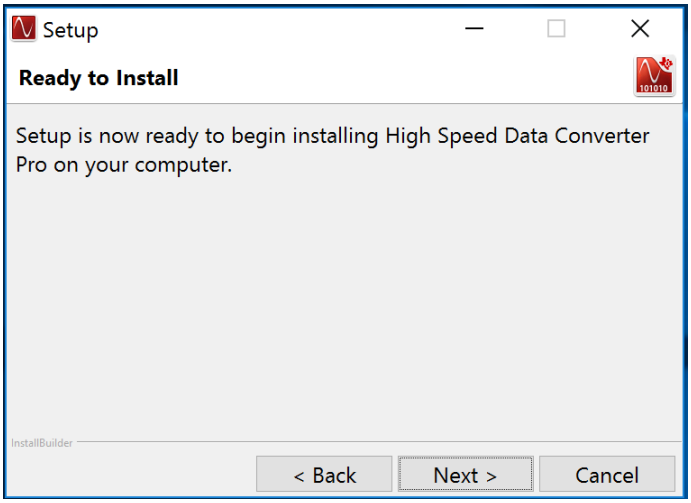


Figure 26. HSDC Pro Install (Installation Ready)

7. The Cypress Driver begins installing as shown in Figure 27.

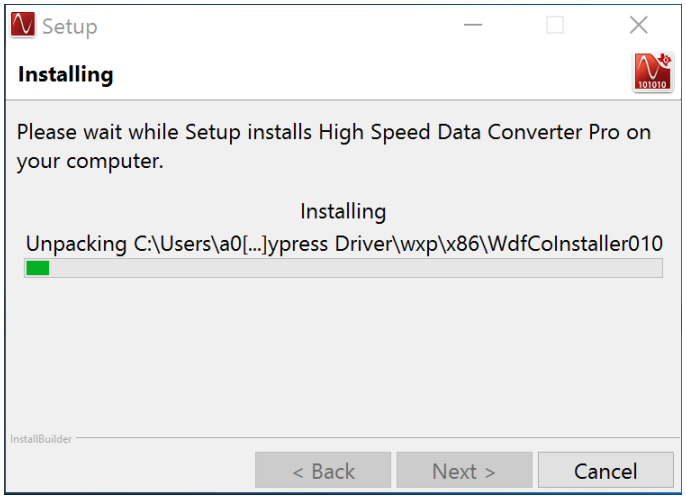


Figure 27. HSDC Pro Install (Cypress Driver Install)

8. Click *Finish* to continue installation, as shown in Figure 28.

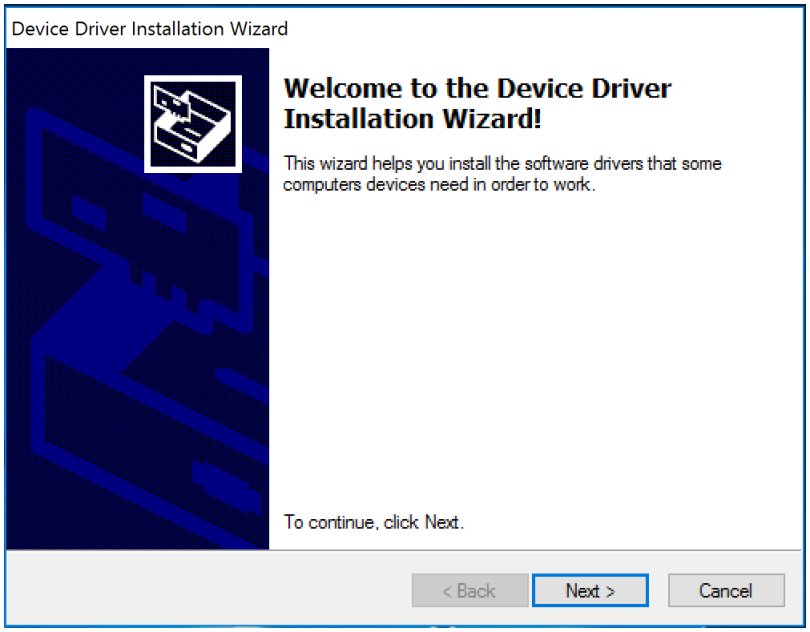


Figure 28. HSDC Pro Install (Continue Installation)

9. Click *Finish* to continue installation, as shown in Figure 29.

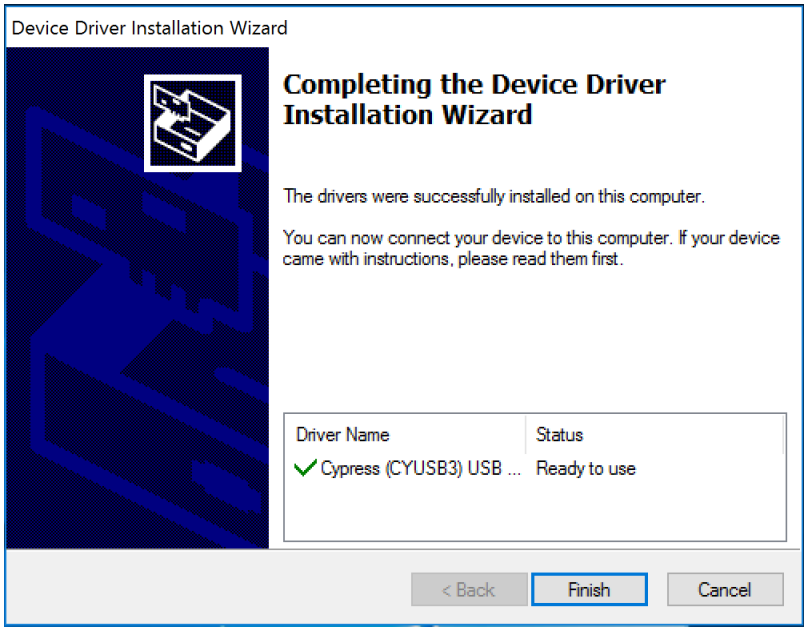


Figure 29. HSDC Pro Install (Continue Driver Installation)

10. Finish HSDC Pro installation by choosing the appropriate installation options and pressing *Finish*, as in Figure 30.

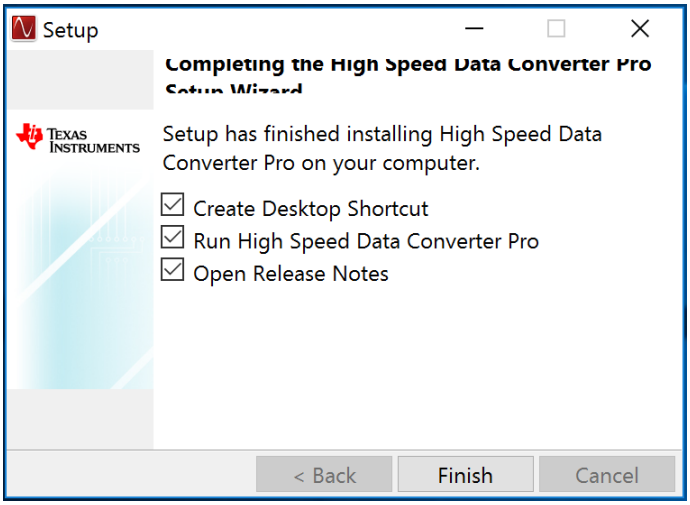


Figure 30. HSDC Pro Install (Finish Installation)

A.2 AFE5832 GUI Installation

Download the AFE5832 EVM GUI from the mySecureSoftware folder at https://www.ti.com/securesoftware/docs/securesoftwarehome.tsp.

1. Unzip the saved file and run the installer executable as administrator by right clicking on the file and selecting *Run as Administrator*. Press the *Next* button once the graphic in Figure 31 appears.

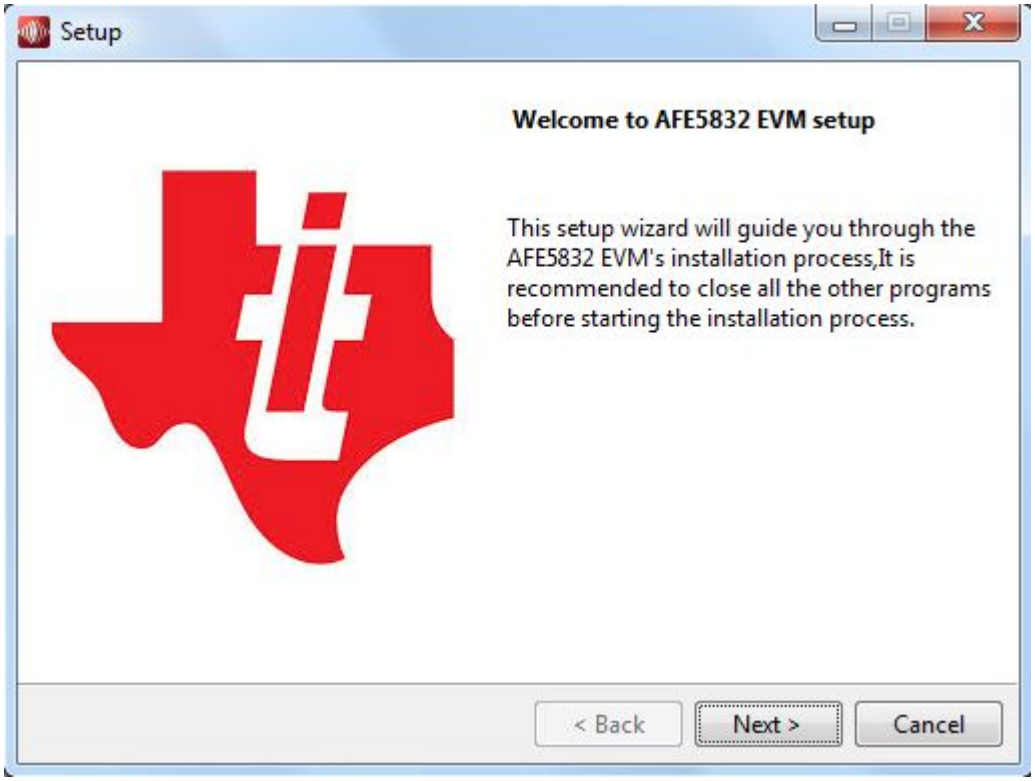


Figure 31. AFE5832 GUI Install (Begin Installation)

2. Read the Texas Instruments License Agreement and select *I accept the agreement* followed by the *Next* button, as in Figure 32.

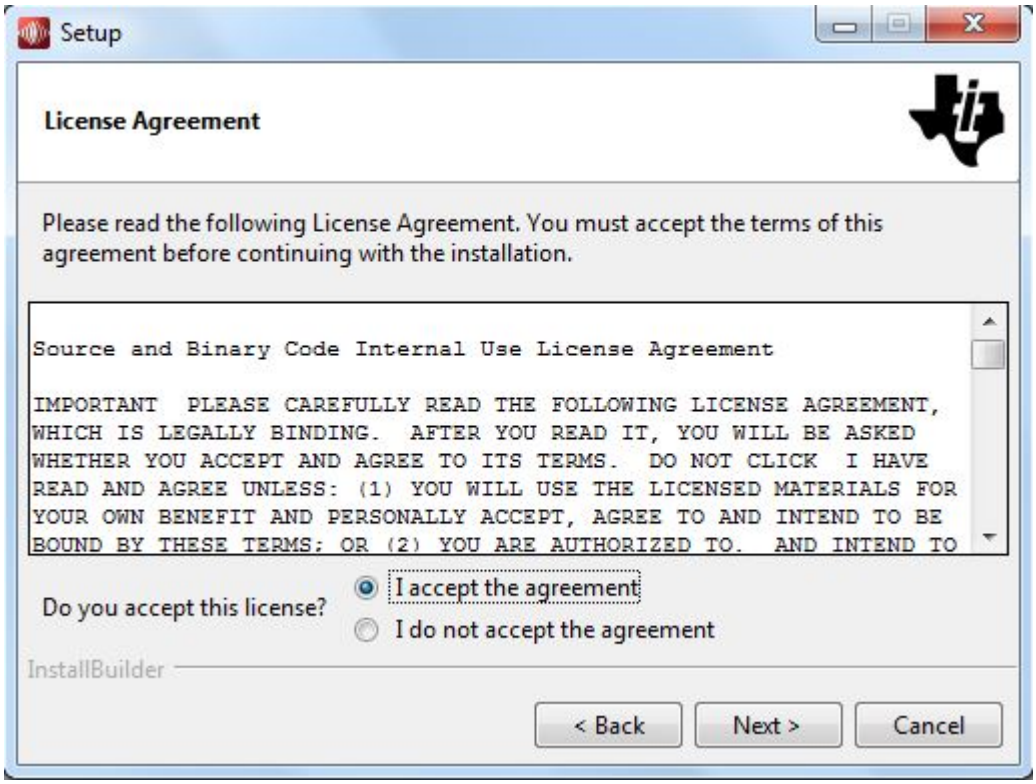


Figure 32. AFE5832 GUI Install (TI License Agreement)

3. Read the National Instruments® License Agreement and select *I accept the agreement* followed by the *Next* button, as in Figure 33.

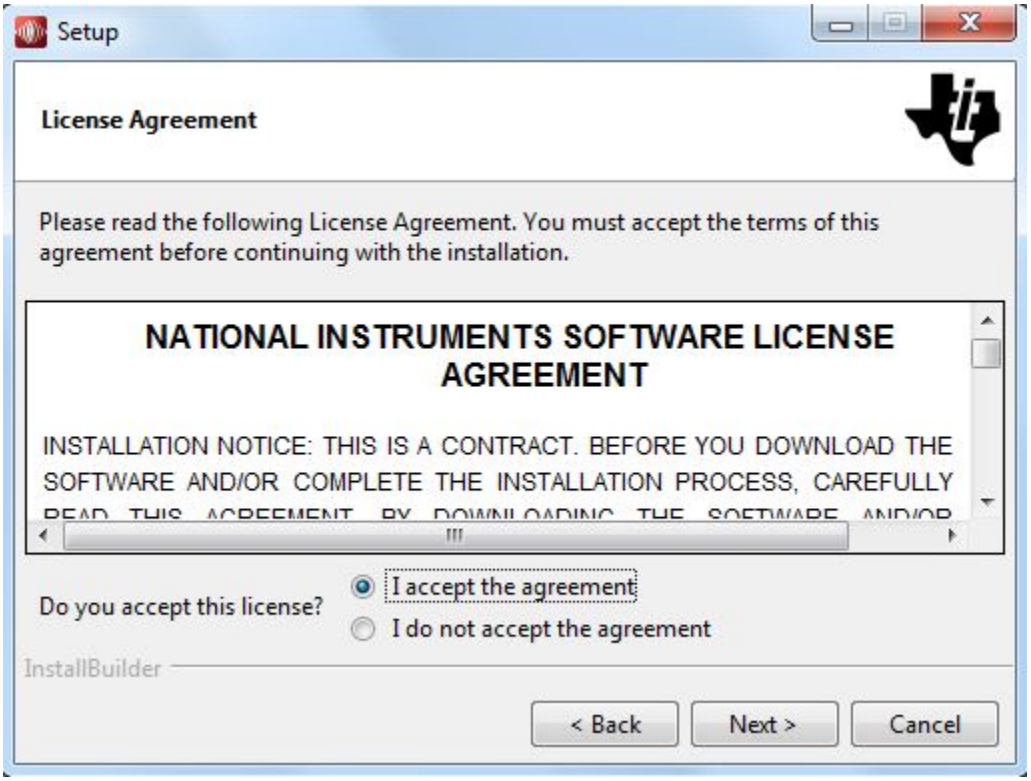


Figure 33. AFE5832 GUI Install (National Instruments® License Agreement)

4. Read the PSF License Agreement for Python® 2.7 and select *I accept the agreement* followed by the *Next* button, as in Figure 34.

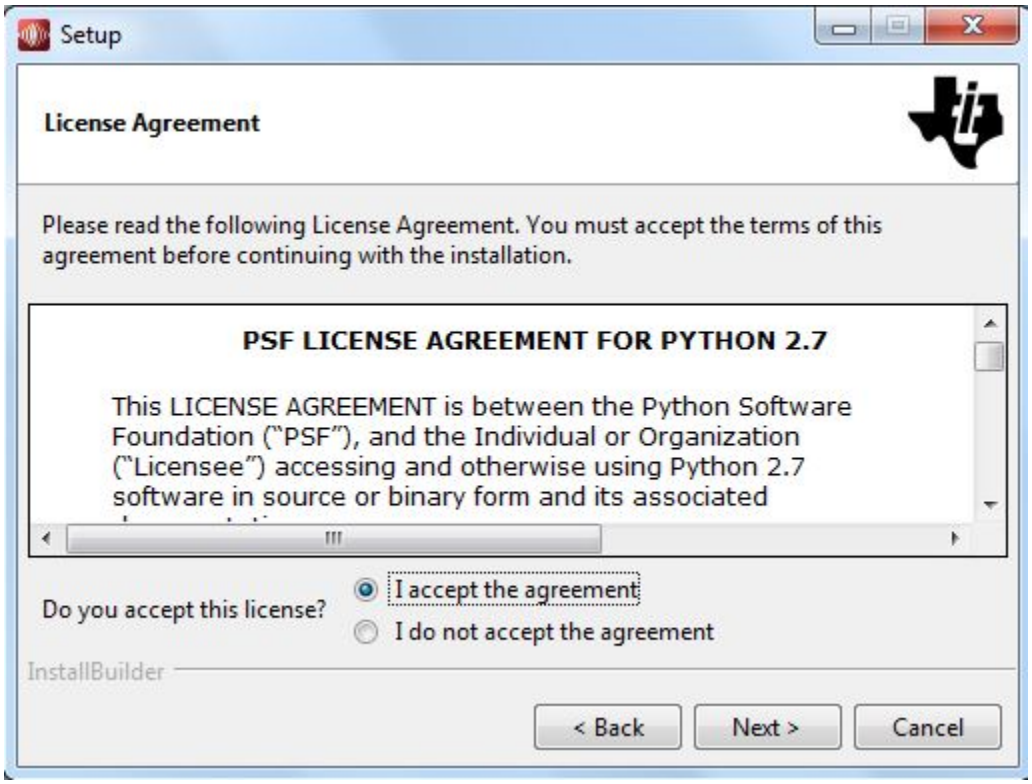


Figure 34. AFE5832 GUI Install (PSF License Agreement)

5. Allow the software to be installed in the default location by pressing the *Next* button, as in Figure 35.

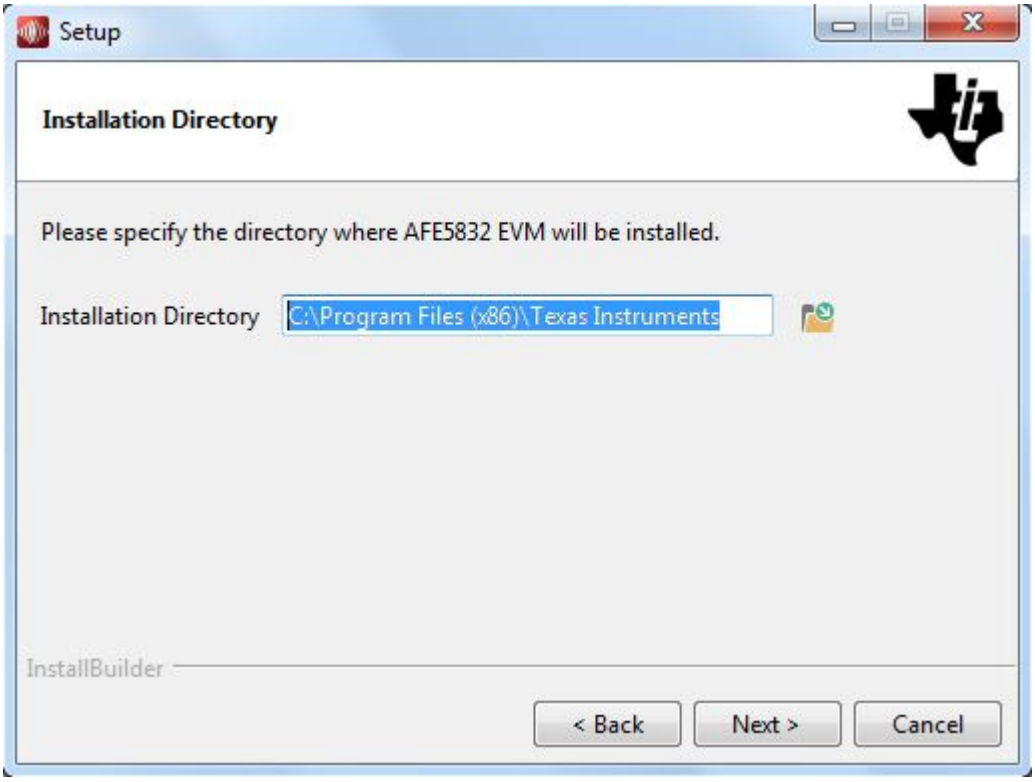


Figure 35. AFE5832 GUI Install (Install Directory)

6. Select the components to install and press *Next*.

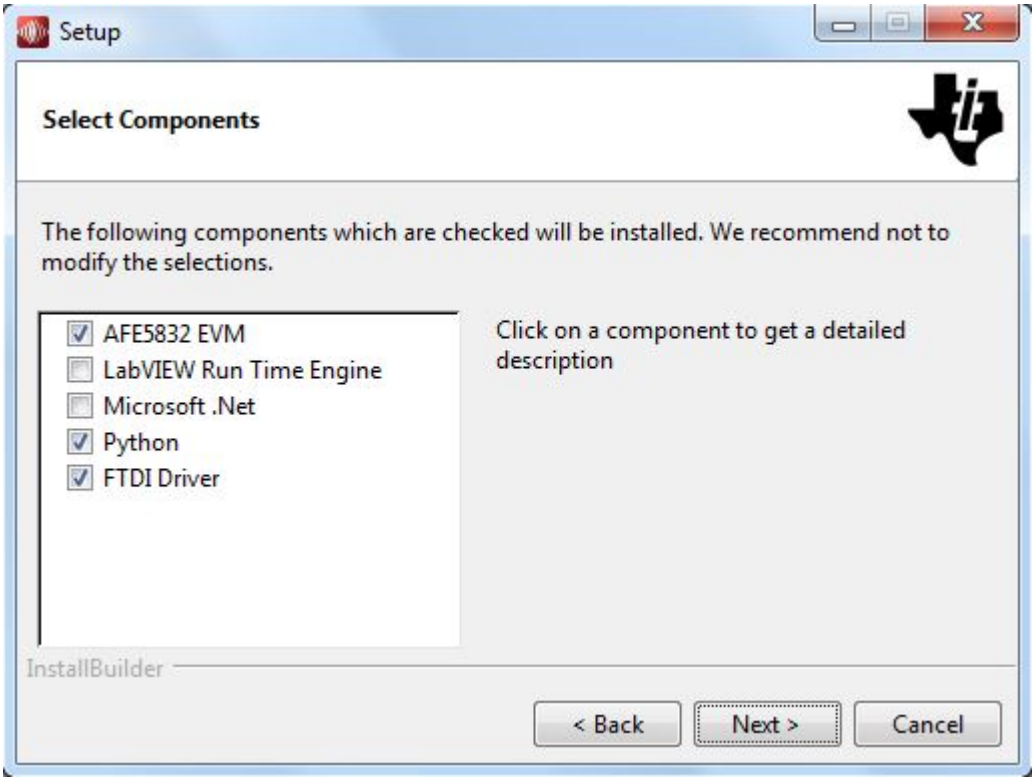


Figure 36. AFE5832 GUI Install (Select Components)

7. Pressing the *Next* button begins installation, as shown in Figure 37.

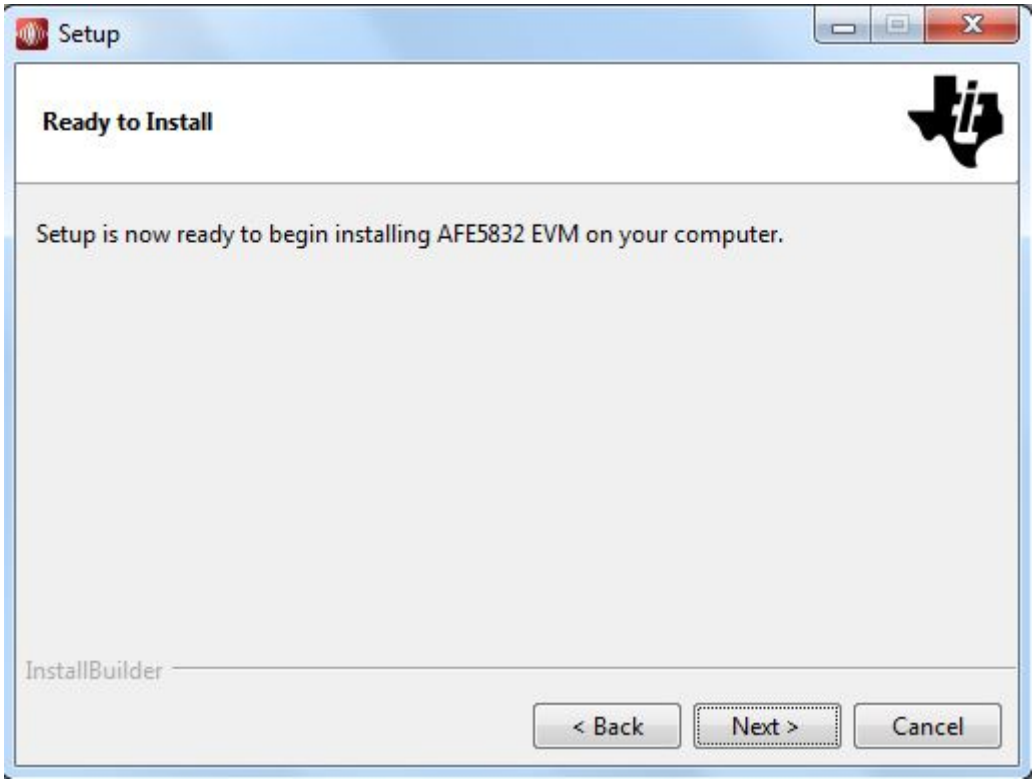


Figure 37. AFE5832 GUI Install (Installation Ready)

8. The window shown in Figure 38 appears showing that the installation is in progress.

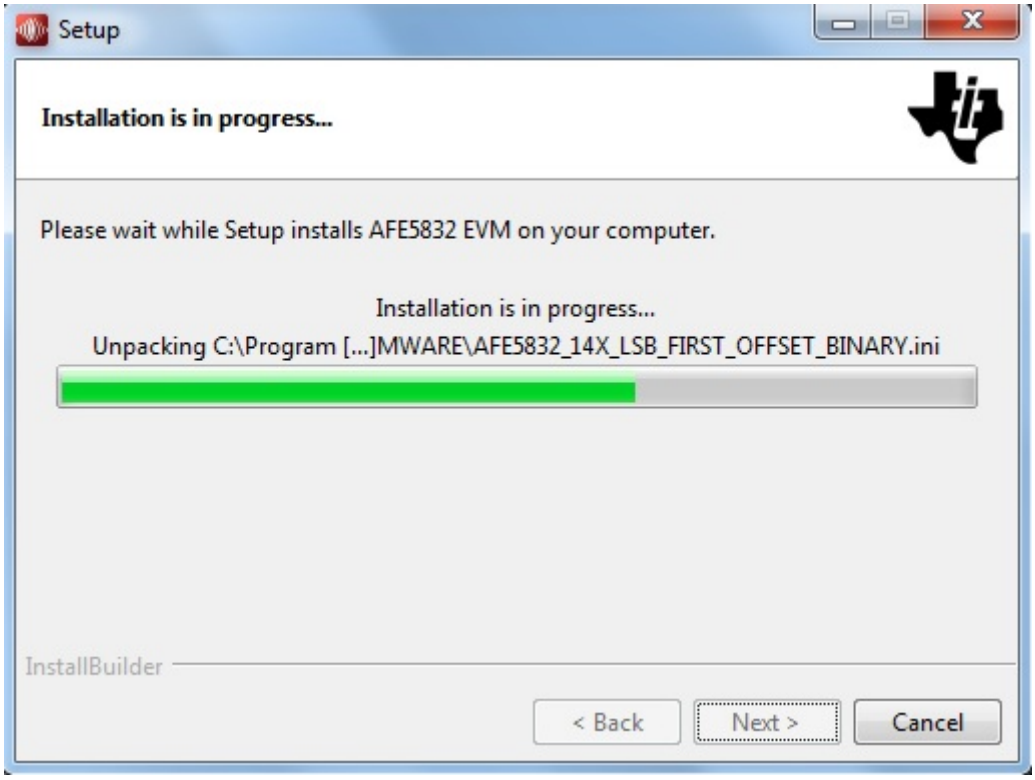


Figure 38. AFE5832 GUI Install (Installation Progress)

9. A window for the *Python 2.7 Setup* comes up. Select *Install for all users* as in Figure 39.

Figure 39. AFE5832 GUI Install (Installation for Users)

If Python is already installed, select the option for *Repair Python 2.7*. Proceed to step 13 and click the *Finish* button.

Figure 40. AFE5832 GUI Install (Python® is Already Installed)

10. Allow the software to be installed in the default destination directory as in Figure 41.

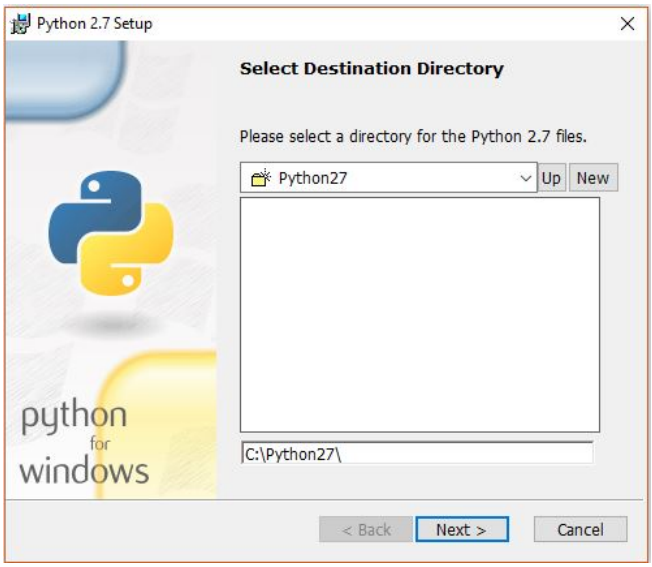


Figure 41. AFE5832 GUI Install (Destination Directory)

11. Click *Next* on the screen displayed in Figure 42.

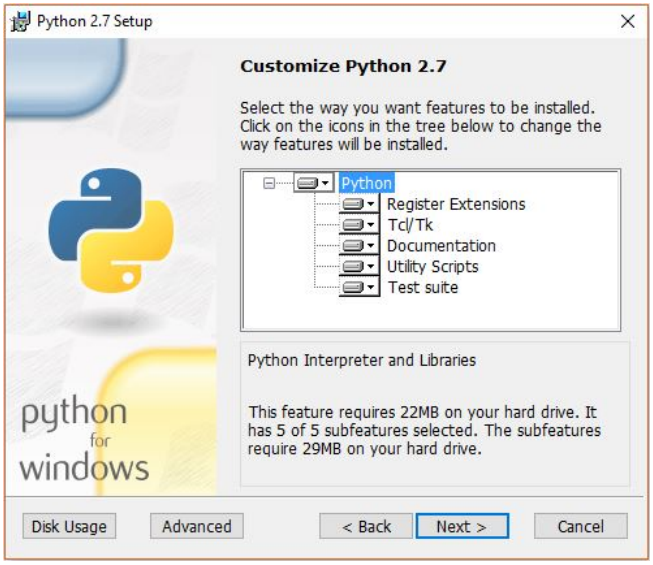


Figure 42. AFE5832 GUI Install (Customize Python®)

12. The window shown in Figure 43 appears showing that the installation is in progress.

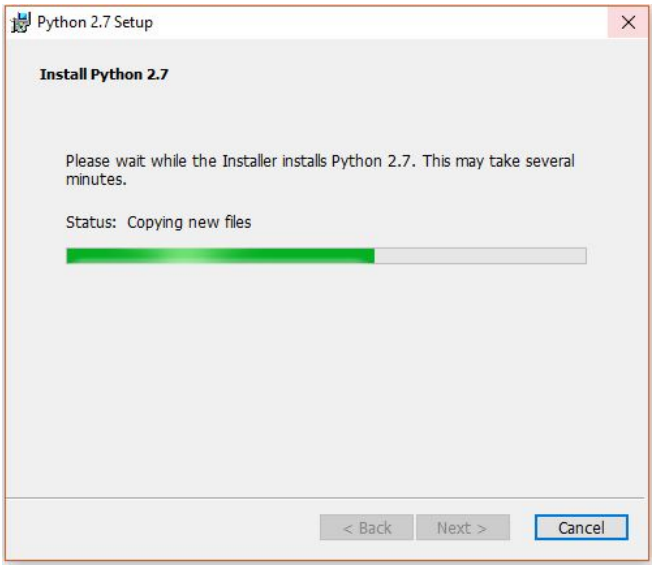


Figure 43. AFE5832 GUI Install (Python® Installation Progress)

13. Press the *Finish* button, as in Figure 44.

Figure 44. AFE5832 GUI Install: (Python® Finished)

14. Press the *Finish* button, as in Figure 45.

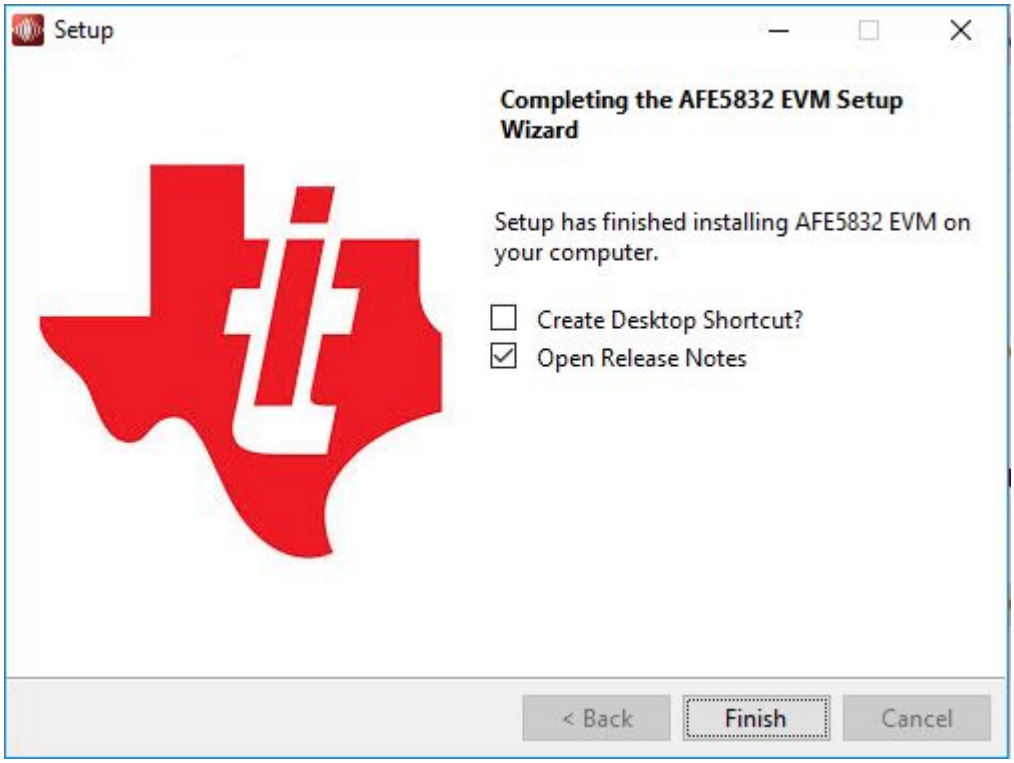


Figure 45. AFE5832 GUI Install (Finished)

The AFE5832 GUI is launched automatically from HSDC Pro, once a device has been selected. Therefore, there is no need to launch AFE5832 GUI manually and there is no need for a desktop shortcut.

Overview of the AFE5832 EVM GUI Features

This section provides a quick overview of the features and functions of the AFE5832 EVM GUI. The GUI allows the user to easily configure the various functions of the AFE such as receiver gain, bandwidth settings, and timing or clocking control settings.

Operations in the GUI should only be performed after the status at the bottom left-hand corner of the GUI reads **Idle**.

Furthermore, hovering over a control within any of the GUI subtabs provides a description of what the specific control does and shows what register fields would be updated using this control. For example, in Figure 46, hovering over 'LNA_HPF_PROG' or its corresponding drop-down menu brings up a light yellow box describing what this control is responsible for and what register it corresponds to.

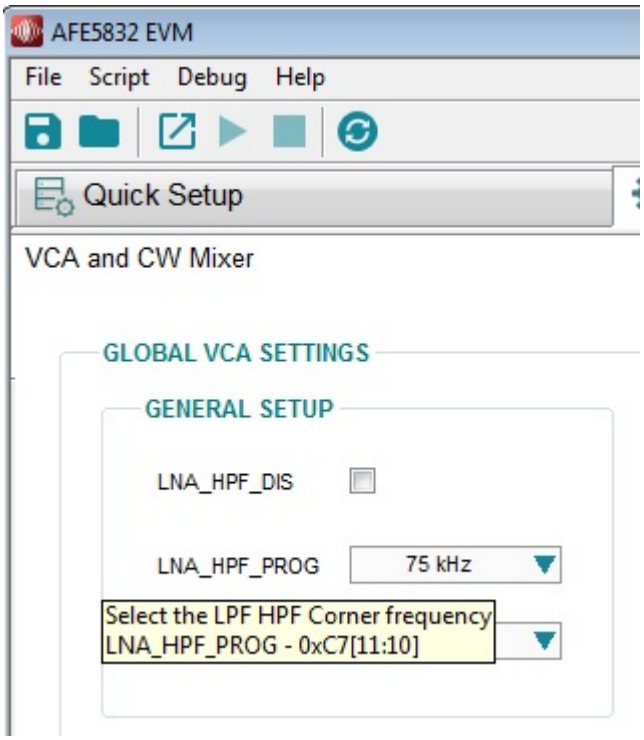


Figure 46. AFE5832: Hovering Over Controls

The 5 main tabs and their subtabs are as follows:

- **Quick Setup**
  - HSDC Pro Related Parameters
    - fsamp
    - ADC Input Target Frequency
  - DUT Reset and Initialize Device
  - Data Format
    - Output Format

        - ADC Format
    - Analog Configuration
        - VCA Gain
        - DTGC Modes
- **VCA**
    - VCA and CW Mixer
        - General Setup
        - VCA PDN Setup
        - TR DIS Setup
        - PD Channel
        - CW Mixer Setup
    - DTGC
        - DTGC Modes
        - Test Modes
        - Profile Parameters
        - Attenuator Setup
- **ADC**
    - Top Level
        - General Setup
        - PDN Setup
        - PLL Setup
    - Test Pattern
        - Global Test Pattern Setup
        - PAT_LVDS
        - PAT_PRBS_LVDS
    - Digital Signal Processing
        - Digital_Offset
        - Digital_Gain
        - Invert_LVDS
        - Misc DSP Setup
        - DIG_HPF
- **Register Map Configuration**

B.1 Quick Setup Tab

The *Quick Setup* tab has the following features:

1. *DUT Reset* and *Initialize Device* buttons
2. Data Format 'check-box' menus to select the appropriate *OUTPUT* and *ADC* formats for running various tests
3. Choice of *Analog Configuration* for how VCA gain and DTGC modes need to be configured
4. Information boxes on the right-hand side that display the *HSDC Pro related Parameters* and *Device Status*

Figure 47 illustrates the *AFE5832 Quick Setup* tab.

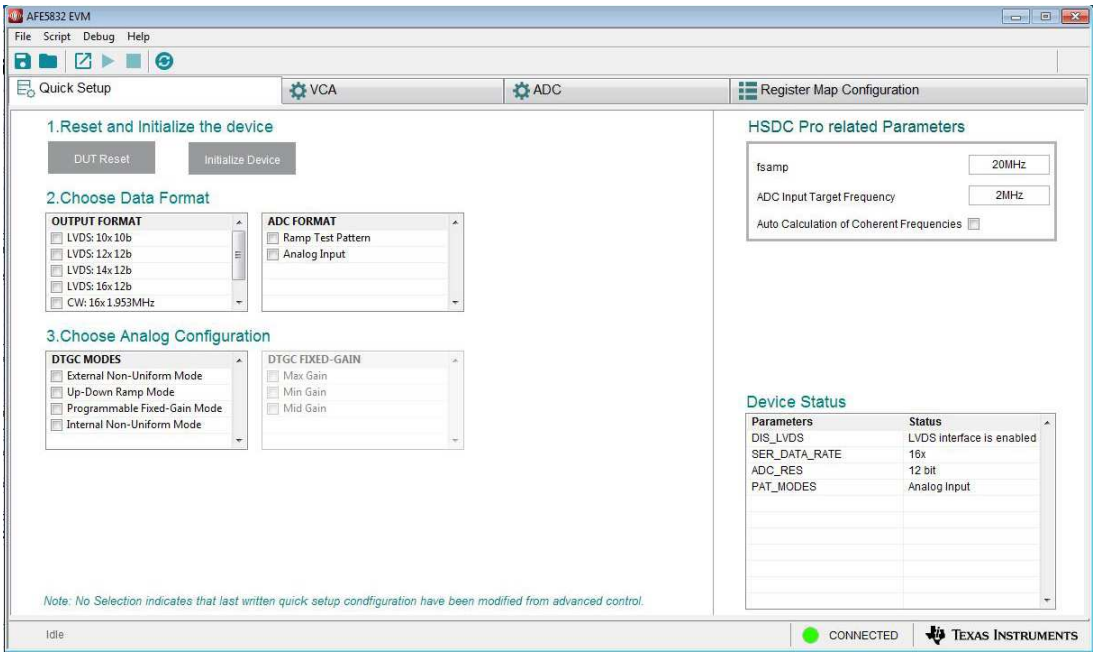


Figure 47. AFE5832: Quick Setup Tab

B.1.1 HSDC Pro Related Parameters

The *Quick Setup* tab includes advanced features under the *HSDC Pro related Parameters* section on the right side of the GUI. The feature explanations follow and are shown in Figure 48.

- *fsamp*: Displays the sampling frequency
- *ADC Input Target Frequency*: This frequency should closely match the input signal that is being supplied

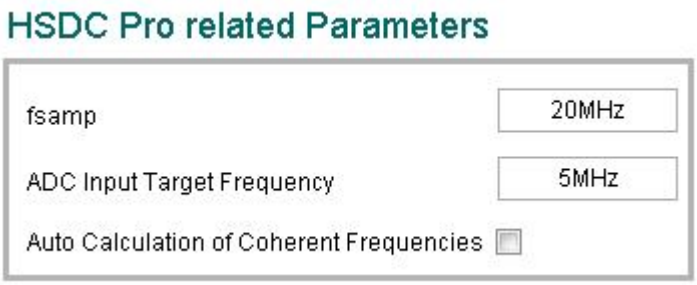


Figure 48. AFE5832: Quick Setup: HSDC Pro Related Parameters

B.2 VCA Tab

The *VCA* tab contains two subtabs: *Global VCA Settings* and *CW Mixer*.

B.2.1 VCA and CW Mixer Subtab

The *VCA and CW Mixer* subtab for the AFE5832 has the following features:

1. Settings for configuring LNA high-pass filter and setting corner and cut-off frequencies
2. Enable or disable LNA HPF at certain channel inputs
3. Fully or partially powering down entire blocks or individual channels in the VCA block
4. Configuring the device in CW mode
5. Controls for setting the corresponding CW mixer channel phases

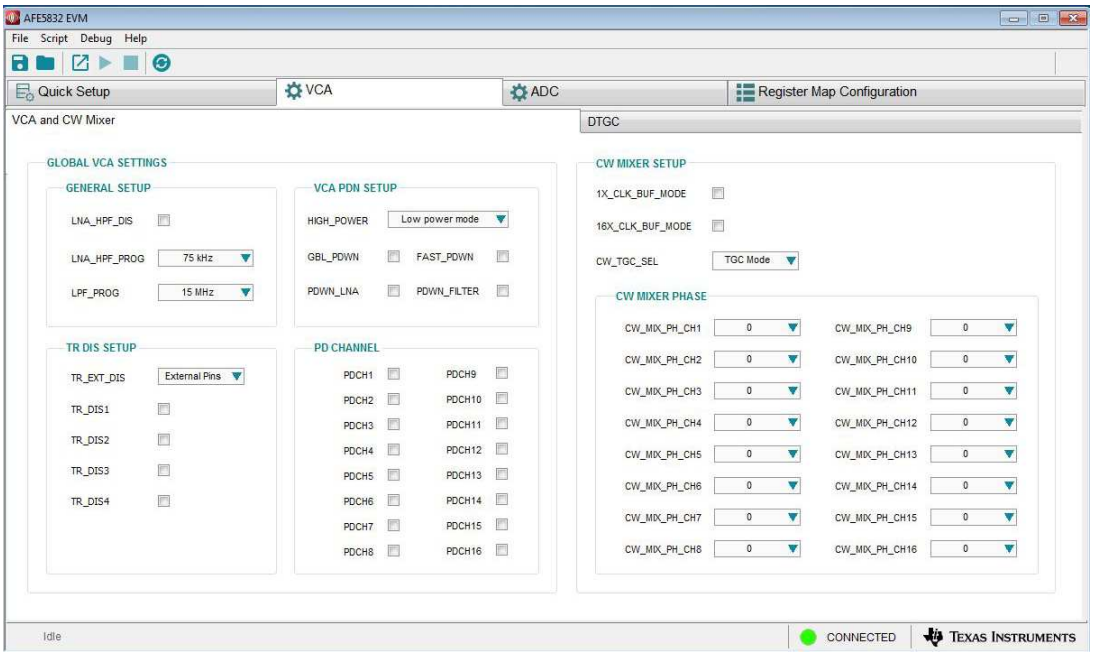


Figure 49. AFE5832: VCA: VCA and CW Mixer

B.2.2 DTGC Subtab

The *DTGC* subtab for the AFE5832 has the following features:

1. Options for selecting different DTGC modes and setting parameters within these modes
2. Enable interrupts and provide pulses on the TGC pin
3. Configure specific parameters for different profiles by setting gains, start and stop indices, and attenuation factors
4. Enable and disable the attenuator

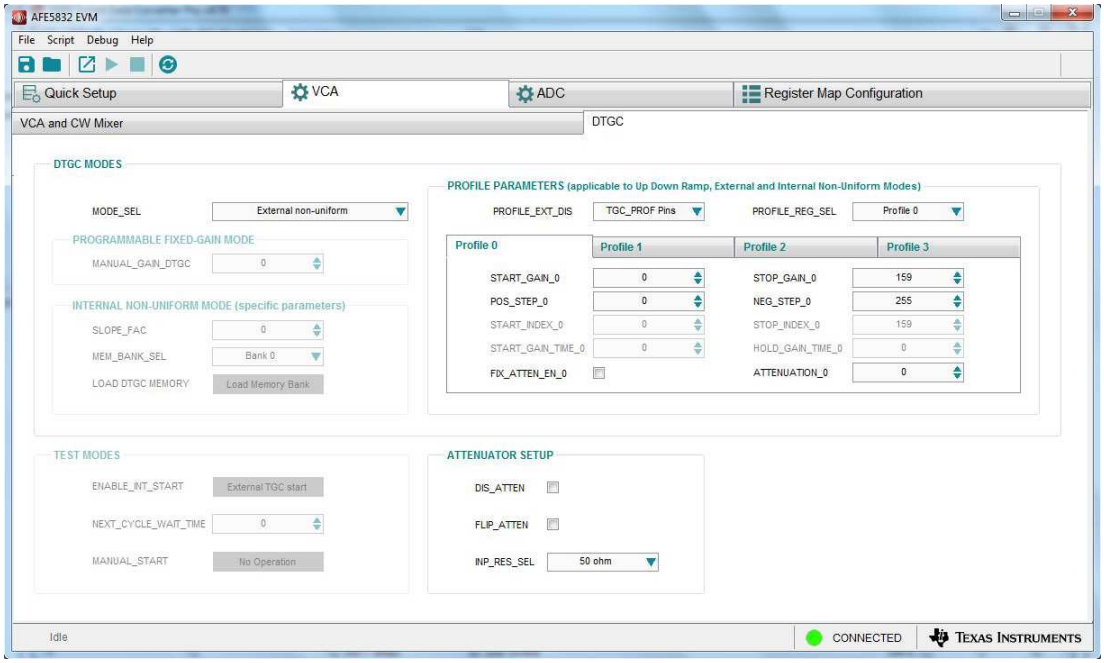


Figure 50. AFE5832: VCA: DTGC

B.3 ADC Tab

The *ADC* tab contains three subtabs: *Top Level*, *Test Pattern*, and *Digital Signal Processing*.

B.3.1 Top Level Subtab

The *Top Level* subtab for the AFE5832 has the following features:

1. Enabling and disabling the LVDS interface and selecting data rates, delays, and resolutions
2. Powering down individual LVDS output lines
3. Software and PLL resets

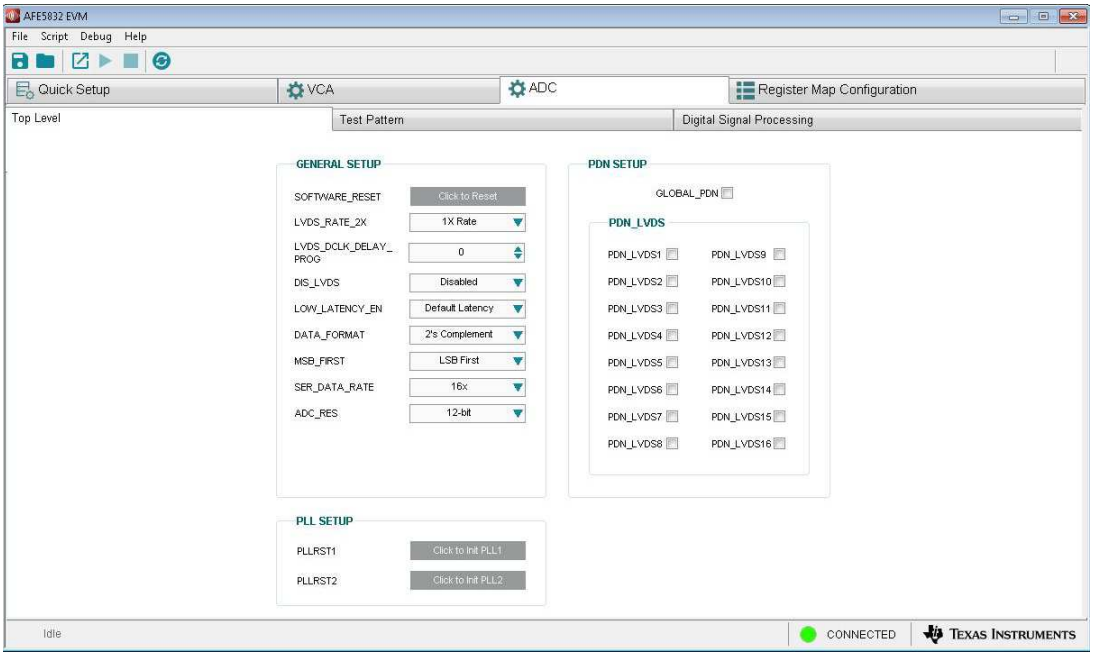


Figure 51. AFE5832: ADC: Top Level

B.3.2 Test Pattern Subtab

The *Test Pattern* subtab for the AFE5832 has the following feature:

- Selecting preset or custom test patterns to be generated by ADC for LVDS or on certain clock lines

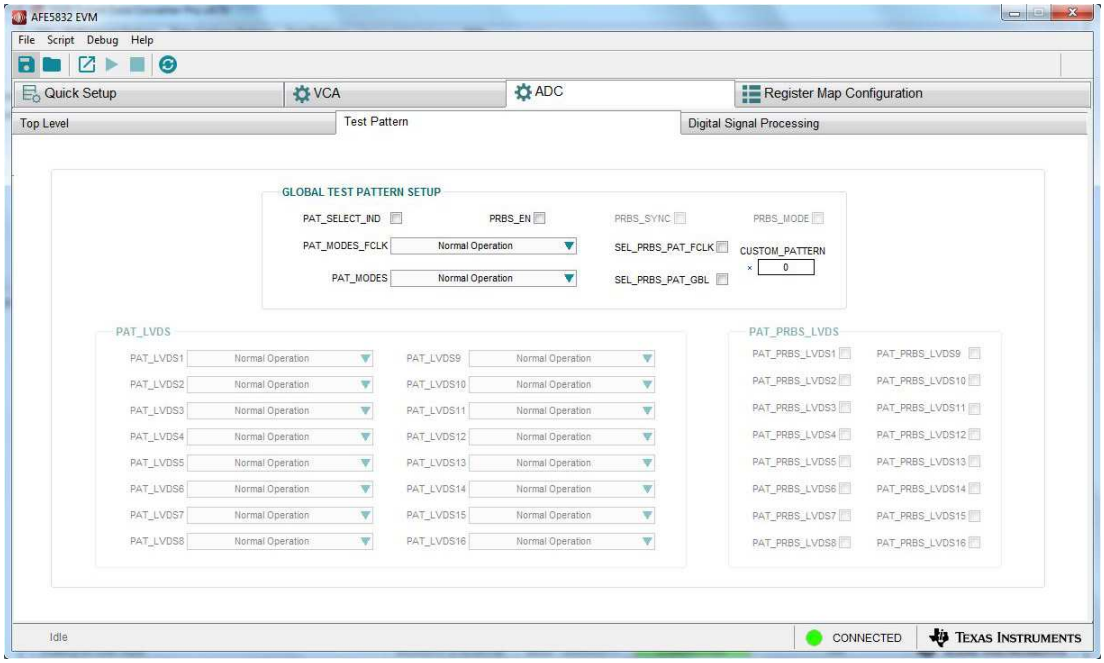


Figure 52. AFE5832: ADC: Test Pattern

B.3.3 Digital Signal Processing Subtab

The *Digital Signal Processing* subtab for the AFE5832 has the following features:

1. Setting the digital gain and digital offset or automatically calculating a channel offset for each of the 16 ADC channels, individually
2. Inverting the digital outputs on various LVDS output lines
3. Enabling or disabling the digital high pass filter for groups of channels

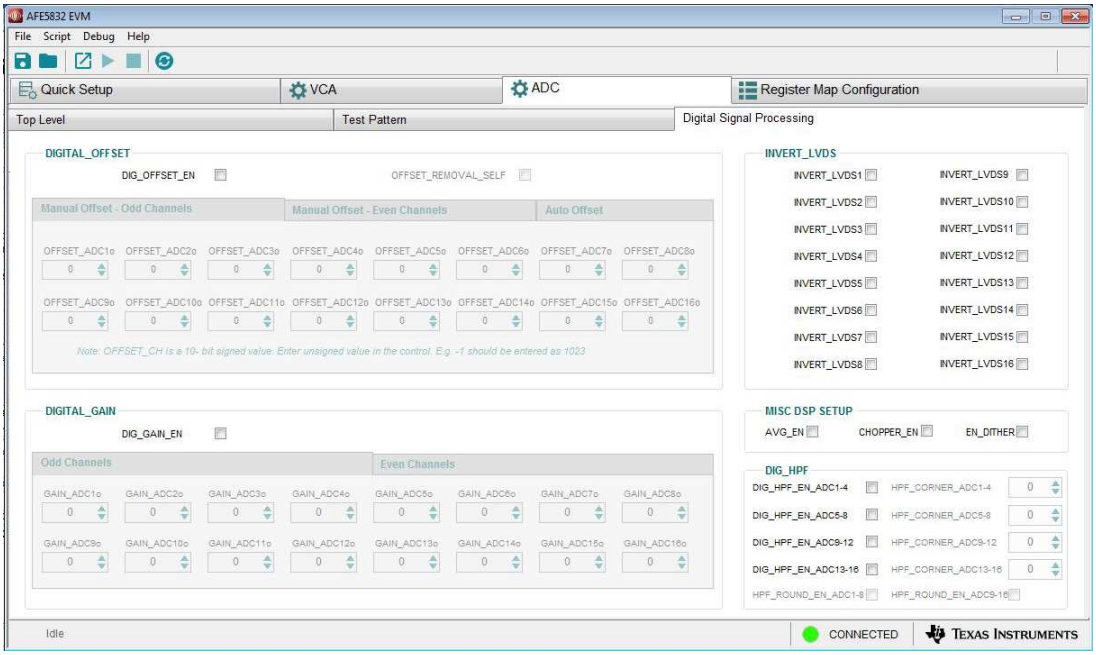


Figure 53. AFE5832: ADC: Digital Signal Processing

B.4 Register Map Configuration Tab

The *Register Map Configuration* tab is a tool to write to and read from specific registers using SPI. The tab contains multiple useful subsections and features that allow the user to interact with the register map, select update modes, and manipulate register values.

B.4.1 Tab Subsections

The following key words are useful in navigating the map:

- *Register Map*: Displays all the details for each of the registers in the device as well as the fields and bits contained within that register
- *Field View*: Displays all the *Field Names* and *Field Values* corresponding to those names
- *Register Description*: Describes each of the fields within the registers and what writing a certain sequence of '0s' and '1s' indicates in that particular field
- *Update Mode*: Allows the user to choose an *Immediate* or *Deferred* method of updating the content of the registers
- *Export HSDC Parameters*: Updates HSDC Pro GUI with the register-level changes made to the AFE5832EVM.

B.4.2 Register Map Interaction

Clicking on a register name produces a list of the fields within that specific register. Clicking on a field name highlights the bits within the register that correspond to that field. In Figure 54, *Register 3* has been clicked. All the fields within Register 3 come up on the right-hand side of the GUI. Clicking on any one of these field names highlights the corresponding bits for this field in the *Register Map*.

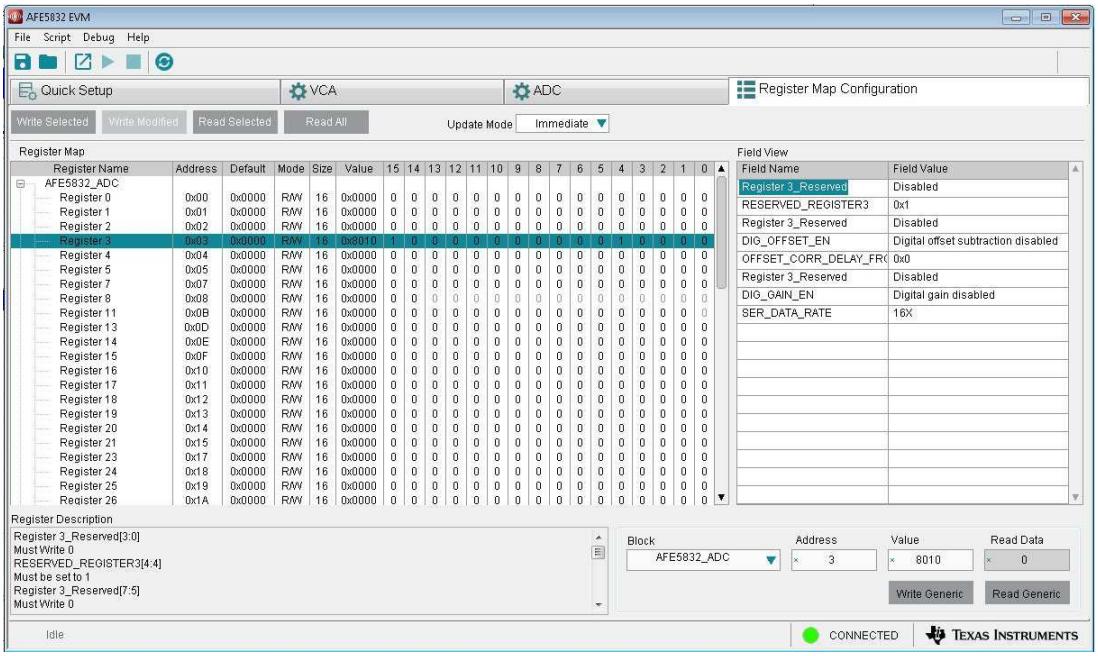


Figure 54. Clicking on Register and Field Names

B.4.3 Update Modes

There are two options to change the *Update Mode* on the GUI as shown in Figure 57: (a) Immediate and (b) Deferred.

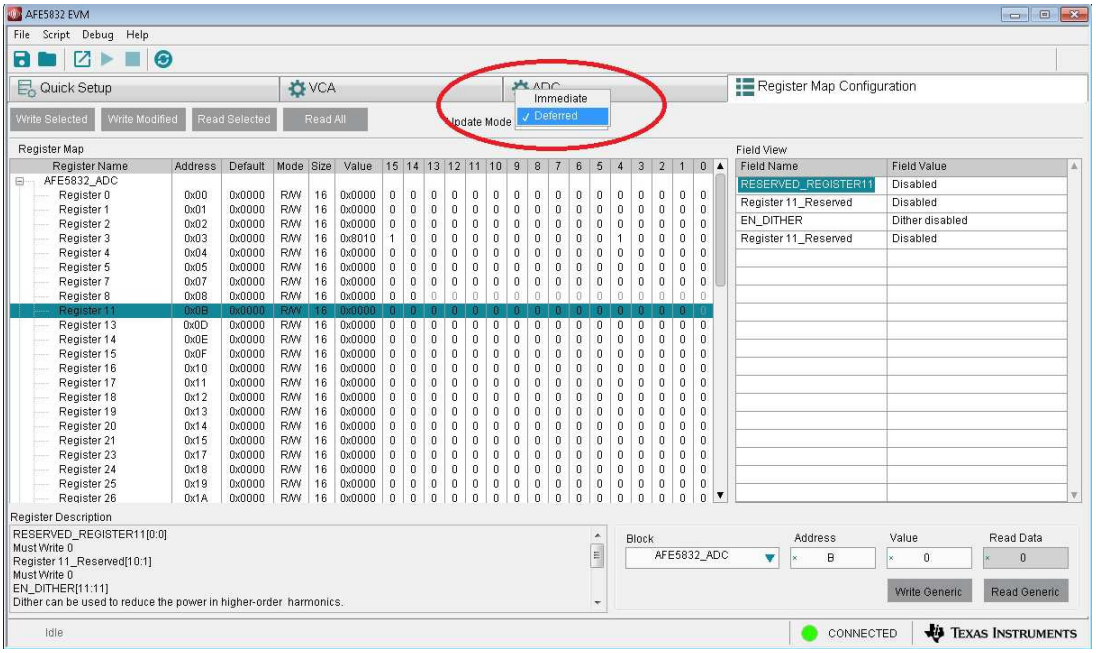


Figure 55. AFE5832: Register Map Configuration: Update Modes

1. The *Immediate* update mode allows the user to change the values of any number of bits or fields within the registers, and these changes are immediately written to the device. Within this update mode, there exists options to (a) *Read Selected* data, (b) *Read All* data, and (c) *Write Selected*.
    1. *Read Selected*: Clicking this option in the top left-hand corner displays the value contained in the register in the *Read Data* field in the lower right-hand corner of the GUI. In the same area of the GUI, the *Address* field will display the address of the selected register, and the *Value* field will display the value contained in that register as shown in Figure 56.
    2. *Write Selected*: This option indicates that only the values in a **selected** register is written to the device. In order to select a particular register to write to, click on any register under *Register Name* and then choose to write to the selected register.
    3. *Read All*: This option reads data from all the registers in the device regardless of whether they are selected or not.

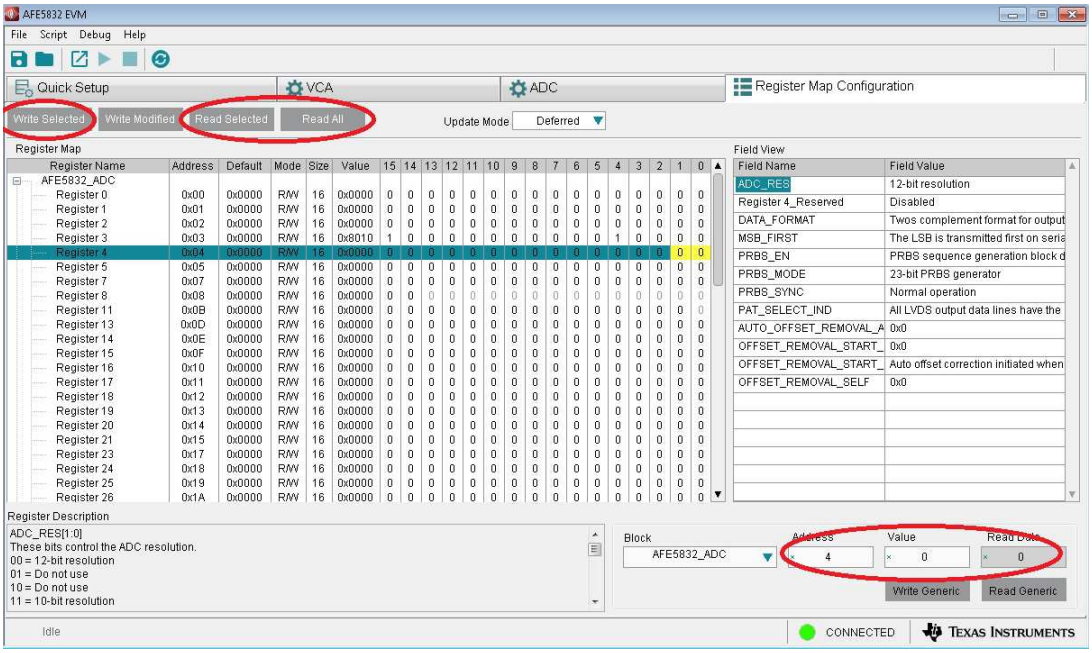


Figure 56. AFE5832: Register Map Configuration: Immediate Update Mode

2. The *Deferred* update mode allows the user to change the values of any number of bits or fields within the registers, but these changes will not be written to the device instantly. Unless the changes are implemented, data cannot be read from the registers either.
   When a user changes the contents of a register in *Deferred* mode, the GUI will turn the changed register font a blue color. These *blue-font registers* indicate that a change has been made but not yet implemented.
   Within the *Deferred* update mode, there exist options in the top left-hand corner of the GUI for deciding how the changes should be implemented (shown in Figure 57): (a) *Read Selected* data, (b) *Write Selected* data, and (c) *Write Modified* data, or (d) *Read All* data.
   1. *Read Selected*: Clicking this option in the top left-hand corner displays the value contained in the register in the *Read Data* field in the lower right-hand corner of the GUI. In the same area of the GUI, the *Address* field will display the address of the selected register, and the *Value* field will display the value contained in that register as shown in Figure 57.
   2. *Write Selected*: This option indicates that only the values in a **selected** register is written to the device. In order to select a particular register to write to, click on any register under *Register Name* and then choose to write to the selected register.
   3. *Write Modified*: If the user has made changes to multiple registers in the register map, this option allows the user to write the changes within **all** modified registers to the device. Once all changes have been written, there will no longer be any *blue-font registers*, indicating that all the changes have been implemented.
   4. *Read All*: This option reads data from all the registers in the device regardless of whether they are selected or not.

NOTE: If any number of registers contains modified values that are not yet written, none of the *Read* options can be used. The user is prompted to either write the modified fields to the device or discard the changes.

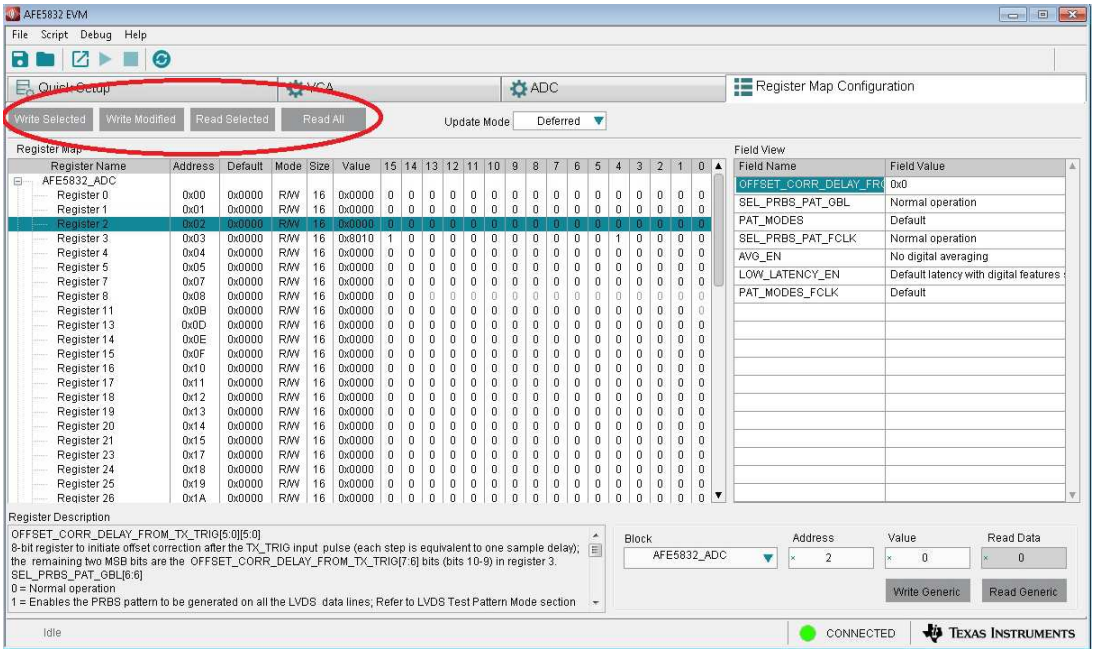


Figure 57. AFE5832: Register Map Configuration: Deferred Update Mode

B.4.4 Manipulating Register Values

Writing to a register or changing the existing value in a register can be accomplished via (1) GUI controls, or (2) manual data entry:

1. *GUI Controls*: Hovering over the corresponding *Field Value* to a *Field Name* generates a drop-down menu from which a series of options can be picked to populate that field as Figure 58 shows. The change shows up in the register map. The value for a specific bit can also be changed by clicking on the bit in the register map.

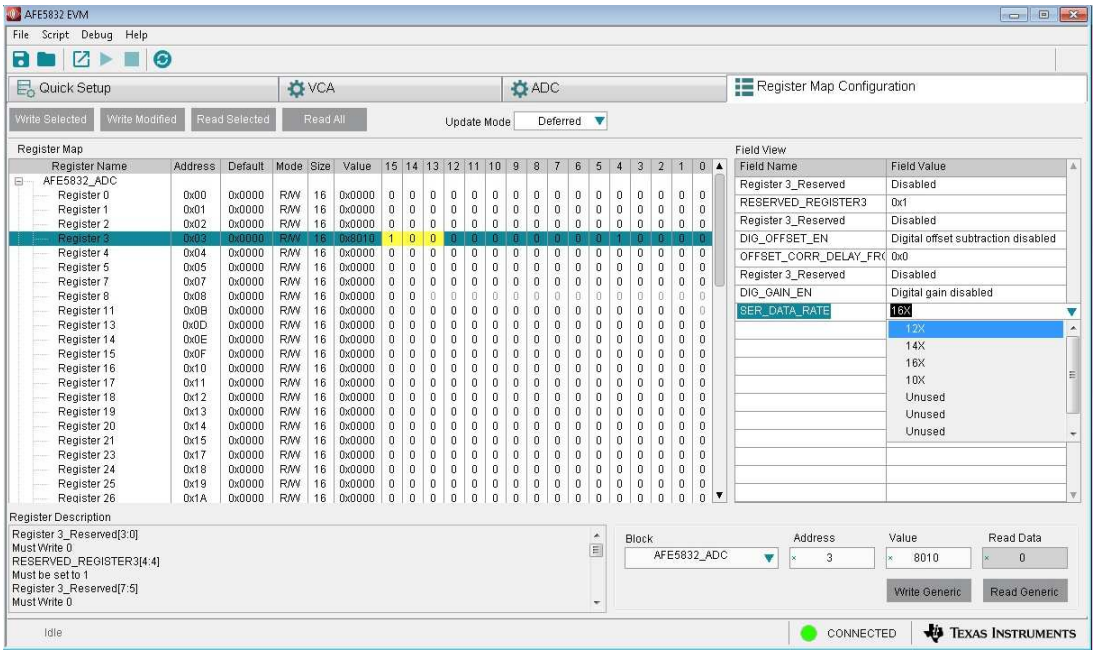


Figure 58. AFE5832: Register Map Configuration: Changing Register Value

2. *Manual Data Entry*: The value for a register can also be changed by manually typing in a hexadecimal value under the *Value* field in the bottom right-hand corner of the GUI. After typing in a value, clicking *Write Generic* will write this change to the device. The change will show up in the register map. Clicking *Read Generic* will read the data from that register and the hexadecimal value will show up in the *Read Data* field.

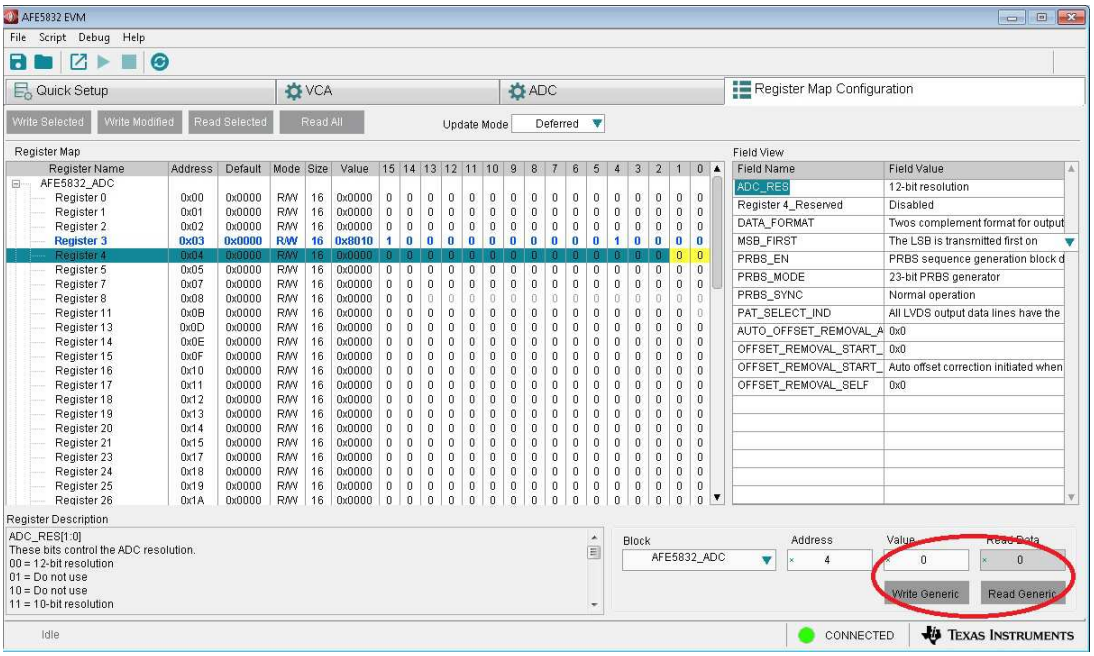


Figure 59. AFE5832: Register Map Configuration: Manual Data Entry

Hardware Configuration

C.1 EVM Headers, Test Points, and Configuration

This section describes the functions of the headers on the EVM. It also provides a list of test points on the EVM that are useful for debug and general-use purposes.

C.1.1 EVM Header Configuration

The AFE5832 EVM is flexible in its configurability through the use of 2- and 3-pin headers. The default configuration of the EVM is set to facilitate initial testing, requiring minimal bench equipment. Figure 60 shows the default positions of all headers.

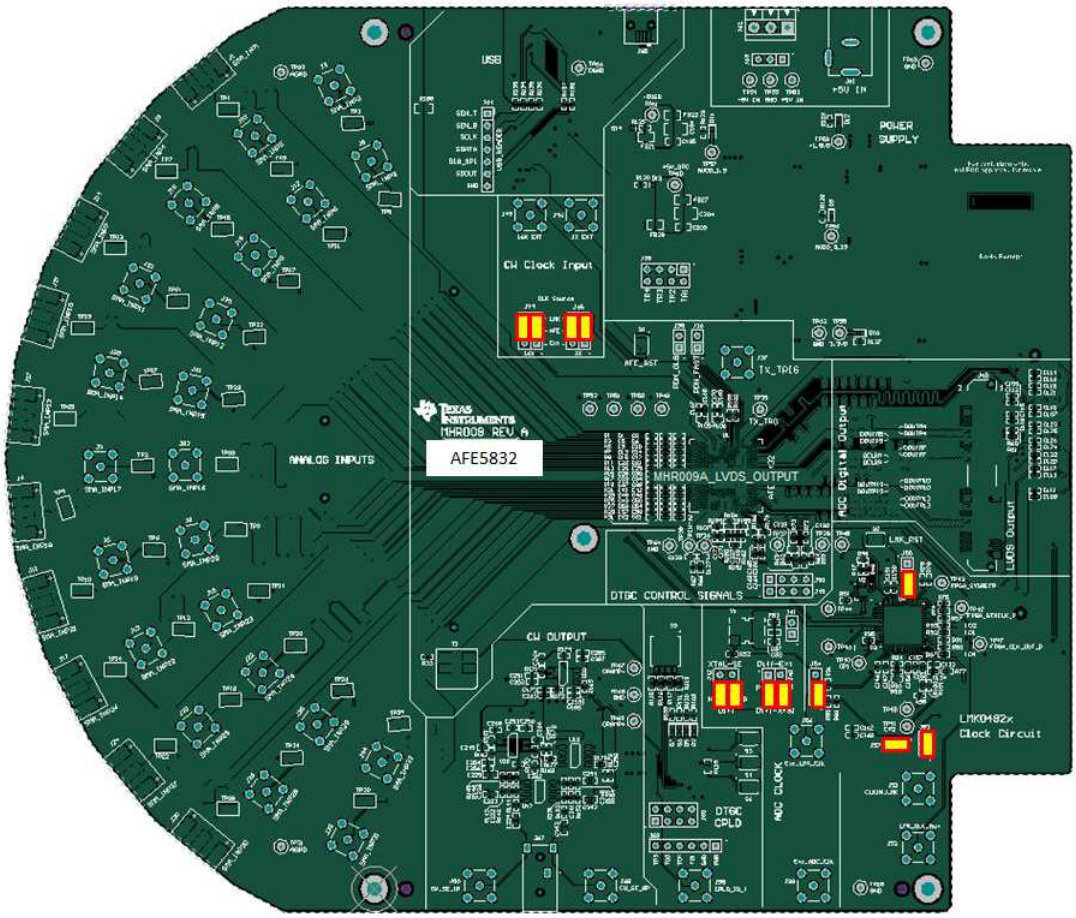


Figure 60. Default Jumper Positions

Table 1 lists the default header configurations and descriptions.

Table 1. Default Header Configuration Table Rev. A

Jumper	Circuit	Description	Pin Numbers	Selection
J63	Power Supply	±5V Input Power Connector	–	–
J64	USB/SPI	SPI Signals Probe Point	–	–
J35	PDN	PDN_Global	–	–
J36	PDN	PDN_Fast	–	–
J41	ADC Clock	OSC1 Xtal Power supply +3.3VD	–	3.3V
J42	ADC Clock	Clk source selector for SE Xtal or Diff	2-4,1-3	Differential
J40	ADC Clock	Diff CLK Source selector, Ext Xfmr or LMK	3-5, 4-6	LMK CLK
J44	CW CLK	16x CLK Source Selector	3-5, 4-6	Ext
J45	CW CLK	1x CLK Source Selector	3-5, 4-6	Ext
J50	DTGC	DTGC Digital Input Signals	–	–
J49	DTGC	GND for Dig Input Signals	–	–
J60	DTGC	CPLD JTAG Programming Header	–	–
J58	DTGC	CPLD GPIO	–	–
J55	LMK	LMK Chip Reset	1-2	–
J53	LMK	LMK Supply for 125M Xtal	1-2	–
J57	LMK	Power Supply for 40 MHz VCO	1-2	3.3V
J54	LMK	Input Clk selector for Clkin1	1-2	125 MHz Xtal
J38	LNA TR Enable	TR_EN 1-4	–	–

C.1.2 EVM Testpoints

Table 2 lists all test points on the AFE5832 EVM and their purposes.

Table 2. EVM Rev. A Testpoints

Testpoint	Circuit	Label	Testpoint Description
TP62-65, 69	GND	GND	Digital Ground Reference for EVM
TP31, 32	GND	AGND	Input Signal Ground Reference for EVM
TP66	GND	DGND	USB Ground Reference for EVM
T53	Power Supply	+5V_IN	+5V_IN
T54	Power Supply	–5V_IN	–5-V supply for Op-Amp circuitry
T59	Power Supply	+1.8 VD	AFE 1.8-V supply
TP67	Power Supply	OPAMP-	–5-V Supply for Op Amp circuitry
TP58	Power Supply	3.3 VD	+3.3 VA
TP56	Power Supply	AVDD_3.15	AFE analog supply for 3.15 V
TP68	Power Supply	ODAMP+	+5-V Supply for Op Amp circuitry
TP57	Power Supply	AVDD_1.9	AFE analog supply for 1.9-V
TP60	Power Supply	+5V_SRC	+5-V source for entire EVM
TP61	Power Supply	–5VSS	–5V Supply for CW Op Amp circuitry
TP1-30, 33, 34	Analog Inputs	SMA_INPx	Analog Input Channel 1-32
TP35	External Trigger	TX_TRG	TX_Trig input
TP38	DTGC	None	Ext TGC_Profile2 Input
TP36	DTGC	None	Ext TGC_Profile1 Input
TP37	DTGC	TGC_SLP	Ext TGC_Slope
TP39	DTGC	TGC_UD	Ext TGC_Up/Down
TP40,41	LMK Clock Circuit	CP1,CP2	LMK Output CP1,CP2
TP42	LMK Clock Circuit	None	None
TP43	LMK Clock Circuit	None	None
TP44	LMK Clock Circuit	None	LMK ADC Clock to Dut P/N
TP45	LMK Clock Circuit	None	None
TP47	LMK Clock Circuit	FPGA_CLK_OUT_P	LMK ADC CLK to FPGA P

Table 2. EVM Rev. A Testpoints (continued)

Testpoint	Circuit	Label	Testpoint Description
TP48	LMK Clock Circuit	None	LMK VCXO output
TP46	LMK Clock Circuit	None	LMK Clock to CPLD
TP49	IC 0.5-V Source Bias	None	SRC_BIASO
TP50	IC 2.5-V Bias	None	BIAS_2P5E
TP51	IC BandGap Bias	None	BAND_GAPE
TP52	IC LNA Bias	None	LNA_IN_CME

C.1.3 ADC Clock Source Configuration

The AFE clock input can be driven differentially (sine wave, LVPECL, or LVDS) or single-ended (LVCMOS). The clock input of the device has an internal buffer and clock amplifier which is enabled or disabled automatically, depending on the type of clock provided (auto-detect feature). Therefore, the EVM allows for multiple clocking options.

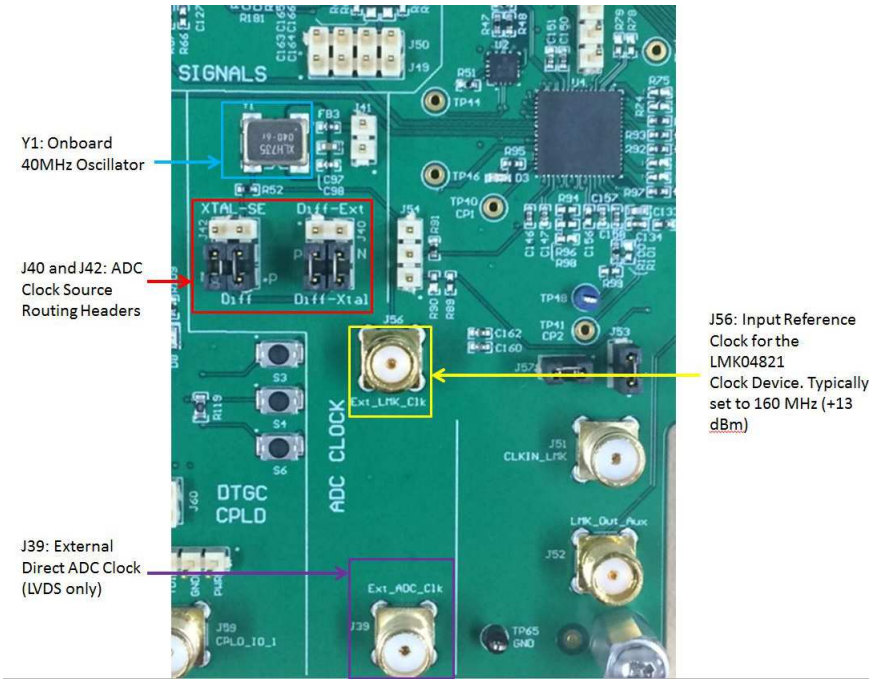


Figure 61. EVM ADC Clock Source Configuration

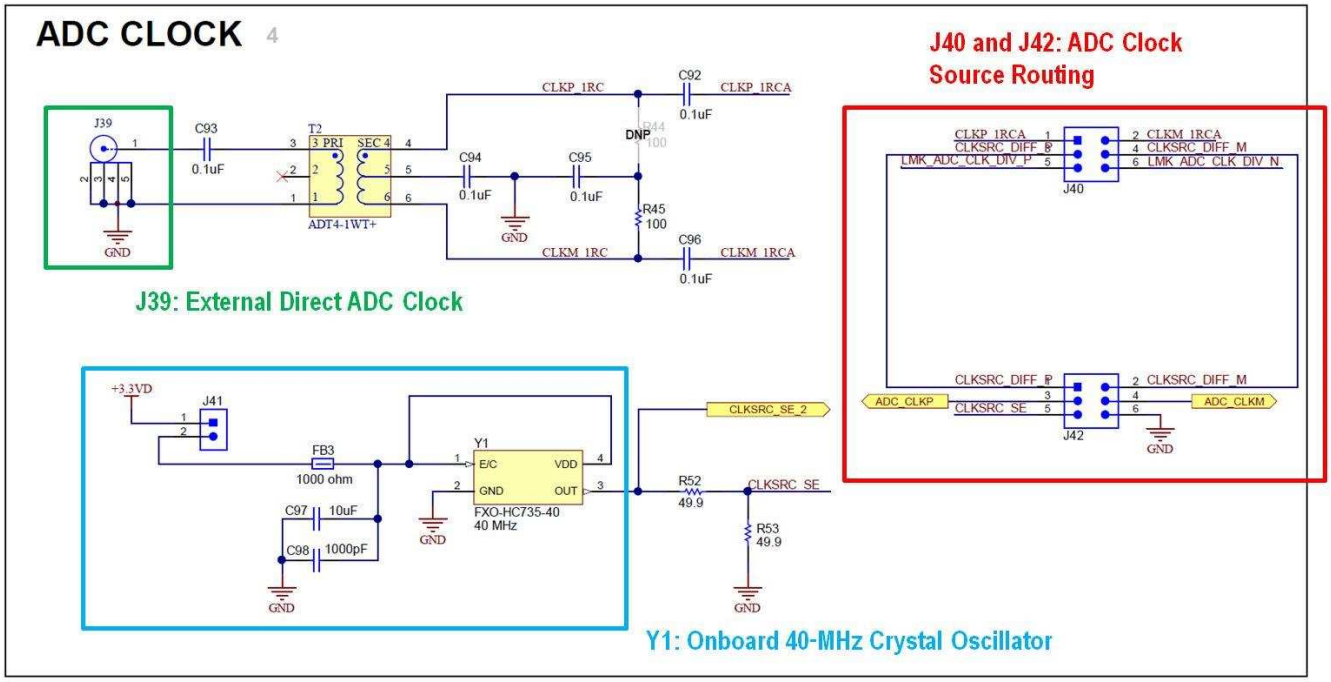


Figure 62. AFE EVM ADC Clock Source Configuration Schematic

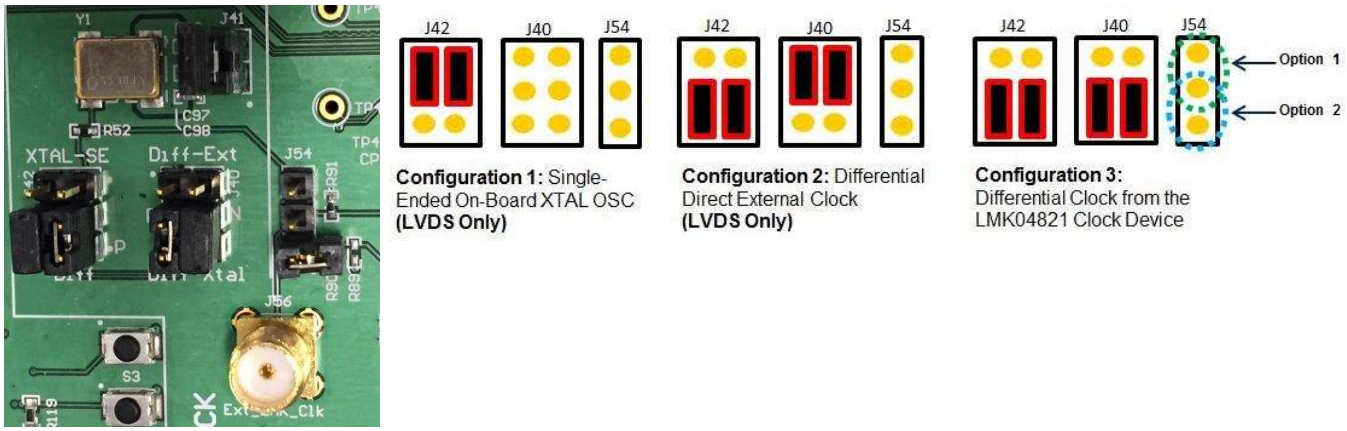


Figure 63. EVM ADC Clock Source Configuration Examples

Configuration 1: To use the onboard single-ended crystal oscillator as the clock source for the AFE, connect shunt jumpers for configuration 1 (as seen in Figure 63). Note: J41 powers the onboard oscillator with 3.3 V, due to the power limitations of the FXO-HC735-40 low-jitter crystal oscillator. The recommended ADC clock input for new designs is to use low-jitter square signals (LVCMOS levels, 1.8-V amplitude).

Configuration 2 (LVDS Only): To use a direct external clock as the clock source for the AFE, connect shunt jumpers for configuration 2 (as seen in Figure 63). Connect a single-ended external clock generator to SMA J39. Set the clock source to an appropriate frequency, such as 10 MHz to 100 MHz, and +13-dBm amplitude.

Configuration 3: To use the differential outputs from the LMK04821 as the clock source for the AFE, connect shunt jumpers for configuration 3 (as seen in Figure 63). The clock signal can be generated either from the 40-MHz onboard crystal (Y1), the 125-MHz onboard crystal (Y2), or an external clock generator. To use the 125-MHz onboard crystal, connect the J54 jumper as indicated by option 2 (Figure 63). To use the 40-MHz onboard crystal, connect the J54 jumper as indicated by option 1 (Figure 63). For an external source, connect an external clock generator to J56, and set the clock source to 160 MHz, and +13-dBm amplitude. For an external source, leave the J54 jumper as in configuration 2.

C.1.4 Complex Programmable Logic Device (CPLD)

The AFE5832 board has a Xilinx™ CPLD, designated by U21 on the schematic. This CPLD is controlled by four switches contained in **S5** on the board. When all of these switches are in the 'off' position, LEDs D5 – D8 should light up on the board as shown in Figure 64.

Figure 64. CPLD Switches and LEDs

The following describes the function of each of the four switches contained in S5:

Switch 1: In the 'off' position, this switch turns on the TGC signals. In the 'on' position, these signals are turned off.

Switch 2: This switch determines whether the CPLD outputs signals for *Up-Down Ramp Mode* or *External Non-Uniform Mode* when running a DTGC test. In the 'off' position, the CPLD outputs for *Up-Down Ramp Mode*, and in the 'on' position, the CPLD outputs for *External Non-Uniform Mode*.

Switch 3: This switch controls the distance between two consecutive TGC_SLOPE pulses for *Up-Down Ramp Mode*.

Switch 4: This switch controls TX_TRIG. The TX_TRIG pulse resets the phase of the test pattern generator, the odd and even sampling phase selection, and the phase of the frame clock. This phase reset can corrupt the ADC data because the clock dividers will no longer be synchronized. In the 'off' position, *Switch 4* turns on the TX_TRIG pulse, and in the 'on' position, the TX_TRIG pulse is turned off.

The switches controlling the CPLD must be manipulated for some of the modes outlined in this user guide. Switch 4 is the most important to pay attention to as it controls whether or not the phase is reset. As a summary, the modes with their corresponding *Switch 4* settings are outlined in the following list:

- LVDS Capture – Switch 4 off and LED D8 on
- DTGC Mode Test – Switch 4 off and LED D8 on
- CW Mode Test – Switch 4 on and LED D8 off

D.1 ADC Synchronization and TX_TRIG

In the analog-front-end, 16 ADCs are being used to convert the 32 inputs. Each ADC converts one odd-numbered input and one even-numbered input. For example, ADC 1 converts inputs 1 and 2; ADC 2 converts inputs 3 and 4, and so forth. As two inputs need to be processed by each ADC, the inputs are alternately converted using two sampling circuits within each ADC.

The device has many PLLs and clock dividers that can synchronize the various test patterns generated. The device has a TX_TRIG input that is used to synchronize the clock dividers inside the device, and this enables multiple parallel devices to be synchronized as well. This TX_TRIG signal provides the means to determine when the odd and even signals should be sampled with respect to the rest of the system and its clock.

Refer to the *ADC Synchronization Using TX_TRIG* and *Input Multiplexer and Sampler* sections in the AFE5832 data sheet (SBAS823) for more information.

D.2 Software Trigger

One method of triggering the TSW EVM, AFE EVM as well as other bench equipment such as function generators is to generate the trigger from the TSW EVM itself. This requires a feedback loop from the TSW trigger output to the TSW trigger input using a short SMA cable. Secondly, a second trigger output from the TSW board can be routed to the AFE EVM, if needed, or to external bench equipment such as a function generator. See the TSW or HSDC Pro manual for more information.

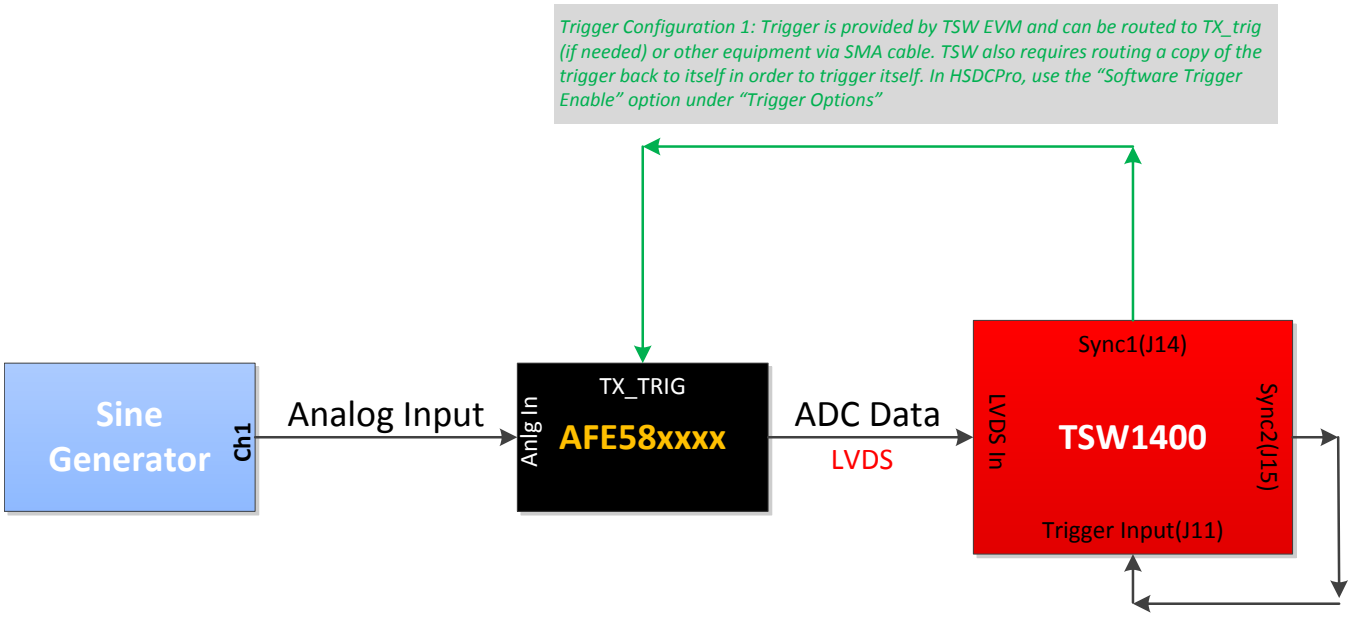


Figure 65. HSDC Pro Trigger Configuration for SW

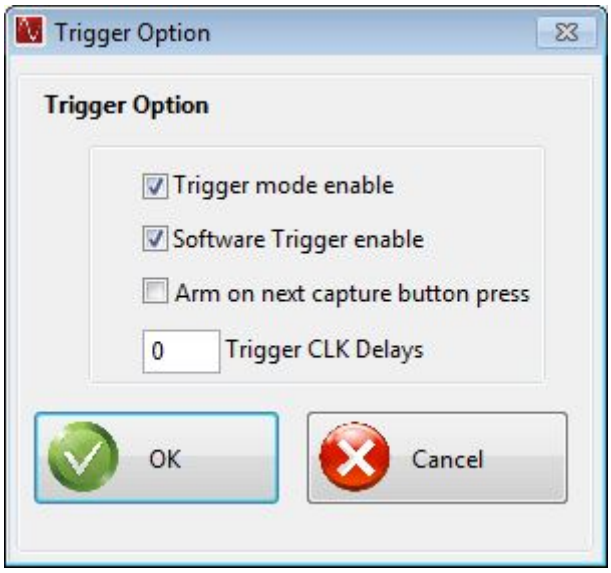


Figure 66. HSDC Pro Trigger Configuration for SW Trigger

D.3 External Trigger

Another method of triggering the TSW EVM and AFE EVM as well as other bench equipment such as function generators is to generate the trigger from a bench trigger source such as the function generator. This requires feeding the trigger source to the TSW trigger input using an SMA cable. Secondly, a second trigger output from the trigger source can be routed to the AFE EVM, if needed. See the TSW or HSDC Pro manual for more information.

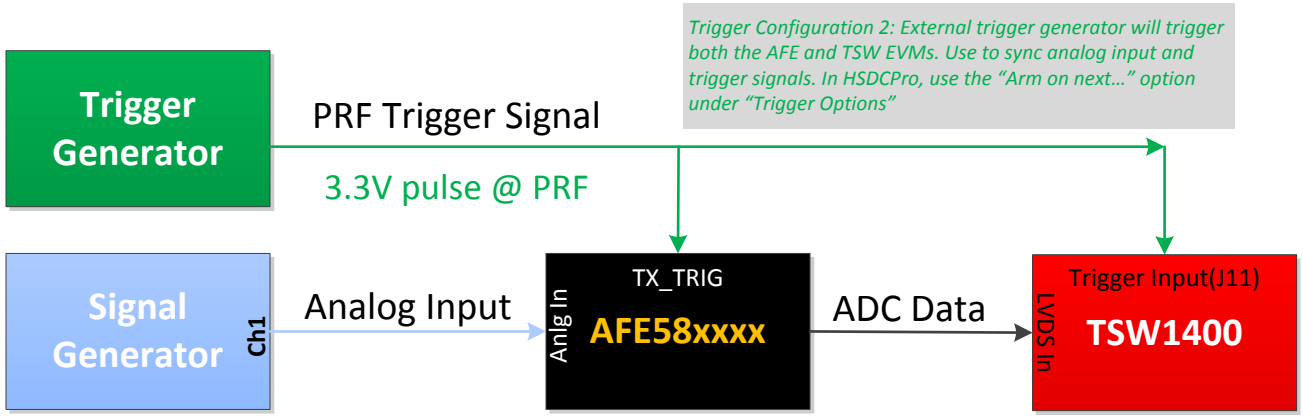


Figure 67. HSDC Pro Trigger Configuration for HW

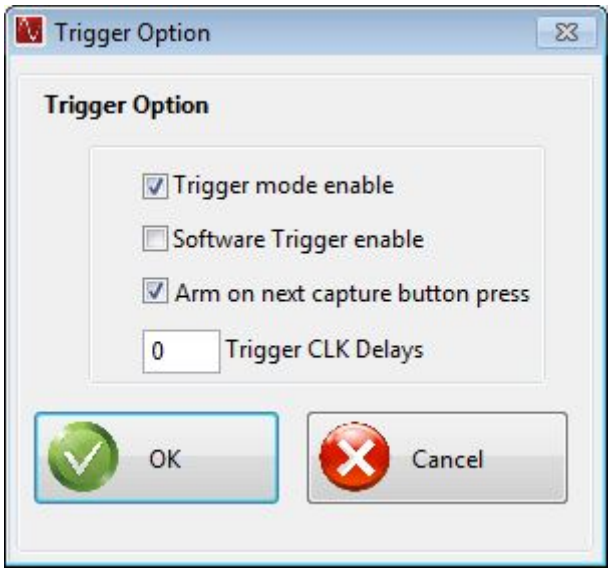


Figure 68. HSDC Pro Trigger Configuration for HW External Trigger

Common Hardware Modifications

E.1 External SPI Programming

The AFE EVM allows for external access to the SPI bus for the AFE only, not the LMK device. This is done by connecting SPI signals at J64 and removing R140 near U14 on the bottom side of the board.

F.1 AFE5832 EVM Hardware Overview

The following images give an overview illustration of the EVM hardware.

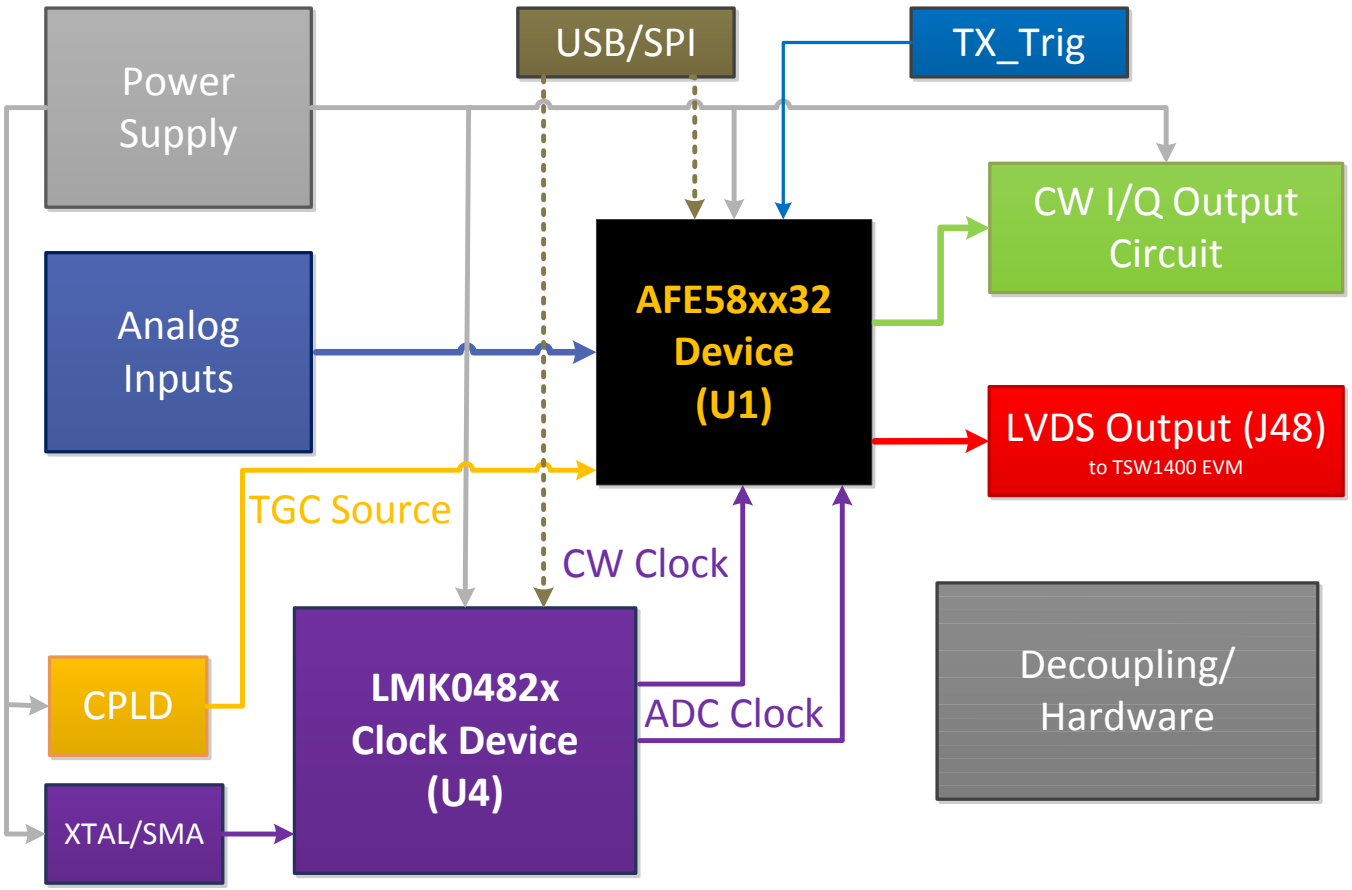


Figure 69. AFE5832 EVM Block Diagram

F.2 AFE5832 EVM Schematic

Figure 70 through Figure 81 illustrate the EVM schematics.

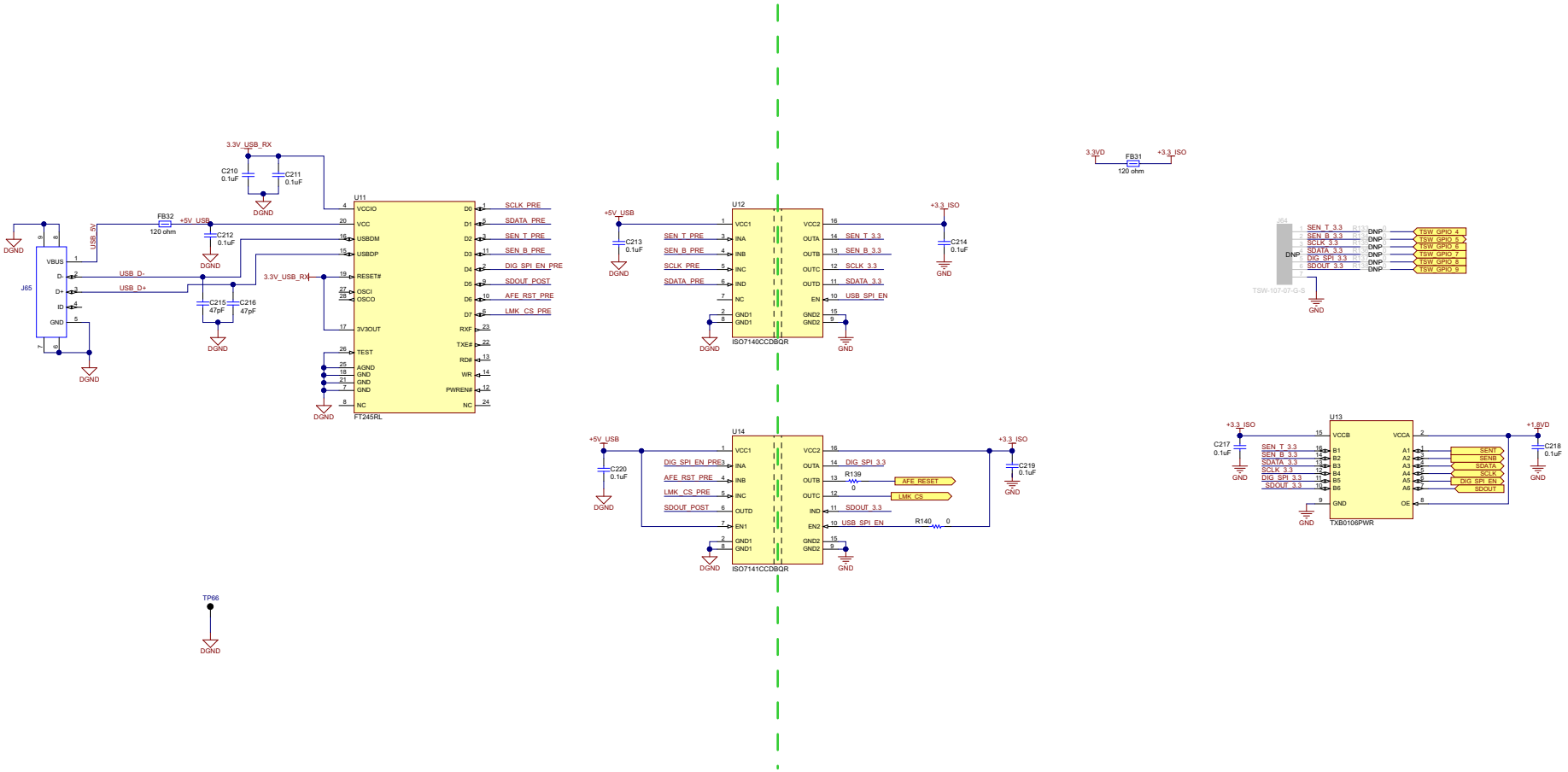


Figure 70. AFE5832 Rev. A EVM Schematic 1 of 12

DTGC CPLD

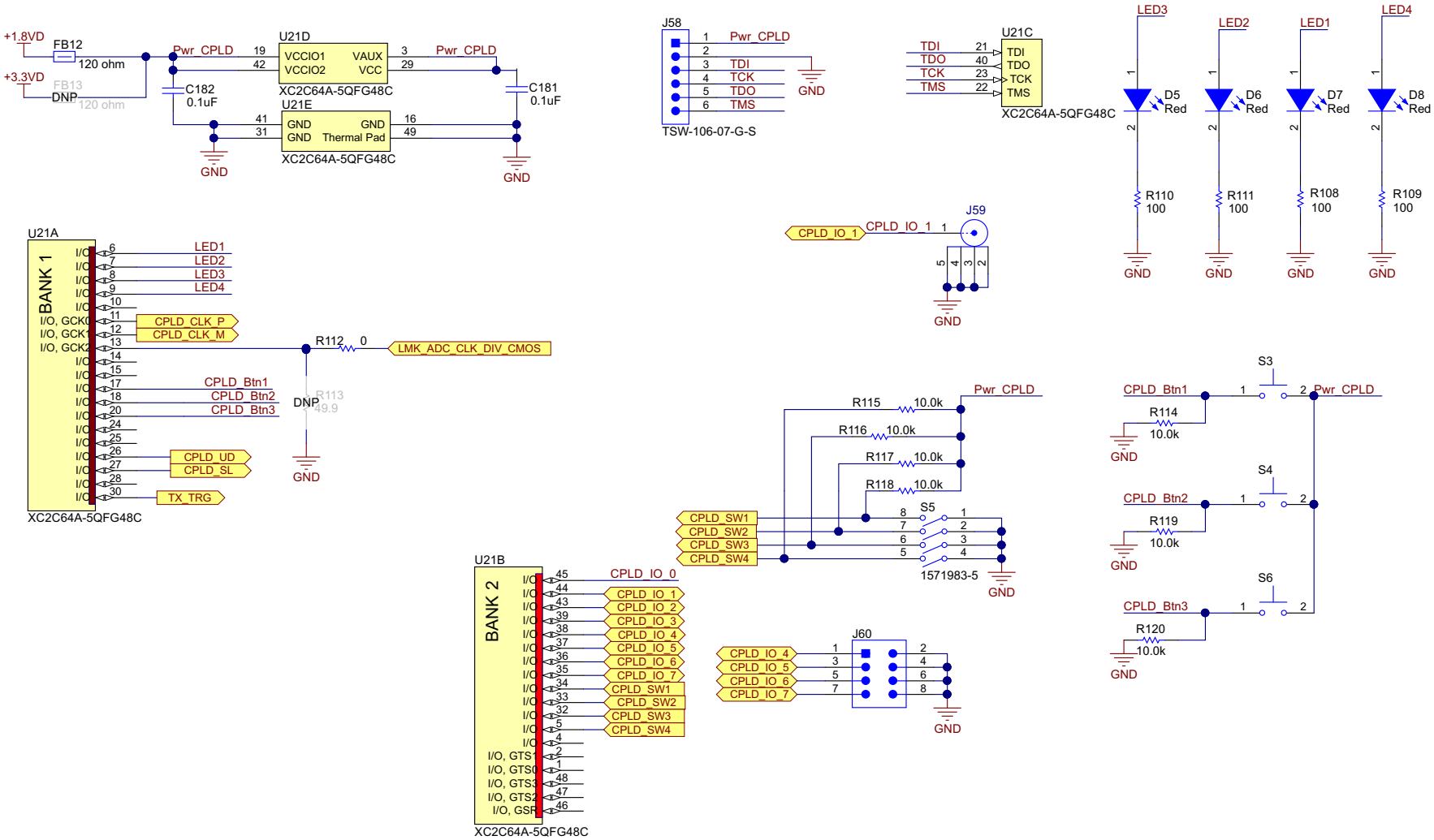


Figure 71. AFE5832 Rev. A EVM Schematic 2 of 12

ADC LVDS OUTPUT 9

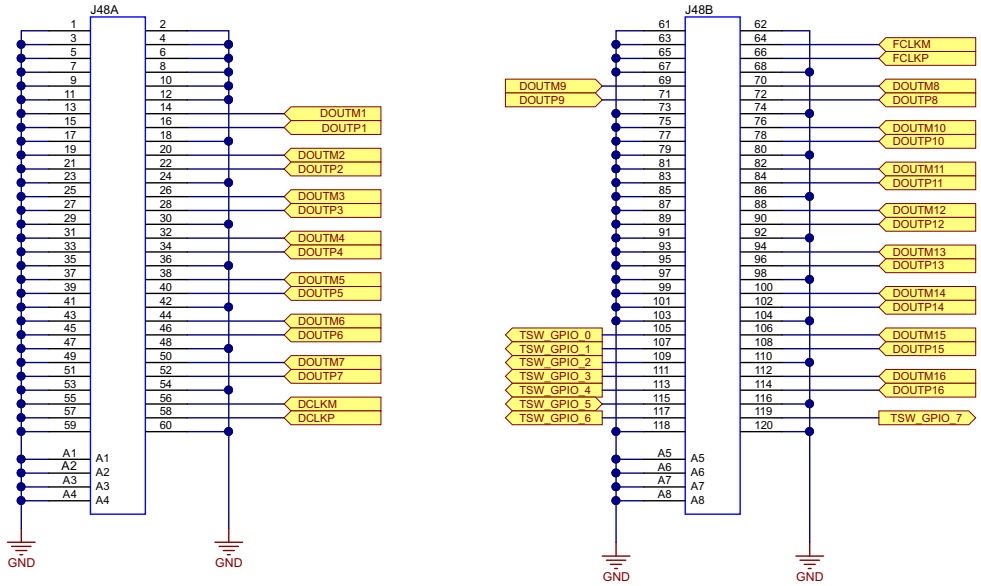


Figure 72. AFE5832 Rev. A EVM Schematic 3 of 12

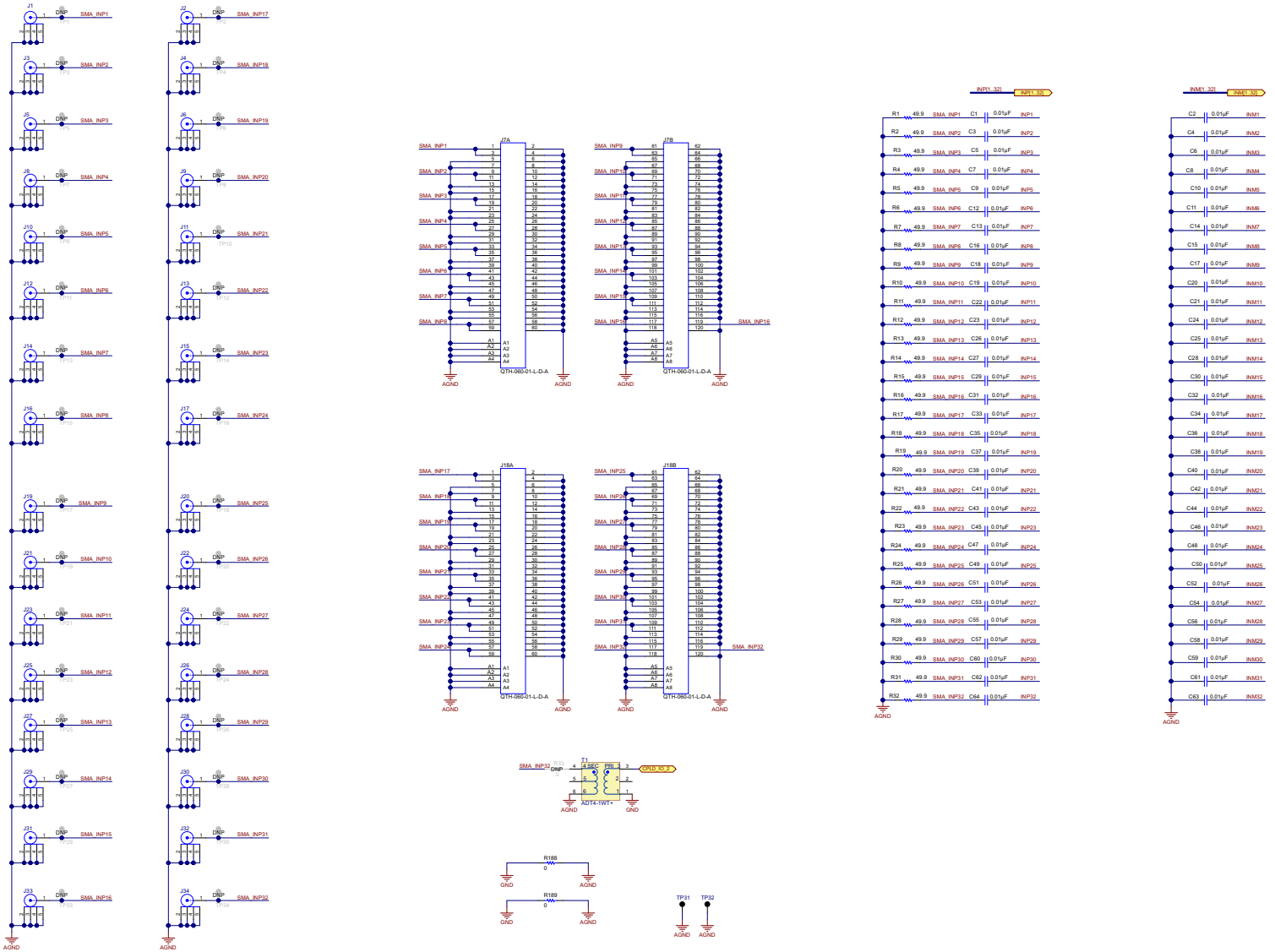


Figure 73. AFE5832 Rev. A EVM Schematic 4 of 12

CW I/V OUTPUT 3

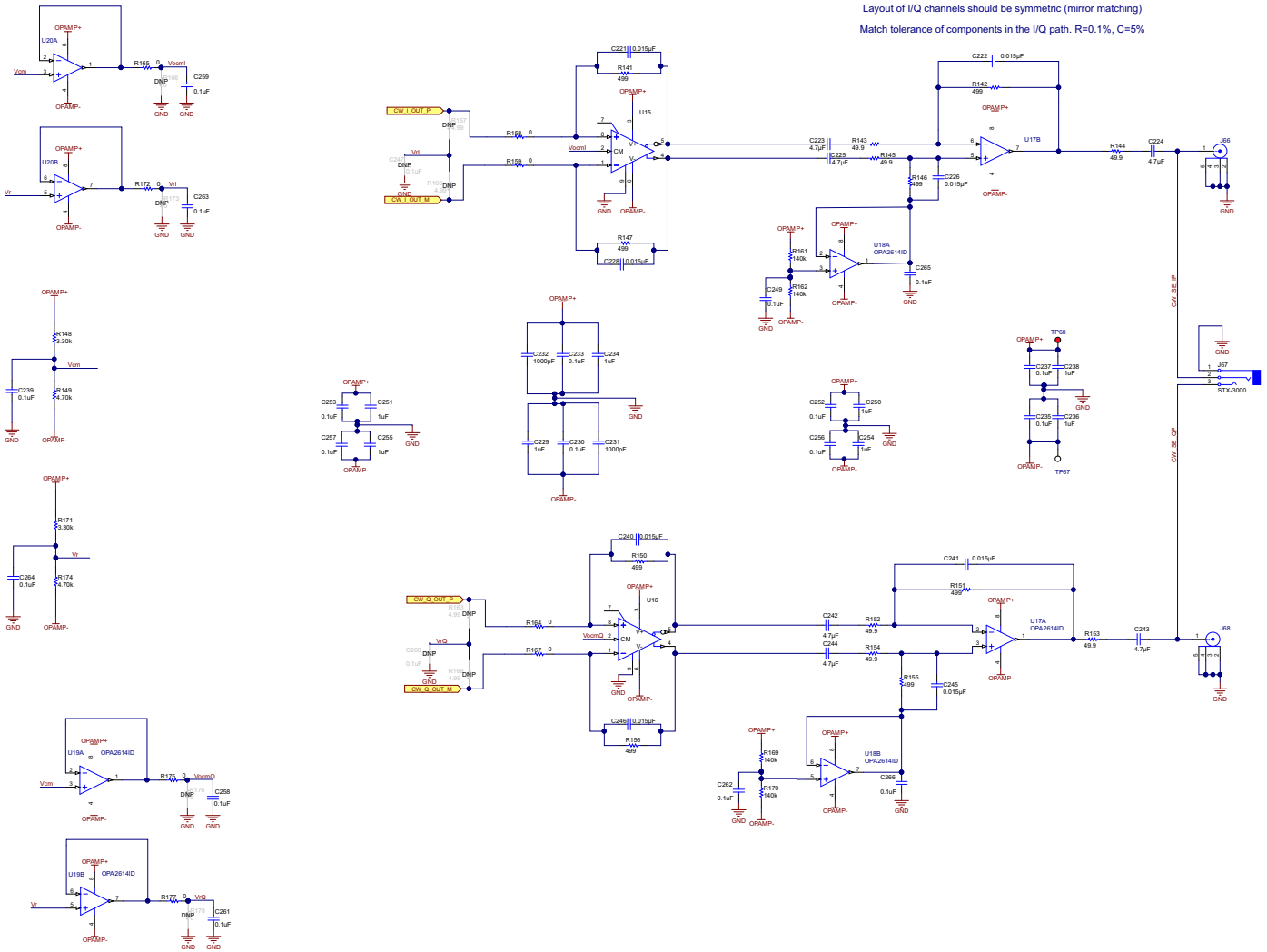


Figure 74. AFE5832 Rev. A EVM Schematic 5 of 12

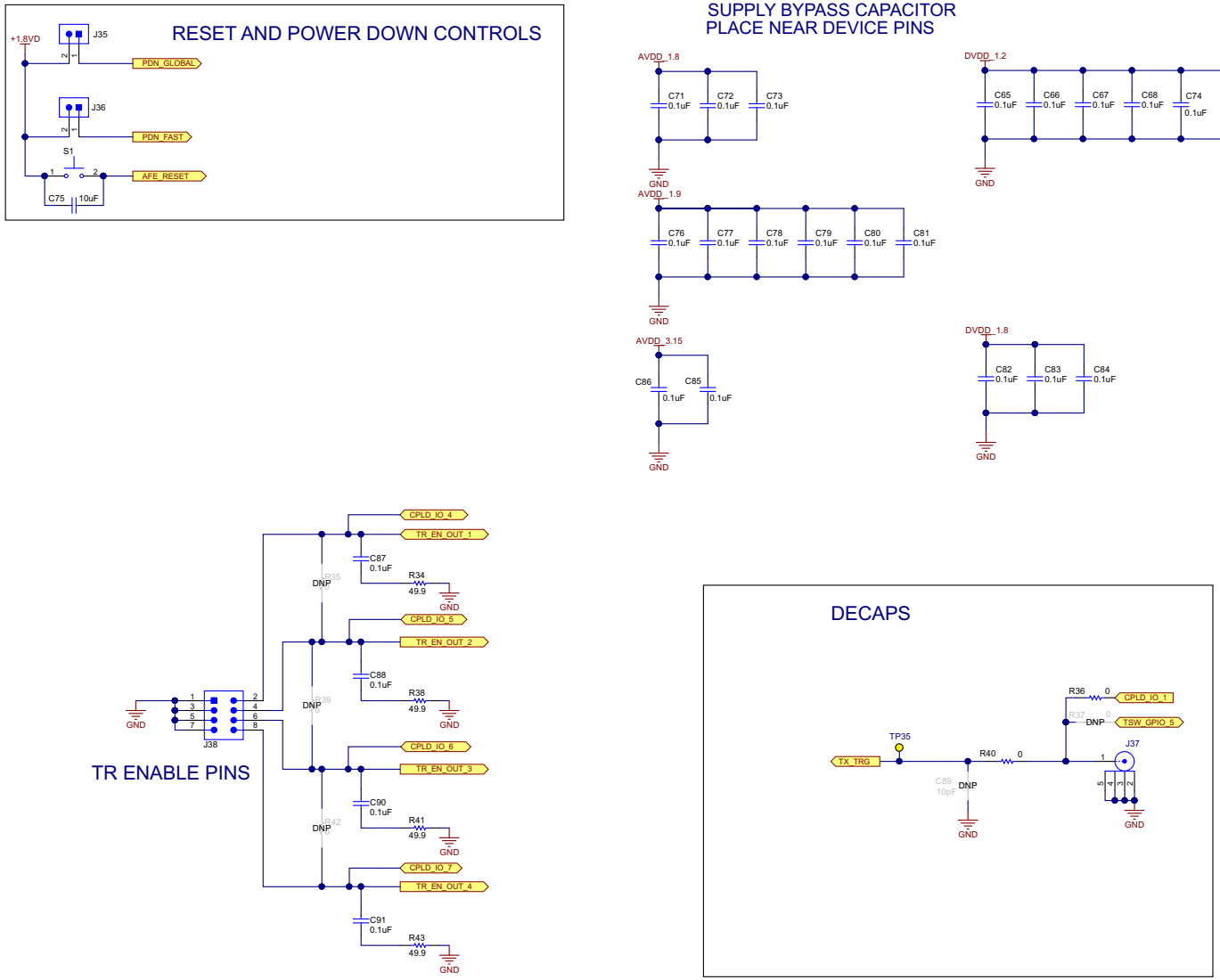
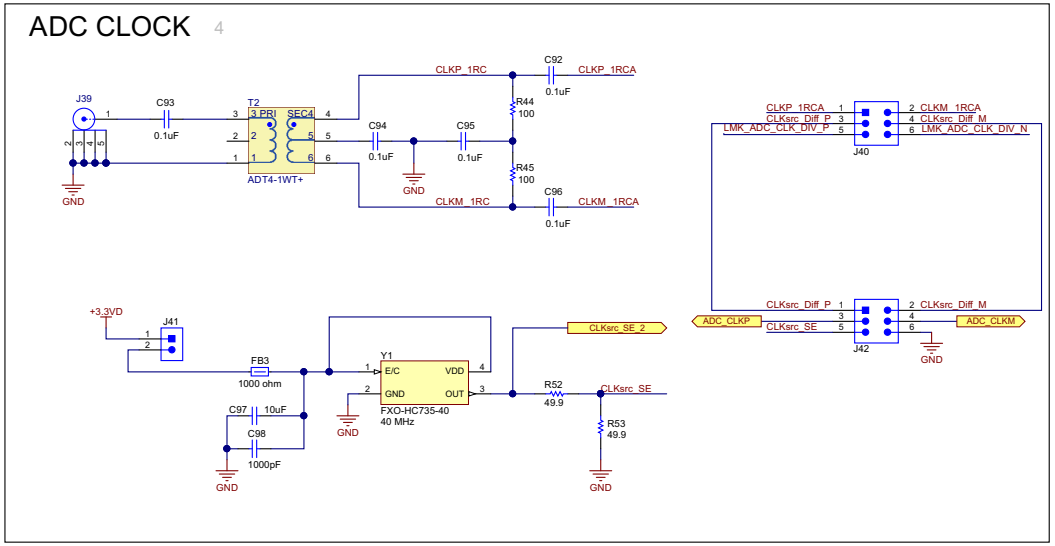
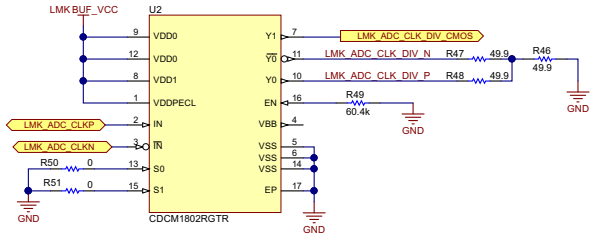
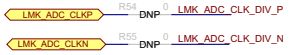


Figure 75. AFE5832 Rev. A EVM Schematic 6 of 12







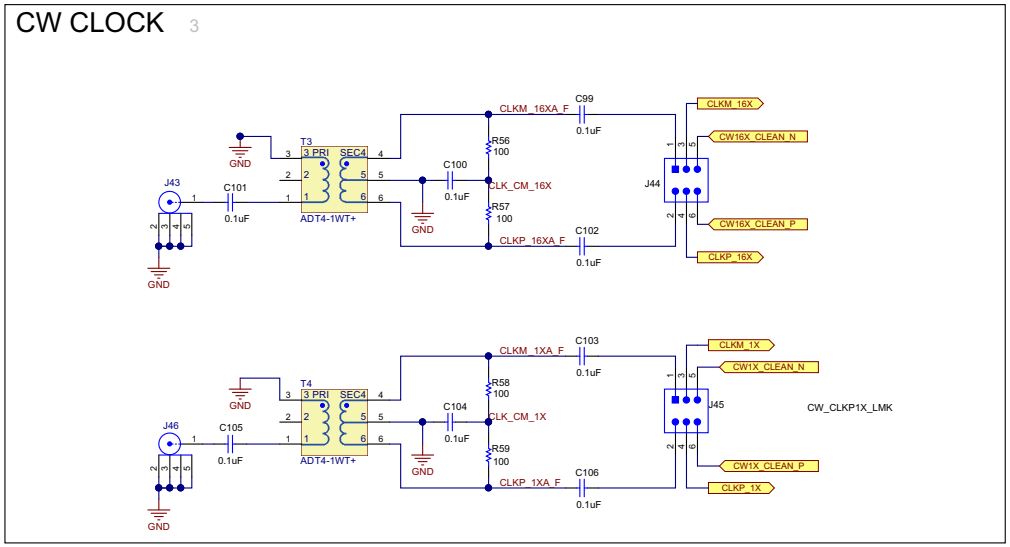


Figure 76. AFE5832 Rev. A EVM Schematic 7 of 12

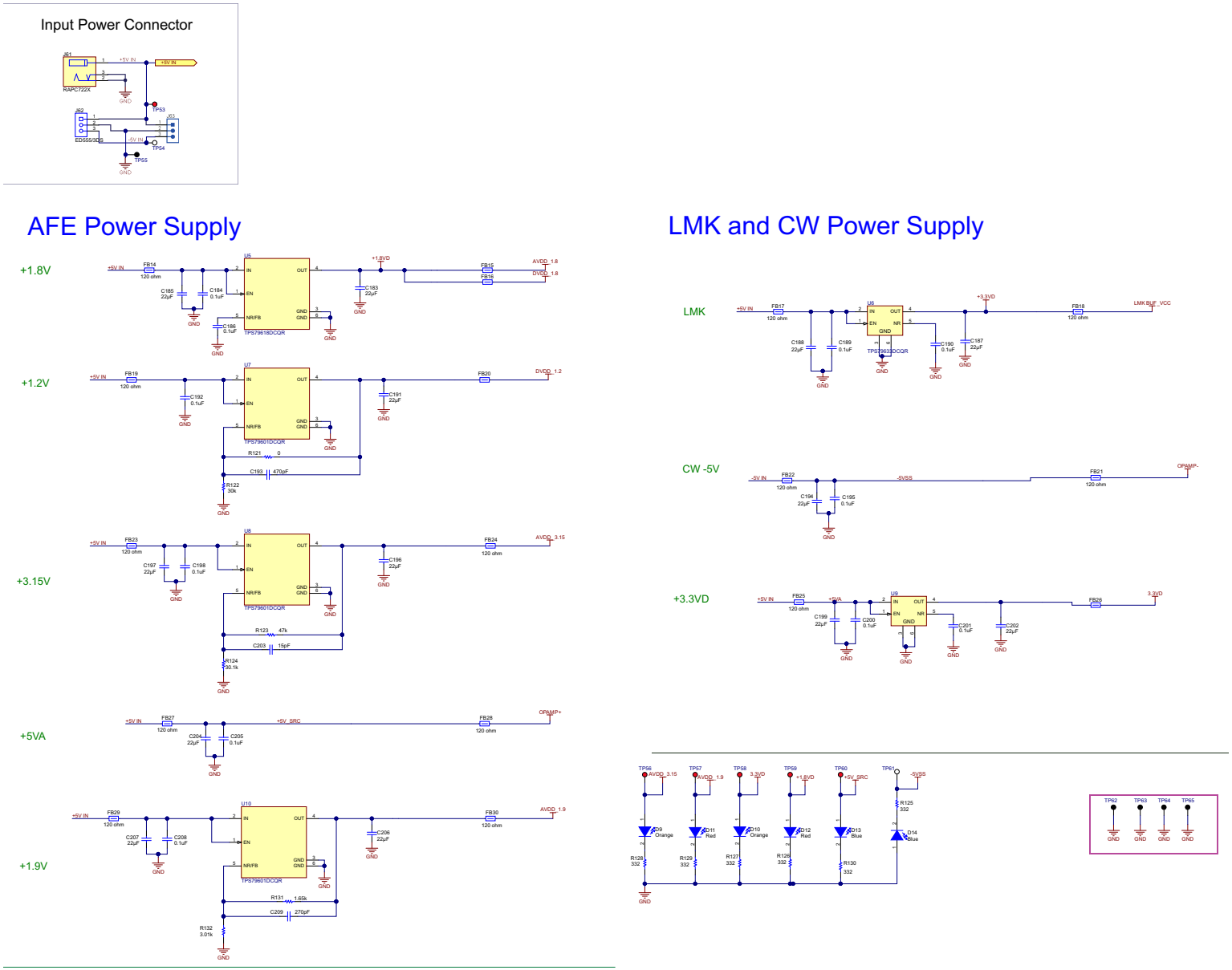


Figure 77. AFE5832 Rev. A EVM Schematic 8 of 12

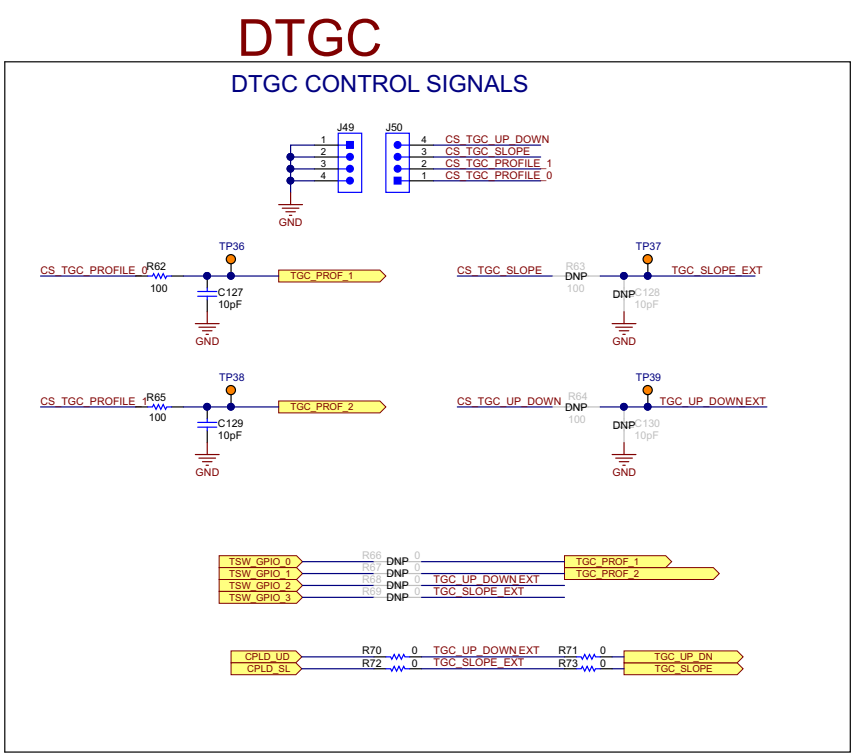


Figure 78. AFE5832 Rev. A EVM Schematic 9 of 12

MHR009 pin configuration

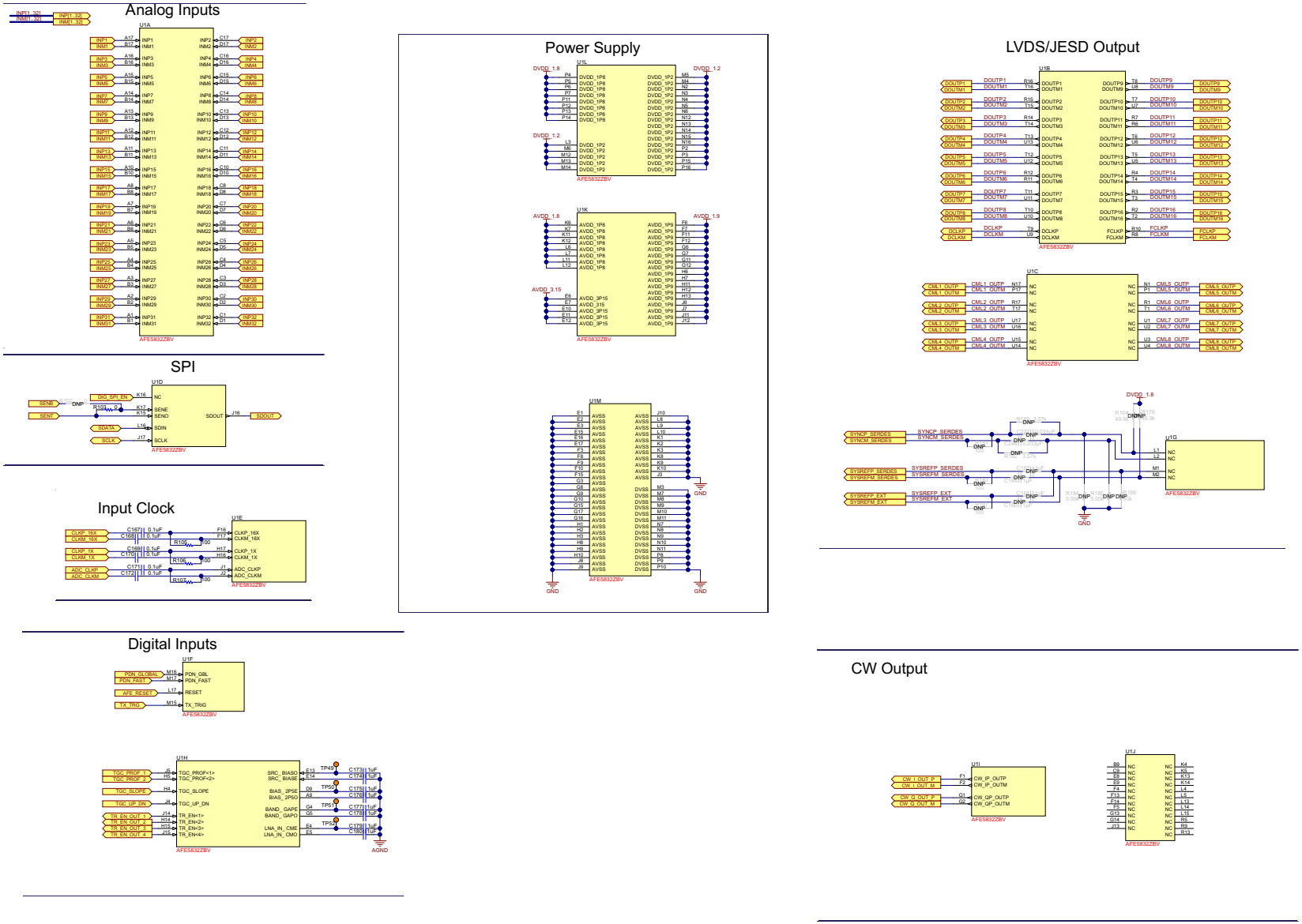


Figure 79. AFE5832 Rev. A EVM Schematic 10 of 12

LMK04826 7

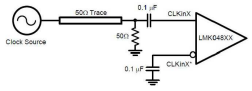


Figure 7-4. CLKinX/X* Single-ended Termination

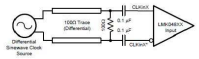
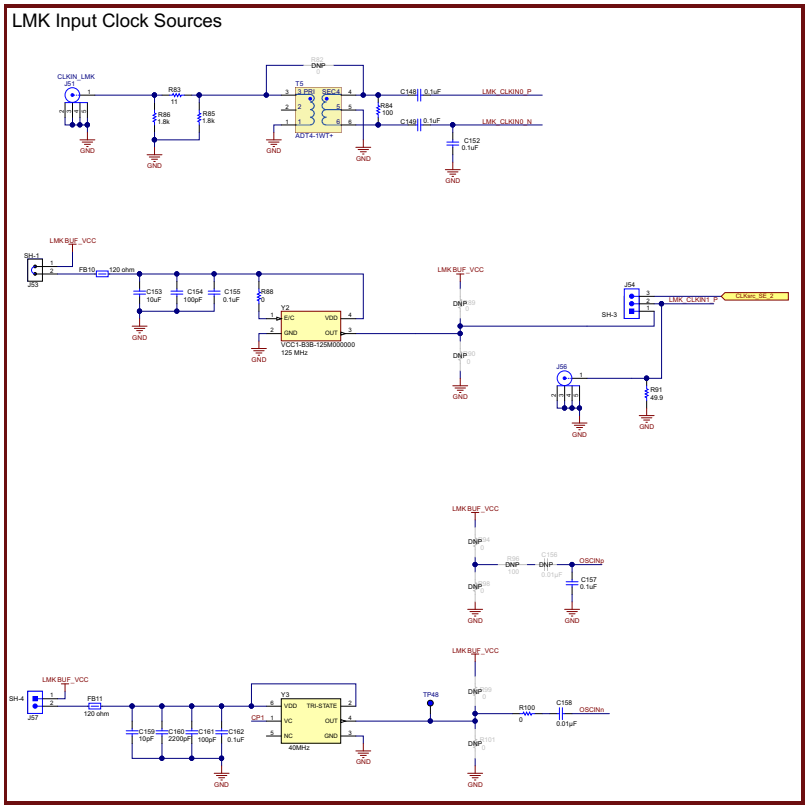


Figure 7-3. CLKinX/X* Termination for a Differential Sinewave Reference Clock Source



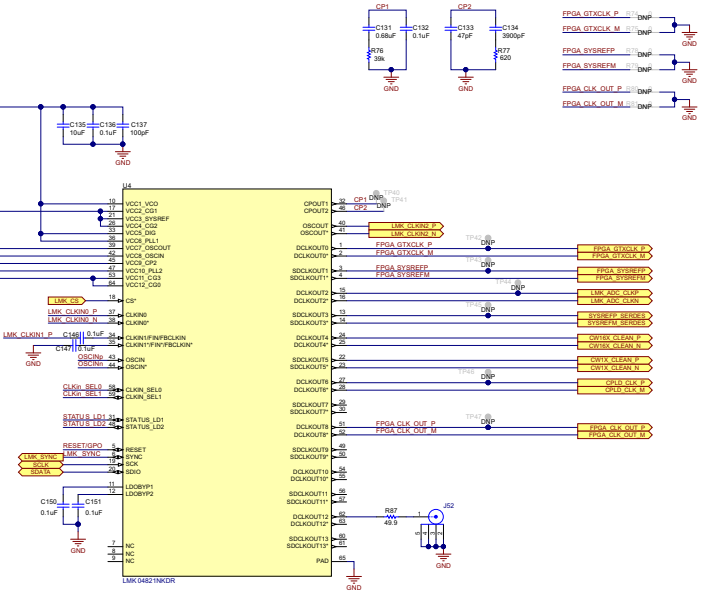
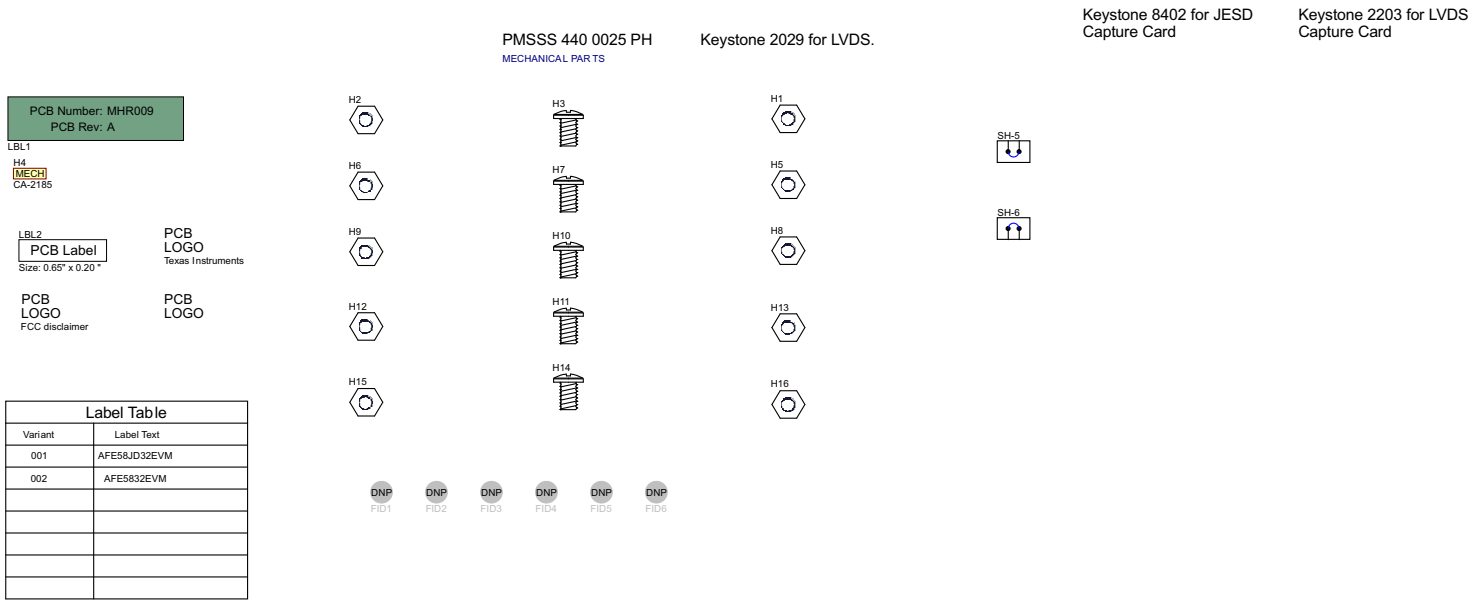


Figure 80. AFE5832 Rev. A EVM Schematic 11 of 12



Label Table

Variant	Label Text
001	AFE58JD32EVM
002	AFE5832EVM

Figure 81. AFE5832 Rev. A EVM Schematic 12 of 12

F.3 EVM Bill of Materials

Table 3 lists the AFE5832 EVM bill of materials (BOM).

Table 3. AFE5832 EVM Bill of Materials (1)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64	64	0.01 µF	CAP, CERM, 0.01 µF, 6.3 V, +/- 10%, X7R, 0402	0402	GRM155R70J103KA01D	MuRata		

(1) Unless otherwise noted in the Alternate Part Number or Alternate Manufacturer columns, all parts may be substituted with equivalents.

Table 3. AFE5832 EVM Bill of Materials (1) (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C90, C91, C92, C93, C94, C95, C96, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C132, C136, C139, C141, C142, C143, C144, C146, C147, C148, C149, C150, C151, C155, C157, C162, C167, C168, C169, C170, C171, C172, C210, C211, C212, C213, C214, C217, C218, C219, C220, C230, C233, C235, C237, C239, C249, C252, C253, C256, C257, C258, C259, C261, C262, C263, C264, C265, C266	107	0.1µF	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0402	0402	GRM155R71C104KA88D	MuRata		
C75	1	10µF	CAP, CERM, 10 µF, 6.3 V, +80/-20%, Y5V, 0805_140	0805_140	GRM21BF50J106ZE01L	MuRata		
C97	1	10µF	CAP, CERM, 10 µF, 6.3 V, +/- 20%, X5R, 0603	0603	C0603C106M9PACTU	Kemet		
C98, C231, C232	3	1000pF	CAP, CERM, 1000 pF, 6.3 V,+/- 10%, X5R, 0402	0402	GRM155R60J102KA01D	MuRata		

Table 3. AFE5832 EVM Bill of Materials (1) (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
C127, C129, C159	3	10pF	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	GRM1555C1H100JA01D	MuRata		
C131	1	0.68µF	CAP, CERM, 0.68 µF, 10 V, +/- 10%, X5R, 0603	0603	C0603C684K8PACTU	Kemet		
C133	1	47pF	CAP, CERM, 47 pF, 100 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C2A470JA01D	MuRata		
C134	1	3900pF	CAP, CERM, 3900 pF, 50 V, +/- 10%, X7R, 0402	0402	GRM155R71H392KA01D	MuRata		
C135, C138, C145, C153	4	10µF	CAP, CERM, 10 µF, 6.3 V, +/- 20%, X5R, 0603	0603	GRM188R60J106ME47D	MuRata		
C137, C140, C154, C161	4	100pF	CAP, CERM, 100 pF, 50 V, +/- 10%, X7R, 0402	0402	CC0402KRX7R9BB101	Yageo America		
C152	1	0.1µF	CAP, CERM, 0.1 µF, 25 V, +/- 5%, X7R, 0603	0603	06033C104JAT2A	AVX		
C158	1	0.01µF	CAP, CERM, 0.01 µF, 16 V,+/- 10%, X5R, 0402	0402	GRM155R61C103KA01D	MuRata		
C160	1	2200pF	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0402	0402	GRM155R71H222KA01D	MuRata		
C173, C174, C175, C176, C177, C178, C179, C180	8	1µF	CAP, CERM, 1 µF, 6.3 V, +/- 20%, X5R, 0402	0402	GRM152R60J105ME15D	MuRata		
C181, C182, C184, C186, C189, C190, C192, C195, C198, C200, C201, C205, C208	13	0.1µF	CAP, CERM, 0.1µF, 16V, +/- 10%, X5R, 0603	0603	GRM188R61C104KA01D	MuRata		
C183, C187, C191, C196, C202, C206	6	22µF	CAP, CERM, 22 µF, 10 V,+/- 20%, X5R, 0603	0603	GRM187R61A226ME15D	MuRata		
C185, C188, C194, C197, C199, C204, C207	7	22µF	CAP, CERM, 22 µF, 16 V, +/- 20%, X5R, 1206	1206	1206YD226MAT2A	AVX		

Table 3. AFE5832 EVM Bill of Materials (1) (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
C193	1	470pF	CAP, CERM, 470pF, 50V, +/-5%, C0G/NP0, 0603	0603	06035A471JAT2A	AVX		
C203	1	15pF	CAP, CERM, 15 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	06035A150JAT2A	AVX		
C209	1	270pF	CAP, CERM, 270 pF, 50 V, +/- 10%, X7R, 0603	0603	GRM188R71H271 KA01D	MuRata		
C215, C216	2	47pF	CAP, CERM, 47 pF, 50 V, +/- 1%, C0G/NP0, 0402	0402	GRM1555C1H470 FA01D	MuRata		
C221, C222, C226, C228, C240, C241, C245, C246	8	0.015µF	CAP, CERM, 0.015 µF, 16 V,+/- 5%, X7R, 0402	0402	GRM155R71C153J A01D	MuRata		
C223, C224, C225, C242, C243, C244	6	4.7µF	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X5R, 0603	0603	C0603C475K8PAC TU	Kemet		
C229, C234, C236, C238, C250, C251, C254, C255	8	1µF	CAP, CERM, 1 µF, 16 V, +/- 10%, X5R, 0603	0603	C0603C105K4PAC TU	Kemet		
D1, D2, D3, D4	4	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190KGKT	Lite-On		
D5, D6, D7, D8, D11, D12	6	Red	LED, Red, SMD	Red LED, 1.6x0.8x0.8mm	LTST-C190CKT	Lite-On		
D9, D10	2	Orange	LED, Orange, SMD	1.6x0.8x0.8mm	LTST-C190KFKT	Lite-On		
D13, D14	2	Blue	LED, Blue, SMD	BLUE 0603 LED	LB Q39G-L2N2-35-1	OSRAM		
FB3	1	1000 Ω	Ferrite Bead, 1000 Ω @ 100 MHz, 0.3 A, 0402	0402	BLM15AG102SN1 D	MuRata		
FB4, FB5, FB6, FB7, FB8, FB9, FB12, FB14, FB15, FB16, FB17, FB18, FB19, FB20, FB21, FB22, FB23, FB24, FB25, FB26, FB27, FB28, FB29, FB30, FB31, FB32	26	120 Ω	Ferrite Bead, 120 Ω @ 100 MHz, 0.8 A, 0805	0805	BLM21AG121SN1 D	MuRata		
FB10, FB11	2	120 Ω	Ferrite Bead, 120 Ω @ 100 MHz, 4 A, 1206	1206	HI1206P121R-10	Laird-Signal Integrity Products		

Table 3. AFE5832 EVM Bill of Materials [(1)] (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
H1, H5, H8, H13, H16	5		HEX STANDOFF 4-40 ALUMINUM 1/2"	HEX STANDOFF 4-40 ALUMINUM 1/2"	2203	Keystone		
H2, H6, H9, H12, H15	5		HEX, M-F STANDOFF 4-40 ALUMINUM 5/8"	HEX, M-F STANDOFF 4-40 ALUMINUM 5/8"	8402	Keystone		
H3, H7, H10, H11, H14	5		MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4"	PMSSS 440 0025 PH	B&F Fastener Supply		
H4	1		CABLE ASSY STR 2.1MM 6' 24 AWG		CA-2185	Tensility		
J1, J4, J8, J11, J14, J17, J21, J24, J27, J30	10		Connector, End launch SMA, 50 Ω, SMT	End Launch SMA	142-0701-801	Johnson		
J2, J3, J5, J6, J9, J10, J12, J13, J15, J16, J19, J20, J22, J23, J25, J26, J28, J29, J31, J32, J33, J34, J37, J39, J43, J46, J51, J52, J56, J59, J66, J68	32		SMA Straight PCB Socket Die Cast, 50 Ω, TH	SMA Straight PCB Socket Die Cast, TH	5-1814832-1	TE Connectivity		
J7, J18, J48	3		Socket, 0.5MM, 60x2, Gold, SMT	Socket, Female, 0.5MM, 60x2, SMT	QTH-060-01-L-D-A	Samtec		
J35, J36, J41, J53, J57	5		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec		
J38, J60	2		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec		
J40, J42, J44, J45	4		Header, TH, 100mil, 3x2, Gold plated, 230 mil above insulator	3x2 Header	TSW-103-07-G-D	Samtec		
J49, J50	2		Header, TH, 100mil, 4x1, Gold plated, 230 mil above insulator	4x1 Header	TSW-104-07-G-S	Samtec		
J54, J55, J63	3		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec		
J58	1		Header, 100mil, 6x1, Gold, TH	6x1 Header	TSW-106-07-G-S	Samtec		

Table 3. AFE5832 EVM Bill of Materials (1) (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
J61	1		Power Jack, mini, 2.1mm OD, R/A, TH	Jack, 14.5x11x9mm	RAPC722X	Switchcraft		
J62	1		Terminal Block, 3.5mm Pitch, 3x1, TH	10.5x8.2x6.5mm	ED555/3DS	On-Shore Technology		
J65	1		Connector, Receptacle, USB - mini AB, R/A, SMD	Receptacle, 5-Leads, Body 9.9x9mm, R/A	67803-8020	Molex		
J67	1		Audio Jack, 3.5 mm, Stereo, R/A, TH	Connector, 3-Leads, 3.5mm Stereo Jack R/A, TH	STX-3000	Kycon Inc		
LBL1	1		Printed Circuit Board		MHR009	Any		
LBL2	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650≈ x 0.200"W	THT-14-423-10	Brady	-	-
R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R34, R38, R41, R43, R46, R47, R48, R52, R53, R87, R91, R143, R144, R145, R152, R153, R154	49	49.9	RES, 49.9, 1%, 0.063 W, 0402	0402	CRCW040249R9FKED	Vishay-Dale		
R36, R40, R50, R51, R60, R61, R70, R71, R72, R73, R88, R100, R103, R112, R139, R140, R158, R159, R164, R165, R167, R172, R175, R177	24	0	RES, 0, 5%, 0.063 W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale		

Table 3. AFE5832 EVM Bill of Materials (1) (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
R44, R45, R56, R57, R58, R59, R84, R105, R106, R107, R108, R109, R110, R111	14	100	RES, 100, 1%, 0.1 W, 0402	0402	ERJ-2RKF1000X	Panasonic		
R49	1	60.4k	RES, 60.4k Ω, 1%, 0.063W, 0402	0402	CRCW040260K4FKED	Vishay-Dale		
R62, R65	2	100	RES, 100, 1%, 0.1 W, 0603	0603	CRCW0603100RFKEA	Vishay-Dale		
R76	1	39k	RES, 39 k, 5%, 0.063 W, 0402	0402	CRCW040239K0JNED	Vishay-Dale		
R77	1	620	RES, 620, 5%, 0.063 W, 0402	0402	CRCW0402620RJNED	Vishay-Dale		
R83	1	11	RES, 11, 5%, 0.063 W, 0402	0402	CRCW040211R0JNED	Vishay-Dale		
R85, R86	2	1.8k	RES, 1.8 k, 5%, 0.063 W, 0402	0402	CRCW04021K80JNED	Vishay-Dale		
R92, R93, R95, R97	4	750	RES, 750, 5%, 0.063 W, 0402	0402	CRCW0402750RJNED	Vishay-Dale		
R114, R115, R116, R117, R118, R119, R120	7	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1002V	Panasonic		
R121	1	0	RES, 0 Ω, 5%, 0.125W, 0805	0805	CRCW08050000Z0EA	Vishay-Dale		
R122	1	30k	RES, 30k Ω, 5%, 0.125W, 0805	0805	CRCW080530K0JNEA	Vishay-Dale		
R123	1	47k	RES, 47 k, 5%, 0.1 W, 0603	0603	CRCW060347K0JNEA	Vishay-Dale		
R124	1	30.1k	RES, 30.1 k, 1%, 0.1 W, 0603	0603	CRCW060330K1FKEA	Vishay-Dale		
R125, R126, R127, R128, R129, R130	6	332	RES, 332, 1%, 0.063 W, 0402	0402	CRCW0402332RFKED	Vishay-Dale		
R131	1	1.65k	RES, 1.65 k, 1%, 0.1 W, 0603	0603	CRCW06031K65FKEA	Vishay-Dale		
R132	1	3.01k	RES, 3.01k Ω, 1%, 0.1W, 0603	0603	CRCW06033K01FKEA	Vishay-Dale		
R141, R142, R146, R147, R150, R151, R155, R156	8	499	RES, 499, 1%, 0.063 W, 0402	0402	CRCW0402499RFKED	Vishay-Dale		

Table 3. AFE5832 EVM Bill of Materials (1) (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
R148, R171	2	3.30k	RES, 3.30 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF3301X	Panasonic		
R149, R174	2	4.70k	RES, 4.70 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF4701X	Panasonic		
R161, R162, R169, R170	4	140k	RES, 140 k, 1%, 0.063 W, 0402	0402	CRCW0402140KFKED	Vishay-Dale		
R188, R189	2	0	RES, 0, 5%, 0.125 W, 0805	0805	MCR10EZPJ000	RΩ		
S1, S2, S3, S4, S6	5		Switch, push-button, SMD	2.9x2x3.9mm SMD	SKRKAEE010	Alps		
S5	1		Switch, SPST, 4 Pos, Top Actuated, SMD	SMD, 8-Leads, Pitch 1.27mm	1571983-5	TE Connectivity		
SH-1, SH-2, SH-3, SH-4, SH-5, SH-6	6	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
T1, T2, T3, T4, T5	5		RF Transformer, 50 Ω, 2 to 775 MHz, SMT	CD542	ADT4-1WT+	Minicircuits		
TP31, TP32, TP55, TP62, TP63, TP64, TP65, TP66, TP69	9	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
TP35	1	Yellow	Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone		
TP36, TP37, TP38, TP39, TP49, TP50, TP51, TP52	8	Orange	Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone		
TP48	1	Blue	Test Point, Miniature, Blue, TH	Blue Miniature Testpoint	5117	Keystone		
TP53, TP56, TP57, TP58, TP59, TP60, TP68	7	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone		
TP54, TP61, TP67	3	White	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone		

Table 3. AFE5832 EVM Bill of Materials (1) (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
U1	1		32-Channel Ultrasound AFE with 41.5-mW/Channel Power, 1.5nV/vHz Noise, 12-Bit, 40-MSPS or 10-Bit, 50-MSPS output and Passive CW Mixer, ZBV0289A (NFBGA-289)	ZBV0289A	AFE5832ZBV	Texas Instruments		Texas Instruments
U2	1		CLOCK BUFFER WITH PROGRAMMABLE DIVIDER, LVPECL I/O + ADDITIONAL LVCMOS OUTPUT, RGT0016A	RGT0016A	CDCM1802RGTR	Texas Instruments	CDCM1802RGTT	Texas Instruments
U3	1		64K I2C Smart Serial EEPROM, SOIC-8	SOIC-8, 208mil wide	24LC65-I/SM	Microchip		
U4	1		Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs, NKD0064A (WQFN-64)	NKD0064A	LMK04821NKDR	Texas Instruments	LMK04821NKDT	Texas Instruments
U5	1		Ultralow-Noise, High PSRR, Fast, RF, 1A Low-Dropout Linear Regulator, DCQ0006A	DCQ0006A	TPS79618DCQR	Texas Instruments		Texas Instruments
U6, U9	2		Single Output High PSRR LDO, 1 A, Fixed 3.3 V Output, 2.7 to 5.5 V Input, 6-pin SOT-223 (DCQ), -40 to 125 degC, Green (RoHS and no Sb/Br)	DCQ0006A	TPS79633DCQR	Texas Instruments	Equivalent	None

Table 3. AFE5832 EVM Bill of Materials (1) (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
U7, U8, U10	3		Ultralow-Noise, High PSRR, Fast, RF, 1A, Low-Dropout Linear Regulator, DCQ0006A	DCQ0006A	TPS79601DCQR	Texas Instruments		Texas Instruments
U11	1		USB FIFO IC, 28SSOP	SSOP28	FT245RL	FTDI		
U12	1		4242-VPK Small-Footprint and Low-Power Quad Channels Digital Isolators, DBQ0016A	DBQ0016A	ISO7140CCDBQR	Texas Instruments	ISO7140CCDBQ	Texas Instruments
U13	1		6-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR WITH AUTO-DIRECTION SENSING AND ±15-kV ESD PROTECTION, PW0016A	PW0016A	TXB0106PWR	Texas Instruments		Texas Instruments
U14	1		4242-VPK Small-Footprint and Low-Power Quad Channels Digital Isolators, DBQ0016A	DBQ0016A	ISO7141CCDBQR	Texas Instruments	ISO7141CCDBQ	Texas Instruments
U15, U16	2		HIGH-SPEED, LOW-NOISE, FULLY-DIFFERENTIAL I/O AMPLIFIERS, DGN0008D	DGN0008D	THS4131CDGNR	Texas Instruments	THS4131CDGN	Texas Instruments

Table 3. AFE5832 EVM Bill of Materials (1) (continued)

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
U17, U18, U19, U20	4		Dual, High Gain Bandwidth, High Output Current, Operational Amplifier with Current Limit, 5 to 12 V, -40 to 85 degC, 8-pin SOIC (D8), Green (RoHS and no Sb/Br)	D0008A	OPA2614ID	Texas Instruments	Equivalent	Texas Instruments
U21	1		XC2C64A CoolRunner-II CPLD, QFG48	QFN-48	XC2C64A-5QFG48C	Xilinx		
Y1	1		OSC, 3.3 V, 40 MHz, SMD	SMD, 4-Leads, Body 7x5mm	FXO-HC735-40	Fox Electronics		
Y2	1		OSC, 3.3 V, 125 MHz, 15 pF, SMD	7x5mm	VCC1-B3B-125M000000	Vectron		
Y3	1		OSC, 40 MHz, 3.3V, SMD	7x5mm	ASVV-40.000MHZ-N102-T	Abracon Corportation		

FAQ and Troubleshooting

G.1 Common Issues

The following section illustrates some of the common problems seen when attempting to use the EVM hardware and software.

G.1.1 Issues

- **Other Versions of Windows**: Officially, the EVM software supports Windows 7 and Windows 10.
- **Power supply capacity:** It is likely that both the AFE EVM and the TSW EVM do not have a wall power supply. Instead, they include the ability to connect to a bench-top supply via the provided cable. It is critical that each of these EVMs has access to 2 A of current capacity.
- **No Capture in HSDC Pro:** It is possible that once the GUIs and EVMs are configured for capture, and the capture button in HSDC Pro is pressed, that nothing seems to happen and eventually the GUI will timeout and a pop-up an error appears as seen in Figure 82. Reasons for this can include the following:
  - Incorrect firmware loaded
  - Current starvation on at least one EVM, 2 A is sufficient
  - Missing Data output clock from the AFE to the FPGA. With LVDS, this could be the FCLK or DCLK. D5 of the TSW1400 should turn on, and if not, this is probably the reason.
    - Verify that the EVMs are mechanically mated correctly
    - Verify power supply to both EVMs
    - Verify jumper settings on the AFE EVM. Particularly inspect J54, J53, J57, J41, J40 and J42.
    - Use an oscilloscope to test the frequency of the clock at header J40 or J42. This should be 40-MHz.
- **Even-odd channel swap observed with LVDS capture**: Make sure that Switch 4 in S5 is in the "off" position with LED D8 on. Ensure that there is no SMA cable connected to J37 on the AFE5832EVM before retrying capture in HSDC Pro.

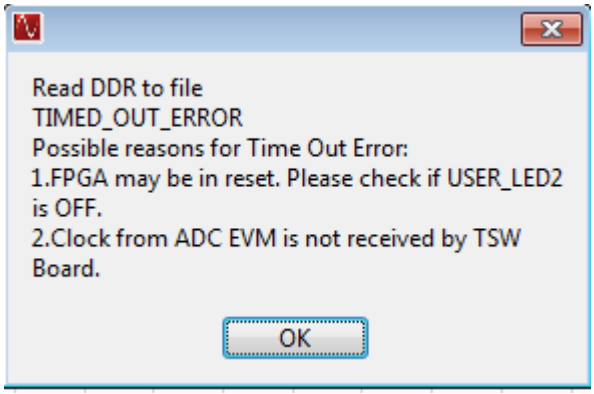


Figure 82. Read DDR Error for No Capture

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265