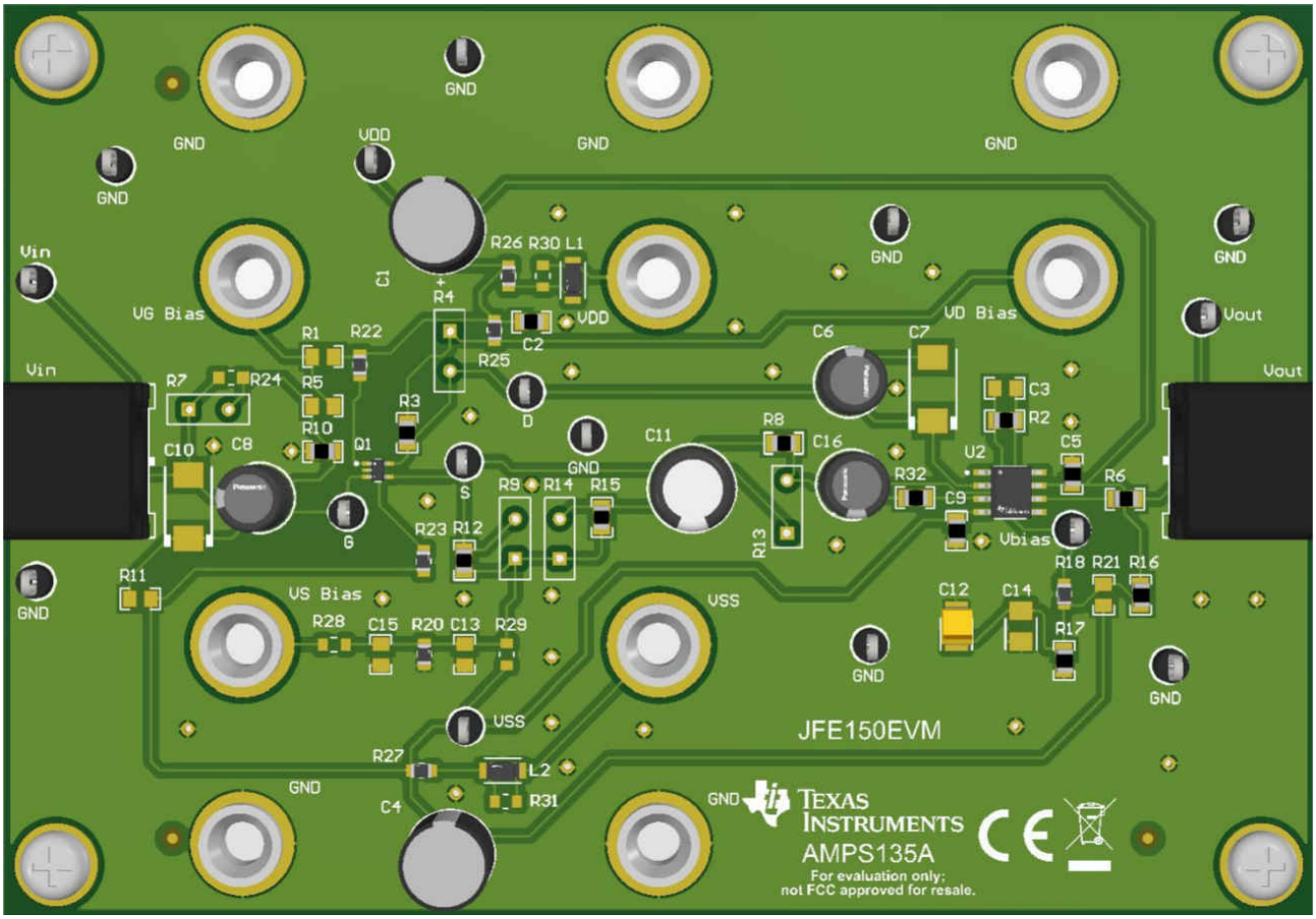
User's Guide

JFE150 Evaluation Module

ABSTRACT



This user's guide contains information and support documentation for the JFE150 evaluation module (EVM). Included are the circuit description, schematic, and bill of materials of the JFE150EVM. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the JFE150EVM.

Table of Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Overview

1.1 JFE150

The JFE150 is an ultra-low-noise, low-gate-current, N-channel JFET capable of operating over a wide drain-to-source voltage of up to 40 V and a gate-to-drain voltage down to –40 V. The JFE150 yields excellent noise performance for currents from 50 µA to 20 mA with extremely high input impedance (> 1 TΩ). When biased at 5 mA, the device yields 0.8 nV/√Hz. The device is offered in 5-pin SOT23 and SC-70 packages.

1.2 JFE150EVM

The JFE150EVM is intended to provide basic functional evaluation of the JFE150 device. Key EVM features include the following:

- JFE150 Ultra-Low-Noise Pre-Amp default configuration
- BNC connections for input and output
- Convenient test points to all pertinent nodes
- Resistor and capacitor through hole and surface mount pad options for critical signal paths
- Banana plug connections for power supplies and bias nodes

1.3 Related Documentation

The documents listed in Table 1-1 provide information about TI's integrated circuits and support tools for the JFE150EVM.

Table 1-1. Related Documentation

Document	Literature Number
JFE150 product data sheet	SLPS732
JFE150 application note	SLPA018
OPA202 product data sheet	SBOS812

1.4 Evaluation Module Limitations and Cautions

The default JFE150EVM configuration is designed to operate within the specified voltage and current regions of the JFE150 N-channel JFET and the OPA202 op amp. User modifications can be made to the JFE150EVM. Take care by referencing the respective product data sheets to maintain specified operating conditions for each device. In addition to observing the specified current and voltage levels, proper electrostatic discharge precautions are advised when handling and applying the EVM.

1.5 Electrostatic Discharge Caution

CAUTION

Many of the components on the JFE150EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM. Failure to observe ESD handling procedures may result in damage to the EVM components.

2 Getting Started

This section explains the connectors and test points, and details the basic EVM functionality.

2.1 Power Supplies

The JFE150EVM is configured by default to operate from a single supply voltage of VDD = 12 V and VSS = GND. VSS can be tied to GND by using a short BNC cable from the VSS banana jack to any GND banana jack shown in Figure 4-2. If dual-supply operation is required, VSS can be powered separately; adjust components R25 and R12 to bias the JFE150 to the desired bias point. Set Vbias to midsupply, as discussed in section Section 2.3.

2.2 Input

The input to the JFE150EVM is designed to interface high-impedance sources to the gate of the JFET. The input is ac-coupled with capacitor C8 and the dc gate bias voltage is set with resistor R10. A single BNC connector and Vin test point are available at the input to allow for an easy interface with signal generators or other equipment. The midband gain of the circuit is approximately 1000 V/V or 60 dB, as shown in Figure 3-2. For example, a 1-mVpp, 1-kHz input signal produces an approximately 1-Vpp, 1-kHz signal measured on the output. The Design tools and simulation tab on the device web folder can assist with other configurations.

2.3 Vbias

The section labeled Vbias in Figure 4-1 consists of a simple voltage divider. The default voltage divider configuration is used to set the Vbias node to midsupply on a single supply voltage. Operating the EVM on a single supply voltage of VDD = 12 V and VSS = GND results in Vbias ≅ 6 V. Vbias sets the common-mode voltage of the OPA202 resulting in a dc voltage of approximately 6 V seen at the Vout of the EVM. Monitor Vbias by using the test point labeled Vbias. When using the EVM in a dual-supply configuration, set the Vbias point to midsupply by removing resistor R16 and replacing R17 with a 0-Ω resistor.

2.4 Output

Monitor the EVM output by using the BCN connector labeled Vout or the test point labeled Vout. Resistor R6 is used as an isolation resistor on OPA202 output to improve circuit stability while driving high capacitive loads greater than 1 nF. Resistor R6 can be removed if no capacitive load drive is required.

2.5 Capacitors

When altering the JFE150EVM default configuration, consider the polarity of tantalum and electrolytic capacitors. The JFE150EVM is populated with bipolar electrolytic capacitors for capacitors C6, C8, and C16.

3 Application Circuit

The JFE150EVM may be configured in standard JFET circuits for evaluation. See the JFE150 data sheet for typical applications.

3.1 JFE150 Ultra-Low-Noise Pre-Amp

The default configuration of the JFE150EVM is shown in Figure 4-1. The JFE150EVM is configured to operate on a single supply of VDD = 12 V and VSS = GND. The output voltage, Vout, settles to approximately midsupply or 6 V, as shown in Figure 3-1. A theoretical explanation of the preamplifier with a JFE150 front end in a closed-loop circuit is detailed in the *JFE150 Ultra-Low-Noise- Pre-Amp* application report.

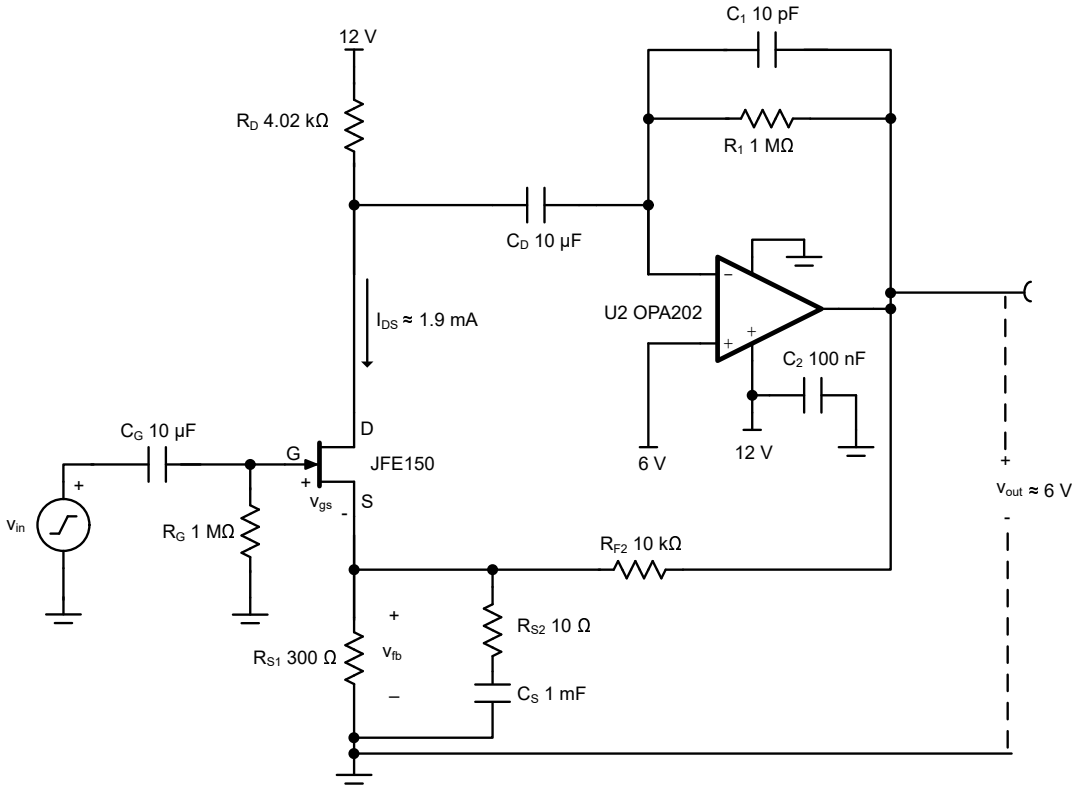


Figure 3-1. Pre-Amp With JFE150 Front End in a Closed-Loop Circuit

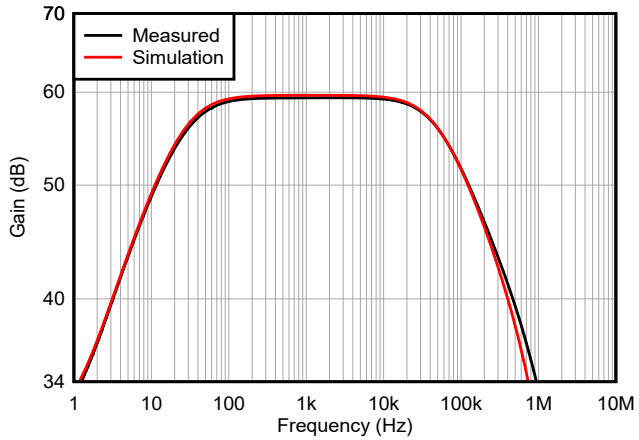


Figure 3-2. Gain vs Frequency

4 Schematic, PCB Layout, and Bill of Materials

4.1 JFE150EVM Schematic

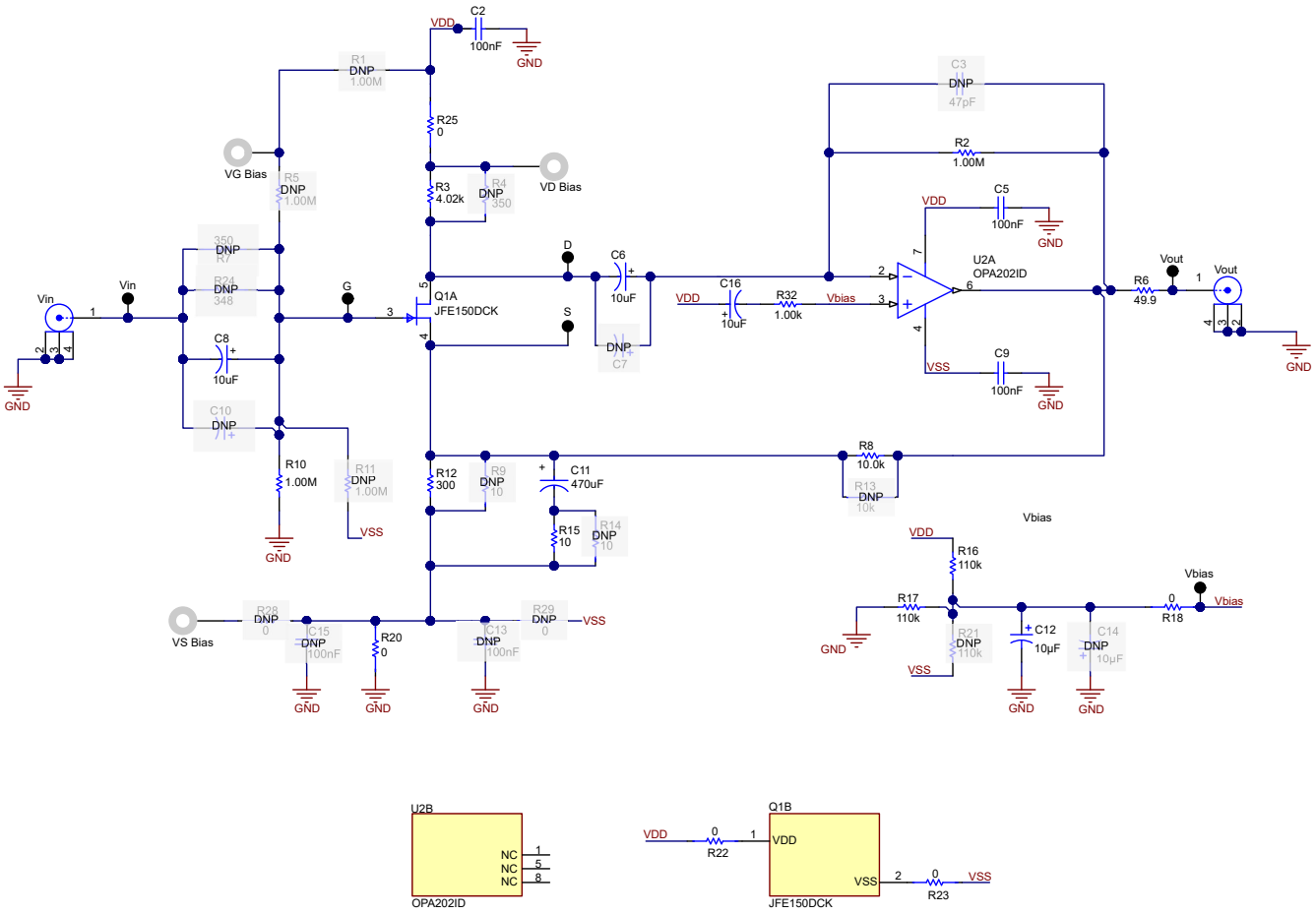


Figure 4-1. JFE150EVM Default Configuration Schematic

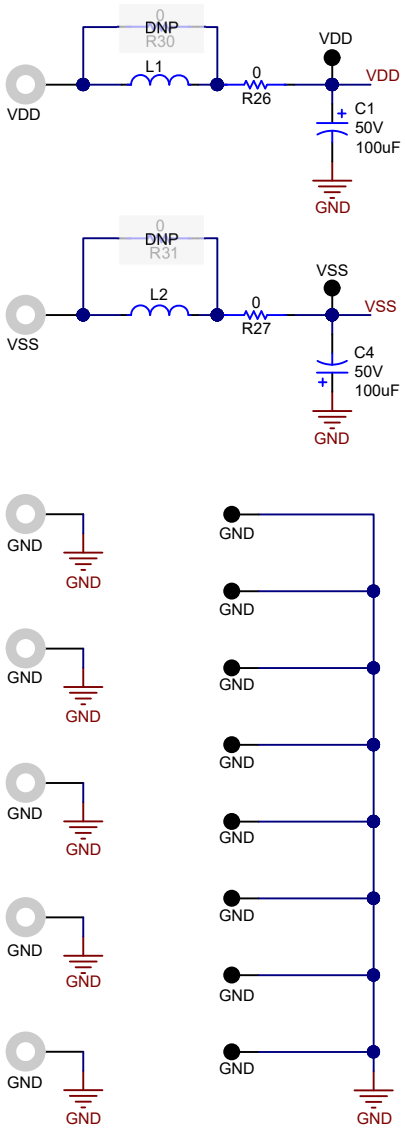


Figure 4-2. JFE150EVM Power Supply Connections

4.2 PCB Layout

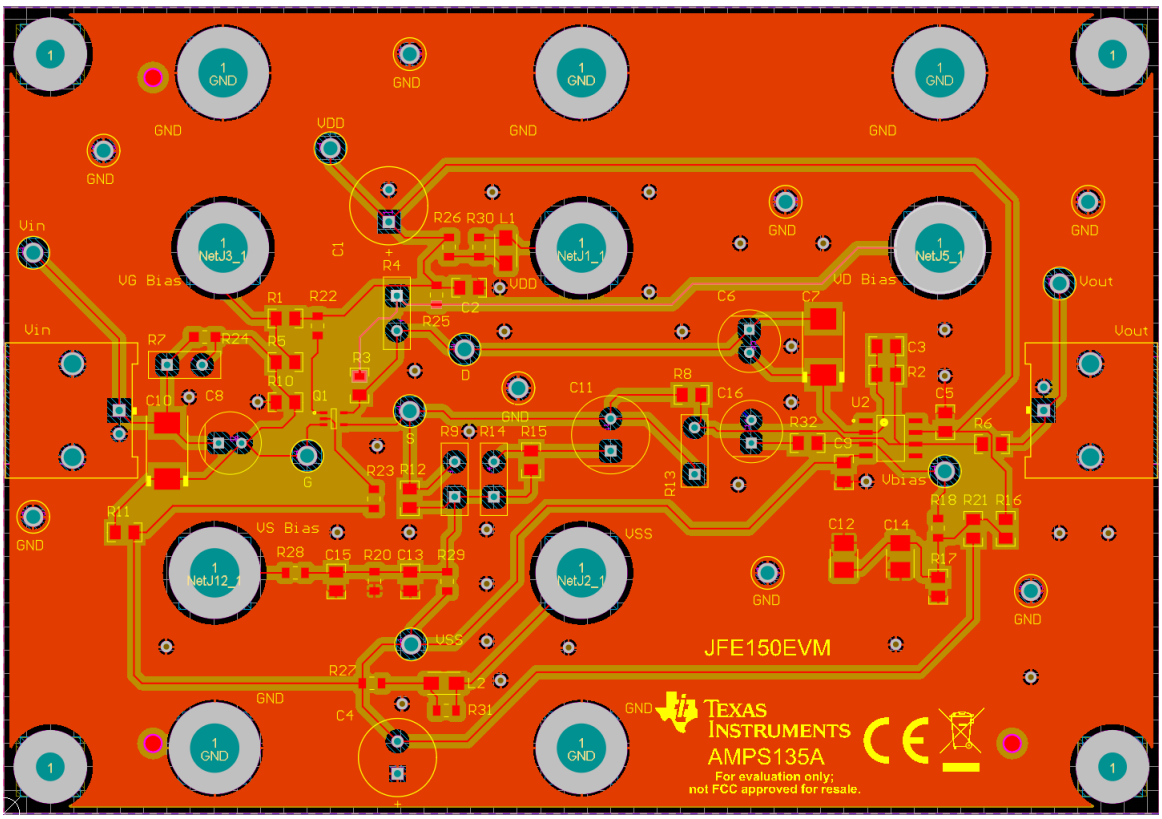


Figure 4-3. JFE150EVM PCB Layout

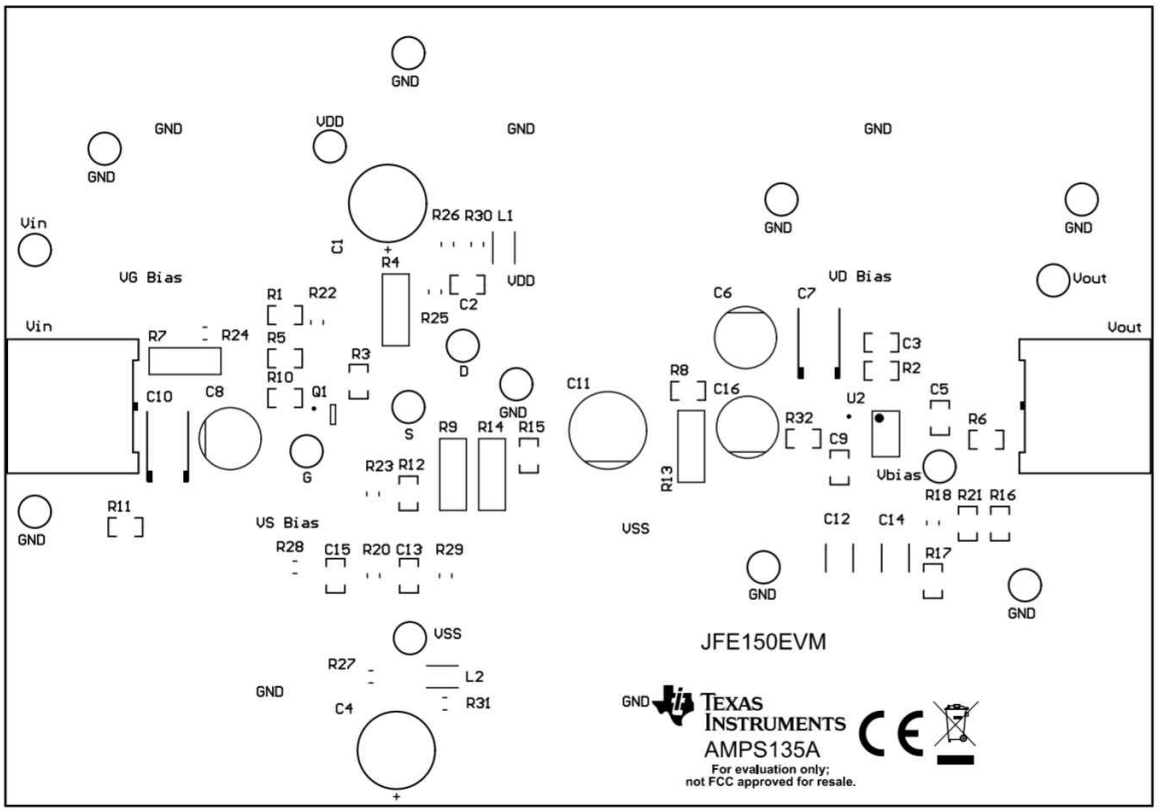


Figure 4-4. JFE150EVM Top Overlay

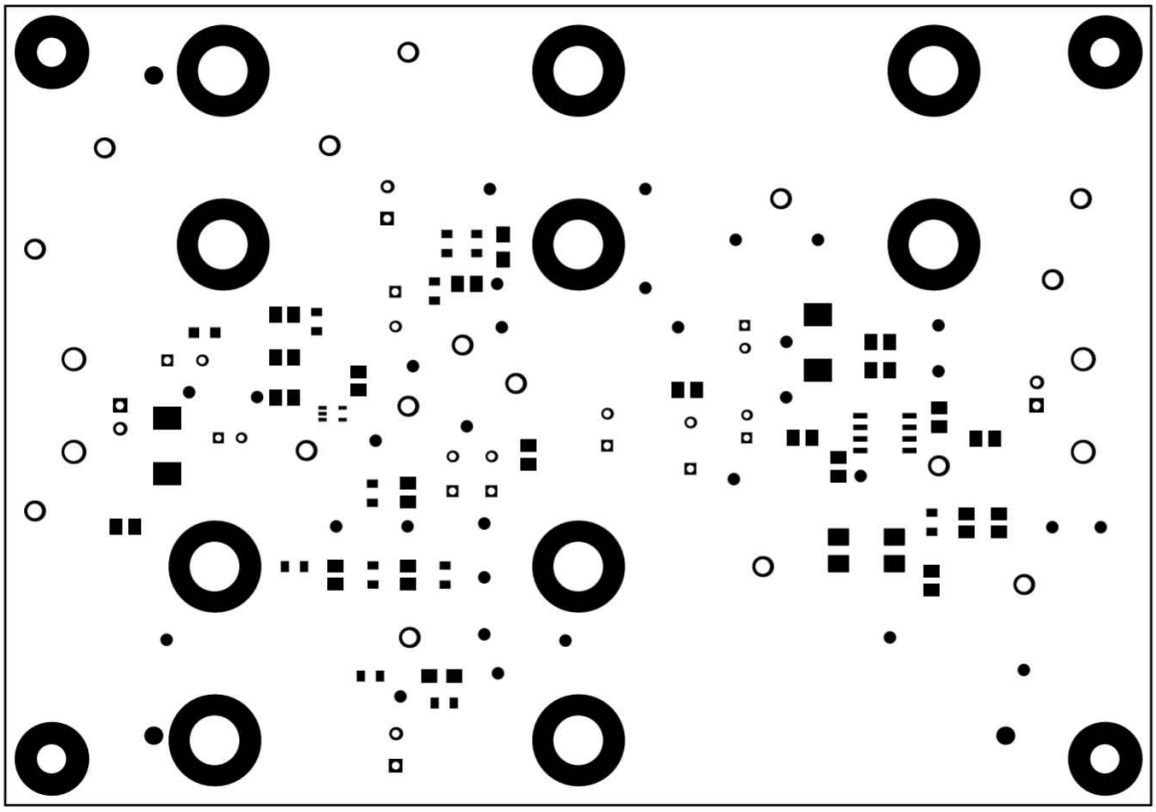


Figure 4-5. JFE150EVM Top Solder Mask

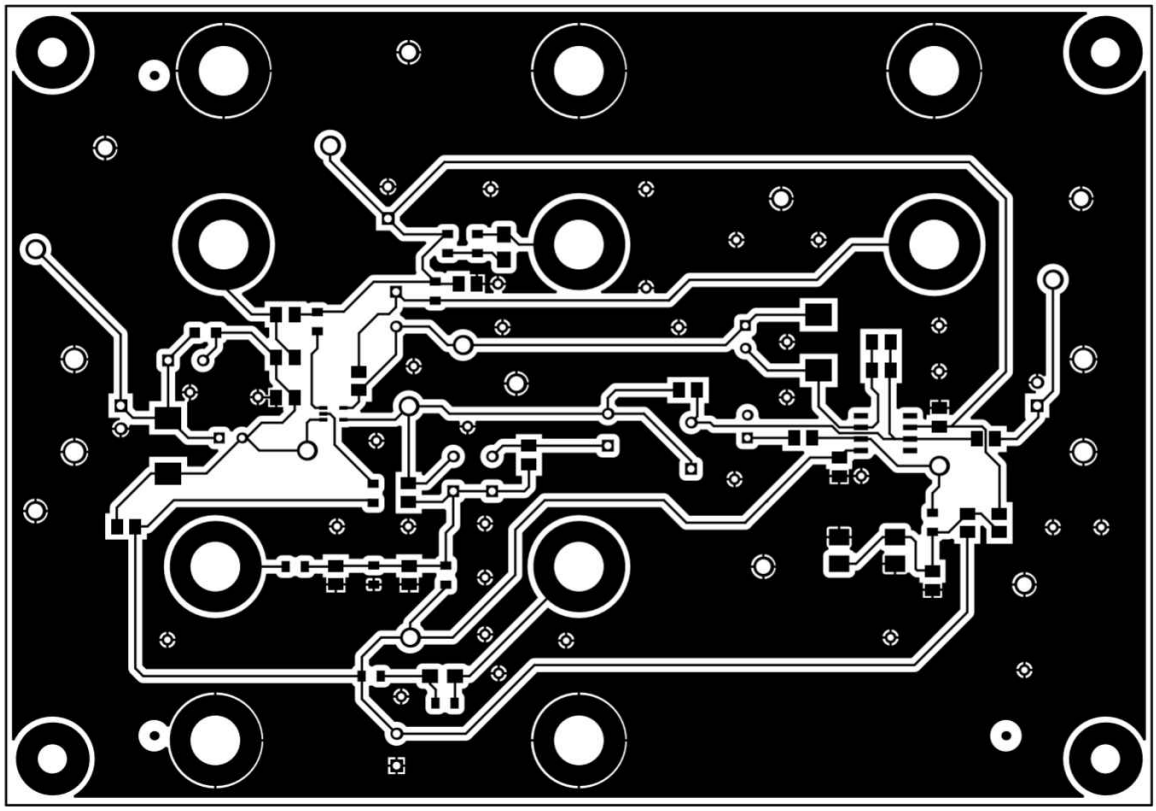


Figure 4-6. JFE150EVM Top Layer

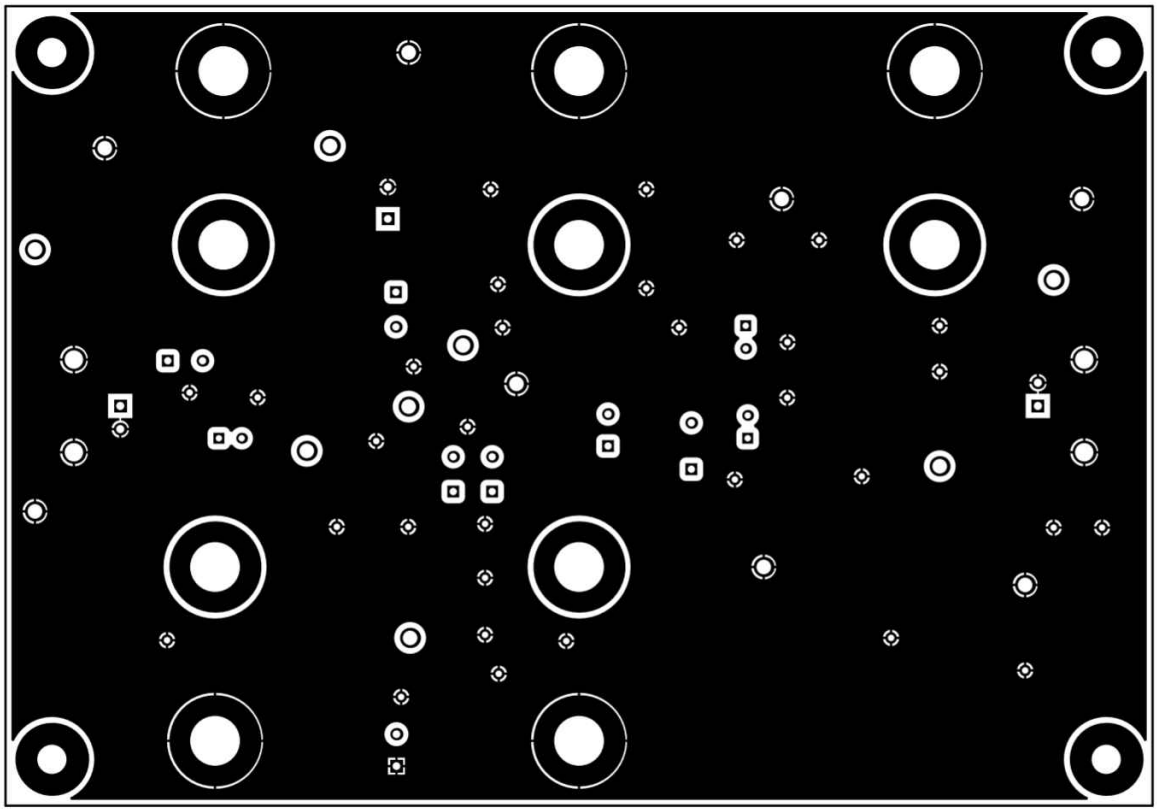


Figure 4-7. JFE150EVM Signal Layer 1

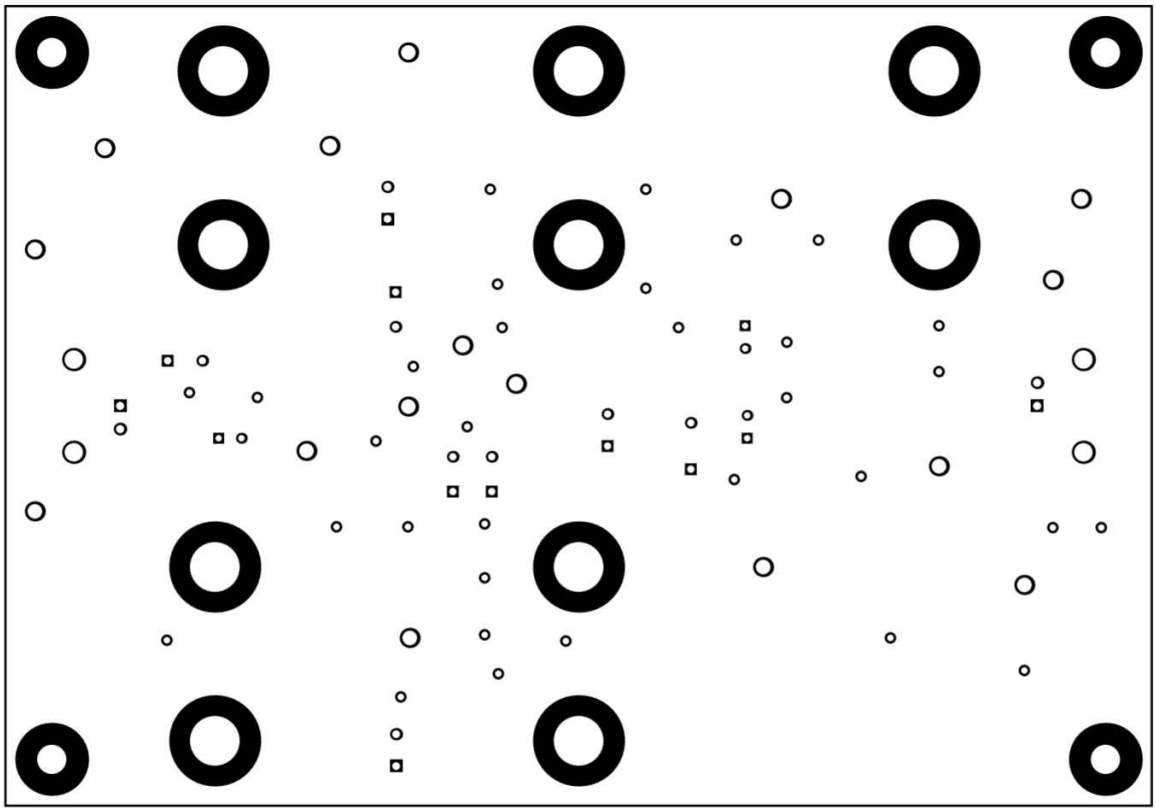


Figure 4-8. JFE150EVM Signal Layer 2

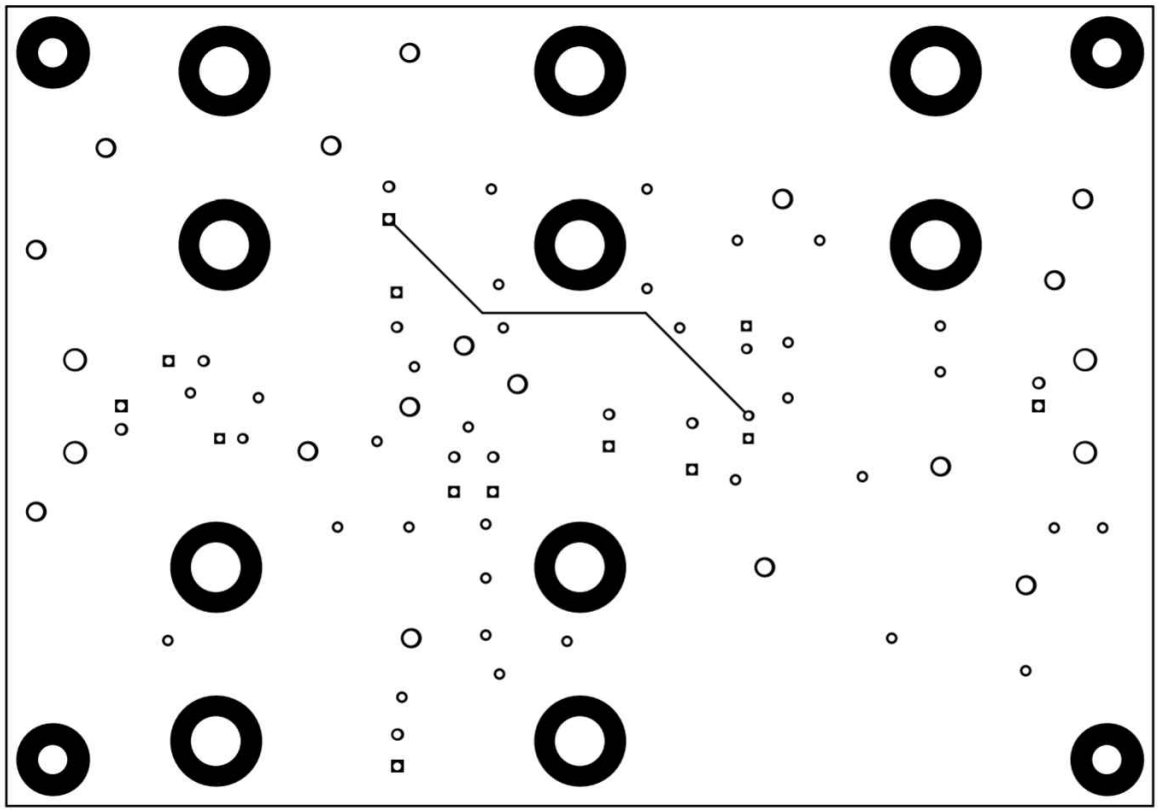


Figure 4-9. JFE150EVM Bottom Layer

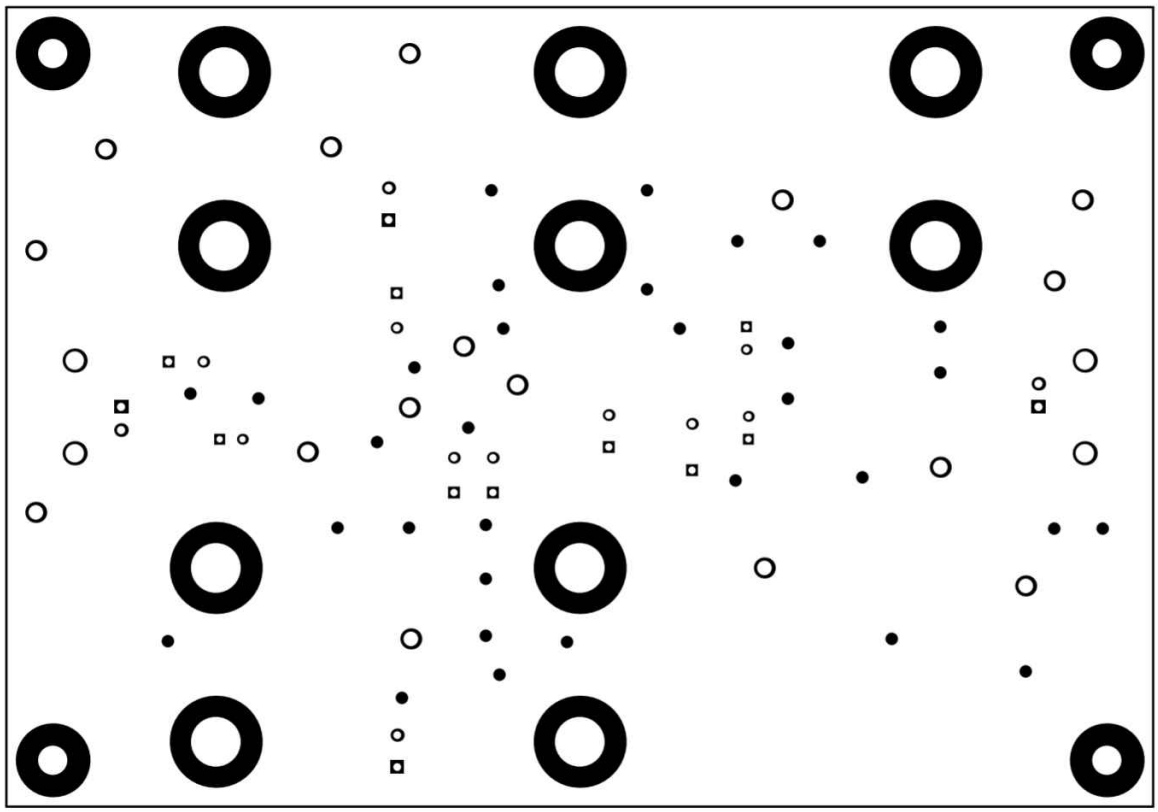


Figure 4-10. JFE150EVM Bottom Solder Mask

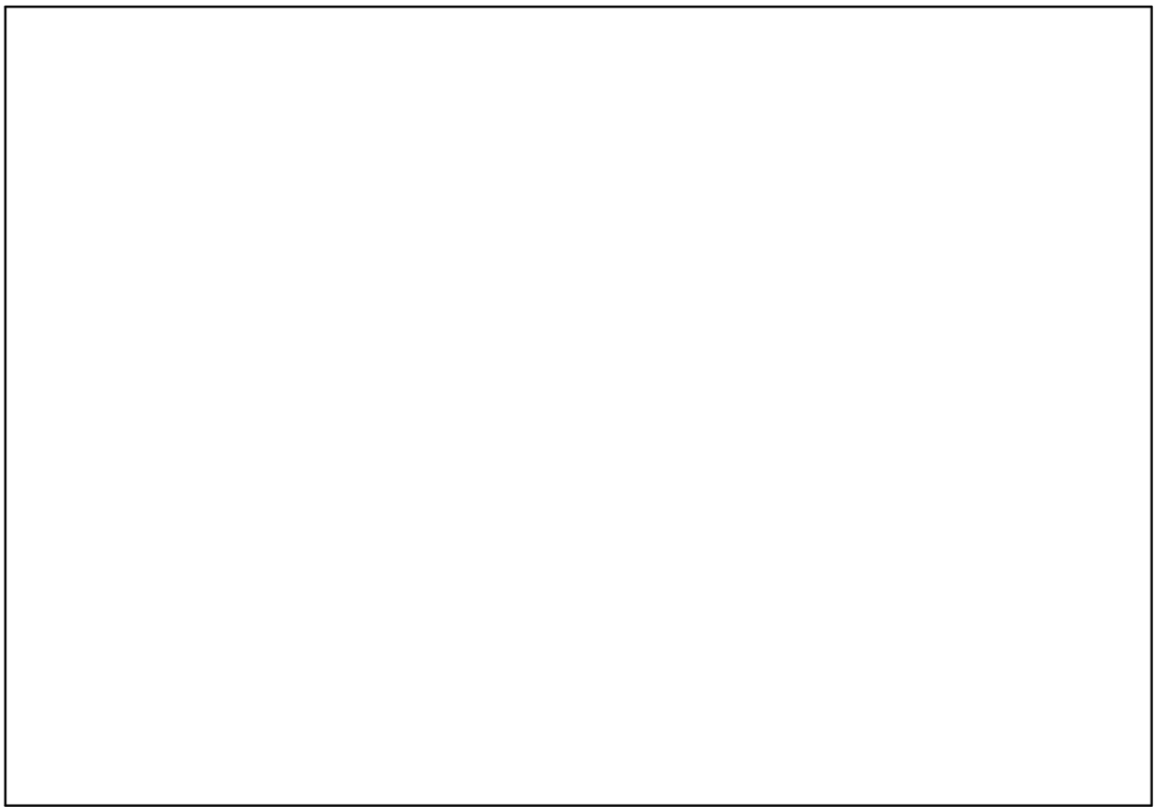


Figure 4-11. JFE150EVM Bottom Overlay

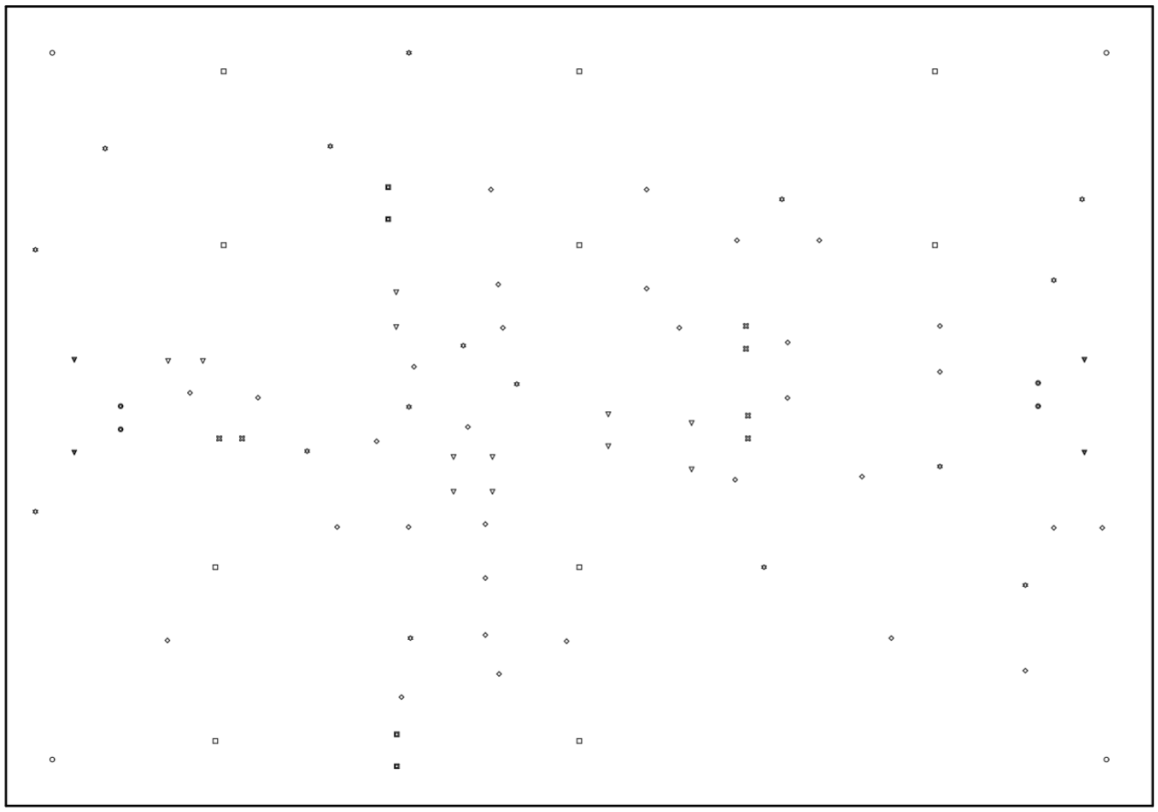


Figure 4-12. JFE150EVM Drill Drawing

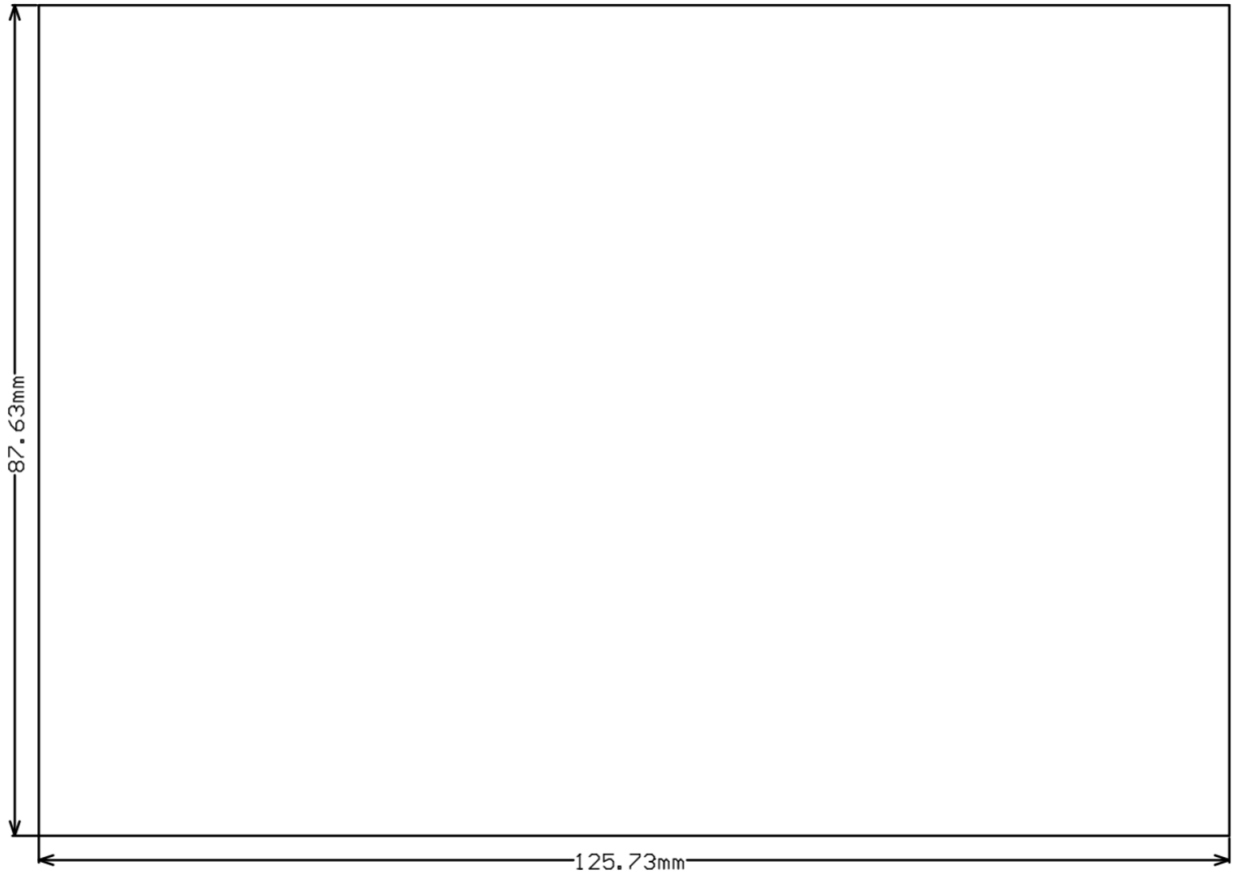


Figure 4-13. JFE150EVM Board Dimensions

4.3 Bill of Materials

Table 4-1 lists the complete bill of materials for the JFE150EVM. Data for each component is available from the corresponding manufacturer's web site.

Table 4-1. JFE150EVM BOM

Designator	Quantity	Value	Description	PartNumber	Manufacturer
C1, C4	2	100uF	CAP, AL, 100 uF, 50 V, +/- 20%, 0.17 ohm, TH	50YXJ100MT78X11.5	Rubycon
C2, C5, C9	3	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 0805	08055C104JAT2A	AVX
C6, C8, C16	3	10µF	Cap Aluminum 10uF 50V 20% (6.3 X 11.2mm) Radial 2.5mm 50mA 2000 hr 85C Bulk	ECE-A1HN100U	Panasonic
C11	1	470µF	470 µF 16 V Aluminum Electrolytic Capacitors Radial, Can - 2000 Hrs @ 85°C	ECA-1CM471	Panasonic
C12	1	10uF	CAP, Tantalum Polymer, 10 µF, 35 V,+/- 20%, 0.2 ohm, 3528-21 SMD	TCJB106M035R0200	AVX
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone
J1, J2, J3, J4, J5, J8, J9, J10, J11, J12	10		Standard Banana Jack, Uninsulated, 5.5mm	575-4	Keystone
L1, L2	2	100uH	Wire Wound Ferrite Inductor for Power Lines 100µH ±10% 15.6 Ohm 80mA 1206	LQH31CN101K03L	Murata
Q1	1		Ultra-Low Noise, Low-Input Bias Current, Dual, Discrete, Audio, N-Channel JFET	JFE150DCK	Texas Instruments
R2, R10	2	1.00Meg	RES, 1.00 M, 0.1%, 0.125 W, 0805	RG2012P-105-B-T5	Susumu Co Ltd
R3	1	4.02k	RES, 4.02 k, 0.1%, 0.125 W, 0805	RT0805BRD074K02L	Yageo America
R6	1	49.9	RES, 49.9, 0.5%, 0.1 W, 0805	RR1220Q-49R9-D-M	Susumu Co Ltd
R8	1	10.0k	RES, 10.0 k, 0.1%, 0.125 W, 0805	RG2012P-103-B-T5	Susumu Co Ltd
R12	1	300	RES, 300, 0.1%, 0.125 W, 0805	RG2012P-301-B-T5	Susumu Co Ltd
R15	1	10.0	RES, 10.0, 0.1%, 0.1 W, 0805	CRT0805-BY-10R0ELF	Bourns
R16, R17	2	110k	RES, 110 k, 0.1%, 0.125 W, 0805	RG2012P-114-B-T5	Susumu Co Ltd
R18, R20, R22, R23, R25, R26, R27	7	0	RES SMD 0 OHM JUMPER 1/8W 0805	RC0805FR-070RL	Yageo

Table 4-1. JFE150EVM BOM (continued)

Designator	Quantity	Value	Description	PartNumber	Manufacturer
R32	1	1.00k	RES, 1.00 k, 0.1%, 0.125 W, 0805	RG2012P-102-B-T5	Susumu Co Ltd
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	16		Test Point, Multipurpose, Black, TH	5011	Keystone
U2	1		General Purpose Amplifier 1 Circuit Rail-to-Rail 8-SOIC	OPA202ID	Texas Instruments
Vin, Vout	2		Connector, BNC, Jack, 50 ohm, Gold, R/A, TH	1-1634612-0	TE Connectivity
C3	0	47pF	CAP, CERM, 47 pF, 50 V, +/- 5%, C0G/NP0, 0805	C0805C470J5GACTU	Kemet
C7, C10	0	100uF	CAP, Tantalum Polymer, 100 uF, 20 V, +/- 20%, 0.055 ohm, 7.3x4.3mm SMD	20TQC100MYF	Panasonic
C13, C15	0	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 0805	08055C104JAT2A	AVX
C14	0	10uF	CAP, Tantalum Polymer, 10 µF, 35 V,+/- 20%, 0.2 ohm, 3528-21 SMD	TCJB106M035R0200	AVX
R1, R5, R11	0	1.00Meg	RES, 1.00 M, 0.1%, 0.125 W, 0805	RG2012P-105-B-T5	Susumu Co Ltd
R4, R7	0	350	Res Metal Foil 350 Ohm 0.01% 3/5W ±2ppm/°C Molded RDL Thru-Hole Bulk	Y0007350R000T9L	Vishay
R9, R14	0	10	Res Metal Foil 10 Ohm 0.05% 3/5W ±2ppm/°C Molded RDL Thru-Hole Bulk	Y000710R0000A9L	Vishay
R13	0	10k	Res Metal Foil 10K Ohm 0.01% 0.6W Molded RDL Bulk	Y078510K0000T9L	Vishay
R21	0	110k	RES, 110 k, 0.1%, 0.125 W, 0805	RG2012P-114-B-T5	Susumu Co Ltd
R24	0	348	348 Ohms ±0.1% 0.125W, 1/8W Chip Resistor 0805 (2012 Metric) Automotive AEC-Q200 Thin Film	ERA-6AEB3480V	Panasonic Electronic Components
R28, R29, R30, R31	0	0	RES SMD 0 OHM JUMPER 1/8W 0805	RC0805FR-070RL	Yageo

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265