Application Report
SLUA982–July 2019

Debugging UCC28780 ACF Converter Start-up Issues

ABSTRACT

This application note provides a step-by-step debugging process to help designers tackle any UCC28780 active clamp flyback (ACF) converter start-up issues. In this application note, possible start-up issues are described and proper solutions and tips for each issue are presented.

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1 Introduction

This application note presents a step-by-step debug process to help designers debug their UCC28780 high-frequency active clamp flyback (ACF) converters in an efficient manner. In this application note, the most basic issues and their corresponding solutions are covered first, then more difficult ones are tackled.

Figure 1 illustrates a typical converter circuit diagram of the UCC28780 high-frequency ACF converter.

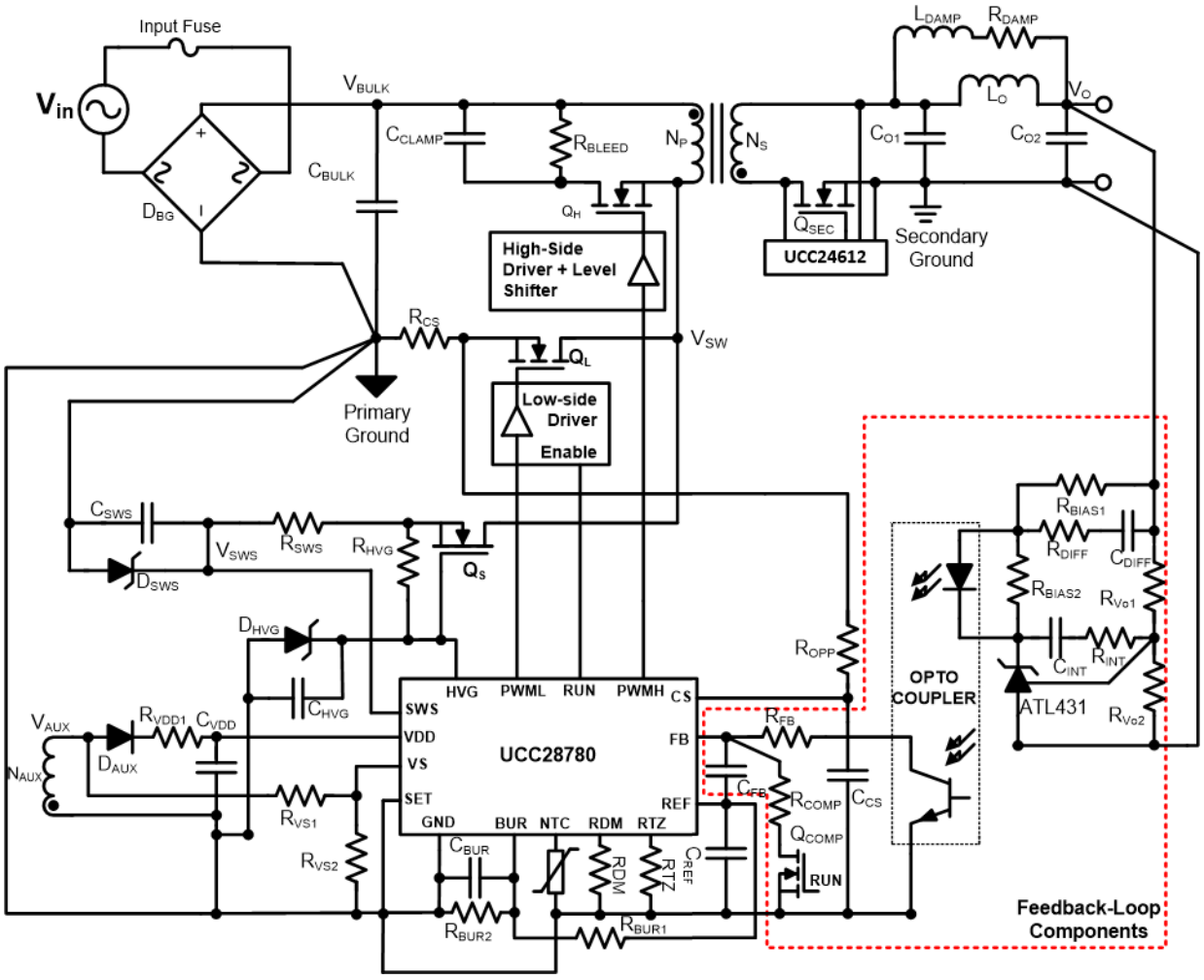

Figure 1. Typical Circuit Diagram of the UCC28780 High-frequency ACF Converter

2 Check-List Table and Debugging Flowchart

To help designers follow a systematic debugging process, this application note provides a troubleshooting list, as shown in Table 1. In this table, the debugging process is organized by the following:

- Steps
- Actions
- Symptoms
- Possible causes
- Solutions
- Section numbers for reference to detail

Additionally, to further help designers have a quick access to a step-by-step power-up debug process, Figure 2 presents a flowchart of the process. The flowchart provides four main steps including the following:

- Input short-circuit investigation
- Initial start-up investigation
- PWML pulse investigation
- Output regulation investigation

Table 1. A Systematic Troubleshooting Process List (1)

STEP	ACTION	SYMPTOM	POSSIBLE CAUSE	PROCESS/SOLUTION	SECTION
1	Design review and visual inspection	Visible defect	• Missing and broken components • Bad solder joints and connections • Backward installation • Improper values	• Mathcad/Excel Design calculator • Ensure components populated properly. • Inspect all solder joints. • Check board vs. BOM and SCH.	Section 3
2	Short-circuit investigation: Vin = 5 V_{rms}	High input current	• Unintended low impedance in primary circuit	• Set up input current limit before starting. • Check primary-side of board for shorts and failed components.	Section 4
3	Initial start-up investigation: Vin = 25 V_{rms}	No switching	• V_{VDD} < $V_{VDD(on)}$ = 17.5 V • V_{SWS}, V_{HVG}, or V_{SW} = 0 V • RUN or REF = 0 V	• Check VDD, SWS, HVG, RUN, REF, and SW. • Check Qs (BSS126) and UCC28780 controller for damage. • Check input circuit loop.	Section 5
4	Number of PWML pulse investigation: Vin = 0.5 V_{BI} (V_{BI} = Input Brown-in Voltage)	0 or 1 PWML	• High transformer primary inductance • Too low Input voltage • Open or short critical pins	• Ensure no critical pins CS, HVG, RDM, RTZ short or open. • Increase input voltage to 90% of V_{BI}: check Equation 1. • Add offset voltage to CS pin. • Decrease transformer primary inductance.	Section 6.1
		3 PWML	• Incorrect transformer polarity • Triggered system fault protection: Table 4 CS pin open • Large capacitor on NTC pin	• Ensure corrected transformer polarities. • Increase input voltage 90% of V_{BI}: check Equation 1. • Add offset voltage to CS pin. • Decrease transformer primary inductance.	Section 6.2
		4 PWML	**Initial checks are complete. Check Table 5 and Table 6 for output regulation issues.**		Section 6.3

(1) If any component is changed in the converter, the converter parameters require to be re-tuned accordingly. For the main difference between GaN and Si MOSFETs, refer to Section 8.

Table 1. A Systematic Troubleshooting Process List [(1)] (continued)

STEP	ACTION	SYMPTOM	POSSIBLE CAUSE	PROCESS/SOLUTION	SECTION
5	Output regulation investigation: V_{in} = 1.1 V_{BI} (V_{BI} = Input Brown-in Voltage)	Start-up failure	• High level noise at CS pin	• Add a capacitor between CS pin and GND up to 300 pF.	Section 7.1
			• VDD voltage drop below UVLO-OFF	• Increase, C_{VDD}, capacitor across VDD pin. • Increase turns-ratio of the auxiliary winding N_{AUX}: check Equation 2.	Section 7.3
			• VDD clamped too low	• Check for loading from other circuitries, such as drive stages. • Replace the auxiliary winding diode D_{AUX} with fast reverse recovery. • Replace the TVS diode D_{HVG} with higher clamping voltage. • Check other leakage paths from VDD or SWS to GND. • Check the UCC28780 controller for damage.	Section 7.3
			• OCP at start-up	• Increase the capacitor C_{CS} between CS pin and GND pin. • Increase R_{OPP}.	Section 7.4
			• NTC pin capacitance	• Remove/decrease capacitor on NTC pin.	Section 7.5
		OVP fault	• Improper voltage divider resistors • Improper transformer turns ratio	• Check resistors R_{Vo1}, R_{Vo2}, R_{VS1}, and R_{VS2} to verify design. • Check transformer turns-ratio from V_o to V_{AUX} to verify design. • Increase OVP threshold.	Section 7.6
			• Improper feedback loop	• Ensure all components in feedback loop are properly connected. • Check R_{FB} for proper range: 20 kΩ–39 kΩ. • Add a resistor R_{FC} in parallel with C_{FB}.	Section 7.8
			• Transition from LPM to ABM	• Slightly increase OVP threshold or RDM.	Section 7.7
		Lack of voltage regulation	• Damaged Q_S (BSS126)	• Measure voltage across R_{SWS}. • Ensure body-diode forward current of BSS126 less than 50 mA. • Reduce C_{SWS} but not lower than 15 pF. • Increase R_{SWS} but not higher than 400 Ω. • Add a capacitor (2.2 nF) between the gate of the BSS126 and GND.	Section 7.9
			• High MOSFET turn-ON/-OFFslew rate (dv/dt)	• Add an external capacitor between gate and source MOSFET. • Increase gate resistor R_G. • Increase R_{PWM}, but not higher than 300 Ω.	Section 7.10
			• High noise level	• Minimize all loop areas. • Separate power ground and signal ground. • Use Kelvin connection for current sensing traces and Optocoupler output. • Avoid overlap between the switch-node copper and GND copper. • Avoid GND copper on RDM, RTZ, VS, and R_{VS2}.	Section 9

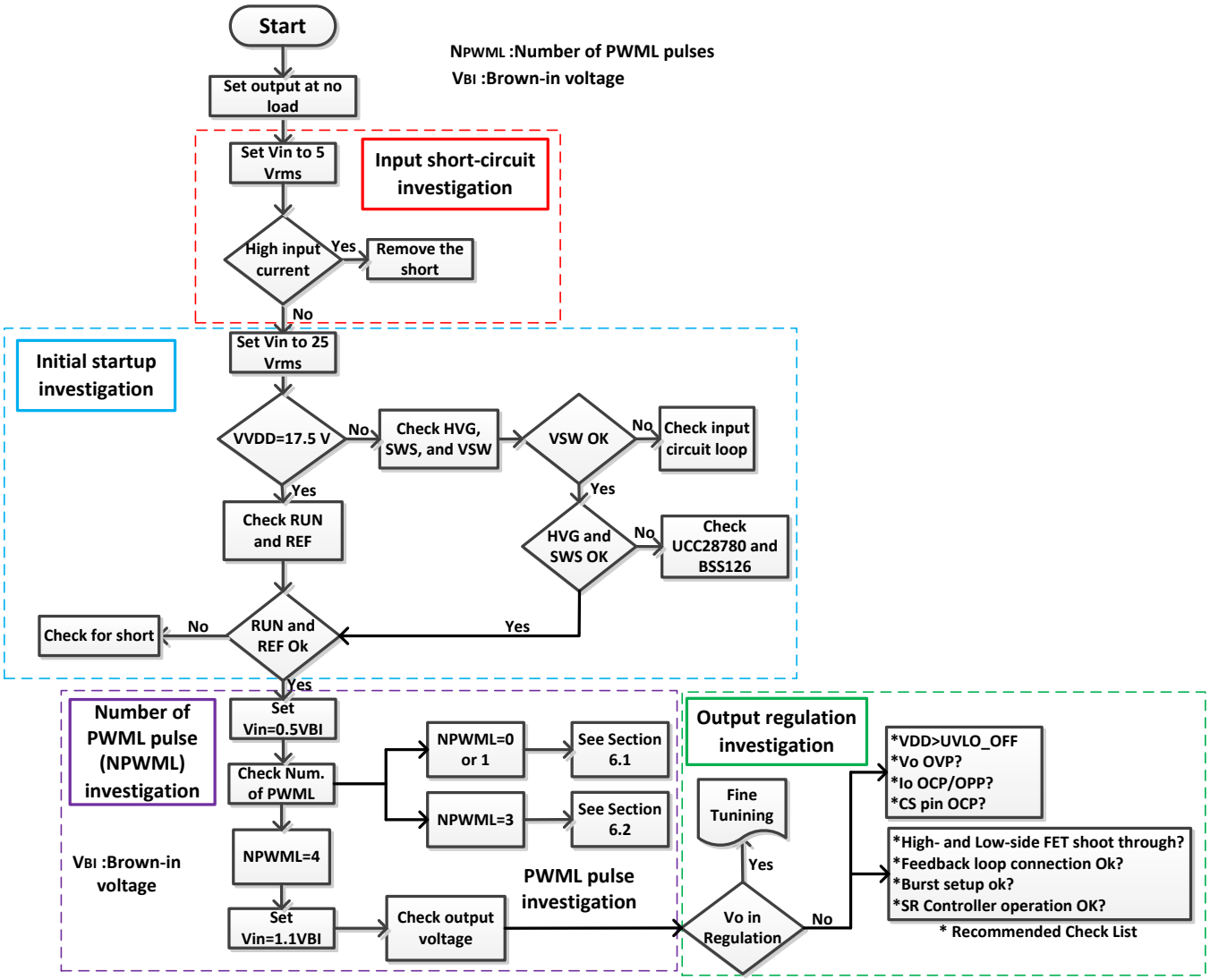

Figure 2. A Procedural Debugging Flowchart for Power-up Process

3 Design Review and Visual Inspection

Before powering up the design board, the first step is to thoroughly review the design to make sure all design parameters are calculated properly. The design calculation tools, such as the Mathcad design calculator or Excel design calculator are helpful tools to investigate the accuracy of the design. Afterwards, it is recommended to do a visual inspection to check for the following:

- Solder bridges
- Solder balls
- Solder skips
- Cold solder joints
- Lifted pads

Also, verify that the correct components are used. For example, the *ISO7710F* is the correct isolator to use instead of the *ISO7710* in case a TI isolator is used. Table 2 provides a list of typical design values for several critical parameters, which can be used as a reference to compare to those of a new design. If a component value is far away from the recommended value in Table 2, it is suggested to recalculate the value to verify that it is correct. Designers are also encouraged to check additional resources in Section 10 for further information.

Table 2. Typical Design Values for 20-V Output

POWER	Q_L, Q_H	Lm	CORE SIZE	NP/Ns	N_P/N_A	C_{Clamp}	C_{o1}
27W	GaN	120 µH	RM6	6.4	7.0	0.44 µF	32 µF
45 W	GaN	115 µH	RM8/ILP	5.2	7.1	0.66 µF	66 µF
65 W	GaN	80 µH	RM8	5.5	4.4	0.44 µF	66 µF
27 W	Si	TBD	TBD	TBD	TBD	TBD	TBD
45 W	Si	115 µH	RM8/ILP	5.2	7.1	0.44 µF	66 µF
65 W	Si	110 µH	RM8	5.0	5.0	0.88 µF	88 µF
POWER	**Q_L, Q_H**	**R_{RTZ}**	**R_{RDM}**	**R_{BUR1}**	**R_{BUR2}**	**R_{COMP}**	**UCC24612 VERSION**
27 W	GaN	300 kΩ	68.0 kΩ	200 kΩ	51.0 kΩ	510 kΩ	UCC24612-1
45 W	GaN	249 kΩ	84.5 kΩ	196 kΩ	63.4 kΩ	750 kΩ	UCC24612-1
65 W	GaN	221 kΩ	82.5 kΩ	191 kΩ	56.2 kΩ	510 kΩ	UCC24612-1
27 W	Si	TBD	TBD	TBD	TBD	TBD	UCC24612-1 or 2
45 W	Si	280 kΩ	95.3 kΩ	196 kΩ	47.5 kΩ	604 kΩ	UCC24612-1 or 2
65 W	Si	130 kΩ	110 kΩ	200 kΩ	47.0 kΩ	500 kΩ	UCC24612-1 or 2

4 Input Short-Circuit Investigation

1. Disconnect the load at the output.
2. Set voltage of the input voltage source to V_{in} = 5 V_{rms} while limiting its current to 0.5 A.
3. Measure the input current.

After a brief, low inrush peak, there should be almost zero continuous input current. If an excessive current is observed, there is a short or abnormally low impedance in the circuit. The cause needs to be determined, and the short must be removed before proceeding.

5 Initial Start-up Investigation

Once the previous steps are complete, the board can be partially powered with no load at its output. Figure 3 illustrates the initial start-up operation, which is defined as operation of the converter from t_0 -t_4. This section explains possible start-up issues of the converter at the initial start-up stage where low input voltage is applied at the input-side, but no voltage is observed at the output. In this stage, since the maximum allowable voltage of VDD is 38 V, it is recommended to set the converter input voltage on 25 V_{rms}. This can help avoid damaging the UCC28780 controller in case there is a misconnection in the controller path. The process shown in Table 1, step 3, and the flowchart (see Figure 2) for the initial start-up investigation can be followed to debug the system in this stage. In order to be able to proceed with further debugging, this troubleshooting step must be completed to have both REF and RUN rise to 5 V.

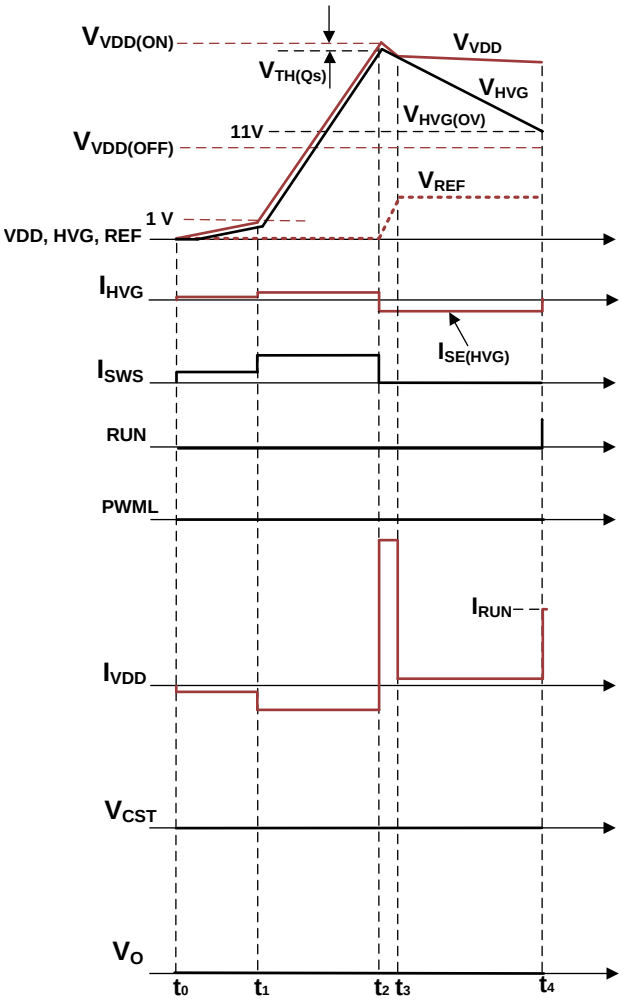

Figure 3. Behavior of the Converter at Initial Start-up Stage

6 Number of PWML Pulse Investigation

The expected behavior of the converter after passing the initial start-up stage is demonstrated in Figure 4. As shown in this figure, after RUN rises to 5 V, the controller enters a run state at time t_4. At time t_5, with both REF and RUN at 5 V, the low-side switch Q_L starts switching. The number of PWML pulses of Q_L in interval t_5–t_6 can be used as an indicator to diagnose the initial power stage issues of the converter. The observed number of PWML pulses during interval t_5–t_6 can be zero, one, three, or four depending on the failure or success scenario.

The following subsections describe the origins and remedies of each scenario based on the observed number of pulses. For debugging purposes, it is recommended to set the input voltage V_{in} at 50% of brown-in voltage V_{BI} for this investigation step.

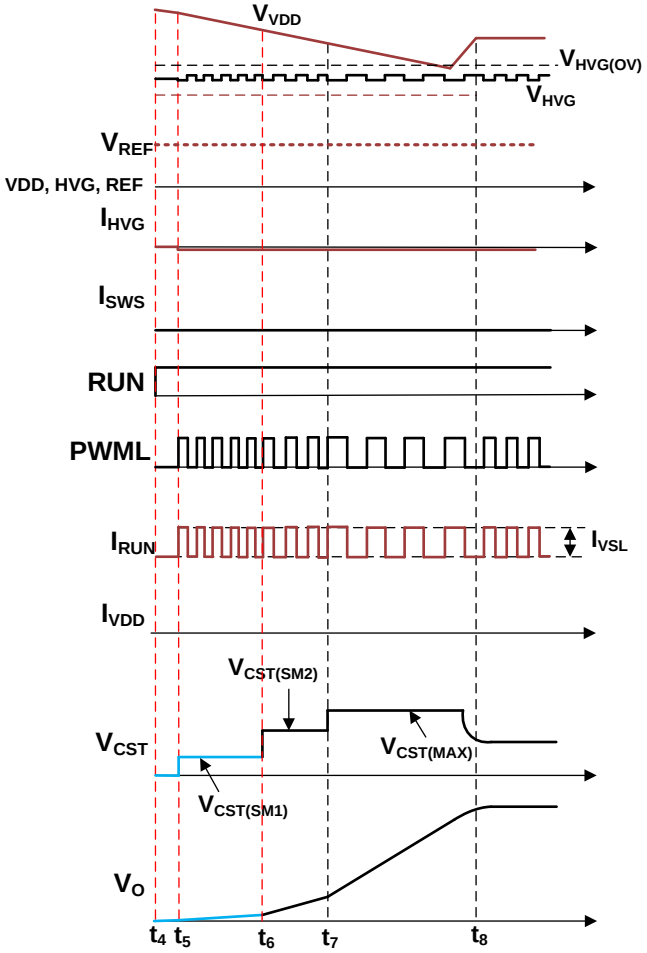

Figure 4. Behavior of Converter at Initial Power Stage

6.1 Observation of Zero or Only One PWML Pulse

In case one or no PWML pulse during interval t_5–t_6 is observed, it is likely that critical pins may be open or shorted. Table 3 summarizes these possibilities. Investigate each one to debug this.

Table 3. Possible System Fault Protection Occurrence Under Observation of One PWML Pulse or No Pulse

PROTECTION	SENSING	CONDITION	BEHAVIOR	ACTION
CS pin short	PWML on-time at first PWML pulse only	> 2 µs (SET= 5 V)	1 PWML pulse only	ULVO reset
		> 2 µs (SET= 0 V, R_{RDM} ≥ 55 kΩ)		
		> 1 µs (SET= 0 V, R_{RDM} < 55 kΩ)		
HVG pin open	HVG current at $UVLO_{ON}$	V_{HVG} ≤12 V in less than 10 µs after V_{VDD} reaches $V_{VDD(ON)}$	None	ULVO reset
HVG pin high	HVG voltage	V_{HVG} > 14 V	None	ULVO reset
RDM pin short	RDM current at $UVLO_{ON}$	V_{RTZ} = 0 V, self-limited i_{RDM}	None	ULVO reset
RDM pin open	RDM current at $UVLO_{ON}$	RDM = Open	None	ULVO reset
RTZ pin short	RDM current at $UVLO_{ON}$	V_{RTZ} = 0 V, self-limited i_{RTZ}	None	ULVO reset
RTZ pin open	RDM current at $UVLO_{ON}$	RTZ = Open	None	ULVO reset

If only one PWML pulse with a width of 2 µs is observed, three main possibilities may exist.

- CS pin is shorted to GND. If this is the case, the issue can be resolved by removing the short.
- Input voltage is too low. Increase the input voltage to 90% of brown-in voltage V_{BI} or calculate the required input voltage with Equation 1.

$$V_{in} = L\frac{\Delta I}{\Delta t} = Lp\frac{(V_{RCS}/R_{CS})}{\Delta t} \approx Lp\frac{(V_{CST(SM1)}/R_{CS})}{2\times10^{-6}s} = Lp\frac{(0.28V/R_{CS})}{2\times10^{-6}s} \quad (1)$$

where

  - R_{CS} and V_{RCS} are current-sense resistor and voltage across R_{CS}, respectively

- Transformer primary inductance, L_p, is high (L_p > 100 µH). In this case, the issue can be resolved by adding an offset voltage to CS with a resistor, R_{REFCS}, between CS pin and REF pin. This can help the CS pin voltage rise quickly to reach 0.28 V in less than 2 µs. R_{REFCS} value depends on R_{OPP} and the required offset.

6.2 Observation of Only Three PWML Pulses

Incorrect transformer polarities can be one possible cause of observation of only three PWML pulses. The transformer winding polarities are required to check to make sure that they are correctly connected. Measure the voltage of the secondary and auxiliary terminals of the transformers V_{AB} and V_{CD} while Q_L is ON, as illustrated in Figure 5. If V_{AB} and V_{CD} are measured as negative during Q_L on-time, the transformer polarities are correct; otherwise, the transformer polarities are required to be corrected.

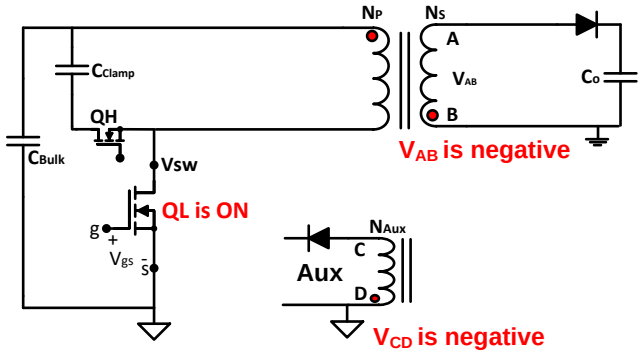

Figure 5. Transformer Test Showing Correct Polarities

Table 4 lists other possible root causes of observing only three PWML pulses at the initial power stage during time interval t_5–t_6. Each possibility should be investigated.

Table 4. Possible System Fault Protection Occurrence Under Observation of Three PWML Pulses

PROTECTION	SENSING	THRESHOLD	DELAY TO ACTION	ACTION
Over-current protection	CS voltage	V_{CST} ≥ 1.2 V	3 PWML pulses	1.5 s restart
Output over-voltage protection	VS voltage	V_{VS} ≥ 4.6 V	3 PWML pulses	1.5 s restart
Brown-in protection	VS current	I_{VSL} < 353 µA	3 PWML pulses	UVLO reset
Over-temperature protection (OTP)	NTC voltage	R_{NTC} ≤ 10 kΩ	3 PWML pulses	VDD restart until R_{NTC} ≥ 10 kΩ
Thermal shutdown	Junction temperature	Tdie > 125°C	3 PWML pulses	UVLO reset
CS pin open	CS voltage	V_{CS} ≥ 1.2 V	3 PWML pulses	1.5 s restart
HVG pin over-voltage	HVG voltage	V_{HVG} ≥ 13.8 V	3 PWML pulses	UVLO reset

6.3 Observation of Only Four PWML Pulses

If four PWML pulses are observed in time interval of t_5–t_6, the initial checks are complete. Now the converter is ready to be tested in the normal operation. Figure 6 illustrates PWML waveform and voltage at CS (V_{CS}) when four PWML pulses are observed.

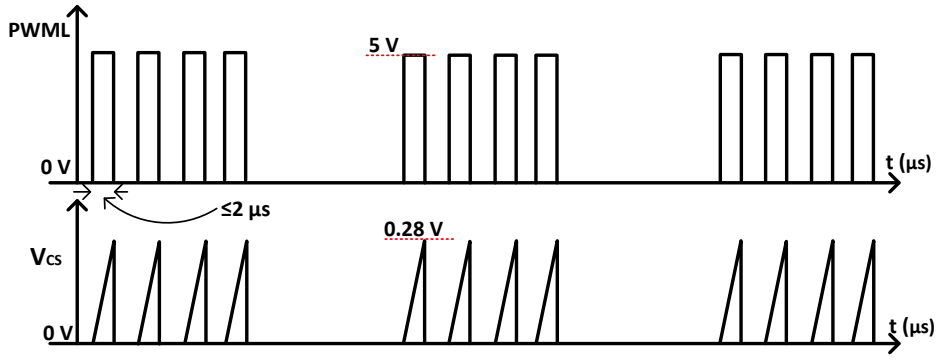

Figure 6. PWML Waveform Along with V_{CS} When Four PWML Pulses Are Observed

7 Output Regulation Investigation

After four PWML pulses are observed, increase the input voltage, V_{in}, to be higher than brown-in voltage, V_{BI} (for example, V_{in} = 1.1 V_{BI}), under no-load condition. The output voltage should be in regulation. If this is the case, the converter is functioning properly. However, if the converter is not in regulation, check the input voltage to make sure it is high enough. If this is verified, then there may be one or more system-level faults to prevent the output voltage from regulation. Table 5 lists all system fault protections. Table 6 shows all open/short fault protections of critical pins. This section describes the most common root causes and remedies of start-up failure and lack of output voltage regulation after observing four PWML pulses.

Table 5. System Fault Protection

PROTECTION	SENSING	THRESHOLD	DELAY TO ACTION	ACTION
VDD UVLO	VDD voltage	$V_{VDD(OFF)} \le V_{VDD} \le V_{VDD(ON)}$	None	UVLO reset
Over-power protection (OPP)	CS voltage	$V_{CST(OPP)} \le V_{CST} \le V_{CST(MAX)}$	t_{OPP} (160 ms)	t_{FDR} restart (1.5 s)
Peak current limit (PCL)	CS voltage	$V_{CST} \le V_{CST(MAX)}$		
Over-current protection (OCP)	CS voltage	$V_{CS} \ge V_{OCP}$	3 PWML pulses	t_{FDR} restart
Output short-circuit protection (SCP)	CS, VS, and VDD voltages	(1)$V_{VDD} = V_{VDD(OFF)}$ and $V_{CST} \ge V_{CST(OPP)}$; (2) $V_{VDD} = V_{VDD(OFF)}$ and $V_{VS} \le$ 0.6 V	$\le t_{OPP}$	t_{FDR} restart
Output over-voltage protection (OVP)	VS voltage	$V_{VS} \ge V_{OVP}$	3 PWML pulses	t_{FDR} restart
Brown-in detection	VS current	$I_{VSL} \le I_{VSL(RUN)}$	4 PWML pulses	UVLO reset
Brown-out detection	VS current	$I_{VSL} \le I_{VSL(STOP)}$	t_{BO} (60 ms)	UVLO reset
Over-temperature protection (OTP)	NTC voltage	$R_{NTC} \le R_{NTCTH}$	3 PWML pulses	UVLO reset until $R_{NTC} \ge R_{NTCR}$
Thermal shutdown	Junction temperature	$T_J \ge T_{J(STOP)}$	3 PWML pulses	ULVO reset

Table 6. Protections for Open and Short of Critical Pins

PROTECTION	SENSING	THRESHOLD	DELAY TO ACTION	ACTION
CS pin short	PWML on-time at first PWML only	> 2 µs (V_{SET} = 5 V)	None	t_{FDR} restart (1.5 s)
		> 2 µs (V_{SET} = 0 V, $R_{RDM} \geq R_{RDM(TH)}$)		
		> 1 µs (V_{SET} = 0 V, $R_{RDM} < R_{RDM(TH)}$)		
CS pin open	CS voltage	$V_{CS} \geq V_{OCP}$	3 PWML pulses	t_{FDR} restart (1.5 s)
HVG open	HVG voltage at $UVLO_{ON}$	V_{HVG} drops to 12 V within 10 µs	None	UVLO reset
HVG pin over-voltage	HVG voltage	$V_{HVG} \geq V_{HVG(OV)}$	3 PWML pulses	UVLO reset
RDM pin short	RDM current at $UVLO_{ON}$	V_{RDM} = 0 V, self-limited I_{RDM}	None	UVLO reset
RDM pin open	RDM current at $UVLO_{ON}$	RDM = Open	None	UVLO reset
RTZ pin short	RTZ current at $UVLO_{ON}$	V_{RTZ} = 0 V, self-limited I_{RTZ}	None	UVLO reset
RTZ pin open	RTZ current at $UVLO_{ON}$	RTZ = Open	None	UVLO reset

7.1 Start-up Failure Due to High Level Noise at CS Pin

A high level of noise at the CS pin can trigger the CS pin fault, causing narrow PWML pulses (approximately 130 ns). A larger capacitor (up to 330 pF) between the CS pin and GND can be used to attenuate the level of noise. However, a larger value of this capacitor increases OPP and OCP levels, due to associated longer turn-off delay.

7.2 Start-up Failure Due to VDD Drop below $VDD_{(OFF)}$

In two different possible scenarios, VDD drops below $VDD_{(OFF)}$ (= 9.8 V) after reaching its $VDD_{(ON)}$ (= 17.5 V).

- The first scenario is that the capacitor across VDD pin, C_{VDD}, is not adequate to store enough energy to maintain bias for the UCC28780 controller before the auxiliary supply takes over to bias the UCC28780 controller.
- The second scenario is that the turns-ratio N_{AS} of the auxiliary winding N_{AUX} to the secondary winding N_S is not adequate.

For either scenario, the same approach can be considered to resolve this issue. Figure 7 demonstrates VDD and output voltage during the start-up operation. At time instant t_{G1}, output voltage reaches V_{O1}, which is lower than targeted output voltage V_{OC}. The auxiliary bias takes over C_{DD} bias at t_{G1}. At this point, V_{VDD} is equal to $V_{VDD1} = (N_{AUX} / N_S) \times V_{O1}$. To avoid the start-up issue, V_{VDD1} should be higher than $V_{VDD(OFF)}$. Moreover, tolerance of other circuit parameter variations should be considered. In order to resolve this issue this way, Equation 2 should be valid.

$$N_{AS} = \left(\frac{\text{Naux}}{N_S}\right) \geq 1.25 \times \left(\frac{V_{\text{VDD (OFF)}}}{V_{oc}}\right) \quad (2)$$

Although a lower percentage ($V_{o1} / V_{oc} \leq 80\%$) can help the start-up process, it adds a steady-state bias to VDD at higher voltages, which can impose limitations on the UCC28780 controller and other devices. Therefore, a trade-off should be made. It is suggested to start with V_{o1} / V_{oc} = 80%.

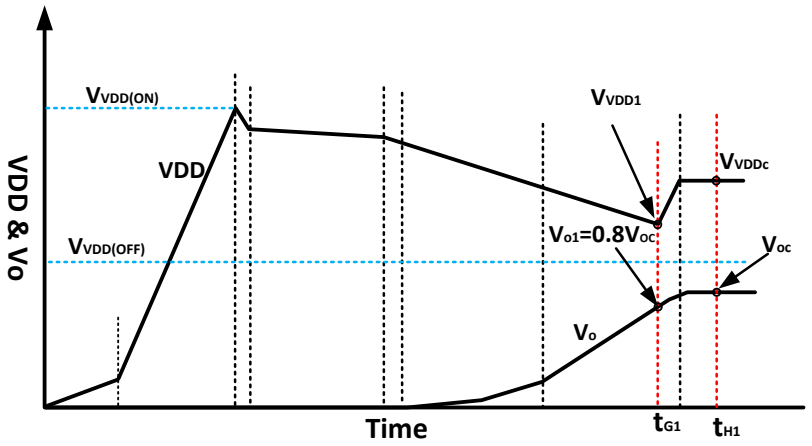

Figure 7. VDD and Output Voltage During Initial and Build-up Power Stages

7.3 Start-up Failure Due to VDD Clamped Low

Figure 8 illustrates a typical start-up configuration of VDD, REF, SWS, and HVG pins and current paths. If VDD is clamped to a voltage lower than 17.5 V, the UCC28780 controller cannot reach its turn-ON threshold level. Therefore, the converter cannot start to operate normally. There are several possibilities for this.

- Available statup current limited by Q_S is too low. Loading from other circuitries such as drive stages, which are connected to VDD, can prevent C_{VDD} from being charged up to reach the VDD turn-ON threshold.
- Reverse current of auxiliary winding diode D_{AUX} is high so VDD may get clamped at about 9 V. To resolve this clamping issue, an auxiliary winding diode with a lower reverse leakage current should be used.
- TVS diode D_{HVG} clamps low, such as when VDD rises to 15 V and clamps at 15 V but is not able to reach 17.5 V. If this is the case, D_{HVG} clamping voltage should be adjusted properly in the range of 18 to 20 V.
- There are other leakage paths from VDD or SWS to GND. If this is the case, the leakage paths should be identified or the total bias current should be adjusted to be higher.
- The UCC28780 controller is damaged and should be replaced.

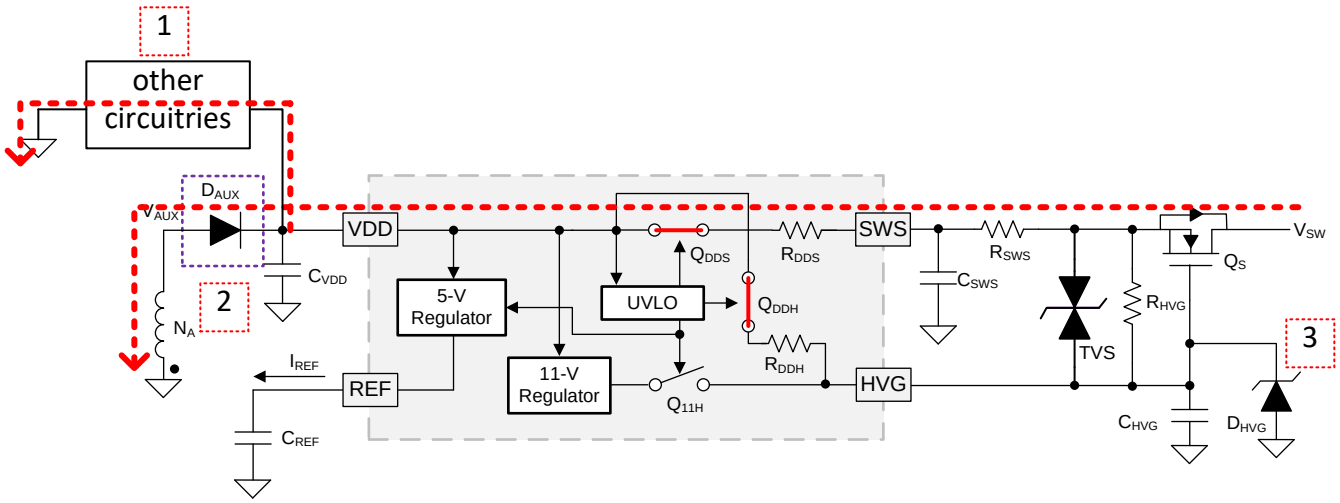

Figure 8. Typical Start-up Configuration of VDD, REF, SWS, and HVG Pins and Current Paths in Start-up

7.4 Start-up Failure Due to OCP

Figure 9 demonstrates a typical configuration of the CS pin. During the start-up process, if the CS pin sees a voltage greater than over-current protection (OCP) threshold (1.2 V), the converter start-up process is disturbed. This may happen especially during the first turn-ON time of Q_L. It is likely to have high-frequency ringings at the switch node (V_{SW}). The ringings are reflected across resistor R_{CS}, which can trigger the OCP threshold. To overcome this issue, capacitor C_{CS} between the CS pin and GND pin or R_{OPP} can be increased to attenuate the noise. However, this is realized at the cost of introducing more delay to the CS pin, consequently leading to increased set-point of OCP and OPP levels.

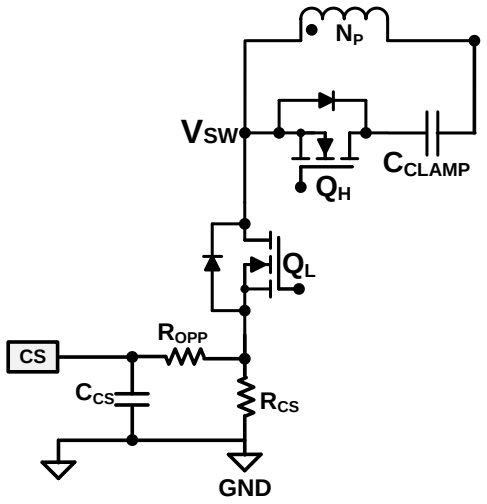

Figure 9. Typical Configuration of the CS Pin

7.5 Start-up Failure Due to NTC Pin Capacitance

In order to avoid unwanted triggering overtemperature protection (OTP) fault, make sure that within 2 µs of RUN going high, the voltage across the NTC pin V_{NTC} reaches above 1 V, as shown in Figure 10. A capacitor across the NTC pin should not be used as it can disturb this condition due to additional capacitor charging time. Therefore, avoid adding a capacitor across the NTC pin, which can trigger a fake OTP.

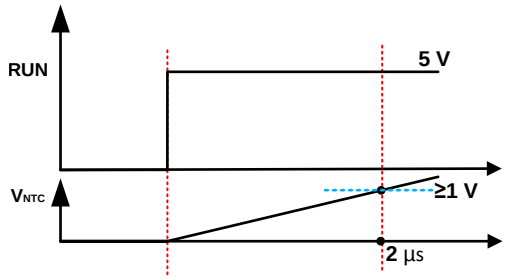

Figure 10. RUN and Voltage Across the NTC Pin

7.6 OVP Fault Due to Improper Divider to Turns-Ratio Matching

- Check voltage divider resistors R_{Vo1} and R_{Vo2} of the output voltage, voltage divider resistors of $R_{VS1}$and R_{VS2}, and the transformer turns-ratio from V_o to V_{AUX} to make sure that they are in good agreement with the intended design.
- Temporarily increase the OVP threshold by adjusting R_{VS1} or R_{VS2} to see if Vo is properly regulated. If the OVP issue is resolved, find corresponding reasons why the adjustment of R_{VS1} or R_{VS2} is needed, then fix the issue. If the output voltage cannot still get regulated, see Section 7.8 and Section 7.7.

7.7 OVP Fault Due to LPM to ABM Transition

In LPM, the high-side switch Q_H (see Figure 1) is always OFF. Therefore, the voltage across the clamping capacitor increases due to the fact that there is not a discharge path for the clamping capacitor. In this way, the very first turn-ON of Q_H during the transition from LPM to ABM results in a increased switch-node voltage (V_{SW}) as well as a high negative current in the transformer winding, due to the high voltage of the clamping capacitor. This voltage is sensed by the VS pin, and consequently the output OVP can be triggered. Figure 11 and demonstrate the PWM waveforms of Q_L and Q_H and primary transformer current (I_{LP}) during transition from LPM to ABM. Do the following to address this issue:

1. Slightly increase the OVP threshold.
2. Slightly increase RDM.
3. Select an MOSFET with proper current rating.

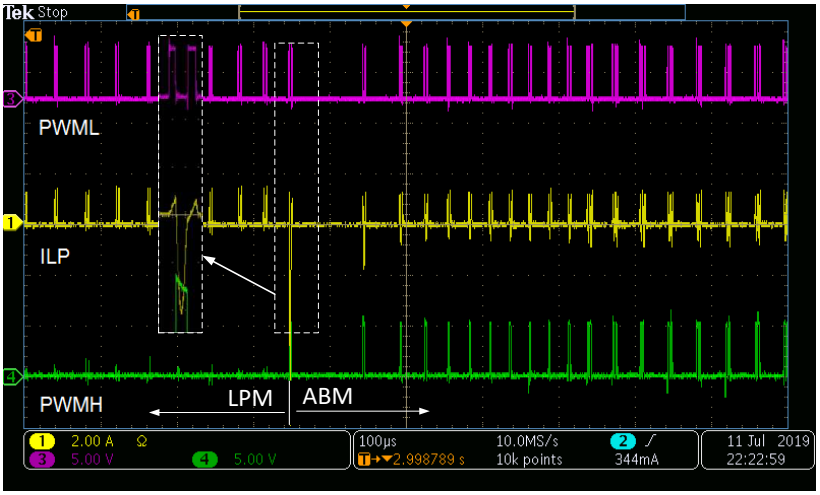

Figure 11. PWM Waveforms of Q_L, Q_H, and Transformer Primary Current in Transition from LPM to ABM

7.8 OVP Fault Due to Improper Feedback Loop

Improper feedback loop can trigger OVP fault.

1. Make sure that all the components in the feedback loop block (as shown in Figure 1) are properly designed, populated, and connected.
2. Verify R_{FB} value, which is typically between 20 kΩ and 39 kΩ, to be in proper range.
3. Replace the existing optocoupler with optocouplers such as TLP383 and FODM8801AV, which offer improved CTR characteristics, to see if the issue can be resolved. If the issue is resolved, the issue is due to low CTR of the used optocoupler.
4. Add a resistor R_{FC} in parallel with C_{FB} to help increase the CTR of the optocoupler, as shown in Figure 12. Note that this method increases standby power.

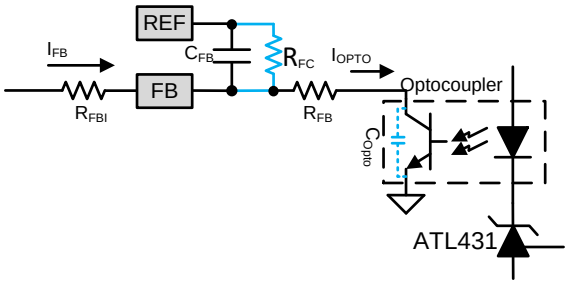

Figure 12. Mitigating Low-CTR Issue by Adding a Resistor Across C_{FB}

7.9 Depletion MOSFET BSS126 Considerations

The depletion MOSFET BSS126 under two possible conditions may fail to be functional or even get damaged.

The BSS126 may experience high body-diode reverse recovery current. Figure 13 and Figure 14 depict a typical configuration of VDD, REF, SWS, and HVG pins and current paths during turn-ON and turn-OFF of Q_L, respectively. This condition can happen when there is a high voltage slew rate during Q_L turn-OFF or a reverse current in the transformer during transient condition. The reverse recovery is related to the forward current right before the point where the reverse recovery occurs. The datasheet of BSS126 suggests maintaining the peak diode current below 64 mA. In a safe design, 20% margin for the current can be considered. Therefore, in a proper design, the peak of forward current should not exceed 50 mA.

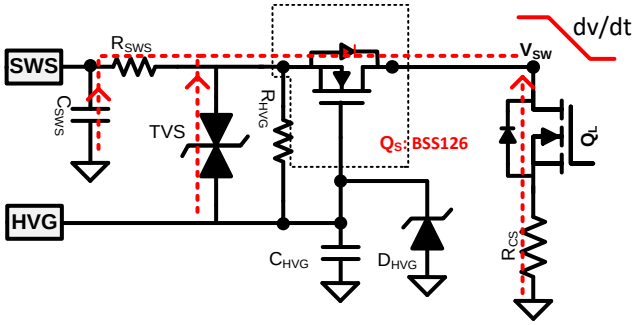

Figure 13. Typical Configuration of VDD, REF, SWS, and HVG Pins and Current Paths Under Condition of Over Stressing Switch BSS126 During Turn-ON of Q_L

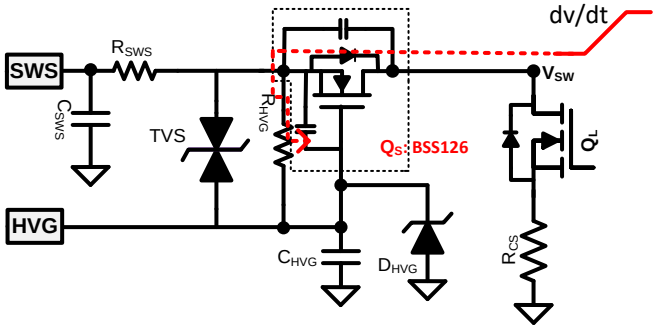

Figure 14. Typical Configuration of VDD, REF, SWS, and HVG Pins and Current Paths Under Condition of Over Stressing Switch BSS126 During Turn-OFF of Q_L

The forward current of the body-diode can be calculated by measuring voltage across R_{SWS}. Figure 15 shows the voltage across R_{SWS} and current through it during transient condition. As shown in Figure 15, the forward current of the body diode is approximately 48 mA, which is 16 mA below the maximum allowable peak current. Figure 16 represents voltage at pin SWS, switching node, and the transformer primary current in transient. The body-diode forward current is caused by discharge of C_{SWS} through R_{SWS} when V_{SW} temporarily reaches 2 V below GND owing to reverse current from the transformer through the GaN MOSFET, as shown in Figure 16. In order to reduce the forward current of the body-diode, decrease C_{SWS} or increase R_{SWS}. The bench test on the EVM shows C_{SWS} = 24 pF and R_{SWS} = 120 Ω can be effectively used. Additional margin can be added by reducing C_{SWS} ,but not lower than 15pF or increasing R_{SWS}, but not higher than 400 Ω in typical applications.

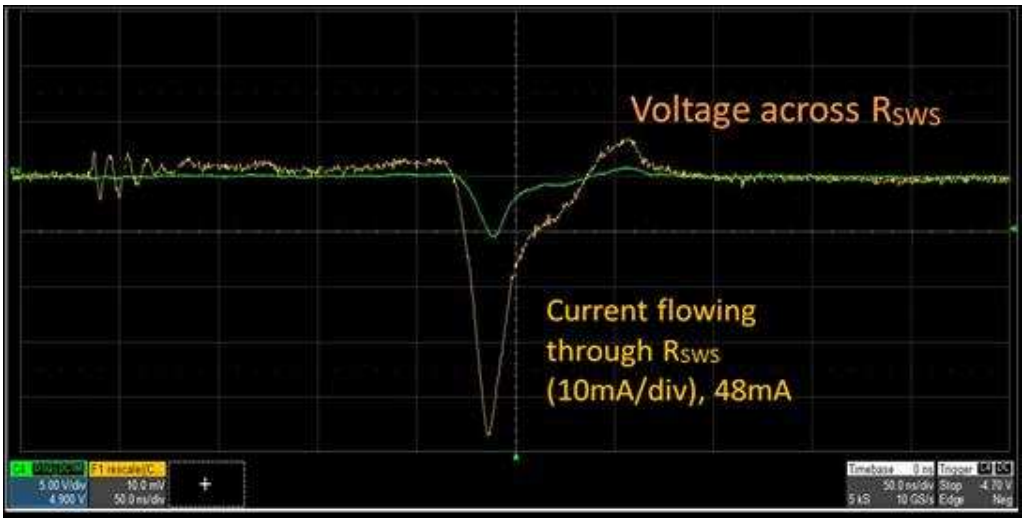

Figure 15. Voltage Across R_{SWS} and Current Through It During Transient

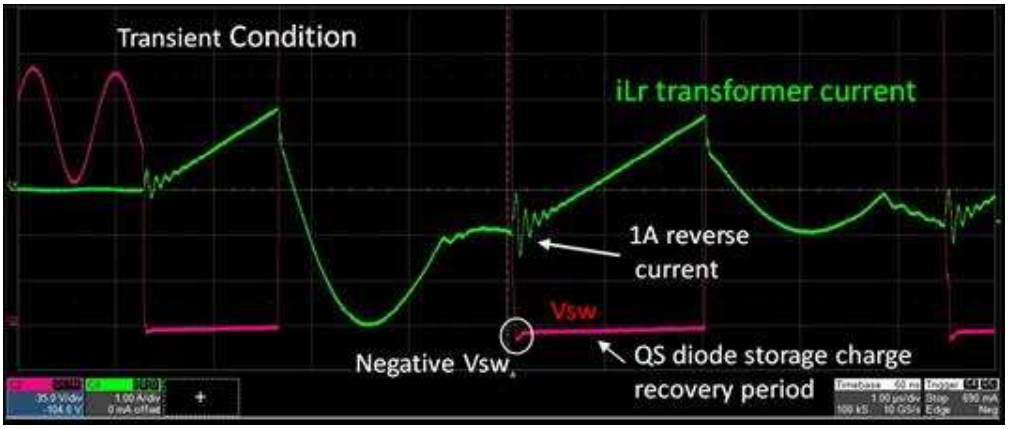

Figure 16. V_{SW} and Transformer Primary Current During Transient

The BSS126 experiences unwanted high gate to source voltage spikes due to high dv/dt during the turn-OFF of Q_L. The high gate to source voltage spikes may damage the BSS126. To avoid this damage, one way is to slow down Q_L turn-ON slew rate, which is covered in Section 7.10. Another way is to increase the applied capacitance across the BSS126 gate and GND. A typical 2.2 nF capacitance is suggested for this purpose. Another solution is to add a bi-directional TVS with clamping voltage about 16 V as shown in Figure 8.

The operation of switching the BSS126 affects voltages at the HVG pin, SWS pin, and switch-node. Consequently, additional design considerations are required to avoid possible damages on the HVG and SWS pins. Both HVG and SWS pins require voltage clamping for protection purposes due to the possible voltage spikes during the MOSFETs transient intervals with high slew rate. The clamping voltage should set up properly not only to achieve required clamping to avoid the pin failure, but also to avoid start-up issues due to clamping HVG too low.

7.10 MOSFET Turn-ON/-OFF Slew Rate Balance

The slew rate of MOSFET turn-ON/-OFF can affect Q_L, Q_H, and the BSS126. In a design using Si MOSFETs, the UCC27712 is a good selection for MOSFET drivers. A high slew rate can cause unwanted MOSFET turn-ON, as shown in Figure 17. To reduce the slew rate of a Si MOSFET, an external capacitor can be placed between gate and source of the switch or increase gate resistor value.

In the case of GaN MOSFET, the low-side GaN turn-ON speed has to be reduced in order to avoid over stress of the BSS126, and to attenuate high current spikes due to the fast turn-ON of the low-side MOSFET. Figure 18 demonstrates a simplified schematic of the NV6117 GaN switch driver (for example). A simple way to reduce the NV6117 turn-ON speed is to increase R_{PWM} (see Figure 18) up to 300 Ω but not less than 100 Ω (100Ω ≤ R_{PWM} ≤ 300Ω).

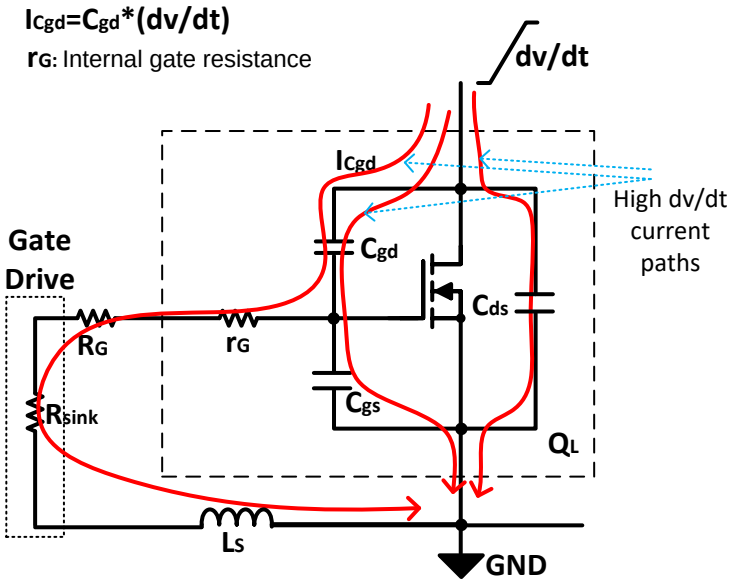

Figure 17. False Turn-ON of a Si MOSFET Under High dv/dt Event

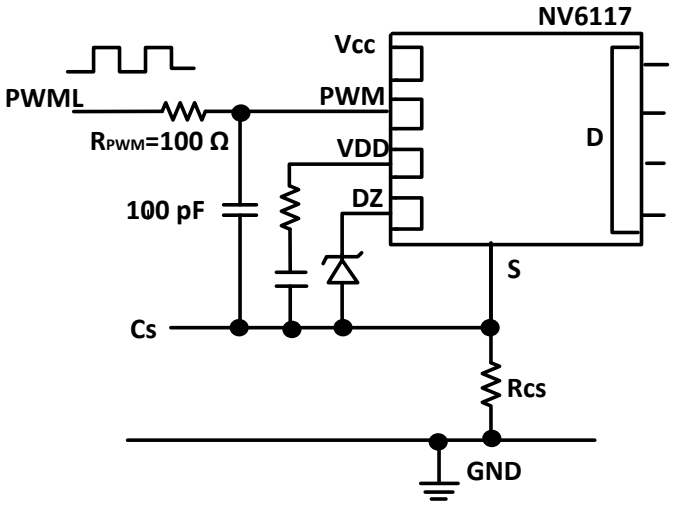

Figure 18. A Simplified Schematic of the NV6117 GaN Switch Driver

8 GaN and Si MOSFETs Difference Considerations

Gallium nitride (GaN) and silicon (Si) MOSFETs exhibit different dynamic behavior. This difference is mainly tied to the magnitude and non-linearity level of the output capacitance (C_{OSS}) of the switches. Figure 19 demonstrates a typical comparison of the C_{OSS} curve between GaN MOSFET and Si MOSFET. GaN MOSFET equivalent body-diode voltage drop can be on order of 2–4 V compared to less than 1 V of Si MOSFET body-diode. These differences affect the performance and operation of the converter. Therefore, these differences should be reflected on the design parameters of the system. In this way, the

magnetizing inductance, clamping capacitance, secondary resonant capacitance, and other design components, which are required to program the UCC28780 controller, should be designed accordingly. For example, since the C_{OSS} of a Si MOSFET is much higher than that of a GaN MOSFET, a larger value of RTZ requires to be selected when using Si MOSFETs. The design parameters can be determined using the design tools mentioned at beginning of this application note.

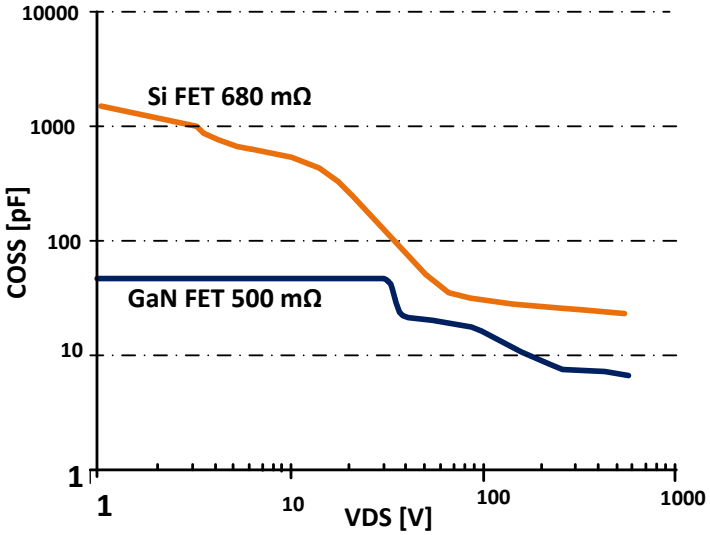

Figure 19. A Comparison of Typical C_{OSS} Between GaN MOSFET and Si MOSFET with Similar $R_{DS(ON)}$

9 Layout Considerations

The importance of creating a good board layout with a low level of noise is often overlooked by designers, but the layout can significantly affect the performance of the system. In some cases, further filtering may be required to reduce the noise of the converter to an acceptable level. However, a noisy system can be very difficult to debug. Figure 20 demonstrates a schematic of a PCB layout guideline of the converter, which emphasizes the most critical points for layout considerations.

Since any loop on the board can pick up radiated noise and convert into the conducted noise, or vice versa, a layout design should follow these general guidelines:

- All the loop areas should be minimized to reduce this effect.
- All Kelvin connections, as illustrated in Figure 20, are required to help the weak signals be immune from noise interference.
- All the labeled grounds should properly be connected as in Figure 20, but an effort should be made to make sure that current from each loop does not cross and flow through other loops or grounds.

These following key points are detailed particularly for the UCC28780:

- All loop areas should be kept to a minimum. The critical loops are demonstrated in Figure 20.
- Separate power ground and signal ground and connect them. Make sure that no power current possibly flows into the signal loop, and vice versa. If it is difficult to make sure that the current flows into the intentioned loop, a separate trace can be created to close the loop.
- GND copper should not overlap the VS pin and low-side resistor, R_{VS2}. This pin is sensitive to the GND capacitance, so the pin has high priority to eliminate GND copper.
- RDM and RTZ along with their associated resistors, RDM and RTZ, are also sensitive to the GND copper; therefore, GND copper on these pins should also be eliminated.
- Optocoupler output to the FB pin and GND pin need to use a Kelvin connection to minimize loop area and noise rejection.
- The CS pin current sensing traces are required to use a Kelvin connection.
- Avoid overlap between the switch-node copper and the GND copper to minimize the switching-node capacitance. This can help to achieve high efficiency and reduce EMI coupling.

Designers are also encouraged to see the Layout section of the UCC28780 datasheet for other critical layout guidelines.

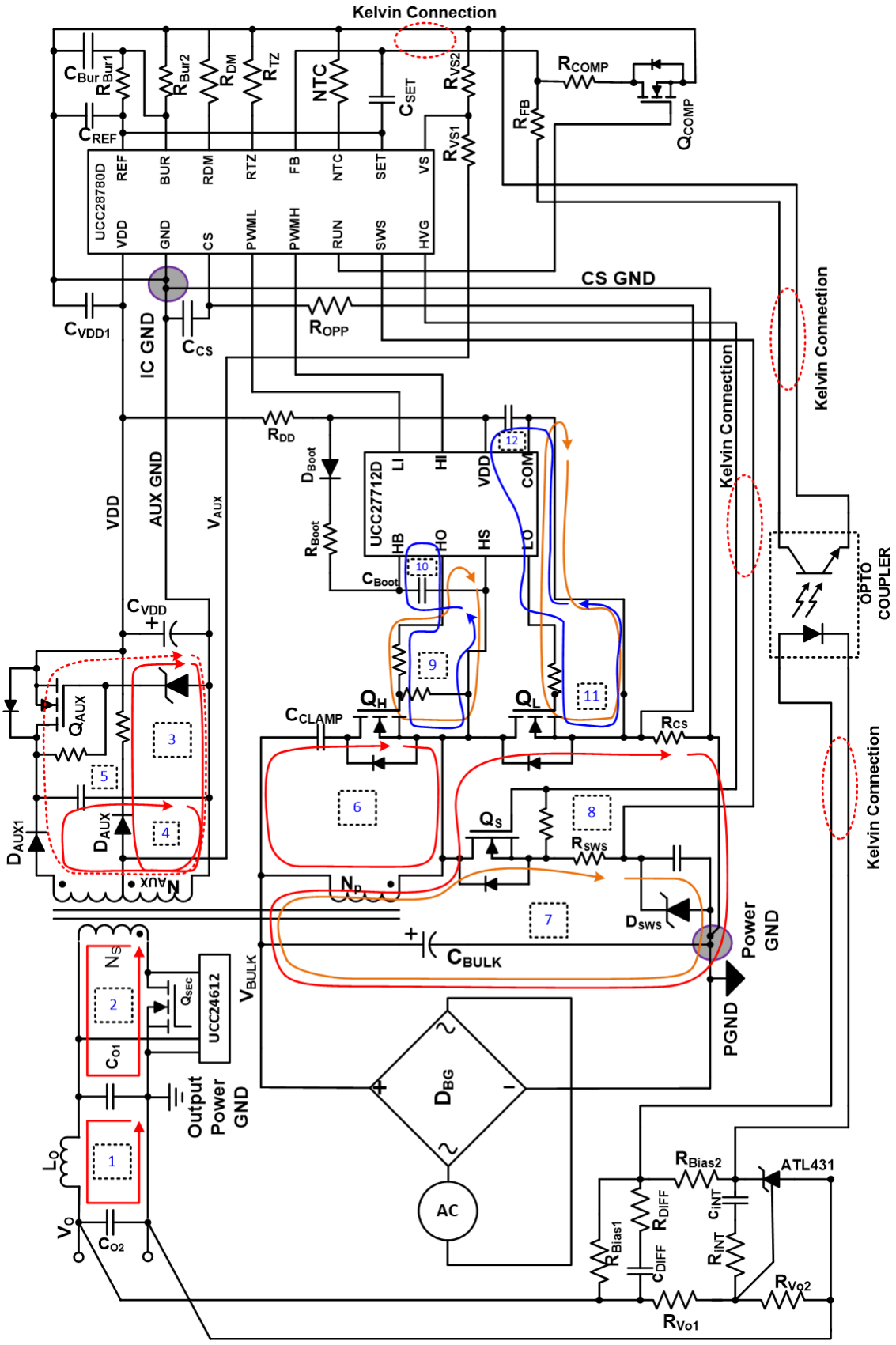

Figure 20. A Schematic of PCB Layout Guideline for the UCC28780 High-frequency ACF Converter

10 References

1. Texas Instruments, UCC28780 High Frequency Active Clamp Flyback Controller Datasheet (SLUSD12)
2. Texas Instruments Video, Making Power Supplies Smaller: An Overview of the Active Clamp Flyback Chipset
3. Texas Instruments Video, The Active Clamp Flyback: Part 1
4. Texas Instruments Video, The Active Clamp Flyback: Part 2
5. Texas Instruments Video, Demystifying Active-clamp Flyback Loop Compensation
6. Texas Instruments, Comparison of GaN-and Silicon FET-based Active Clamp Flyback Converters Seminar
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8. Increasing Power Density with the Active Clamp Flyback Controller Application Report (SLUA871)
9. TI E2E Support Forum
10. Texas Instruments, Using the UCC28780EVM-002 45-W 20-V High Density GaN Active-Clamp Flyback Converter User's Guide (SLUUBO8)
11. Texas Instruments, Using the UCC28780EVM-021, 45-W, 20-V High- Density Silicon (Si) Based, Active-Clamp Flyback Converter/Evaluation Module User's Guide (SLUUBV6)

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