Application Note

How to Extract Raw Data of DC/DC Converter Loop Response Bench and Simulation Tests

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ABSTRACT

DC/DC converter loop response tests are common in IC development phase as well as in system development phase. Loop response reflects DC/DC converters stable performance. Tuning loop compensation parameters or external components is needed to make sure a desired performance. Using correlated simulation model and bench would significantly shorten optimization time.

This application note introduces the bench and simulation methods of measuring loop response, explains why need to do bench and simulation correlation, and provides how to extract raw data from bench and simulation results to correlate loop response for DC/DC converters both in time domain and frequency domain.

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1 Introduction

Loop response performance is critical for the proper operation in a DC/DC converter system. During a new IC product design phase or an end equipment evaluation phase, loop response bench test and simulation results could be the good reference to improve converter loop response and stability. The most common methods of measuring loop response are load transient in time domain and bode plot test in frequency domain.

In bench test time domain, load transient performance can be measured by oscilloscope to reflect loop response. During the load transient, the output voltage overshoot and undershoot can be observed. Based on the amount of overshoot, undershoot and ringing occurring during the load transient, the converter loop response phase margin and crossover frequency can be estimated (see: *Evaluation and Performance Optimization of Fully Integrated DC/DC Converters*, as shown in Figure 1-1.

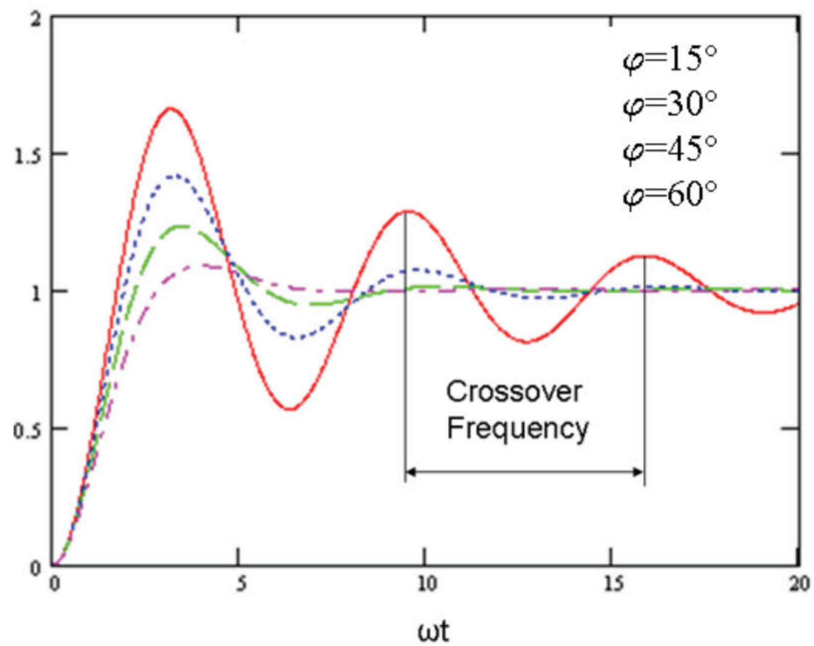


Figure 1-1. Step Response vs. Loop Phase Margin and Crossover Frequency

In bench test frequency domain, bode plot can be measured by using a network analyzer or a specific loop gain measurement instrument as available from AP Instruments to judge the loop response. The gain and phase are plotted against the frequency. Phase margin and crossover frequency can be directly obtained.

In simulation, load transient in time domain can be simulated both in Simplis and Candence. Bode plot in frequency domain can be simulated using Simplis. The common methods of loop response test can be summarized as shown Figure 1-2.

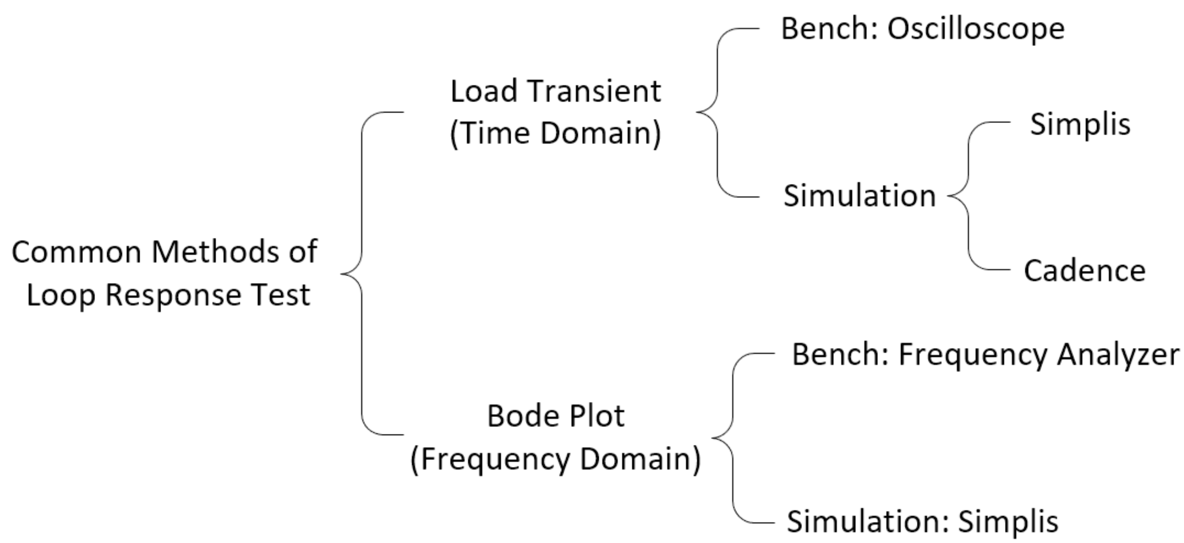


Figure 1-2. Common Methods of Loop Response Test

Loop response reflects DC/DC converters stable performance. In IC development phase, IC designers need to look into the simulation results and actual bench test results, correlate the DC/DC device model, to make the model better and more close to silicon. As well as during system evaluating and debugging phase, engineers can use correlated simulation to guide bench test which will be more effective. To get a correlated model, extracting raw data from bench and simulation into one format (for example, CSV file) to compare difference is the first step. This application note introduces how to extract raw data of DC/DC converter loop response bench and simulation tests.

2 Time Domain Correlation

2.1 Load Transient Correlation Structure

Load transient response is the response to a sudden load fluctuation, which reflects the response of DC/DC converter in the period until the time until the output voltage returns to a preset value after falling or rising. In contrast with load regulation, it is the name implies a transient-state characteristic.

Load transient response can not only be tested on bench by oscilloscope, but also be simulated in Simplis and Cadence. Both bench oscilloscope waveform and simulation waveform can be saved into CSV file in each environment. After that, all the CSV data can be put into one CSV file so as to plot all the bench and simulation results in one chart for correlation analysis.

The time domain load transient correlation structure can be described as Figure 2-1.

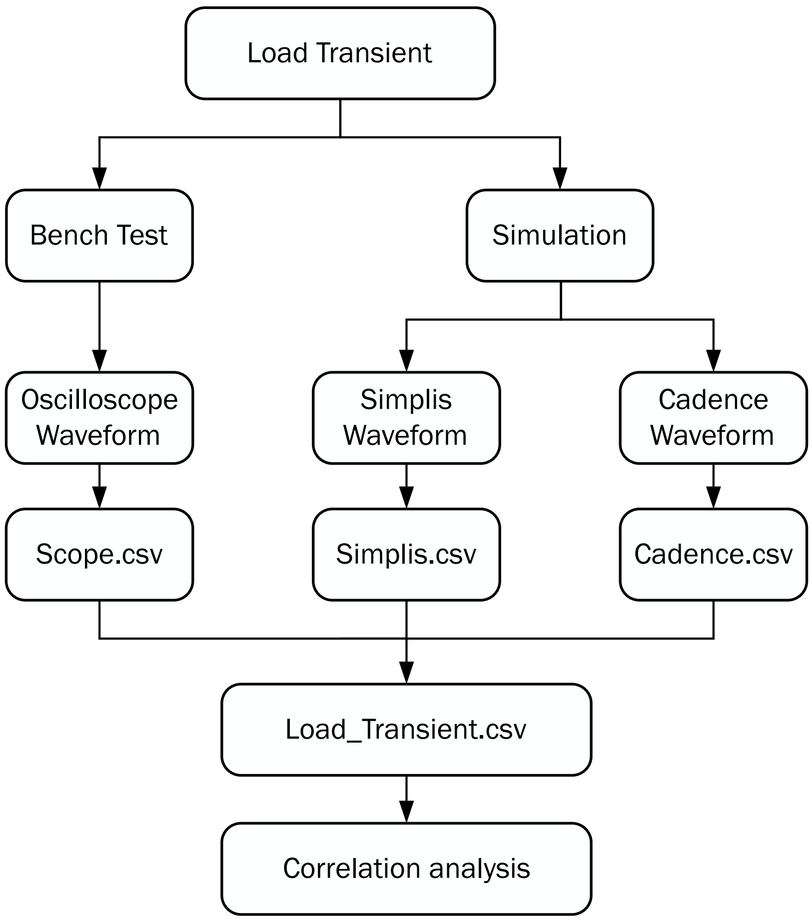


Figure 2-1. Time Domain Load Transient Correlation Structure

2.2 Example Based on TPS56C231

TPS56C231 is a small, high-efficiency synchronous buck converter with an adaptive on-time DCAP3 control mode. It operates with supply input voltage from 3.8 V to 17 V and is designed to provide up to 12-A output current. It has competitive features including a very accurate reference voltage, fast load transient response, and no requirement for external compensation, adjustable current limit, and both Eco-mode and FCCM operation modes for selection at light-load condition through the configuration of MODE pin (see TPS56C231 3.8-V to 17-V Input , 12-A Synchronous Step-Down Converter).

TPS56C231 is designed for data center and enterprise computing POLs, wireless infrastructure, IPCS, factory automation, high-end DTV and distributed power systems with typical 5-V and 12-V input. This application note will use TPS56C231 as an example to show how to do bench and simulation load transient correlation for loop response.

2.2.1 How to Save Bench Scope Waveform to CSV File

A summary of the TPS56C231 load transient test conditions are provided in Table 2-1. The load transient is tested using TPS56C231EVM under 12 Vin, 1.2 Vout, 800 KHz switching frequency, Eco mode, output current from 0.2 A to 8 A with 2.5 A/us transient slew rate and 1 kHz toggling frequency conditions. Load transient performance is really related with inductor and output capacitor specs that are listed in Table 2-2.

Table 2-1. Load Transient Test Conditions

Specification	Test Condition
Vin (V)	12
Vout (V)	1.2
Mode	800kHz Eco Mode
Transient Parameters	0.2-8 A, 2.5 A/us, 1 kHz Frequency

Table 2-2. List of Materials

Material Description	Part Number
Inductor	1pcs IHLP2525CZERR68M01
Cout	4pcs GRM21BR61A476ME15L
Oscilloscope	Tektronix DPO3054
Eload	Chroma Eload 6314A

To make the transient response measured effectively, two scope channels are needed. The first channel should be across the output of converter close to the regulation point. Measuring the output voltage away from the regulation point will cause a DC offset between heavy load and light load, due to voltage drop in the output cabling. It is extremely important to use proper probe measurement techniques. The tip and barrel probe method can make the ground loop as small as possible which is showed in Figure 2-2. The second channel should be the output current which is synchronous to the transient load change. The current measurement could be used as a trigger so that the resulting output voltage deviation could be seen clearly.

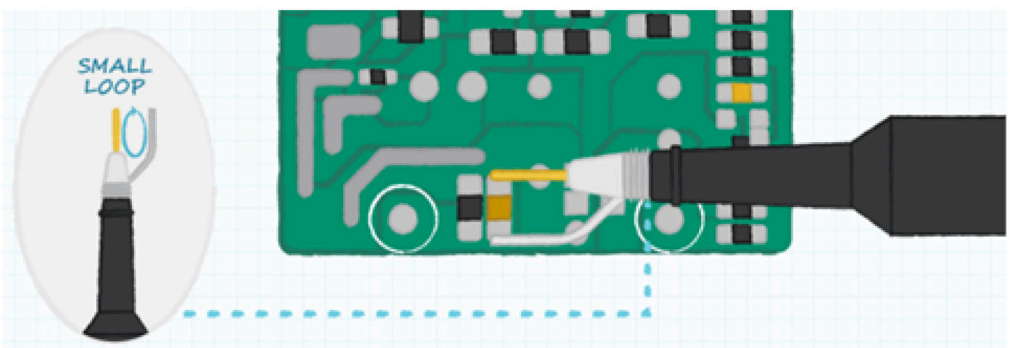


Figure 2-2. Tip and Barrel Probe Method

Using Tektronix DPO3054 oscilloscope and Chroma Eload 6314A with proper measurement method, load transient waveform in Figure 2-3 is obtained. Channel 1 is output voltage, using 1.2 V DC offset. Channel 4 is output current without offset.

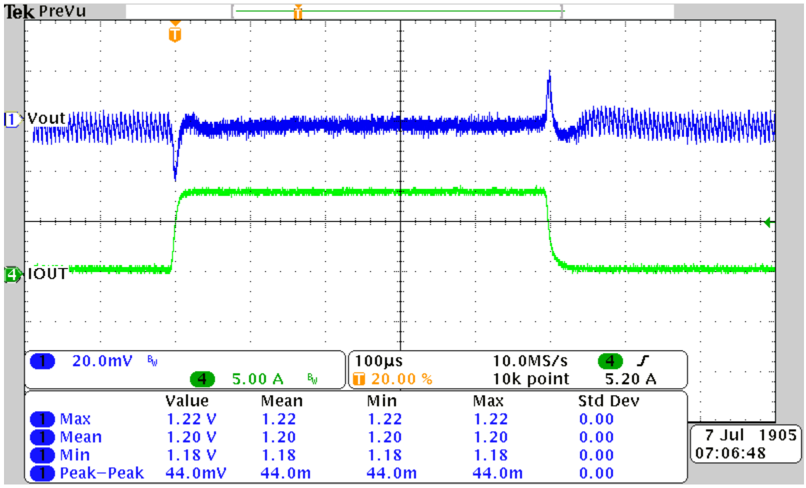


Figure 2-3. Load Transient Waveform

Before saving data, measuring the real transient slew rate manually is necessary for correlation as the configuration transient slew rate of Eload and the real slew rate are usually not same. The real rising and falling slew rate are 0.68 A/us as Figure 2-4 shows.

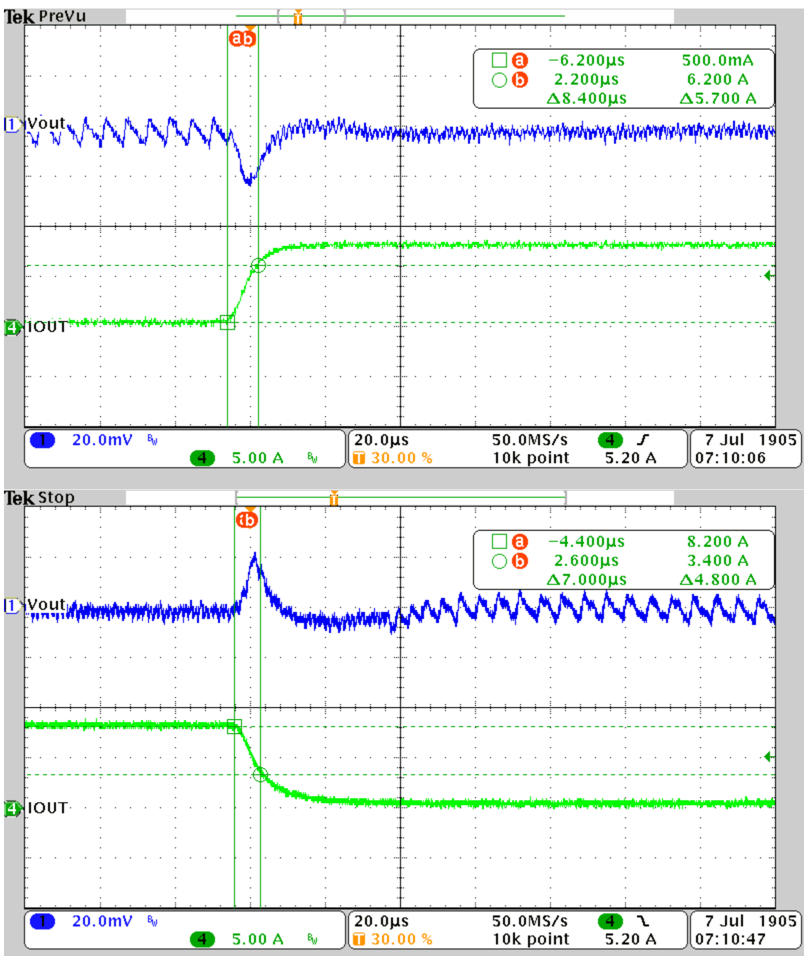


Figure 2-4. Load Transient Slew Rate

To save waveform as CSV file, first click the oscilloscope bottom button of *Menu*, select *Save Waveform* button, then at the right side of the screen select all source and change the definition to CSV file. For DPO3054 oscilloscope, there is no storage inside and an USB is used to save the CSV file. Figure 2-5 is the flow chart of how to save scope waveform to CSV file.

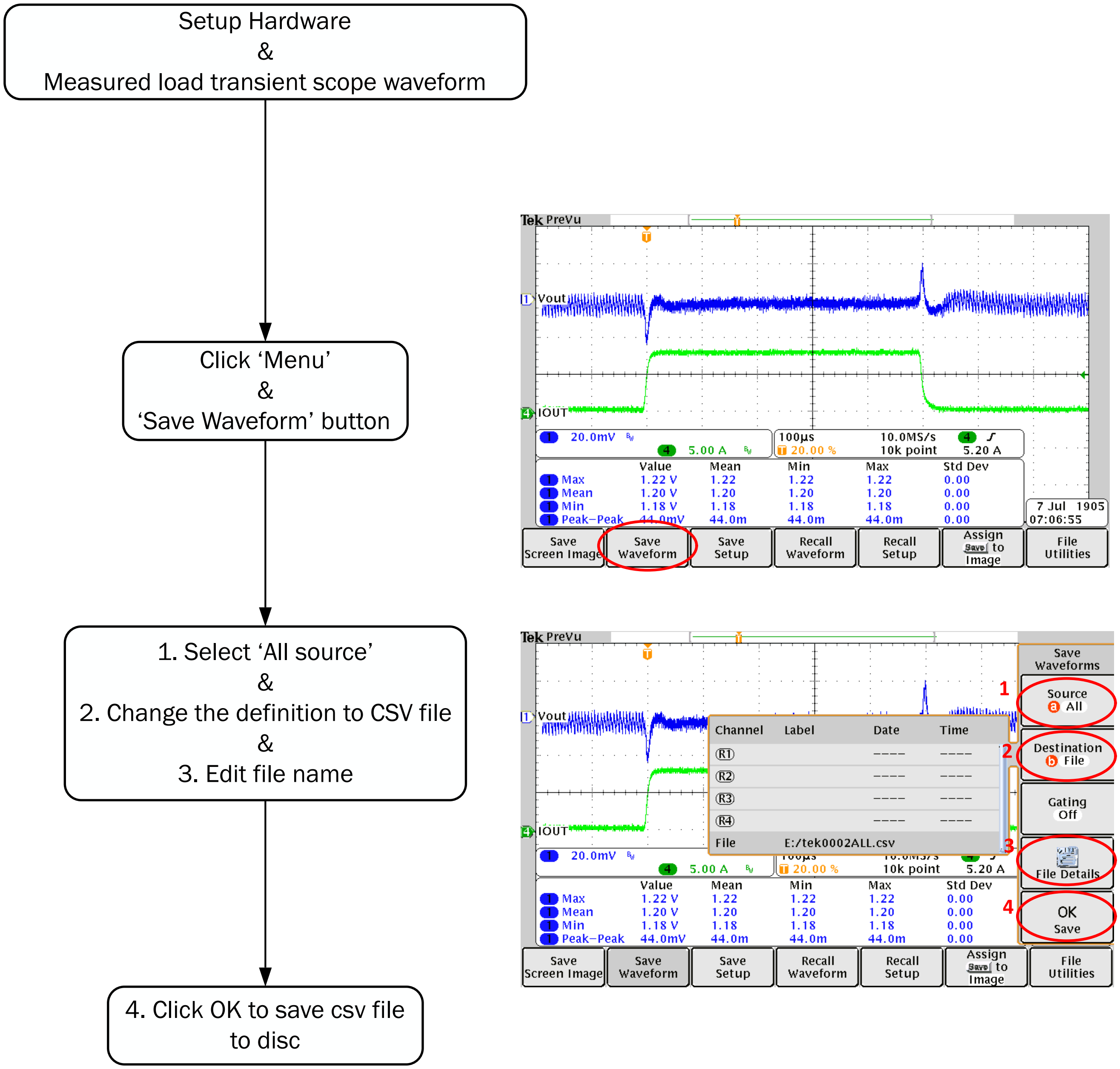


Figure 2-5. How to Save Scope Waveform to CSV File

2.2.2 How to Save Simplis Simulation to CSV File

SIMPLIS (SIMulation of Piecewise LInear Systems) is a circuit simulator specifically designed to handle the simulation challenges of switching power systems. Like SPICE, SIMPLIS works at the component level but typically can perform a transient analysis of a switching circuit 10 to 50 times faster. For switching power systems, the piecewise linear (PWL) modeling and simulation techniques employed by SIMPLIS result in qualitatively superior convergence behavior.

To correlate, the Simplis simulation conditions should match with the bench test setup. According to bench test conditions in Section 2.2.1, a summary of TPS56C231 Simplis load transient simulation conditions are listed in Table 2-3.

Table 2-3. Simplis Load Transient Simulation Conditions

Variable	Simulation Conditions
Vin (V)	12
Vout (V)	1.2
Mode	800 kHz Eco Mode
Transient current (A)	0.2-8
Transient Rising and Falling Time (us)	11
Inductor (uH)	0.68
Inductor DCR (mOhm)	5.5
Output Capacitor (uF)	168 (after derating)
ESR (mOhm)	0.75
Feedback Top and Bottom Resistor (Kohm)	30

After setting simulation conditions, two analysis setting steps are also required. One is to add the probe. For load transient, Vout signal probe should be added. Second is setting the simulation analysis. On the top menu, select Simulator and Choose Analysis. The Choose SIMPLIS Analysis table will be popped up, as Figure 2-6 shows. Then select Transient analysis and voltages only or probes only options. What's more, analysis parameters of saving data time should match with oscilloscope saving waveform time.

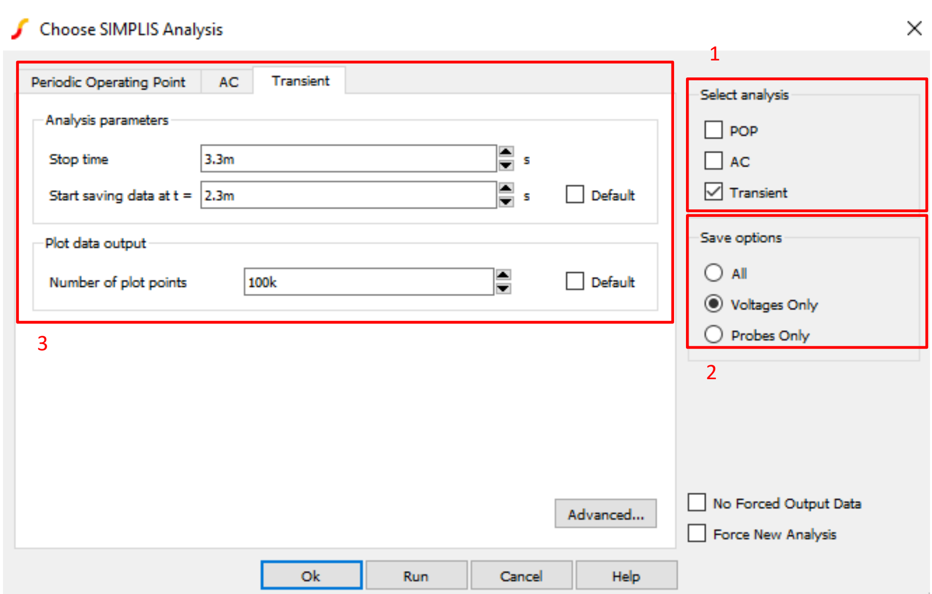


Figure 2-6. Simplis Analysis Setup for Transient

On the top menu, select Simulator and Run Schematics. The load transient simulation result of Vout is generated, as shown in Figure 2-7.

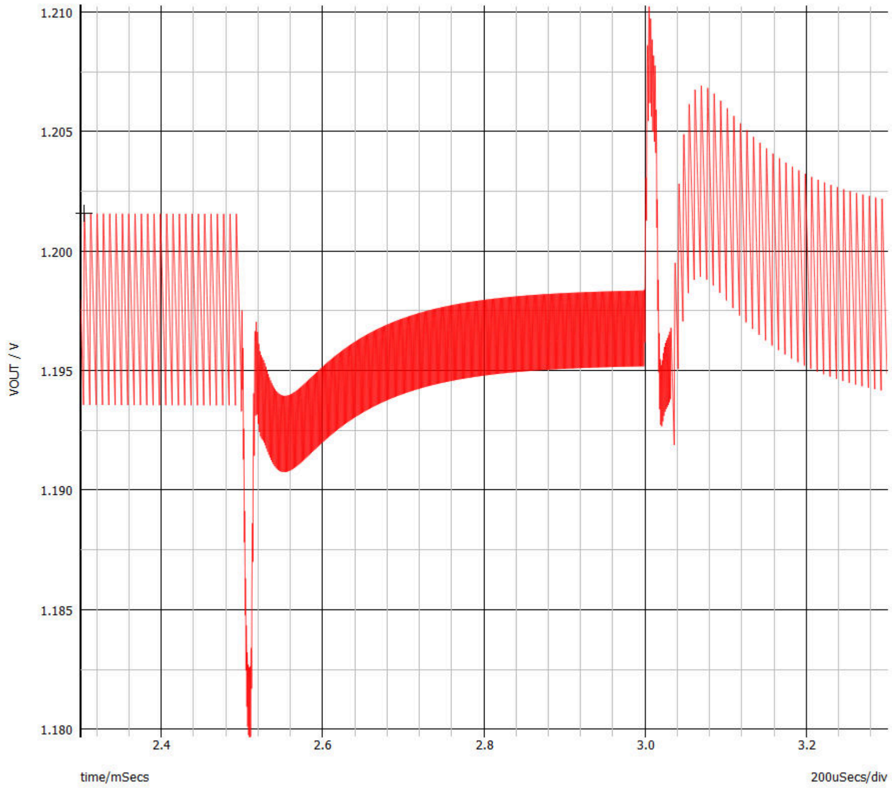
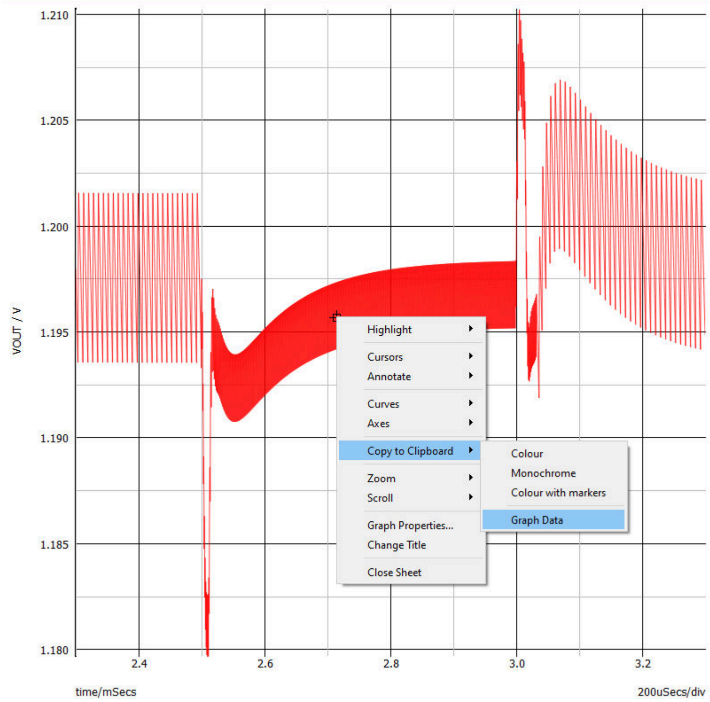
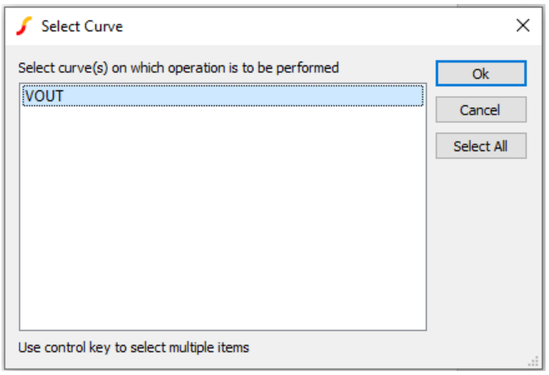


Figure 2-7. Simplis Load Transient Simulation Waveform

Next step is saving simulation waveform to CSV file. Right click the Waveform Window, choose *Copy to Clipboard*, click *Graph Data*, then select the VOUT curve, click *OK*, and open the excel to paste the data, as shown in Figure 2-8.



(a)



(b)

	E	F
1	Time /s	Simplis Vout /V
2	0.0023	1.197963761
3	0.0023	1.197951855
4	0.0023	1.197939948
5	0.0023	1.197928042
6	0.0023	1.197916136
7	0.0023	1.197904229
8	0.0023	1.197892323
9	0.0023	1.197880417
10	0.0023	1.19786851
11	0.0023	1.197856604
12	0.0023	1.197844698
13	0.0023	1.197832791
14	0.0023	1.197820885
15	0.0023	1.197808978
16	0.0023	1.197797072
17	0.0023	1.197785166
18	0.0023	1.197773259
19	0.0023	1.197761353
20	0.0023	1.197749447

(c)

Figure 2-8. How to Save Simplis Waveform to CSV File

2.2.3 How to Save Cadence Simulation Waveform to CSV File

In Cadence simulator, Virtuoso ADE Product Suite or Spectre X Simulator, using same parameters as Table 2-3, the load transient simulation waveform is shown in Figure 2-9.

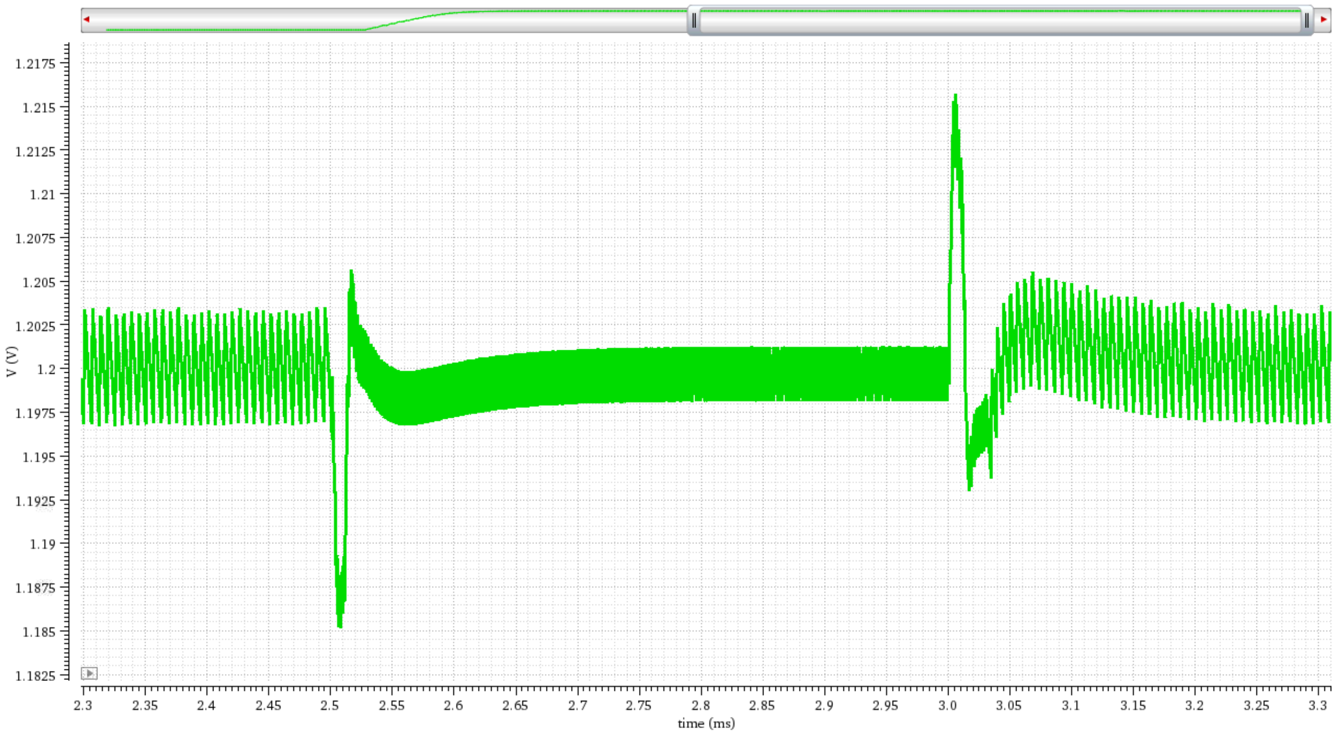
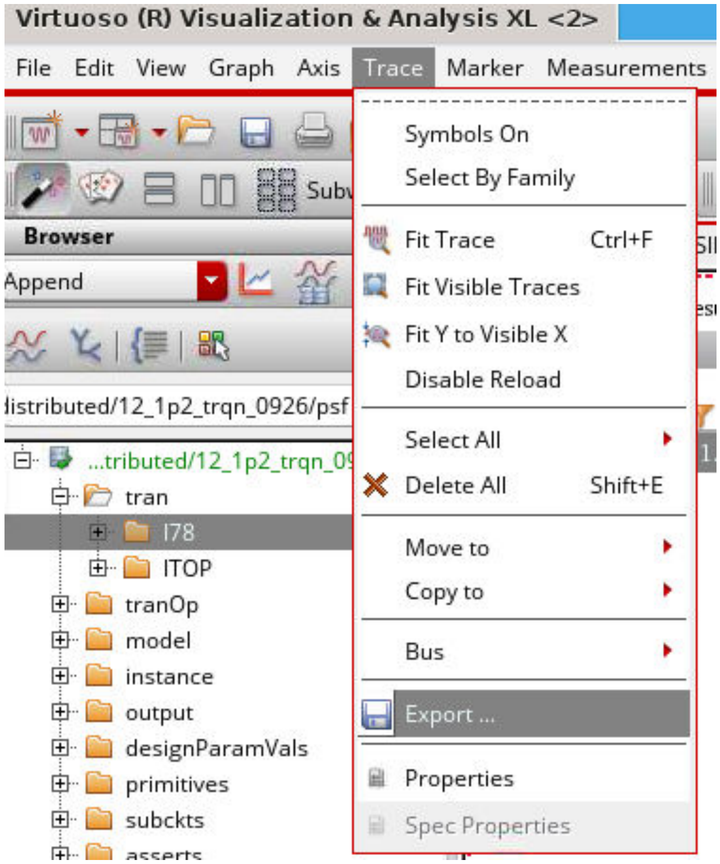
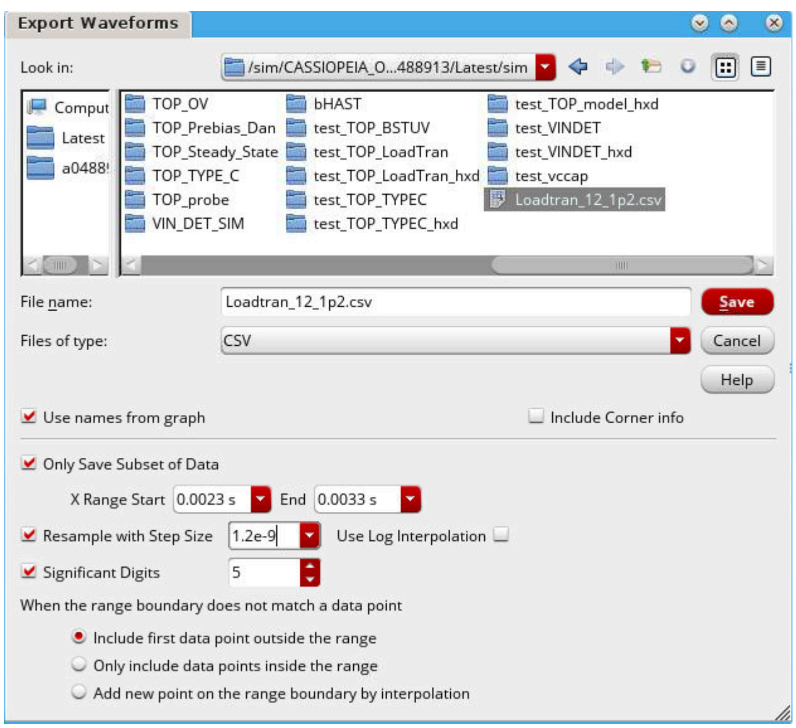


Figure 2-9. Cadence Load Transient Simulation Waveform

Next step is saving Cadence simulation waveform to CSV file. On the top menu, click Trace, then choose *Export*, and in the pop up window, select the files of type to CSV, change other setup parameters as needed, click *Save*, as shown in Figure 2-10.



(a)



(b)

Figure 2-10. How to Save Cadence Waveform to CSV File

2.2.4 Correlation Data

All the CSV files, including bench test, Simplis simulation and Cadence simulation results of CSV files, can be copied into one excel file to do correlation. Figure 2-11 is the load transient correlation waveform. Based on this waveform, tuning parameters would be effective based on overshoot, undershoot, response time differences. This application note would not describe how to tune loop parameters to make results match.

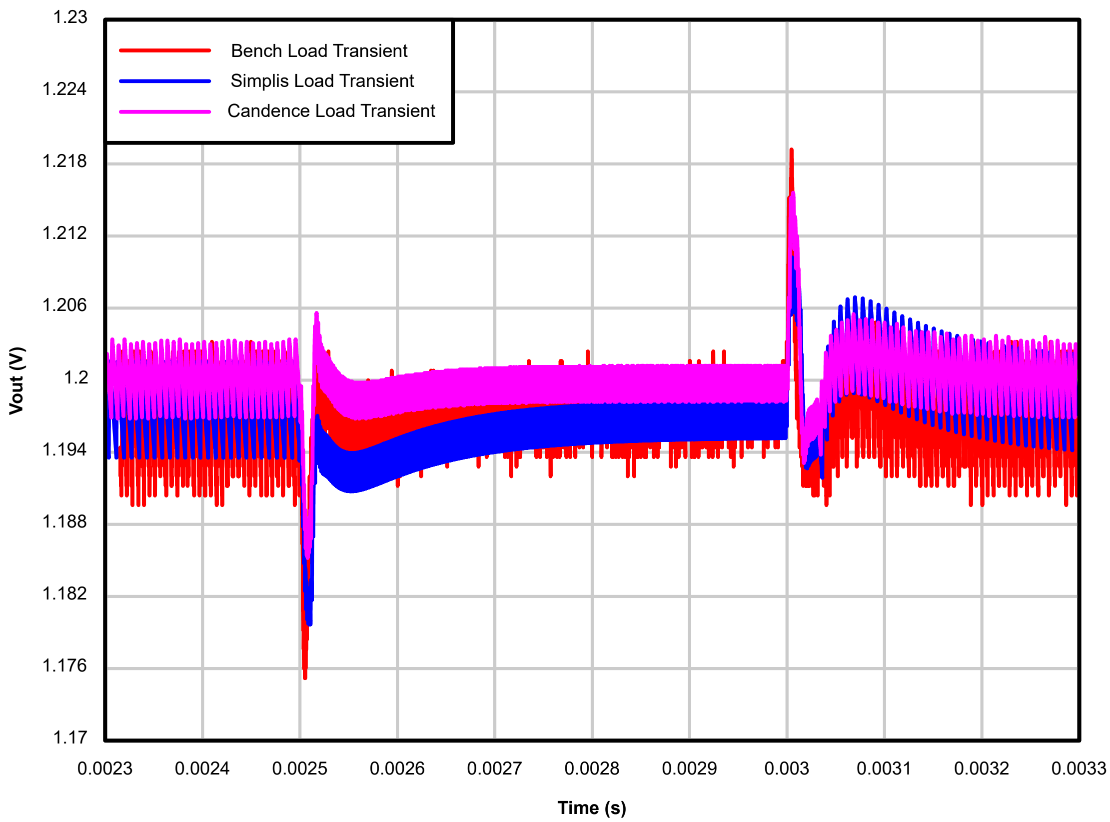


Figure 2-11. Load Transient Correlation Waveform

3 Frequency Domain Correlation

3.1 Frequency Response Bode Plot Correlation Structure

Bode plot is a graph of the frequency response of a system. It is usually a combination of the magnitude (in dB) and phase of the transfer function versus frequency, phase margin and crossover frequency can be directly obtained. Bode plot measurements are essential for system stability and transient response optimization.

Bode plot can not only be tested on bench with a network analyzer or a specific loop gain measurement instrument, but also be simulated in Simplis. Bench network analyzer bode plot and simulation bode plot can be saved into CSV file in each environment. After that, all the CSV data can be put into one CSV file so as to plot bench and simulation results in one chart for correlation analysis.

The frequency response bode plot correlation structure is described in Figure 3-1.

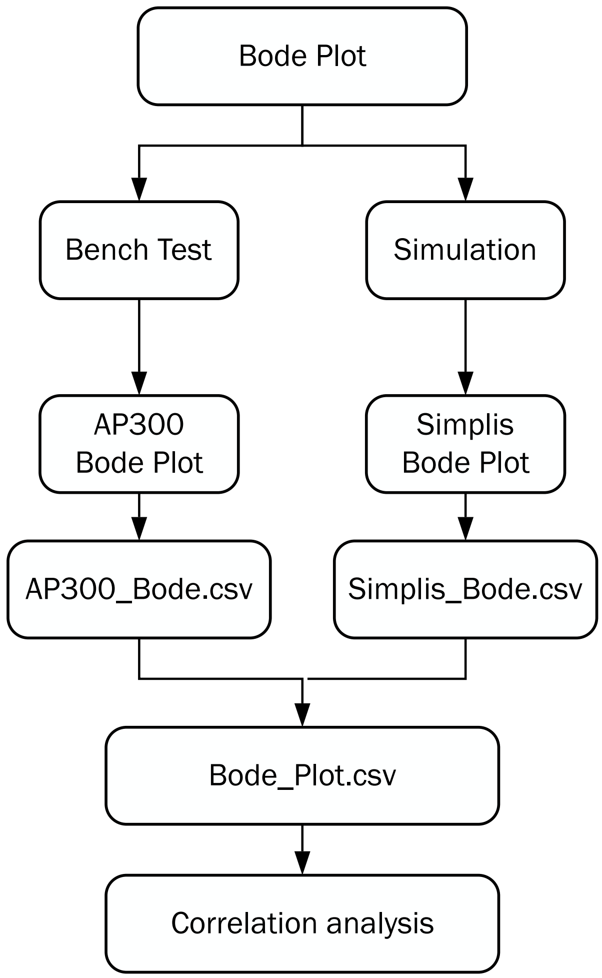


Figure 3-1. Frequency Response Bode Plot Correlation Structure

3.2 Example Based on TPS56C231

In this section, still using TPS56C231 as an example to show how to correlate frequency response bode plot between bench and simulation.

3.2.1 How to Save Bench Bode Plot to CSV File

Using AP Instruments' Model 300 Frequency Response Analyzer, the bode plot is completed on TPS56C231EVM under conditions listed in Table 3-1. Inductor and output capacitors are same as Table 2-2.

Table 3-1. Bode Plot Test Conditions

Specification	Test Conditions
Vin (V)	12
Vout (V)	1.2
Mode	800kHz Eco Mode
Iout (A)	6

Click the *Run* button in AP computer interface, then it shows the bode plot as Figure 3-2, where shows 114.68kHz crossover frequency and 43.573deg phase margin.

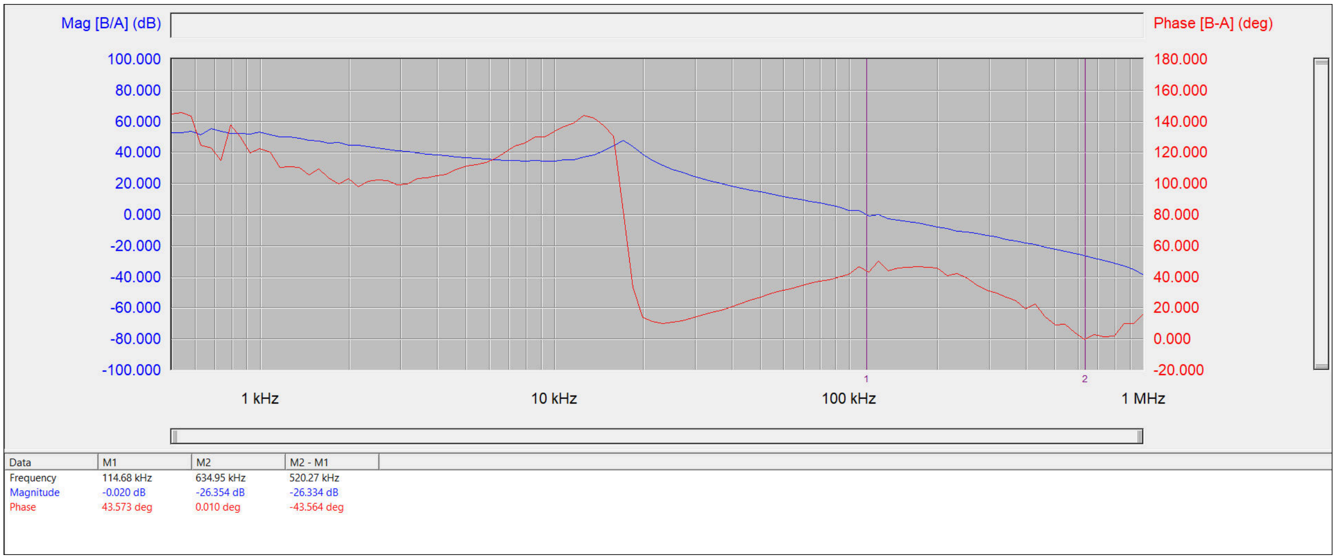
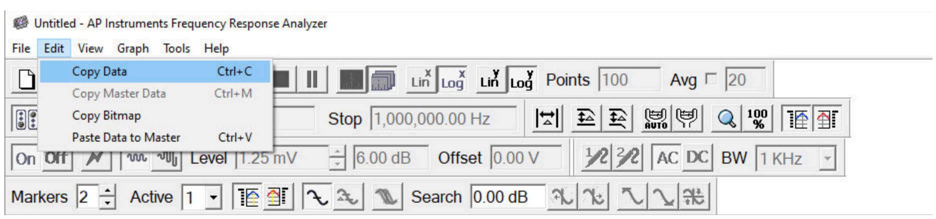


Figure 3-2. Bench Test Bode Plot of TPS56C231

Click *Edit* on the top menu and choose *Copy Data*, as shown in Figure 3-3 (a), then open the Excel spreadsheet to paste the data, the first column is *Frequency (Hz)*, the second column is *Mag [B/A] (dB)*, and the third column is *Phase [B-A] (deg)* as shown in Figure 3-3 (b) which is the raw data of bench test bode plot.



(a)

	A	B	C
1	Frequency (Hz)	Mag [B/A] (dB)	Phase [B-A] (deg)
2	5.00E+02	5.28E+01	1.45E+02
3	5.40E+02	5.29E+01	1.46E+02
4	5.83E+02	5.38E+01	1.43E+02
5	6.30E+02	5.12E+01	1.25E+02
6	6.80E+02	5.53E+01	1.23E+02
7	7.34E+02	5.34E+01	1.15E+02
8	7.93E+02	5.22E+01	1.38E+02
9	8.56E+02	5.21E+01	1.30E+02
10	9.24E+02	5.17E+01	1.20E+02
11	9.98E+02	5.32E+01	1.22E+02
12	1.08E+03	5.12E+01	1.20E+02
13	1.16E+03	5.01E+01	1.11E+02

(b)

Figure 3-3. How to Save Bode Plot to CSV File

3.2.2 How to Save Simplis Bode Plot Simulation to CSV File

Setting Simplis simulator as Figure 3-4, then run AC simulation to get Simplis bode plot, as shown in Figure 3-5. The simulation result shows 124.24kHz crossover frequency and 55.37deg phase margin.

Using same method in Section 2.2.2, Simplis bode plot raw data can be extracted.

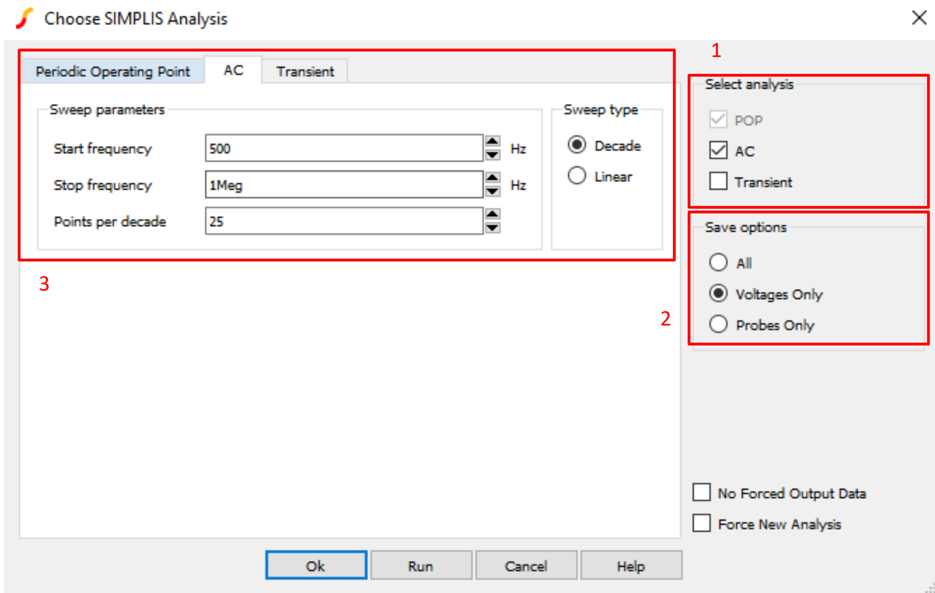


Figure 3-4. Simplis Analysis Setup for AC

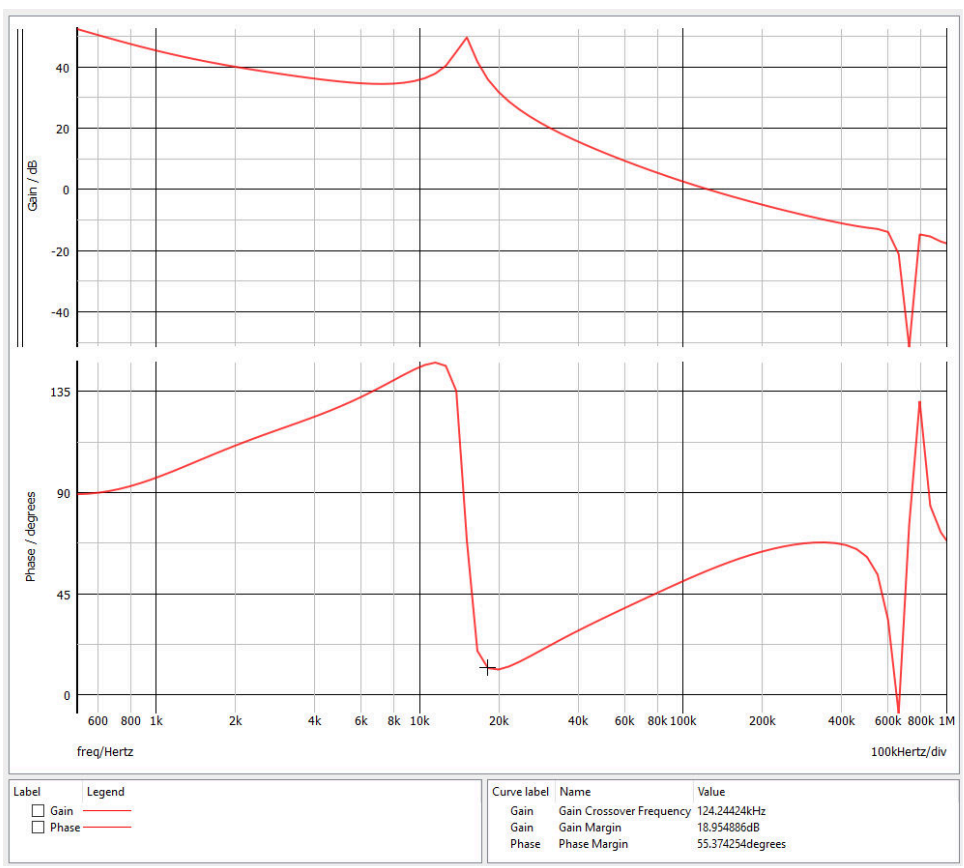


Figure 3-5. Simplis Bode Plot Simulation Waveform

3.2.3 Correlation Data

Both the CSV files, including bench bode plot test and Simplis simulation bode plot can be copied into one CSV file to do correlation. Figure 3-6 is the bode plot gain and phase margin correlation waveforms.

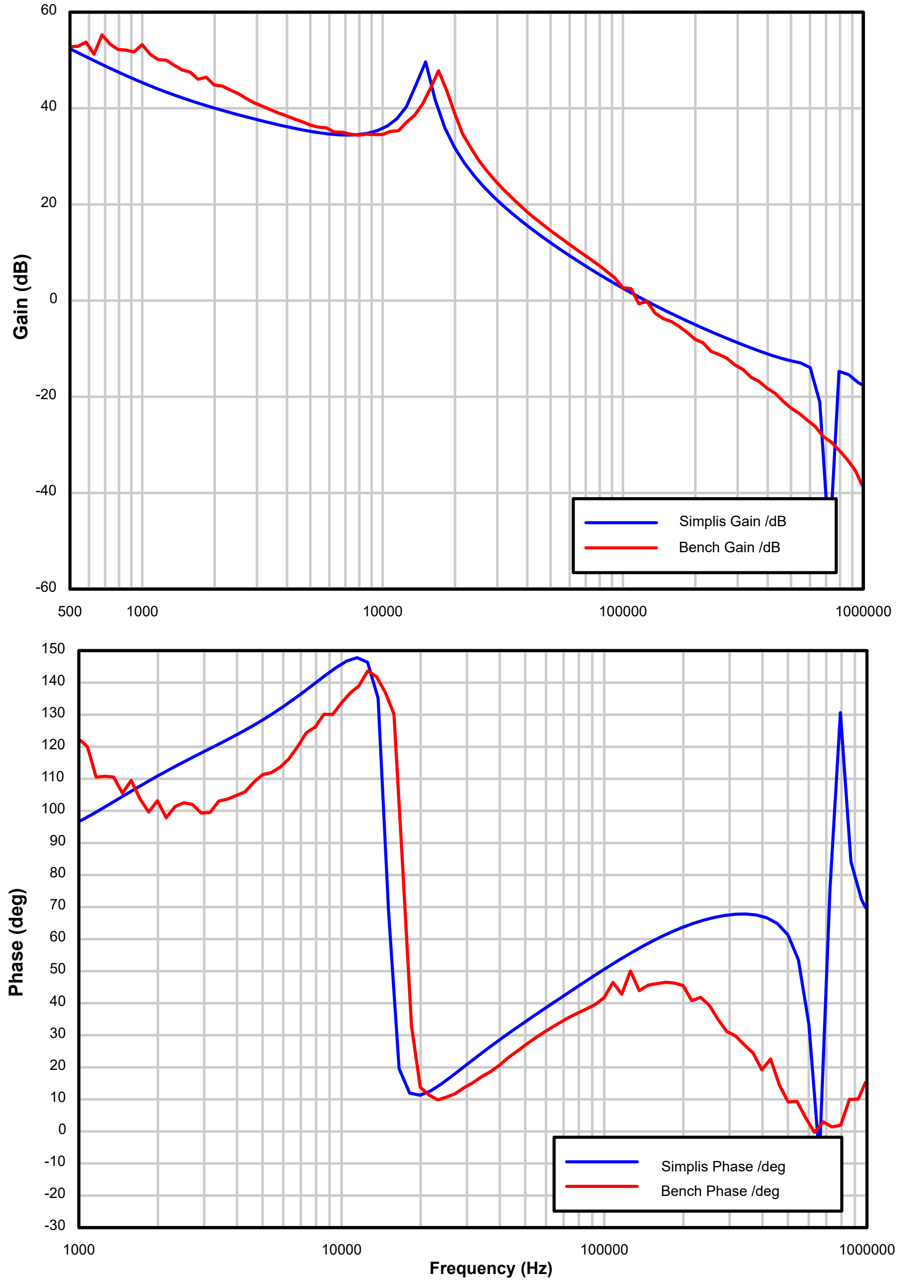


Figure 3-6. Correlation Gain of Bode Plot

As previously shown, the bode plot correlation of simplis simulation vs. bench test are not very good, the LC double-pole frequencies (peak point) are not well matched. This may be due to the L values in Table 2-2 are not actual values. Considering 15% inductance detaining (0.578uH), the Simplis bode plot is updated in Figure 3-7, which matches the bench result better.

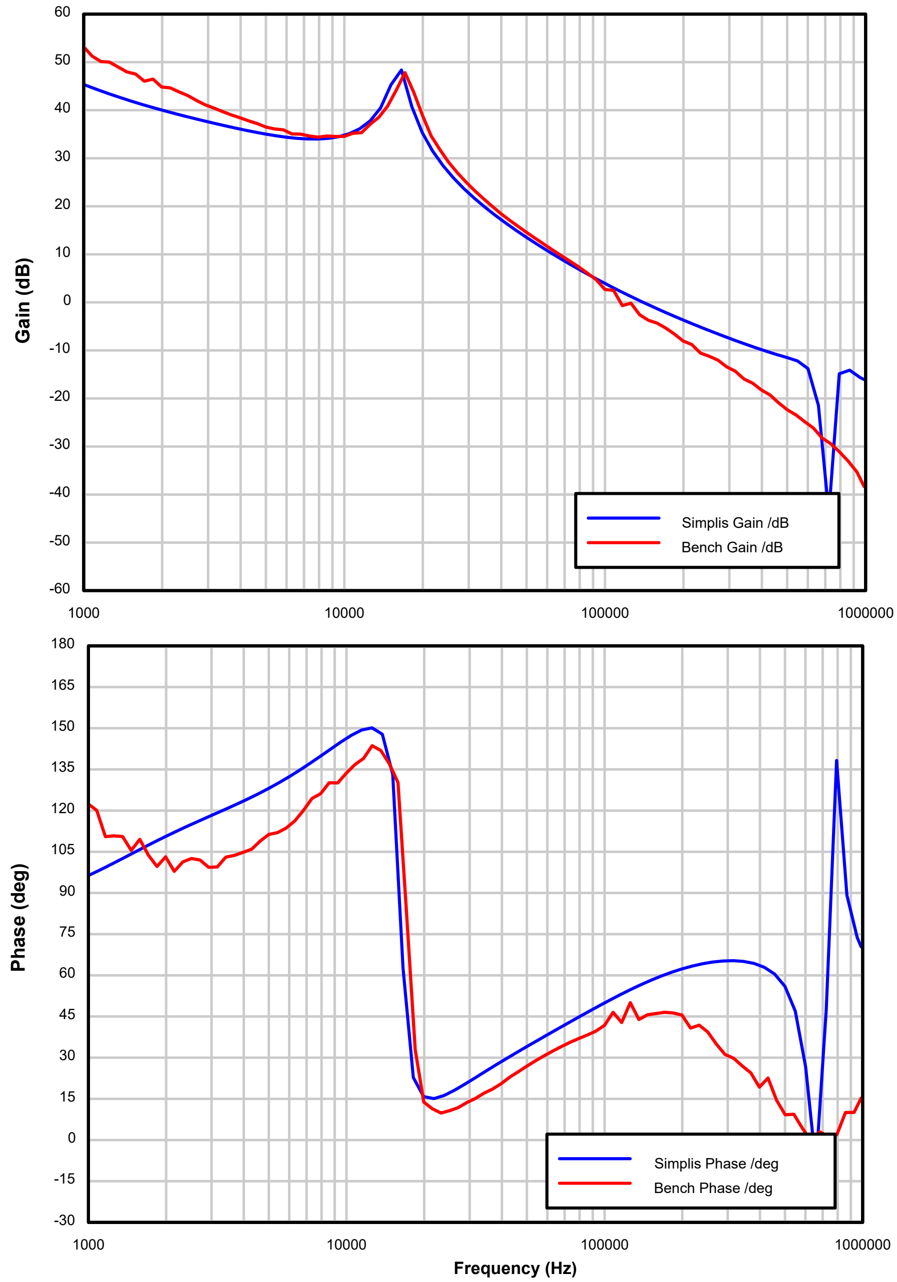


Figure 3-7. Correlation Phase of Bode Plot

4 Summary

This application note gives methods of extract raw data from bench test and simulation result to analyze DC/DC loop response, including in time domain and frequency domain. The correlation work between bench and simulation tests are useful for board-level loop response check, also useful for IC-level loop stability validation.

5 References

- Texas Instruments, *Evaluation and Performance Optimization of Fully Integrated DC/DC Converters*
- Texas Instruments, *TPS56C231 3.8-V to 17-V Input , 12-A Synchronous Step-Down Converter*, data sheet