Texas Instruments

UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Preregulator

Application Note

UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Preregulator

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ABSTRACT

Power factor corrected (PFC) preregulators are generally used in higher power ac-to-dc offline power converters or to meet line harmonic requirements such as EN61000−3−2. The designs are typically done using a boost topology with the average current mode control offered by PFC controllers such as TI/Unitrode's UC3854 and UCC3817. These 16-pin controllers are pulse width modulators (PWM) that require many external components to achieve near unity power factor (PF). However, in some applications, it may not be necessary to acheive the levels of PF and the current total harmonic distorion (THD) that the average current mode control can provide. The PFC preregulator can be designed using a critical conduction mode control (also referred to as transition mode control). The 8-pin UCC38050 PFC controller is designed for such an application. The UCC38050 operates with pulsed frequency modulation (PFM) in a critical conduction mode.

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1 Introduction

This application note reviews the design process for a 100-W offline power factor corrected preregulator using the UCC38050 Transition Mode PFC Controller.

- The application note was generated using typical parameters rather than worst-case values.
- Please refer to the Table 1 and Figure 1 for design specifications and component placement.
- Please refer to Table 2, the variable definition table for all variable definitions.

Table 1. Design Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}		85		265	V_{RMS}
Input frequency			60		Hz
V_{OUT} dc	V_{IN} = 85 V_{RMS}	370	400	425	V
V_{OUT} dc	V_{IN} = 265 V_{RMS}	370	390	410	V
P_{OUT}		0		100	W
Output voltage ripple	V_{IN} = 85 V_{RMS}, P_O = 100 W			3%	
Efficiency	V_{IN} = 265 V_{RMS}, P_O = 100 W	90%			
Total harmonic distortion (THD)	V_{IN} = 265 V_{RMS}, P_O = 100 W		5%		
Total harmonic distortion (THD)			15%		
Hold-up time		16.7			ms

The following table lists and defines all of the variables that are going to be used in this application note.

Table 2. Variable Definitions

VARIABLE	DEFINITION
I_{RMS_C3}	RMS current in the boost capacitor
C_{DIODE}	Boost diode capacitance
COMP	Dynamic range of the comp pin of the multiplier
C_{OSS}	FET drain to source capacitance
f_{LINE}	Input line frequency
f_S	Minimum switching frequency
GC(s)	Control transfer function
$G_{CO(s)}$	Control to output transfer function
gM	Transconductance amplifier gain
G_{VEA}	Gain of the voltage amplifier
H_S	Voltage divider gain

VARIABLE	DEFINITION
I_{PEAK}	Peak inductor current, peak diode current, peak switch current
I_{RMS_DIODE}	Boost diode current
I_{RMS_FET}	RMS current in the FET
I_{RMS_L}	RMS inductor current
P_{SEMI}	Power dissipated by a semiconductor device
P_{CON_FET}	Conduction losses in the FET
P_{COND_DIODE}	Diode conduction losses
P_{COSS}	Power dissipated by the FET's drain to source capacitance
P_{DIODE}	Total loss in the boost diode
P_{DIODE_CAP}	Loss due to boost diode capacitance
P_{FET_TR}	FET transition losses
P_{GATE}	Power dissipated by gate of the FET
P_{OUT}	Maximum output power
PQ1	Total FET losses
Q_{GATE}	FET gate charge
$R_{DS(on)}$	On resistance of the FET
RΘcs	Thermal impedance case to sink
RΘjc	Thermal impedance junction to case
RΘsa	Thermal impedance sink to air
T_{AMB}	Ambient tempature
t_F	FET fall time
t_{HOLDUP}	Boost capacitor hold up time
$T_{J(max)}$	Maximum semiconductor temperature
t_{ON}	Boost inductor energizing on time
t_R	FET rise time
$T_{S(f)}$	Voltage loop gain
V_{CSENSE}	Maximum current sense voltage
V_{DROP}	Amount of voltage the boost capacitor has to hold up
$V_{EA(max)}$	Maxim voltage amplifier output.
$V_{EA(min)}$	Minimum voltage amplifier output.
V_{GATE}	Gate drive voltage
$V_{IN(max)}$	Maximum RMS input voltage
$V_{IN(min)}$	Minimum RMS input voltage
V_{OUT}	Boost output voltage
V_{PP}	Output peak-to-peak ripple voltage
VR3	Average multiplier input voltage at low line input voltage
V_{REF}	UCC38050 Internal Reference
η	Efficiency
%THD	Percentage of allowable current total harmonic distortion.

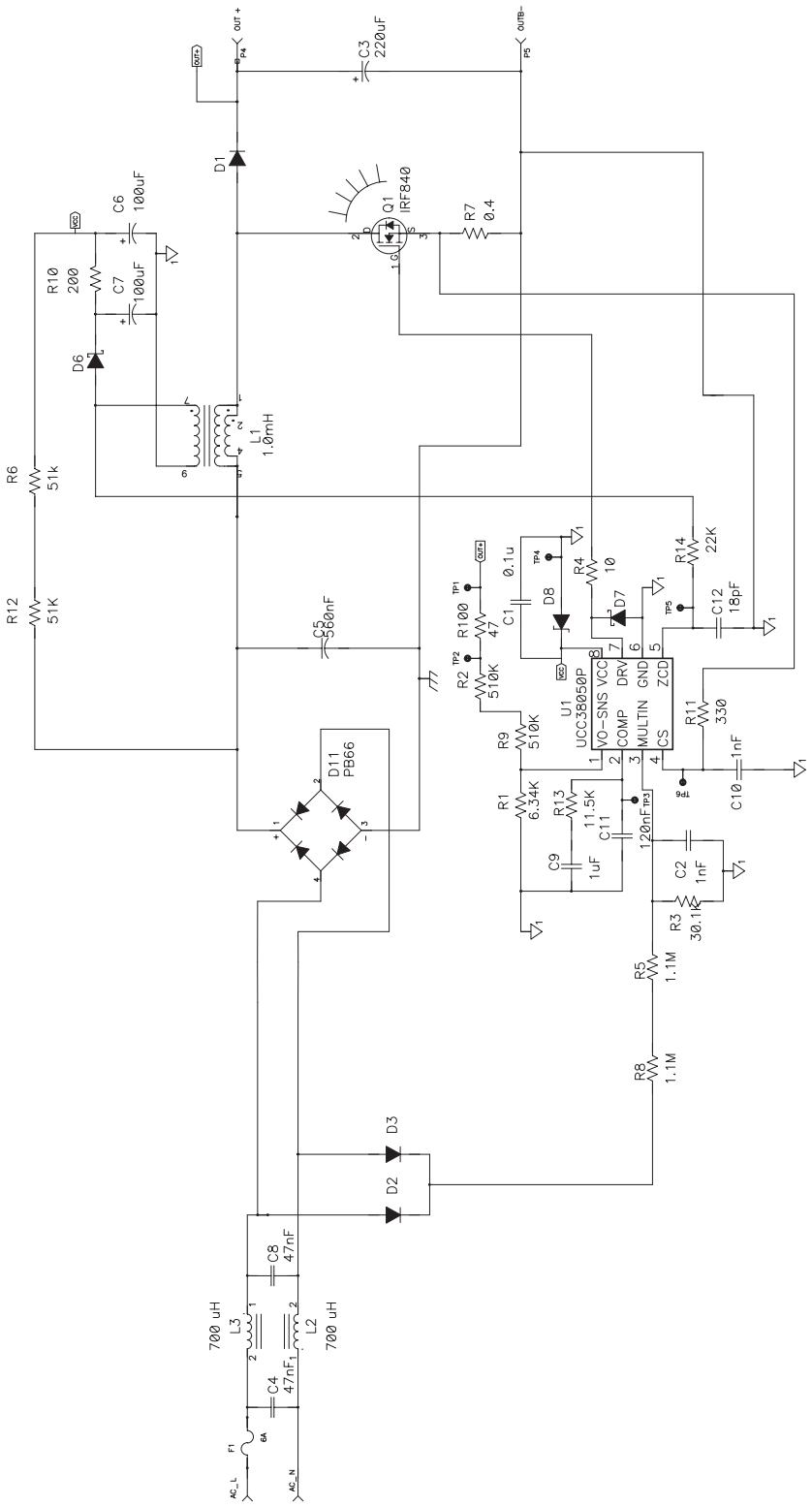


Figure 1. UCC38050 Schematic

2 Power Stage Design

2.1 Inductor Selection

The boost inductor is selected based on the maximum ripple current at the peak of minimum line voltage and the minimum switching frequency. The minimum switching frequency (f_S) needs to be set at a frequency above the audible range. for this design f_S was selected to be 25 kHz. The following equation can be used to calculate the required inductor for the power stage for a critical conduction design. The calculated inductance for this design was roughly 1 mH. To make the design process easier the inductor was designed by Cooper Electronics part number CTX16−15954.

$$L1 = \frac{\left(V_{OUT} - \sqrt{2}V_{IN(min)}\right) \times \eta \times V_{IN(min)}^{2}}{2 \times f_S \times V_{OUT} \times P_{OUT}} \quad (1)$$

In this design an auxiliary winding was taken off the boost inductor to power the UCC38050 PFM controller. The turns ratio (N) was calculated with the following equation.

$$N = \frac{V_{OUT} - V_{IN(max)} \times \sqrt{2}}{2\,V} \quad (2)$$

2.2 Boost Switch Selection (D1) and Boost Diode Selection (Q1)

To properly select D1 and Q1 a power budget is generally set for these devices to maintain the desired efficiency goal. The following equations can be used to estimate power loss in your switching devices.

To meet the power budget for this design an IRF840 HEX FET and HFA08TB60STRR fast recovery diode from International Rectifier were chosen for this design to meet the power constraints.

Equations used to calculate the loss In Q1:

$$I_{RMS\_FET} = \frac{P_{OUT} \times 2 \times \sqrt{2}}{\eta \times V_{IN(min)}} \times \sqrt{\frac{1}{6} - \frac{4 \times \sqrt{2} \times V_{IN(min)}}{9 \times \pi \times V_{OUT}}} \quad (3)$$

$$I_{RMS\_L} = \frac{P_{OUT}}{\eta \times V_{OUT(min)} \times \sqrt{6}} \quad (4)$$

$$P_{GATE} = Q_{GATE} \times V_{GATE} \times f_S, \quad (5)$$

$$P_{COSS} = \frac{1}{2}C_{OSS}V_{OUT(min)}^{2} \times f_S, \quad (6)$$

$$P_{COND\_FET} = R_{DS(on)} \times I_{RMS\_FET}^{2} \quad (7)$$

$$I_{PEAK} = \frac{P_{OUT} \times 2 \times \sqrt{2} \times 1.3}{\eta \times V_{IN(min)}} \quad (8)$$

Equations used to estimate the loss in D1:

$$P_{DIODE} = P_{COND\_DIODE} + P_{DIODE\_CAP} \quad (9)$$

$$I_{RMS\_DIODE} = \frac{P_{OUT} \times 2 \times \sqrt{2}}{\eta \times V_{IN(min)}} \times \sqrt{\frac{4 \times \sqrt{2} \times V_{IN(min)}}{9 \times \pi \times V_{OUT}}} \quad (10)$$

$$P_{COND\_DIODE} = Vf \times I_{AVG} \quad (11)$$

$$P_{DIODE\_CAP} = \frac{C_{DIODE}}{2} \times V_{OUT(min)}^{2} \times f_S \quad (12)$$

NOTE: The diode RMS current is used as an estimate of average current to approximate conduction losses in the diode.

2.3 Heat Sinks

The following equation can be used to calculate the minimum required thermal impedance of the heat sinks (Rθsa) required for this design for Q1 and D1. The heat sink was designed to ensure that the junction tempature would not go above 75% of their rated maximum with convection cooling with a maximum ambient temperature of 60°C. The heat sink required for Q1 was an Avvid heat sink part number 593002 B 0 00 00. Because of the zero current switching technique (ZCS) used in this topology a heat sink was not required for D1.[6]

$$R\Theta_{sa} = \frac{T_{J(max)} - T_{AMB} - P_{SEMI} \times \left(R\Theta_{CS} + R\theta_{JC}\right)}{P_{SEMI}} \quad (13)$$

2.4 Output Holdup Capacitor Selection

The following equations were used to estimate the minimum holdup capacitor size (C3) and the maximum allowable RMS current through the boost capacitor (I_{RMS_C3}). The holdup capacitor was designed for 16.7 ms of holdup time (t_{holdup}) allowing the output 85 V of drop (V_{DROP}).

$$C3 \geq 2 \times P_{OUT} \times \frac{t_{HOLDUP}}{V_{OUT}(min)^2 - \left[V_{OUT(min)} - V_{DROP}\right]^2} \quad (14)$$

$$I_{RMS\_C3} = \frac{P_{OUT}}{V_{OUT(min)}} \times \sqrt{\frac{16 \times V_{OUT(min)}}{3 \times \pi \times V_{IN(min)} \times \sqrt{2}} - 1} \quad (15)$$

2.5 Input Holdup Capacitor Selection

Due to the high ripple current of this PFC preregulator topology, holdup capacitance is required. However, if too much capacitance is added, it can cause an unwanted current phase shift. The capacitor is selected to provide half of the input current at low line maximum load when the boost inductor L1 is energizing for time t_{ON}.

$$t_{ON} = \frac{2 \times L1 \times P_{OUT}}{\eta \times V_{IN(min)}^{2}} \tag{16}$$

$$C5 >= \frac{\frac{P_{OUT} \times t_{ON}}{\eta \times 2}}{\left(V_{OUT(min)} \times \sqrt{2}\right)^{2} - \left[V_{OUT(min)} \times \sqrt{2} - V_{DROP}\right]^{2}} \tag{17}$$

2.6 Current Resistor Selection

The following equation can be used to size the current-sense resistor R7. The current-sense resistor should be selected to trip the peak current limit comparitor at 130% of the maximum output power. V_{CSENSE} is the peak current limit comparitor's threshold of 1.7 V.

$$R7 = \frac{V_{CSENSE}}{\frac{P_{OUT} \times 2 \times \sqrt{2}}{\eta \times V_{IN(min)}} \times 1.3} \tag{18}$$

2.7 Multiplier Setup

The multiplier is used to shape the input current waveform and must be set up correctly to get proper PFC. The multiplier was designed for a maximum input voltage range of 3:1. The multiplier's input is sensed from the rectified line voltage. Resistors R8, R5, R3 and C2 form a voltage divider and form a low pass filter. R8 and R5 were selected first and the following equations were used to properly size R3 for a 3 to 1 input range. A 1-nF capacitor (C2) was put in parallel with R3 to filter out high frequency noise.

$$V_{R3} = \frac{V_{C\_SENSE} \times (0.9)}{K \times \left(V_{EA(max)} - 2.5\ V\right)} - 0.075\ V \tag{19}$$

$$R3 = \frac{(R8 + R5)V_{R3}}{V_{IN(min)} - V_{R3}} \tag{20}$$

2.8 Voltage Loop Compensation

Figure 2 shows the small signal control block diagram for this application. The following equations describe each small signal gain block; as well as the voltage loop frequency response T_S.

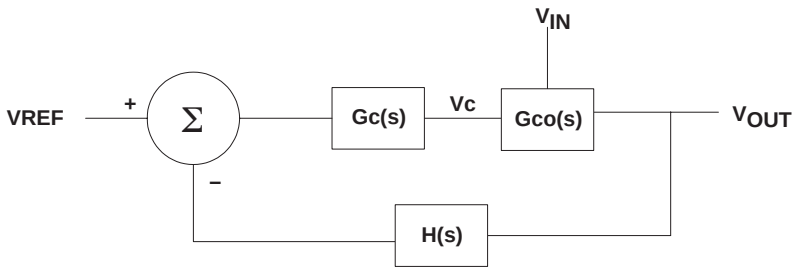


Figure 2. Small Signal Control

$$H_S = \frac{R1}{R1 + R2 + R9} \tag{21}$$

$$G_{C(s)} = gM \times \frac{(s(f) \times R13 \times C9 + 1)}{s(f) \times (C9 + C11) \times \left(\frac{s(f) \times C9 \times C11}{C9 + C11} + 1\right)} \tag{22}$$

$$G_{CO(s)} = \frac{\Delta V_{OUT}}{\Delta V_C} = \frac{k \times V_{IN}^{\ 2}}{s \times C3 \times V_{OUT} \times R7 \times 2} \times \frac{R3}{R5 + R8 + R3} \tag{23}$$

$$T_{S(f)} = -H(s) \times G_{C(s)} \times G_{CO(s)} \tag{24}$$

To reduce third harmonic distortion typically the voltage loop crosses over at roughly 10 Hz to 12 Hz. This design uses the voltage loop crossover (f_C) to be roughly 10 Hz at the maximum input voltage ($V_{IN(max)}$). The following equations were used to select the components to compensate the voltage loop $T_{S(f)}$ to crossover at the desired f_C with 45 degrees of phase margin.

$$R13 = 4 \times V_{OUT}^{\ 2} \times \pi \times f_C \times C3 \times R7 \times \frac{(R3 + R8 + R5)}{\left(V_{REF} \times V_{IN}(max)^2 \times R3 \times gm\right)} \tag{25}$$

$$C9 = \frac{1}{2 \times \pi \times R13 \times F_C} \tag{26}$$

C11 is selected to attenuate the 120-Hz output voltage ripple (V_{PP}) to 1.5% (%THD) of the dynamic range of the comp pin to the multiplier.

$$V_{PP} = \frac{\frac{P_{OUT}}{\eta}}{2 \times \pi \times 120\ Hz \times C12 \times V_{IN(min)}} \tag{27}$$

$$G_{VEA} = \frac{\%THD \times COMP}{V_{PP} \times 100} \tag{28}$$

$$C11 = H(s) \times gm \times \frac{1}{2 \times \pi \times \left(2 \times f_{LINE}\right) \times G_{VEA}} \tag{29}$$

When evaluating the control to output transfer function ($G_{CO(f)}$) it can be observed that the transfer function will change with line voltage (V_{IN}) which result in a change in T_S. After the components are selected it is a good idea to double check that the voltage feedback loop (T_S) is stable with changes in input voltage. After the design was complete the frequency response was measured with a network analyzer and the results are shown in Figure 4. From these results, it can be observed that at high line the phase margin was roughly 45 degrees with a cross over frequency of 8 Hz. These results were close to the design goal. at low line the phase margin was roughly 36 degrees with a crossover frequency of roughly 35 degrees. For this design having a phase margin greater than 35 degrees with changes in line voltage is acceptable.

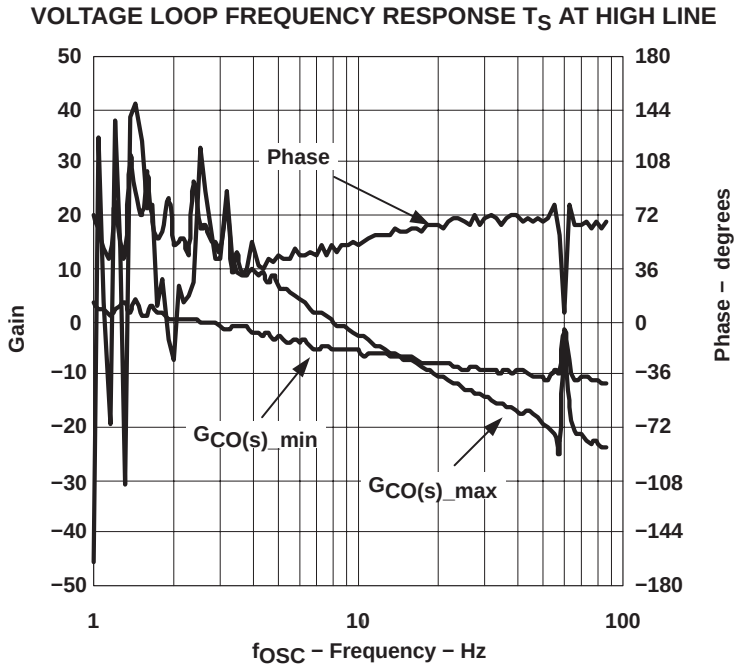


Figure 3.

3 Input Filter Design

The input of a critical conduction PFC preregulator is pictured in waveform A of Figure 4 to meet the less than 10% current THD design goal the input current waveform has to resemble clean sinusoid resembling waveform B of Figure 4. To achieve the current THD design goal an input filter had to be designed. The differential input filter required consists of electrical components C4, C3, L3, and L2.

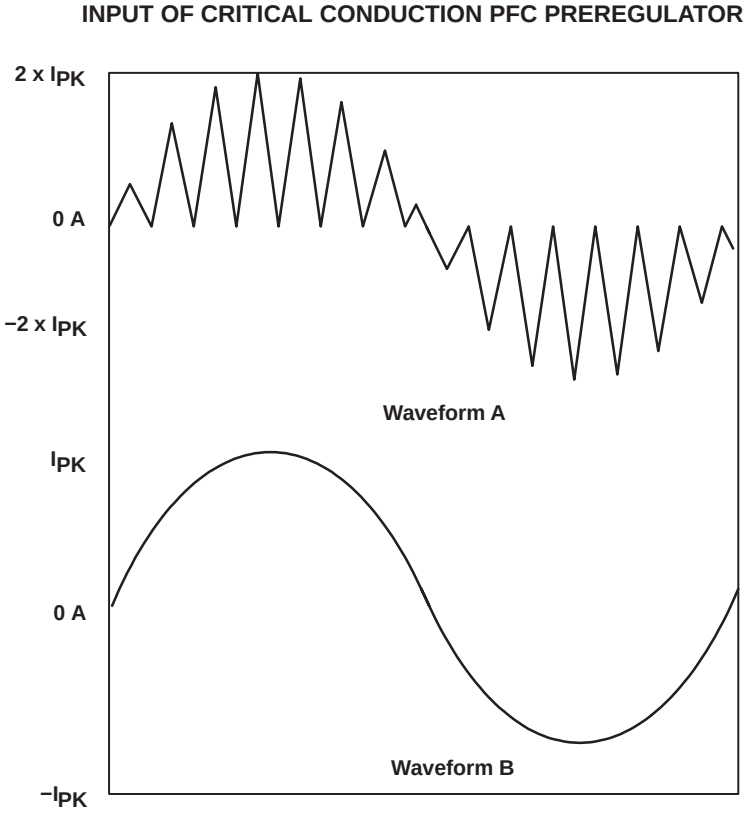


Figure 4.

The following equations can be used to properly design the input filter. The filter inductors (L2 and L3) are designed to ensure a smooth continues input current despite the changes in voltage of the input holdup capacitor C5. The differential mode input filter is bi-directional and the double pole frequency (f_P) can be set to attenuate high frequency noise.

$$L2 = L3 = \frac{\left(V_{IN(min)} \times \sqrt{2} - V_{DROP}\right) \times t_{ON}}{\frac{P_{OUT} \times \sqrt{2}}{\eta \times V_{IN(min)}}} \quad (30)$$

$$C4 = C8 = \frac{1}{\left(2 \times \pi \times f_P\right)^2 L1} \quad (31)$$

4 Design Performance

The following graphs show the measured performance of this application note.

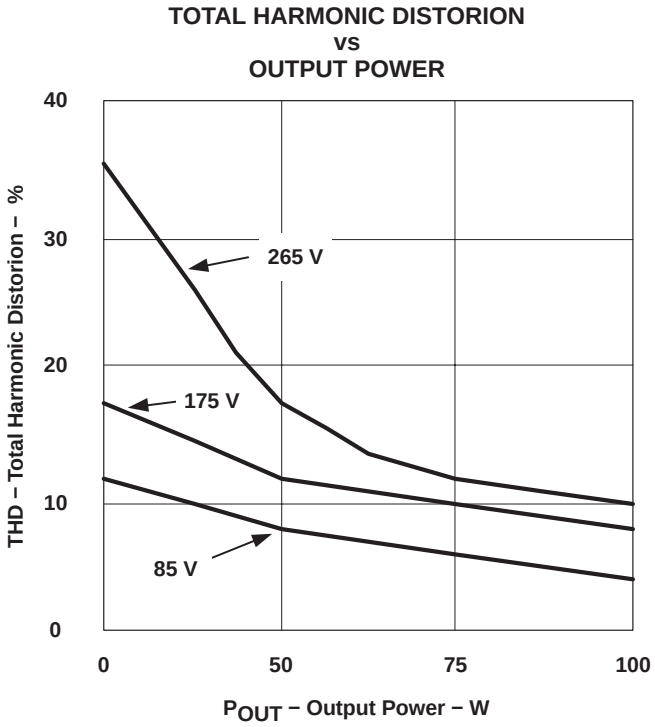


Figure 5

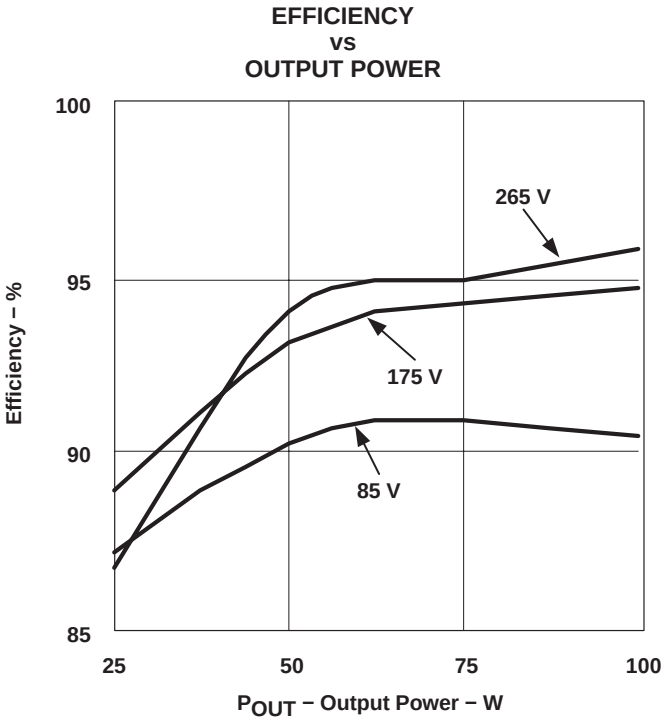


Figure 6

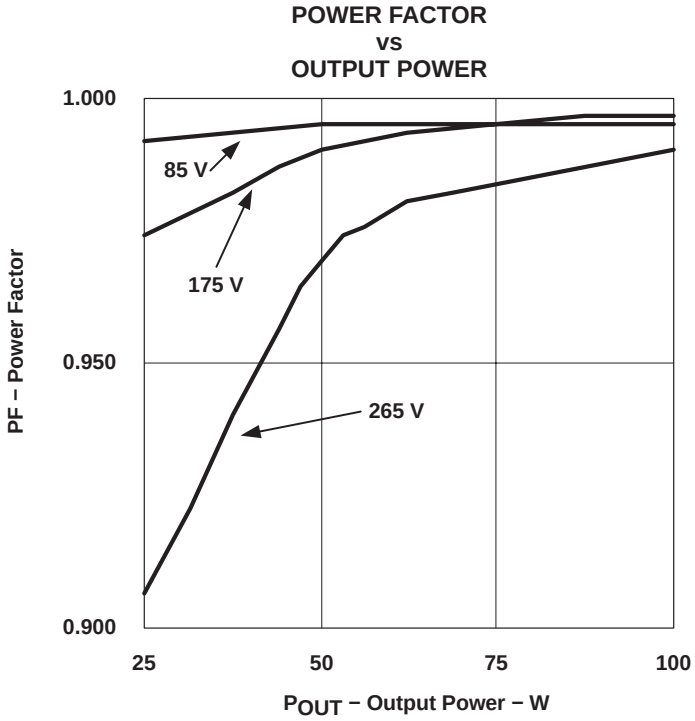
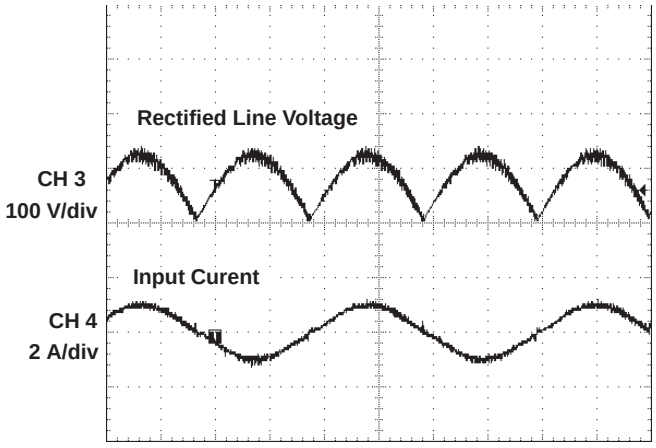


Figure 7

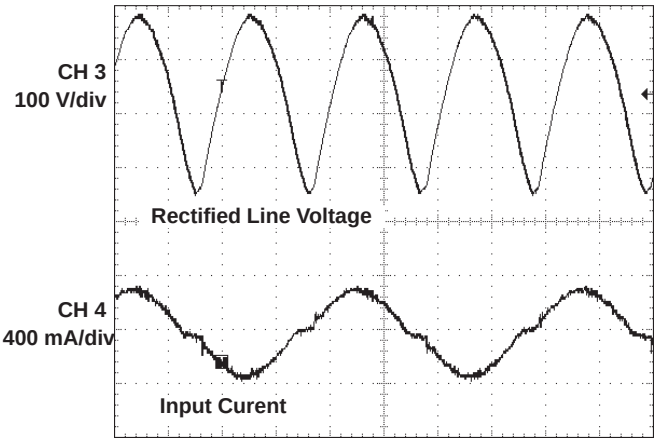
V_{IN} = 85 V, P_{OUT} = 100 W



t − Time − 4 ms/div

Figure 8

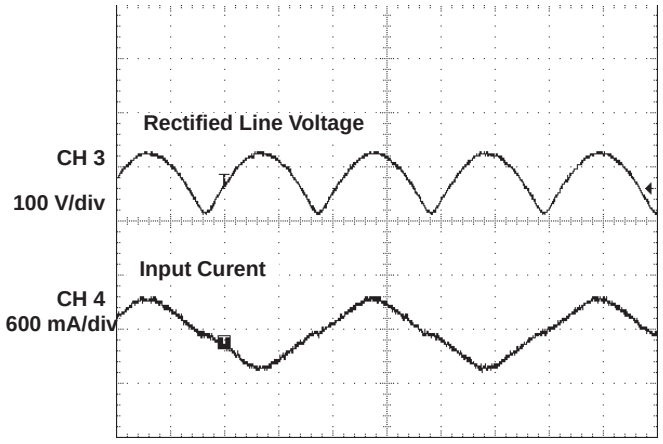
V_{IN} = 265 V, P_{OUT} = 100 W



t − Time − 4 ms/div

Figure 9

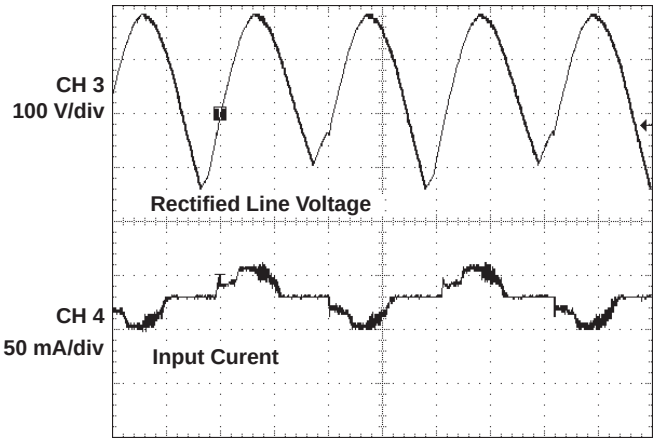
V_{IN} = 85 V P_{OUT} = 25 W



t − Time − 4 ms/div

Figure 10

V_{IN} = 265 V, P_{OUT} = 25 W



t − Time − 4 ms/div

Figure 11

5 Summary

With the UCC38050 Critical Conduction PFC Control device and a carefully designed input filter we were able to reach the design goal of less that 10% THD at full load for a universal input range. This design would meet the input current requirements of EN61000−3−2 while using fewer components than a solution using average current mode control topology.

6 References

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