



## ABSTRACT

This user's guide describes the characteristics, operation, and use of TI's evaluation module (EVM) for the TPS628690, TPS628680 devices. The TPS628690EVM-135 (BSR135) facilitates the evaluation of the TPS628690, 6-A step-down converter with DCS-Control™ in a small 1.5-mm by 2.5-mm QFN package solution. The EVM creates output voltages between 0.2 V and 0.8375 V with 1% accuracy output voltages from higher input voltages between 2.4 V and 5.5 V. The TPS628690 is a highly efficient and tiny solution for point-of-load (POL) converters for space-constrained applications, such as artificial intelligence chips, camera modules, solid state drives (SSDs), LPDDR5 memory, and optical modules.

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## Trademarks

DCS-Control™ is a trademark of TI.

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## 1 Introduction

The TPS628690 is a synchronous, step-down converter, coming in a 1.5- × 2.5- × 1.0-mm QFN package.

### 1.1 Performance Specification

[Table 1-1](#) provides a summary of the TPS628690EVM-135 performance specifications.

**Table 1-1. Performance Specification Summary**

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		2.4	5	5.5	V
Output voltage setpoint		0.2	0.5	0.875	V
Output current		0		6000	mA

### 1.2 Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate the different adjustable output voltage versions of this integrated circuit (IC). On the EVM, additional input and output capacitors can be added.

## 2 Setup

This section describes how to properly use the TPS628690EVM-135.

### 2.1 Input/Output Connector Descriptions

- J1, Pin 1, 2 and 3– VIN** Positive input connection from the input supply for the EVM
- J1, Pin 4, 5 and 6 – GND** Input return connection from the input supply for the EVM
- J2, Pin 1 ,2 and 3– VOUT** Output voltage connection
- J2, Pin 4, 5 and 6 – GND** Output return connection
- J3, Pin 5 – VBUS** The VBUS pin of this header is used to bias the SCL and SDA nodes of I<sup>2</sup>C interface via a resistor.
- J3, Pin 6 – GND** The GND pin of this header is used to connect the grounds of the IC and the I<sup>2</sup>C interface.
- J3, Pin 9 – SCL** Connect the pin of this header to the SCL of the I<sup>2</sup>C interface.
- J3, Pin 10 – SDA** Connect the pin of this header to the SDA of the I<sup>2</sup>C interface.
- JP1 – VID/PG** VID/ PG pin jumper. Place the jumper across VID/ PG and LOW pins before start-up. This sets the output voltage and device address. After start-up, V<sub>OUT</sub> reflects the value set on V<sub>OUT</sub> Register 1 if the jumper is placed across VID/ PG and LOW pins. V<sub>OUT</sub> follows the value set on V<sub>OUT</sub> Register 2 if the jumper is placed across VID/ PG and HIGH pins.
- JP2 – EN** EN pin input jumper. Place the jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC.

### 2.2 Setup

To operate the EVM, set jumpers JP1 and JP2 to the desired position per [Section 2.1](#). Connect the input supply to J1 and connect the load to J2.

### 3 TPS628690EVM-135 Test Results

The TPS628690EVM-135 was used to take the typical characteristics of TPS628690 in the [TPS62868x 2.4-V to 5.5-V Input, 4-A/6-A Synchronous Step-Down Converter with I2C Interface in QFN Package Data Sheet](#). See the device data sheet for the performance of this EVM.

### 4 Board Layout

This section provides the TPS628690EVM-135 board layout and illustrations in [Figure 4-1](#) through [Figure 4-7](#). The Gerbers are available on the EVM product page: [TPS628690EVM-135](#).

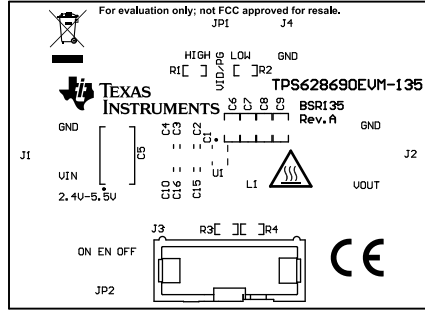


Figure 4-1. Top Assembly

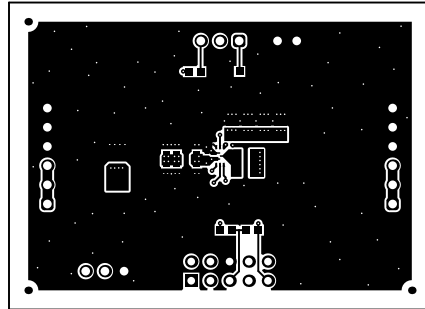


Figure 4-2. Top Layer

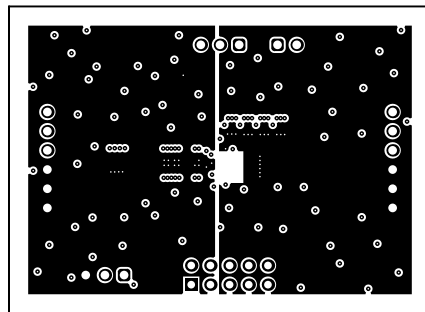
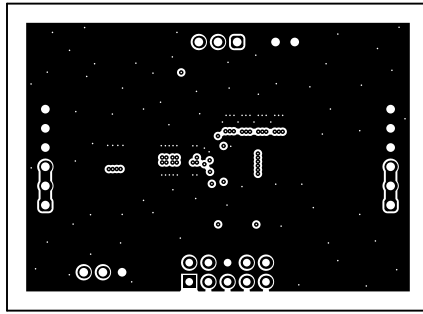
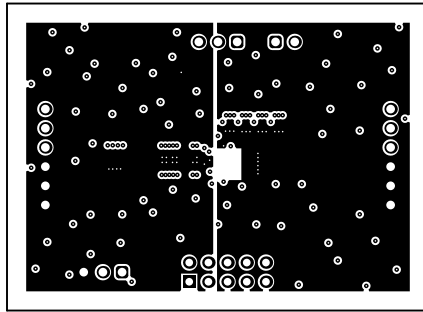


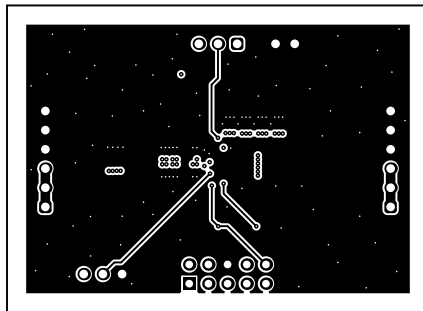
Figure 4-3. Signal Layer 1



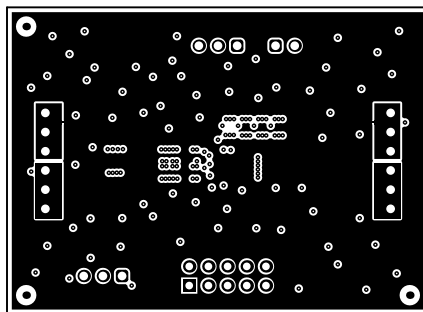
**Figure 4-4. Signal Layer 2**



**Figure 4-5. Signal Layer 3**



**Figure 4-6. Signal Layer 4**



**Figure 4-7. Bottom Layer**

## 5 Schematic and List of Materials

This section provides the TPS628690EVM-135 schematic and list of materials.

### 5.1 Schematic

Figure 5-1 illustrates the EVM schematic.

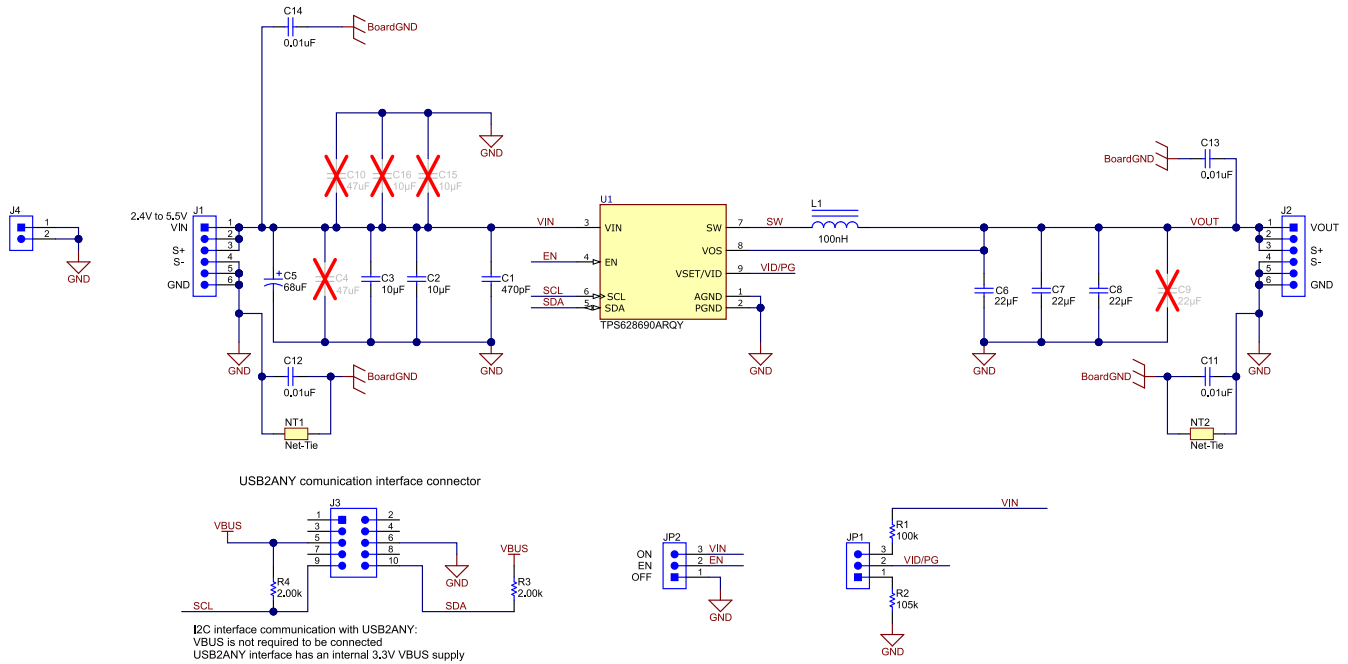


Figure 5-1. TPS628690EVM-135 Schematic

### 5.2 List of Materials

Table 5-1 displays a list of materials for this EVM.

Table 5-1. TPS628690ARQY List of Materials

DESIGNATOR	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
C1	1	Capacitor, Ceramic, 470 pF, 25V, $\pm 5\%$ , C0G/NP0, 0402	GRM1555C1E471JA01D	Murata
C2, C3	1	Capacitor, Ceramic, 10 $\mu$ F, 10 V, $\pm 10\%$ , X7R, 0603	GRM188Z71A106KA73D	Murata
C6, C7, C8	2	Capacitor, ceramic, 22 $\mu$ F, 6.3 V, $\pm 20\%$ , X7R, 0805	GRM21BZ70J226ME44L	Murata
C5	1	Capacitor, tantalum, 68 $\mu$ F, 20 V, $\pm 10\%$ , 7343	T495D686K020ATE150	Kemet
L1	1	Inductor, 100 nH, 28.5 A, 2.04 m $\Omega$ , SMD, 4020	XEL4020-101MEB	Coilcraft
R1	1	Resistor, 100 k $\Omega$ , 1%, 0.1 W, 0603	Std	Std
R2	1	Resistor, 105 k $\Omega$ , 1%, 0.1 W, 0603	Std	Std
R3, R4	2	Resistor, 2.0 k $\Omega$ , 1%, 0.1 W, 0603	Std	Std
U1	1	6-A Step-Down Converter with I <sup>2</sup> C Interface and Wide Output Voltage Range, QFN - 9 Pins	TPS628690ARQY	Texas Instruments

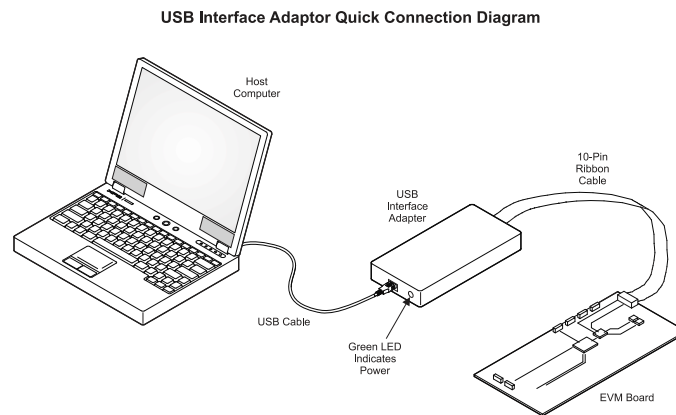
## 6 Software User Interface

### 6.1 Software Setup

A graphical user interface (GUI) is available from the [TPS62869 tools and software page](#), which allows simple and convenient programming of the device through the [TI USB2ANY](#) interface board. Alternatively, you can use any I<sup>2</sup>C-standardized programming tool or I<sup>2</sup>C host to configure the device. Mind the I<sup>2</sup>C pins specification, such as timing parameters and proper pullup resistors, specified in the [TPS62868x 2.4-V to 5.5-V Input, 4-A/6-A Synchronous Step-Down Converter with I2C Interface in QFN Package Data Sheet](#).

### 6.2 Interface Hardware Setup

Connect the USB2ANY adapter to your PC using the supplied USB cable. Connect the EVM connector J3 to the USB2ANY adapter using the supplied 10-pin ribbon cable. The connectors on the ribbon cable are keyed to prevent incorrect installation. [Figure 6-1](#) shows a quick adapter connection overview.



**Figure 6-1. Quick Connection Overview**

## 6.3 User Interface Operation

Upon start-up, the GUI automatically connects to the EVM. If not, click on the *Connect* button in the upper right corner of the GUI window. Ensure the I<sup>2</sup>C Slave Address is correct. The following sections give a short overview of the two main GUI screens.

### 6.3.1 Home Screen

The *Home* screen gives a short overview of the TPS62869 devices. To start evaluating the device, click on the *Start* button or on the *Settings* icons on the left side of the GUI window.

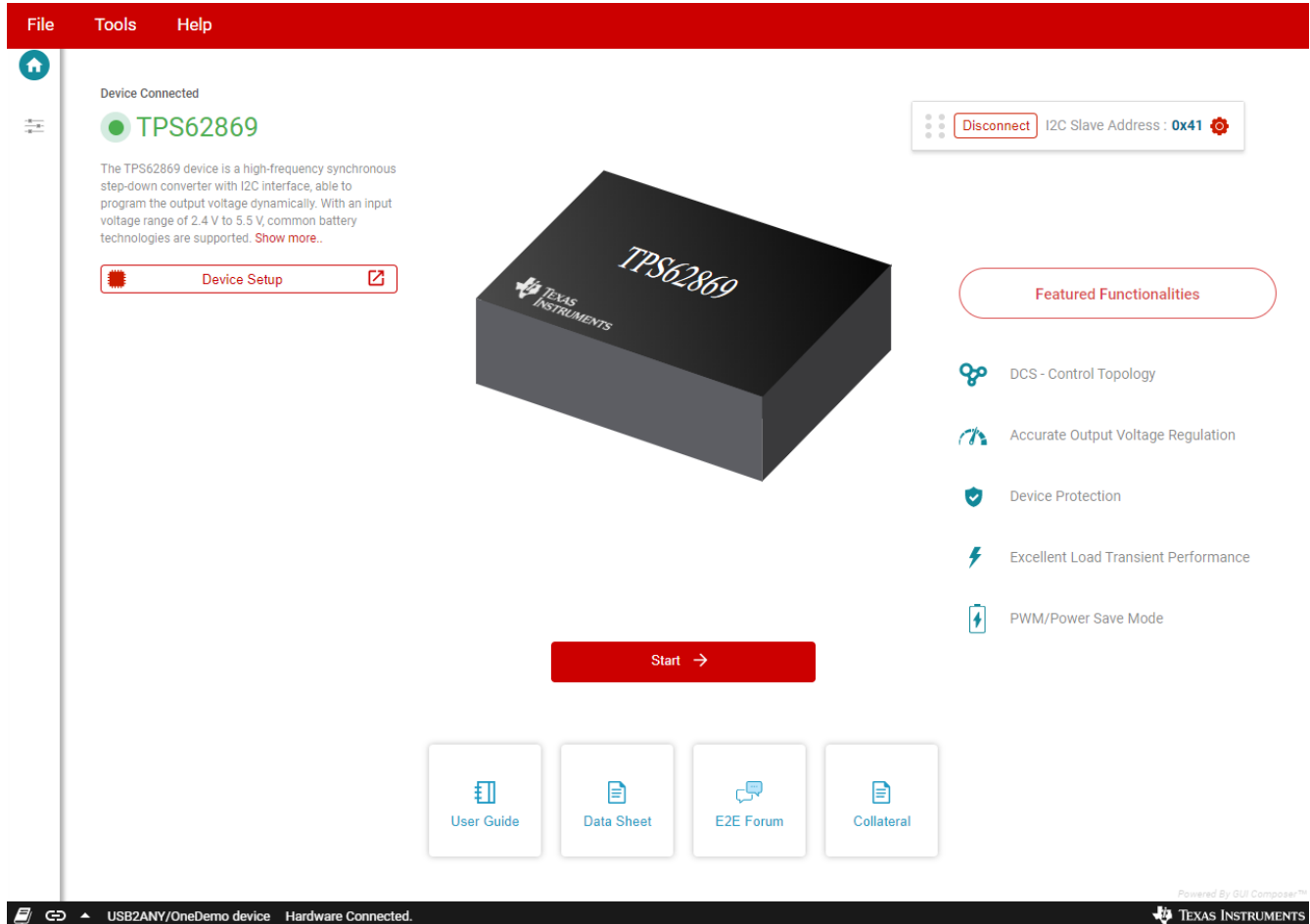


Figure 6-2. GUI Home Screen

### 6.3.2 Settings Screen

The [Settings](#) screen provides control over the output voltage and operating modes of the TPS62869. The [Register Map](#) at the bottom shows a register-wise view of all parameters. Here, single registers can be read or written to the device (if applicable). Refer to the register map in the [TPS62868x 2.4-V to 5.5-V Input, 4-A/6-A Synchronous Step-Down Converter with I2C Interface in QFN Package Data Sheet](#) for a detailed description of the TPS62869 registers.

**Power Saver Mode** | Fault Status: Temperature Good, Input Voltage > UVLO Threshold, No Hiccup

Reset | Shutdown Device

**Output Voltage Selection** | I2C Slave Address: 0x41

Device Output Voltage: **VOUT2** | Switch to VOUT1 | VOUT2 register sets the output voltage when VID/P<sub>̄</sub>G pin is high

**VOUT1**

400 720 1040 1360 1675 | 900 mV

**VOUT2**

400 720 1040 1360 1675 | 900 mV

**Control Functions**

Power Saver Mode

Forced PWM Mode

Voltage Ramp Speed: 1 mV/µs (5 µs/step)

Enable Hiccup

Enable Output Discharge

Enable FPWM Mode during output voltage change

**Register Map** | Auto Read: Off | READ REGISTER | READ ALL REGISTERS | WRITE REGISTER | WRITE ALL REGISTERS | Immediate Write

Register Name	Address	Value	Bits								
			7	6	5	4	3	2	1	0	
Registers											
VOUT1	0x01	0x64	0	1	1	0	0	1	0	0	
VOUT2	0x02	0x64	0	1	1	0	0	1	0	0	
CONTROL	0x03	0x6F	0	1	1	0	1	1	1	1	
STATUS	0x05	0x06	0	0	0	0	0	0	1	1	0

USB2ANY/OneDemo device | Hardware Connected. | TEXAS INSTRUMENTS

Figure 6-3. GUI Settings Screen



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