# Using Advanced Features of the bq2060 Gas-Gauge IC

PMP Portable Power

**ABSTRACT**

The bq2060 is a Smart Battery System (SBS) 1.1-compliant gas-gauge IC for battery-pack or in-system installation. It maintains an accurate record of available charge in rechargeable NiCd, NiMH, Li-Ion, Lead Acid, and other battery chemistries. This application note provides additional information and recommendations for the following:

- Voltage-to-frequency converter offset calibration and digital-filter threshold setting
- System standby load-current measurement or estimate
- Capacity learning algorithm
- Programming recommendations
- Battery and individual cell-voltage measurements

**Contents**



Software routine names, register names, and software storage locations mentioned in this report are set in *Italics*.

# Voltage-to-Frequency Converter Offset Calibration and Digital-Filter Threshold Setting

The bq2060 has automatic offset-cancellation circuitry to measure the charge into and out of the battery pack. It allows effective measurement of offset values one tenth of the minimum offsets measurable by previous Texas Instruments (Benchmarq) gas-gauge ICs, providing more-accurate estimates of available battery capacity to the end user.

Like earlier gas-gauge ICs, the bq2060 has a digital filter (DMF) to prevent the bq2060 from falsely interpreting an offset voltage as an indication of capacity added to or removed from the battery. The DMF in the bq2060 may be set to a much smaller value than in previous gas-gauge ICs. The recommended bq2060 DMF threshold setting for most applications is 50 µV. The bq2060 IC itself can be calibrated to a typical offset of less than 5 µV. This value may double with changes in operating voltage and temperature. The added offset from a well-designed printed circuit board (PCB) is typically less than 15 µV. The designer can characterize the PCB offset to confirm the proper DMF setting. For best results, set the DMF value slightly higher than the total circuit (IC and PCB) offset.

| | |
|---|---|
| bq2060 IC Offset after Calibration | 10 µV |
| Well-designed PCB Offset | 15 µV |
| Total (IC and PCB) Offset | 25 µV |
| Typical DMF Setting | 50 µV |

The bq2060 can also be calibrated to cancel the total (IC and PCB) circuit offset for better measurement accuracy and a lower DMF setting.

## VFC Calibration Procedure

Two VFC calibration commands can be written to *ManufacturerAccess()* (Command Code 0x00) to initiate an automatic VFC calibration. One command cancels the IC offset, and the other cancels the total circuit (IC + PCB) offset. The automatic calibration routine measures the time between two output pulses generated by the bq2060 VFC to determine the offset correction to apply. The lower the offset, the longer the calibration time will be. The bq2060 has a calibration-time limit of 1 hour. If the 1-hour time-out is exceeded without sensing two VFC output pulses, the bq2060 imposes a correction equivalent to +0.6 µV offset. Typical offsets of 50 µV allow the VFC calibration process to complete in 3.75–7.5 minutes.

If VFC calibration is the last test step for a battery pack, the test controller can issue a SEAL command to *ManufacturerAccess()* after the VFC calibration is initiated to put the pack into the access-protected state required for Smart Battery Data (SBD) 1.1 compliance. Access protection prevents initiation of the VFC calibration sequence to prevent unauthorized or unintended calibration. The *ManufacturerAccess()* SEAL command does not set the *SEAL* bit in *Pack Configuration* in the EEPROM. Set this bit in the EEPROM prior to sending the VFC offset calibration command

Once started, calibration completes automatically. The battery pack can be removed from the tester as soon as the calibration is initiated. The offset-calibration values calculated by the bq2060 are automatically stored in bq2060 RAM and the *VFC Offset* location in EEPROM, and offset cancellation is enabled.

Calibration can be done at the circuit module test instead of the battery-pack test, but the module must remain powered on until calibration is complete. For this reason, it is most practical to calibrate the VFC as the last step in the battery-pack test, rather than as part of a circuit-module test before pack assembly.

### *VFC Calibration Options*

The two calibration commands that can be written to *ManufacturerAccess()* for the bq2060 are:

- 0x0653 for the offset of only the bq2060 IC
- 0x067e for the offset of the bq2060 IC and the PCB

Calibrating only the IC offset is accurate enough for most applications. The bq2060 automatically disconnects the sense-resistor inputs during the calibration, and thus ignores any charge or discharge currents that might be applied during the calibration process. This way, unintentional charge or discharge activity does not disrupt accurate calibration of the unit. This calibration method does not account for external PCB-offset influences. A well-designed PCB does not add significant offset. This calibration method generally yields an effective offset less than 25 µV, with a typical value less than 20 µV. The recommended DMF threshold for this calibration method is 50 µV.

The calibration of both IC and PCB offset yields the best measurement accuracy. It requires that the manufacturer ensure that no charge or discharge currents occur until a complete calibration is verified, or after 1 hour following a VFC-calibration start. This method generally yields an effective offset less than 15 µV, with a typical value less than 10 µV. The recommended DMF threshold for this calibration method is 35 µV.

## PCB Offset Evaluation

If the PCB offset is very large, variations due to operating environment are also likely to be large. Therefore, offset cancellation may not yield sufficient accuracy under all conditions. A well-designed PCB adds less than 15 µV to the IC offset. An easy way to characterize the PCB design is to calibrate only the IC offset, followed by calibrating the combined IC and PCB offset. The PCB offset is the difference in the two measurements.

The measured VFC offset initiated with either calibration command is stored by the bq2060 in *VFC Offset* in EEPROM after the calibration, and can be read by the designer. The offset in volts is determined by 0.6/N, where N is the decimal value of the least 20 bits (b19-b0) of this 24-bit word. For example, a 50 µV offset has a value for N of 12000. Bit 20 of this word is the sign bit for the correction value. Bits 21–23 are control bits and are set to 101 after a successful calibration. Thus a negative (discharge) offset of 50 µV has a hex value of 0xA02EE0 (positive 50-µV correction value, bit 20 = 0) stored in EEPROM after calibration.

## System Standby Load Current Measurement or Estimate

There are three methods for accounting for a low-value load current (<2 mA) that may exist for extended periods. If this current is not accounted for, or is measured inaccurately, it can lead to a corresponding inaccuracy in the remaining capacity reported by the bq2060.

### Normal Measurement Method

The normal measurement method uses a sense-resistance value high enough to ensure that the signal across it during the minimum light-load condition is above the DMF threshold. This method is the only option for systems that cannot force the SMBus clock and data lines high during suspend or low host-load conditions.

If the host-suspend current is 2 mA and the bq2060 circuit uses a 50-mΩ sense resistor, the current produces a 100-µV signal. That signal is well above the recommended 50-µV DMF threshold and is measured by the bq2060 with a typical effective-offset error of less than 20 µV, as achieved with the IC-only offset calibration.

If the minimum load current is smaller and system requirements dictate a smaller sense resistor, the VFC offset can be calibrated to include the PCB offset contribution as described previously. This calibration allows a lower DMF threshold, typically 35 µV. A 1.5-mA load current with a 30-mΩ sense resistor yields a 45-µV signal, and is measured by the bq2060 with an effective offset error of less than 10 µV. To measure minimum signal levels of less than 40 µV, the DMF bypass option is recommended.

### Digital Filter Bypass Option

If the low signal level is less than 40 µV and the system can hold the SMBus clock and data lines high during the low-load condition, then the digital-filter bypass option allows the bq2060 to measure the light load without setting the DMF too low. At very low settings (<35 µV), the DMF may not effectively filter erroneous charge or discharge signals when the battery pack is not being used.

The DMF bypass option allows the DMF filter to be set to 50 µV, even if the low-current signal is below 50 µV. With this option, the DMF is automatically set to zero for discharge-current measurements when the SMBus clock and data are pulled high. If the host system is discharging the battery during normal use, the signal levels are always above the DMF threshold and the bypass causes no additional error. When a light-load condition exists and SMBus clock and data are pulled high, the bq2060 measures the light load without the DMF. With a typical offset less than 10 µV, depending on the VFC calibration method used, the bq2060 accurately measures signal levels below the normal DMF threshold setting.

The smaller the low current signal, the greater the measurement error, but measuring a 1-mA load with a 30-mΩ sense-resistor is more accurate than not measuring the signal at all. Without measurement of the 1-mA leakage, the battery drains at 24 mAh per day while the system is in this light-load condition with no corresponding reduction in *RemainingCapacity()*. In this case, the battery is empty before the gauge reports it, causing an unpleasant surprise to the user.

If the DMF bypass option is used under the above conditions, a 10-µV offset might indicate a 40-µV signal instead of the actual 30-µV signal. This value yields a capacity-reduction rate of 1.33 mA instead of 1.0 mA, and the gauge would reduce the battery capacity by 32 mAh each day instead of by 24 mAh. The resulting 8-mAh error per day in this example would send a slightly premature warning of an empty condition.

The error is reduced if a larger sense resistor is used. A 50 mΩ sense resistor reduces the measurement error to less than 4.8 mAh per day. This error is comparable to or lower than the self-discharge rates of many battery packs used in light-load applications.

### Light-Load Estimation Option

The light-load estimation option is useful if the low-value load current is constant, but is too small to measure accurately. This option requires holding the SMBus clock and data high during the light-load condition. This option is not recommended if the AC adapter can be plugged in during the light-load condition, unless the charger responds to *ChargingCurrent()* broadcasts from the bq2060.

The estimated light-load current may be programmed into *Light Discharge Current* in the EEPROM. When the bq2060 detects that SMBus clock and data signals are high and that no charge or discharge activity greater than the DMF threshold is measured, the bq2060 applies the estimated load-current value stored in EEPROM to its capacity calculation. If normal charge or discharge activity above the DMF threshold is detected, or if SMBus clock and data are low, there is no estimated load-current correction.

A potential problem with the light-load estimation procedure arises when an AC adapter supplies the light load after charging the battery to full in a system with a lithium-ion battery. The bq2060 cannot tell that the charger is supplying the light load and applies the estimated light-load compensation even though the battery is not supplying the current. However, if *Fully Charge Clear %* is programmed to a high value, this error is restricted to a small value. For example, if *Fully Charge Clear %* were programmed to 100% and the light-load estimation were 1 mA, the bq2060 would request charging current and turn the charger on as soon as the bq2060 had applied enough load compensation to reduce *RemainingCapacity()* by approximately 0.5%. The charger would turn on for about 1 minute, and the bq2060 would again determine that the battery was full and shut off the charger. This burp charge would occur every 20 hours with a 4000-mAh battery pack. The error in this case is limited to less than 1%. *Fully Charge Clear %* could be reduced to 99%, resulting in an error value of less than 2%. A *Fully Charge Clear %* value of less than 99% is not recommended if the light-load-estimation option is used, unless the AC adapter does not supply power during the system light-load condition.

AC supply is not a problem with NiMH or NiCd chemistry battery packs, because the AC adapter always supplies maintenance-charge current to the battery greater than the DMF threshold.

## Capacity Learning Algorithm

The bq2060 allows more battery-discharge, capacity-learning opportunities during normal operation than previous Texas Instruments (Benchmarq) gas-gauge ICs. The bq2060 can be programmed to learn a large portion of the battery discharge capacity, then add the portion of the discharge curve that was not measured. The bq2060 learning cycle is valid as long as the battery is charged above a programmable upper-end learning threshold, and is then discharged below a programmable low-end threshold without an intervening disqualifying event.

## Top- and Low-End Learning Thresholds

A top-end learning threshold may be established by programming the *Near Full* value into EEPROM. If *RemainingCapacity()* reaches the minimum programmed threshold value determined by *FCC – Near Full* × 2 before discharge, the Valid Discharge Qualification (*VDQ*) flag bit in *Pack Status* is set. The bq2060 learns the discharge capacity of the battery if *VDQ* remains set until the full discharge is completed and the next charge cycle begins.

The bq2060 takes the difference of *FullChargeCapacity()* (*FCC*) and *RemainingCapacity()* at the beginning of the discharge and pre-loads that value into the *Discharge Count* Register (*DCR*). The *DCR* then counts the charge removed as the battery is discharged, adding the actual discharge capacity removed from the battery to the initial pre-loaded value. The *DCR* stops counting when the bq2060 determines that the battery has been discharged to the *EDV2* threshold. The capacity associated with *EDV2*, computed from *Battery Low %*, is then added to *DCR* to account for the unmeasured discharge capacity remaining in the battery. When charging starts again and a valid charge is detected (10mAh), the *DCR* value is transferred to *FCC* if the *VDQ* bit is still set. The new value for *FCC* is limited to a maximum reduction in one learning cycle of 256 mAh, or to a maximum increase in one learning cycle of 512 mAh.

*VDQ* remains set throughout the discharge cycle unless a learning-cycle disqualifying event occurs. These events include

- Any fractional charge greater than 10 mAh
- A low-temperature fault (T<5°C)
- Self-discharge estimation plus light-load current estimation amounts exceeding 256 mAh
- Voltage dropping so fast at *EDV2* that the voltage is at least 256 mV below the *EDV2* threshold at the time the threshold is detected
- No midrange voltage correction occurs during the discharge

These disqualifying events are designed to keep learning cycles from being declared during unusual discharge circumstances.

## Adaptive Learning Algorithm

Pre-loading the DCR value to *FCC – RM* (initial) at the beginning of a discharge cycle describes the exact operation, if the SC bit in Control Mode is programmed to a “1” to disable the adaptive learning-algorithm option. If the SC bit is programmed to a “0”, the learning algorithm is modified slightly. The initial value pre-loaded into *DCR* at the beginning of discharge, *FCC – RM* (initial) value, is reduced by *FCC* / 128 (0.78% of *FCC*). This reduction allows the learned *FCC* value to ‘creep down’ by 0.78% of *FCC* each learning cycle until *RemainingCapacity()* is equal to *FCC* at the beginning of the discharge. Thus, a dumb (non-SBS-compliant) charger that terminates the charge before reaching the programmed detection limit in the bq2060, still allows the bq2060 to reduce *FCC* each learning cycle. Using this technique, capacity fade of the battery does not cause the *FCC* value to remain artificially high, ultimately preventing a dumb charger from charging the battery above the top-end learning threshold required for *FCC* learning.

# Programming Recommendations

## Learning Algorithm

If a Smart Charger (SBS compliant) is used, and the battery can be charged to full if left on charge for sufficient time, there is no need to use the adaptive-learning algorithm. If a dumb charger is used that has been characterized to terminate after the programmed bq2060 termination conditions, there is also no need to use the adaptive-learning algorithm, and the *SC* bit can be programmed to 1.

The adaptive-learning algorithm is useful with a charger that might not charge the battery to 100% even when connected for an extended period. The adaptive-learning algorithm allows the learned-capacity reference *FCC* to creep down until it equals the actual capacity that is put into the battery at charge termination. This prevents the bq2060 from using an inflated full-charge reference when the charger has marginal ability to charge the battery above the minimum capacity required for learning. Programming the *SC* bit in *Control Mode* to 0 selects this adaptive-learning mode.

The adaptive learning algorithm is not recommended if a relatively large top-end learning threshold (0.1–0.25 C) is set, and if the user may frequently disconnect the charger before the battery is full. This situation could allow an unintentional reduction in *FCC*.

## Charge Synchronization

The *CSYNC* bit in *Pack Configuration* is normally programmed to 1 to allow the bq2060 to adjust *RemainingCapacity()* to the *Fast Charge Termination %* of *FCC* when the bq2060 detects a full-charge termination condition. This is true when using a smart charger, and most applications should also have *CSYNC* set even when a dumb charger is used.

### *Lithium Ion*

For lithium-chemistry cells, program *Fast Charge Termination %* to 100% so that the bq2060 adjusts *RemainingCapacity()* to *FCC* when taper termination is detected. *Maintenance Charging Current* is generally programmed to zero, as most lithium cells suffer capacity loss if continually trickle-charged.

### *Nickel Chemistries*

For nickel-chemistry cells, *Fast Charge Termination %* is typically programmed to less than 100% with additional trickle charging provided by *Maintenance Charging Current*. *Fast Charge Termination %* must be programmed to a value high enough for the battery to achieve 100% capacity within a reasonable time on trickle charge. If *Maintenance Charging Current* is only enough to supply the expected self-discharge of the cells, then set *Fast Charge Termination %* to 100%.

A smart charger with sufficient output to charge the battery to full normally does not use the adaptive learning algorithm. The adaptive learning algorithm is recommended for any charger that may consistently terminate before the bq2060 detects a termination condition, or before *RemainingCapacity() = FCC*, to prevent the use of an inflated full charge reference.

## Battery and Individual Cell Voltage Measurements

The bq2060 measures either the overall battery voltage, without connection to individual series cells, or up to 4 series-cell voltages in a lithium-ion battery pack in addition to the overall battery voltage. The bq2060 measures the voltage at the top of the battery-cell stack and subtracts the voltage across the sense resistor, so that the reported battery voltage is only the voltage across the cell stack. Individual cell voltages are determined by subtracting the voltages measured at each node of the battery connected to the bq2060. The bq2060 provides control for optional external FET switches that turn on with a low 12.5% duty-cycle during voltage measurements to allow reduction of current drain from the voltage dividers during normal operation, and also during sleep mode. The simple circuit techniques described below avoid imbalance currents that might be drawn by the voltage dividers from the individual cell connections.

### No Individual Cell Voltage Measurement

A voltage divider from the top of the battery to VSS of the bq2060 provides a fraction of the battery voltage to the VCELL4 input. The voltage divider is sized to prevent the voltage at VCELL4 from ever exceeding 1.25 V. The voltage-reduction ratio of the divider (VBAT/VCELL4) is programmed in EEPPROM for the ADC Voltage-Gain factor. Voltage calibration of the circuit module adjusts this value to accommodate resistor and IC tolerances. The *LCC1* and *LCC0* program bits in *Pack Configuration* are both programmed to 0 to select the option for no individual cell measurement for either lithium- or nickel-chemistry cells.

### Individual Cell Voltage Measurement

Measurement of individual cell voltages requires voltage dividers at the top and at each series cell-connection node in the battery pack. These dividers connect to the bq2060 VCELL4–VCELL1 inputs. Each cell-voltage measurement input must be limited to 1.25 V. To allow proper calibration of the cell inputs, the voltage ratios (not the resistance ratios) for the VCELL3 and VCELL4 inputs must be the same and the voltage ratios for the VCELL1 and VCELL2 inputs must be the same. Furthermore, the voltage ratios for the VCELL3 or VCELL4 inputs must be twice the ratio for the VCELL1 or VCELL2 inputs. The recommended ratios are 16:1 voltage-reduction ratios (top divider resistor equals 15 $\times$ the bottom divider resistor) for VCELL3 and VCELL4 and 8:1 voltage reduction ratios (top divider resistor = 7 $\times$ bottom divider resistor) for VCELL1 and VCELL2. Slight tolerance variations or non-exact ratios are calibrated out by adjustments stored in EEPROM during calibration.

*LCC1* and *LCC0* are programmed to inform the bq2060 how many cells are connected. If the battery pack has fewer than four series cells, some VCELL inputs are not used. VCELL4 is not used for a three-series-cell pack, and neither VCELL3 nor VCELL4 are used for a two-series-cell pack. A single-cell battery pack uses the connection method for no individual cell measurement and uses the VCELL4 input.

## Avoiding Cell Imbalance Currents

Attaching voltage dividers to the nodes between series-connected cells causes the lower cells to deliver more current than the upper cells unless additional circuitry is added to supply the current to the voltage divider. Resistors can be added from the top of the battery to provide the appropriate current and to reduce or eliminate the imbalance currents from the intermediate battery-connection nodes. If resistors at the top of each voltage divider draw the same current as the voltage divider when all cell voltages are equal, there is no imbalance current from the intermediate node connection. If cell voltages are not equal, the imbalance current in the node connection will be in the direction to apply a heavier load to the higher-voltage cells and a lighter load to the lower-voltage cells.

The passive resistor network provides a mechanism for balancing the cell voltages. The circuit shown in Figure 1 is an example network that does not create imbalance currents in the battery pack. If a two- or three-series-cell battery pack is used instead of a four-series-cell pack, the resistors connected to the upper cells are deleted and none of the remaining resistor values are changed to maintain a balanced current configuration.

Note that the cell-current balancing network develops voltages at the cell tap connections that are approximately the same voltage as the battery voltages at that tap. If balancing resistors Rx, Ry, and Rz are used, they may prevent detection of a broken cell-tap connection by the lithium-ion protection circuit.

## Reducing Current Draw from Voltage Dividers

The bq2060 control for external FET switches reduces the average current draw from the battery by the voltage dividers. The duty cycle for the FET-switch control is 12.5% or less. Using the example voltage divider circuit without FET switches causes a total current draw of 29.2 µA from the four-series-cell battery at a nominal 14.4 V. The current is 20.2 µA for a three-series-cell battery. FET switches reduce the overall voltage-divider plus switching-circuit average current drain from 29.2 to 6.8 µA for the four-series-cell battery using the components shown. Current drain from the voltage divider plus control circuitry is further reduced in sleep mode to 2.2 µA.

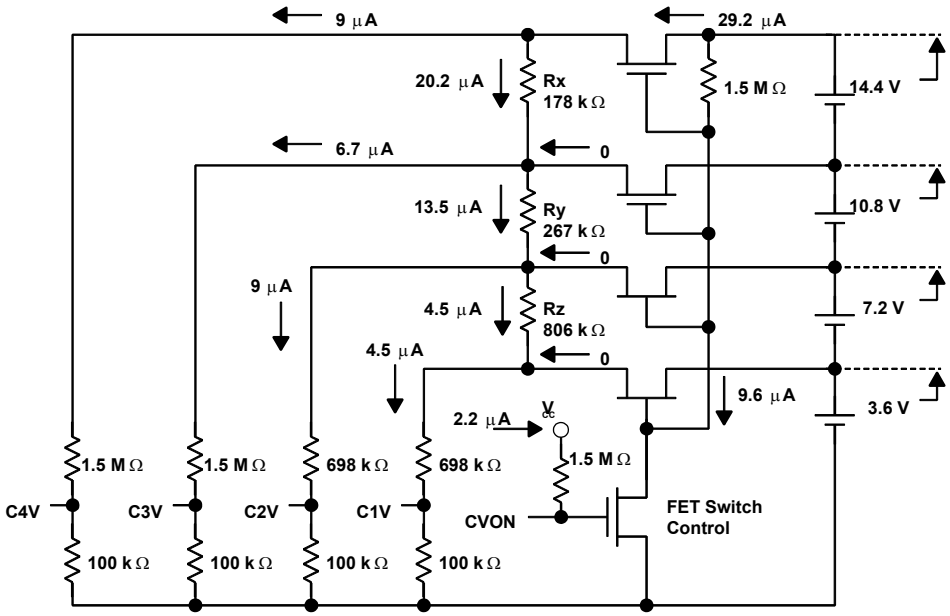


**Figure 1. Control for External FET Switches**

Filter capacitors on the VCELL inputs can affect voltage-measurement accuracy if FET switches are used on the cell voltage-divider inputs. Capacitors on the VCELL inputs larger than 0.1 µF do not allow the voltages to settle fully before the voltage measurement is made, reducing measurement accuracy.

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