AM3517/05 Power Reference Design 3.6-V to 6.3-V Input, High-Efficiency, Integrated 5-Output PMIC

This design was created to help those designers desiring an optimized and highly integrated power management solution for the AM3517 and AM3505 processors. Using a power management integrated circuit (PMIC) to power your processor can greatly reduce the number of components and overall size of your design.

1 Introduction

The input voltage range of these designs is 3.6 V to 6.3 V, which allows for operation using a dc, USB, or Li-ion battery input. The TPS650732 has three dc/dc step-down converters, two LDOs, battery charger, touch screen Interface, and a white LED boost converter.

The AM3505 and AM3517 processors can be operated with VDDSHV configured for 3.3-V operation as well as for 1.8-V operation. Depending on the user's design, different requirements (options) are available for power-up sequencing. See the AM3505 and AM3517 data manual for details.

This document proposes one power solution each for 3.3-V operation and for 1.8-V operation based on the TPS650732.

2 TPS650732-Based Design Features

- 3.6-V to 6.3-V Input Voltage Range
- Charger/Power Path Management:
  - 2-A Output Current on the Power Path
  - Linear Charger; 1.5-A Maximum Charge Current
  - 100-mA/500-mA/800-mA/1300-mA Current Limit From USB Input
  - Thermal Regulation, Safety Timers
  - Temperature Sense Input
- Three Step-Down Converters:
  - 2.25-MHz, Fixed-Frequency Operation for Small Component Size
  - Power Save Mode at Light Load Current
  - Typical 19 µA Quiescent per Converter
  - 100% Duty Cycle for Lowest Dropout
- Two LDOs (200-mA Output Current Each)
  - Fixed-Output Voltage
  - Dynamic Voltage Scaling on LDO2
  - 20-µA Quiescent Current
- WLED Boost Converter:
  - Internal Dimming Using I^2C
  - Up to 2 × 10 LEDs
  - Up to 25 mA per String With Internal Current Sink
- I^2C Interface
- 10-Bit A/D Converter
- Touch Screen Interface

3 Power Requirements

The power requirements for the AM3517/05 devices are listed in Table 1.

For more information and other reference designs, visit www.ti.com/processorpower.

Table 1. AM3517/05 Power Requirements

	Pin Name	Voltage (1) (V)	Imax (mA)	Tolerance	Sequencing Order	Timing Delay	Comments
Core	VDD_CORE	1.2	1500	±3%	4	—	24-mV ripple (pk-pk) at any frequency
	VDDS	1.8 V	400	±5%	1		50-mV ripple (pk-pk)
	VDDSHV	3.3 / 1.8	600	±5%	2		May be combined with VDDS if 1.8 V is used
	VDDS_SRAM_CORE_BG, VDDS_SRAM_MPU, VDDSOSC	1.8 V	200	±5%	3		
	VDDS_DPLL_PER_CORE , VDDS_DPLL_MPU_USBHOST	1.8	50	±5%	5		
	VDDA1P8V_USBPHY, VDDA_DAC	1.8	115	±5%	6		VDDA_DAC: ● 0 -100 kHz < 30 mVp-p ● > 100 kHz Decreases 20 dB/dec. Ex: at 1 MHz the max is 3 mVp-p.
	VDDA3P3V_USBPHY	3.3	10	±5%	6		

(1) For 1.8-V operation, VDDS18, VDDS_SRAM_CORE_BG, VDDS_SRAM_MPU, VDDSOSC, and VDDSHV can be grouped and powered up together

3.1 3.3-V Operation and Sequencing

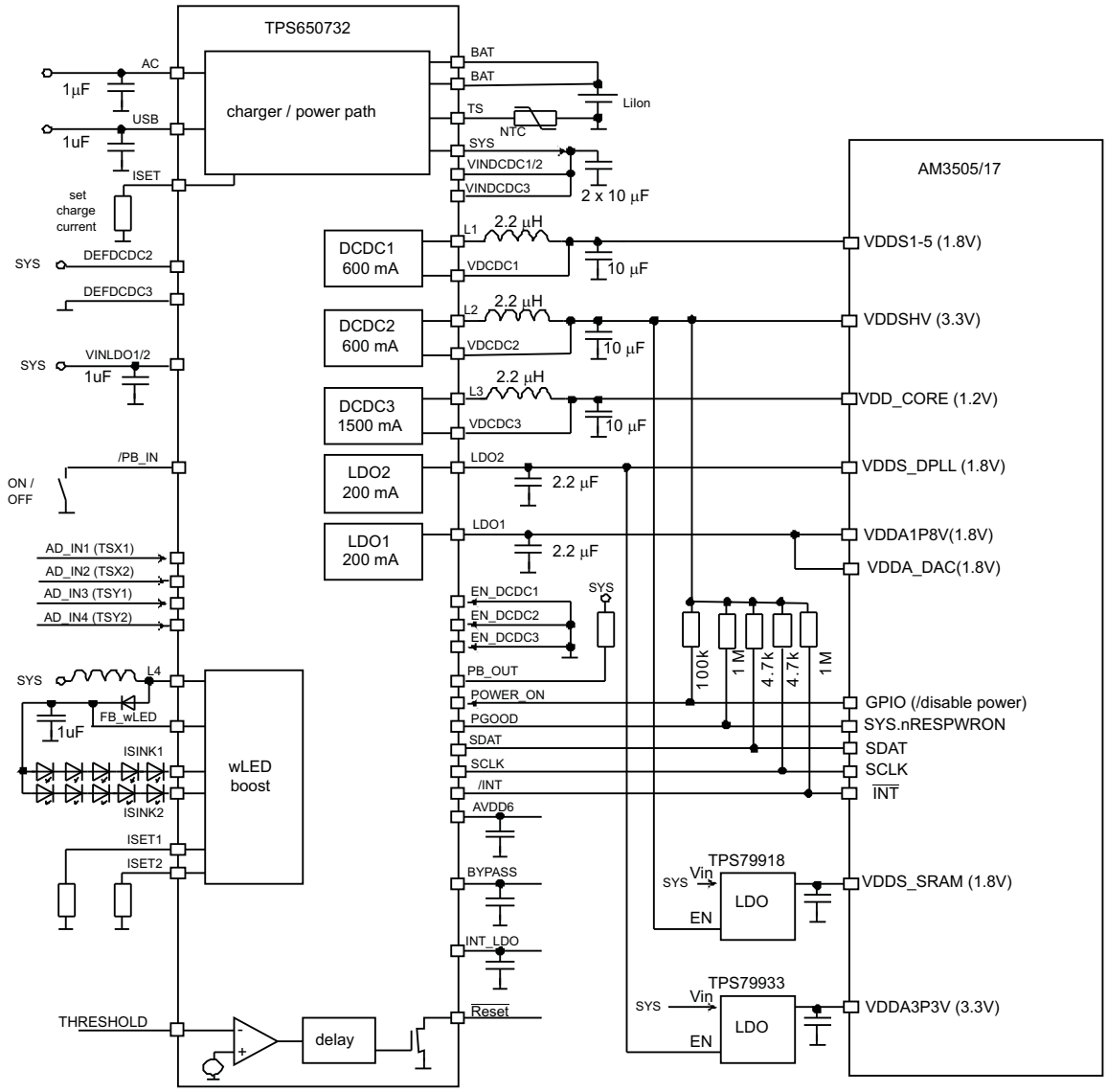

Figure 1. Powering AM3505/17 Using TPS650732 DCDC2 Used for VDDSHV = 3.3 V

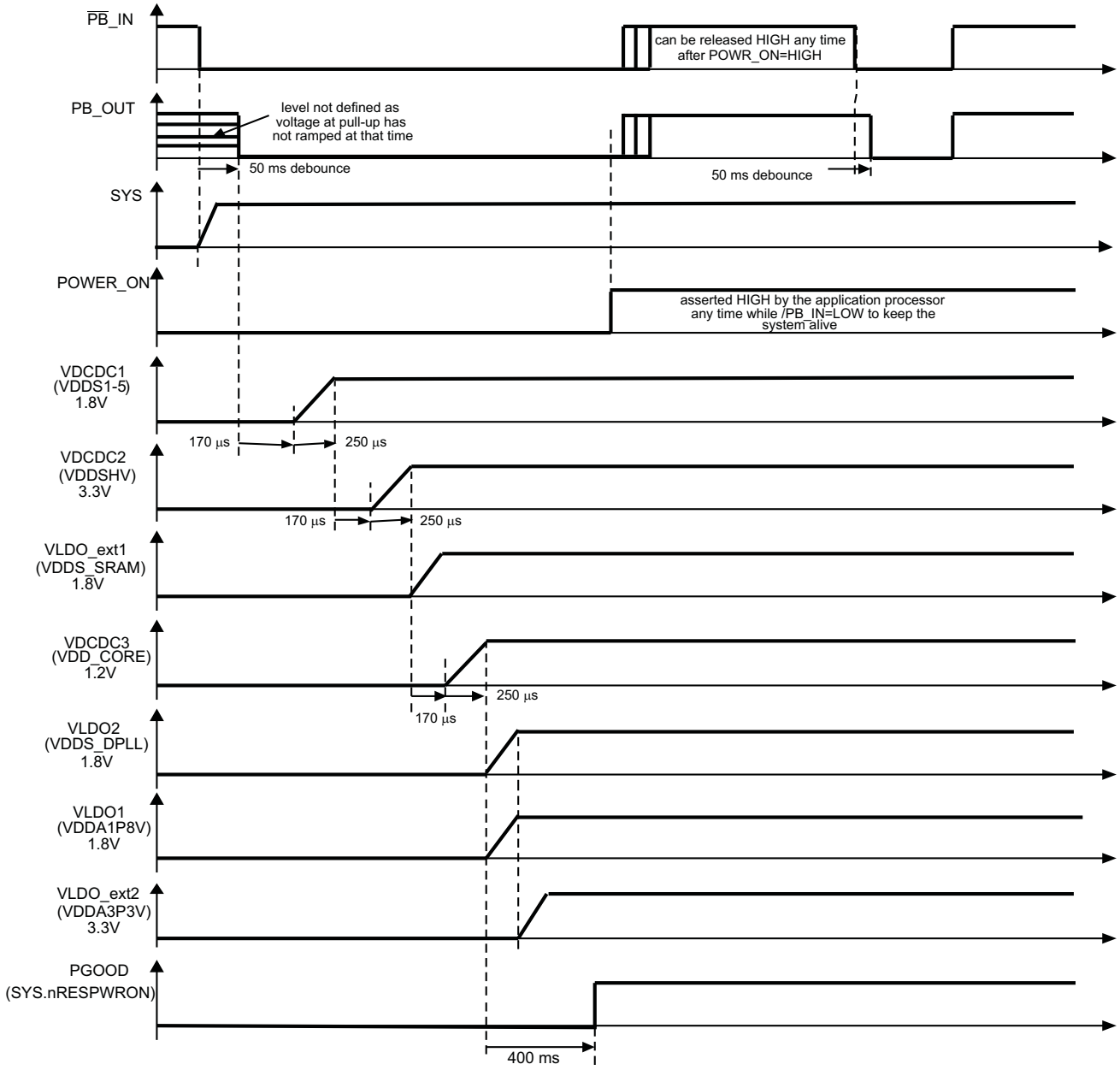

Figure 2. Timing With TPS650732 for AM3505/17 DCDC2 Used for VDDSHV = 3.3 V

3.2 1.8-V Operation and Sequencing

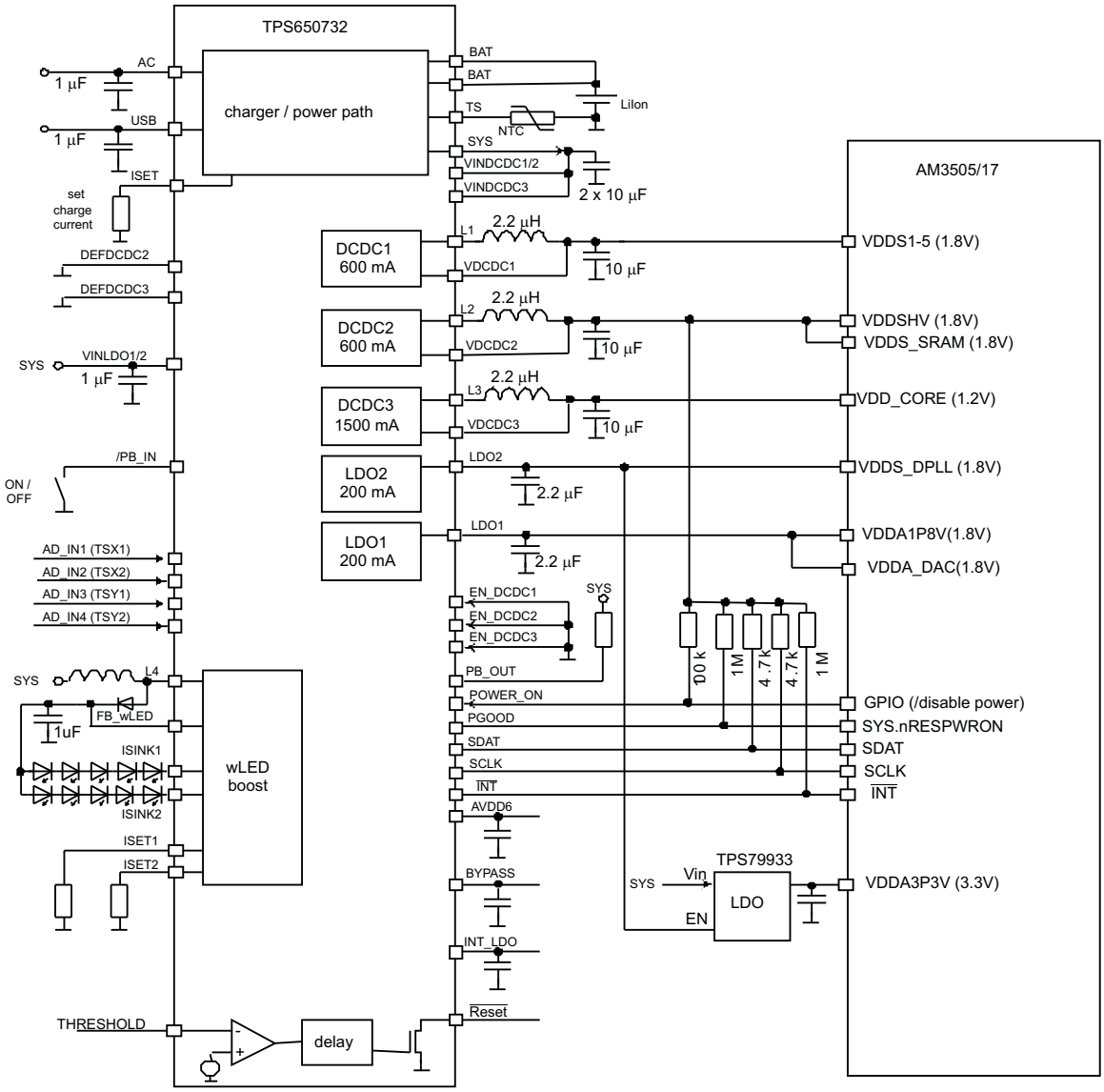

Figure 3. Powering AM3505/17 Using TPS650732 DCDC2 Used for VDDSHV = 1.8 V

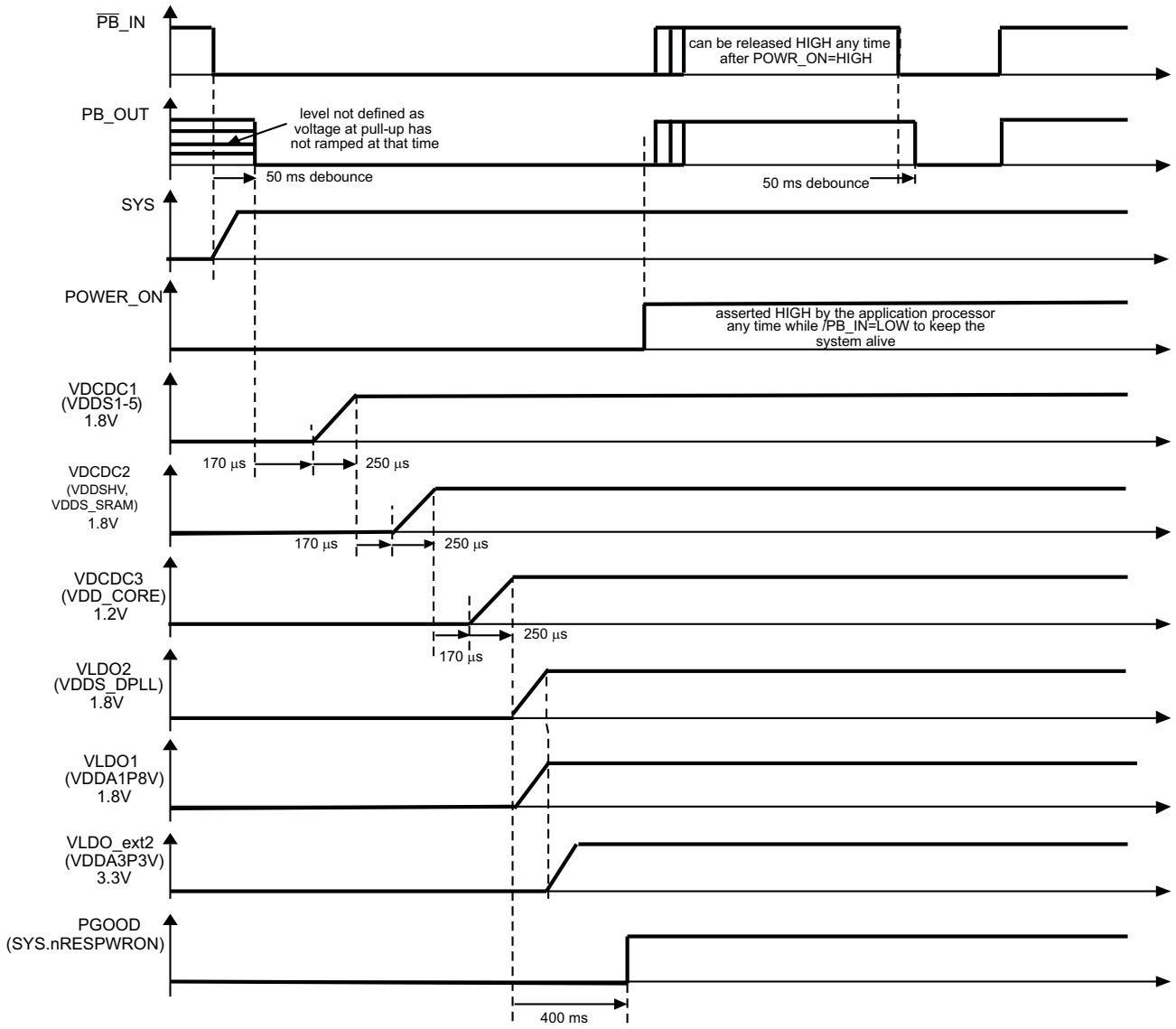

Figure 4. Timing With TPS650732 for AM3505/17 DCDC2 Used for VDDSHV = 1.8 V

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