Application Report

Soft-Stop: TPS2373X Feature Explanation

ABSTRACT

The soft-stop feature, provided by the TPS2373X family of devices minimizes stress on switching power components caused by power shutdown, allowing MOSFET BOM cost reduction, particularly for active clamp forward (ACF) applications. This application report covers active clamp forward topologies. Soft-stop action consists of discharging the output capacitor of the converter in a controlled way. The TPS23730 device is a Power over Ethernet (PoE) powered device with integrated DC/DC control.

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Trademarks

1 Introduction

While the active clamp forward topology enables high efficiencies for PoE DC/DC designs, there are certain design considerations or component selections that require special attention. One such consideration is the stress on the switching MOSFETs. When power is removed, the behavior of the controller can create situations that cause either high voltage or high current in the circuit (or both).

To address this condition, one approach is to increase the ratings of parts (example: a higher voltage MOSFET). While this quickly solves the problem with little design effort, this approach leads to higher system cost. As the output voltage of the DC/DC converter increases, the stress on the MOSFETs increases, driving the cost up disproportionately to the output voltage increase. Since the voltage and current spikes are not the nominal values of the switching voltages and currents, the opportunity for lower cost parts is possible if the spikes are addressed in another way. This will also drive the cost ramp down for higher output voltage active clamp forward designs.

The TPS23730, TPS23734, and TPS23734 devices introduce a new approach, called soft-stop. This approach consists of controlling the discharge of the output capacitor of the converter, and subsequently sending the energy back to the input bulk capacitor.

Figure 1-1 illustrates an active clamp forward design.

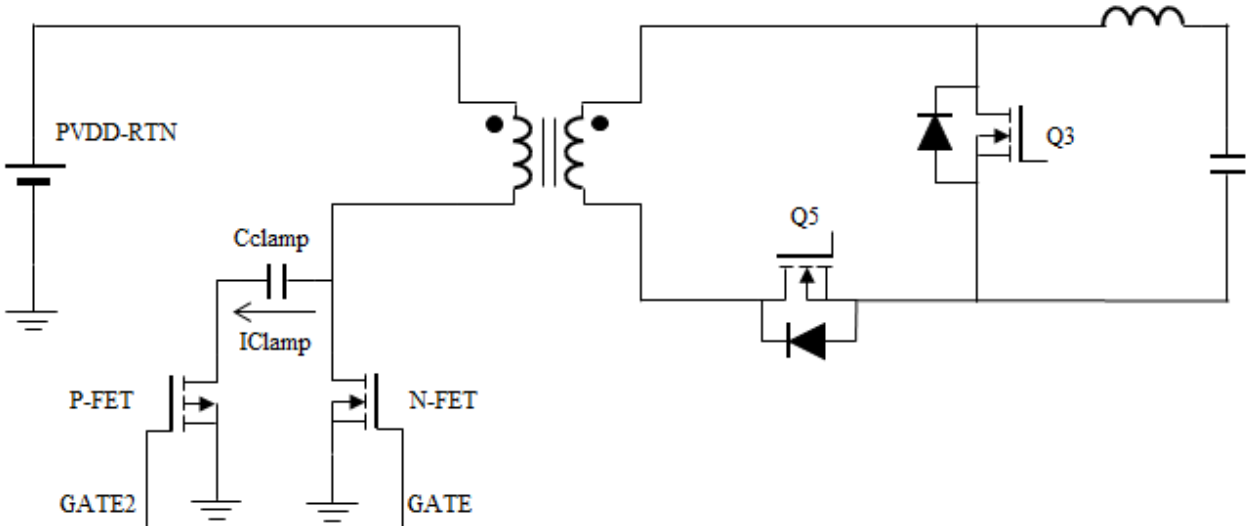

Figure 1-1. Active Clamp Forward Design

2 Background

When the input power is removed, the input voltage rails gradually decrease as the input bulk capacitor is discharged. The converter will remain on as the input voltage decreases to its minimum threshold. As the input voltage decreases, the converter increases the duty cycle to compensate. This leads to shorter and shorter off times, and the voltage across the clamp capacitor approaches higher values since the transformer is being reset so quickly. The end result is oscillations and overvoltages that could potentially damage the MOSFETs. Figure 2-1 illustrates these principles.

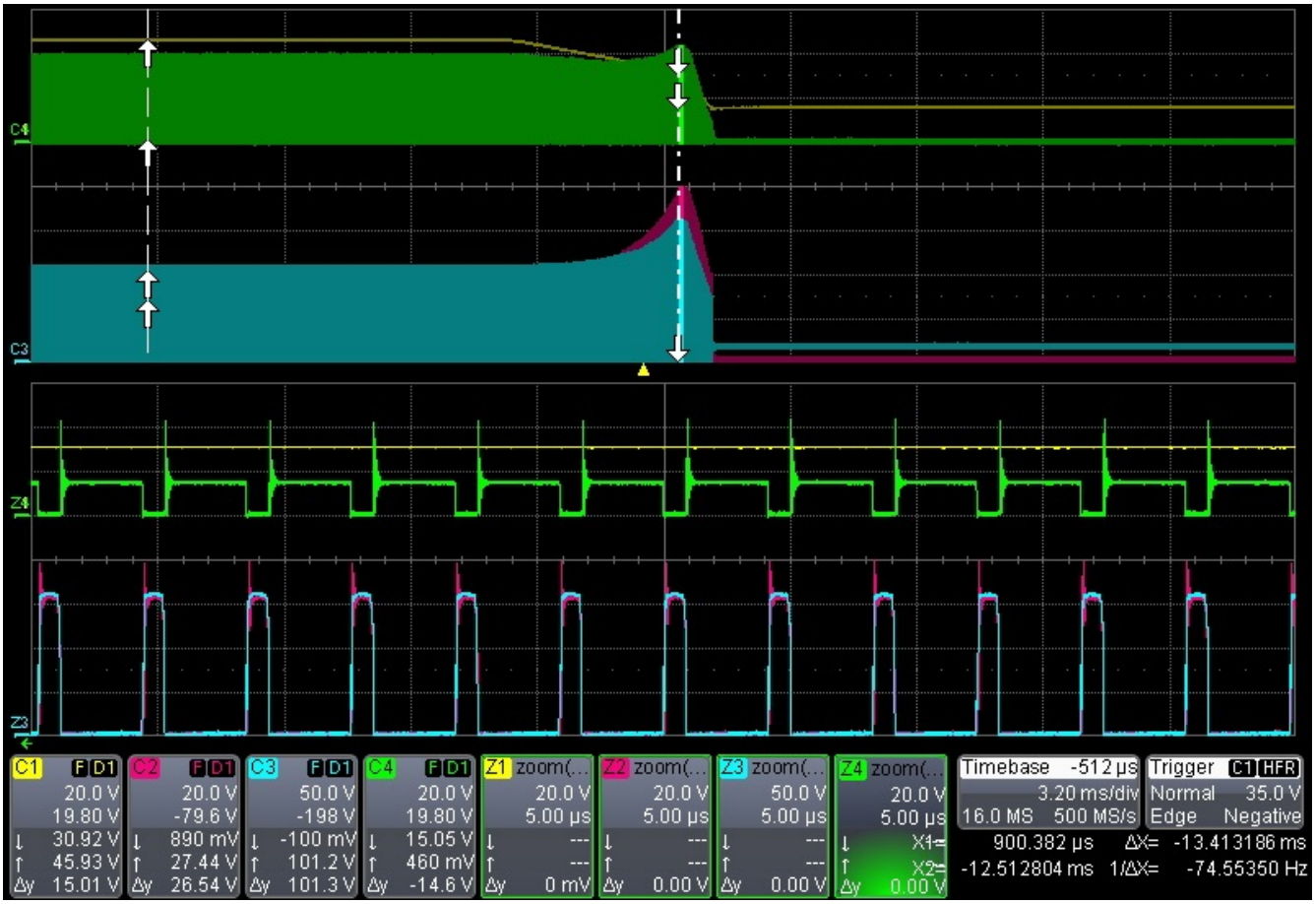

Figure 2-1. Active Clamp Forward Shutdown Sequence Without Soft-Stop

Additionally problematic, if a brief power interruption occurs during the next power up, the clamp capacitor will be precharged, which could cause the transformer to saturate. This causes severe stress on the switching components. In this case, the N-FET on the primary side of the transformer and the secondary sync FET (Q3) are at risk. This is explained in more detail in the *Line Undervoltage Protection* section of the *UCC2897A Advanced Current-Mode Active-Clamp PWM Controller Data Sheet*.

Another case during shutdown is when the converter stops prematurely because the controller has an undervoltage lockout (UVLO). If this threshold is reached when the output voltage is too high, the risk of “backdrive” becomes possible. Backdrive is when the output voltage is high enough to turn on the MOSFET on the secondary side, and this results in energy being driven from the secondary to the primary. The output voltage turns on the gates of both secondary MOSFETs, not at the same time but they eventually are both ON at the same time. Since both MOSFETs are ON, there is approximately 0 V across the transformer secondary inductance.

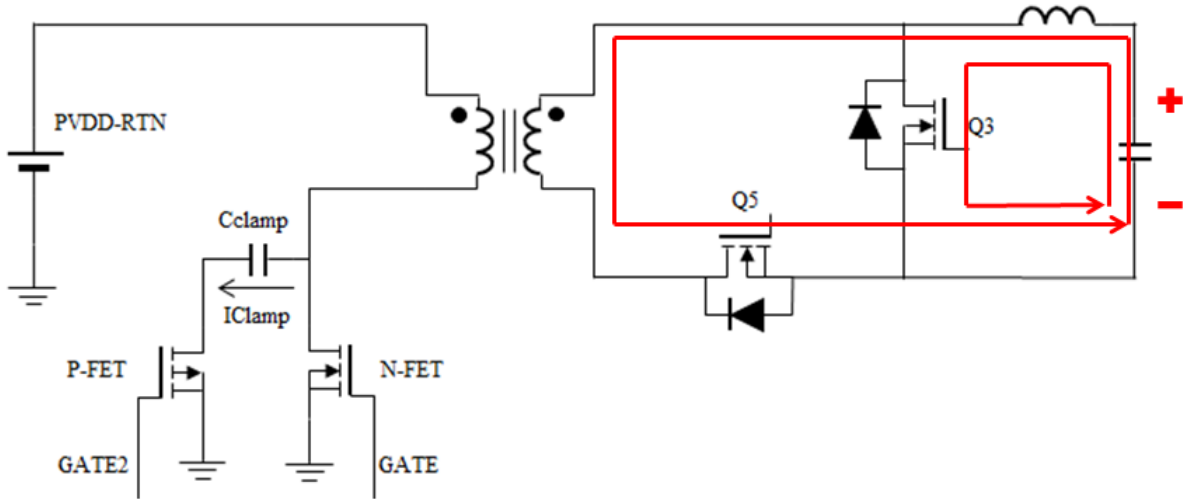

Figure 2-2. Light Load Shutdown When Both MOSFETs are ON

There are now two current paths on the output. The total V_{OUT} discharge current builds up in the inductance, and a fraction of the discharge current flows through the magnetizing inductance of the transformer. After a short time, the inductor current becomes very high. Over time, the output voltage is dropping so both ends of the secondary goes down. This leads to both MOSFETs turning off. However, the transformer magnetizing current has to be maintained, so it gets transferred to the primary side. This is possible because the series synchronous

MOSFET (Q5) is turning off, generating a reverse polarity on the transformer. This forces current through the primary clamp capacitor, and also consequentially, this turns on the parallel synchronous MOSFET (Q3).

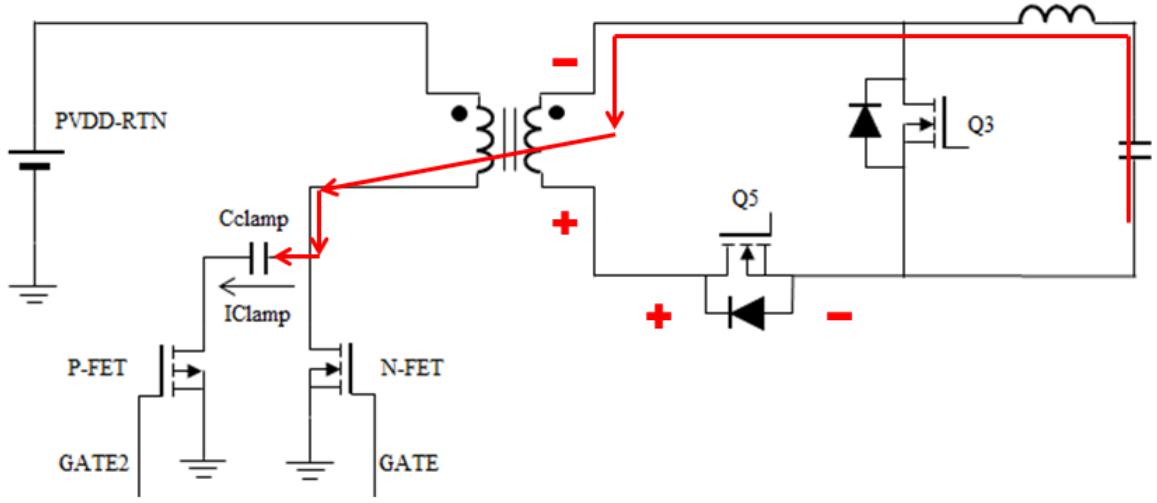

Figure 2-3. Light Load Shutdown When Q5 Turns OFF

Now, the current through the clamp capacitor goes down after some time and will want to change direction. The transformer will change polarity, which will turn on Q5 and turn off Q3, causing a voltage transient across the drain to source. These voltage spikes can damage the MOSFETs.

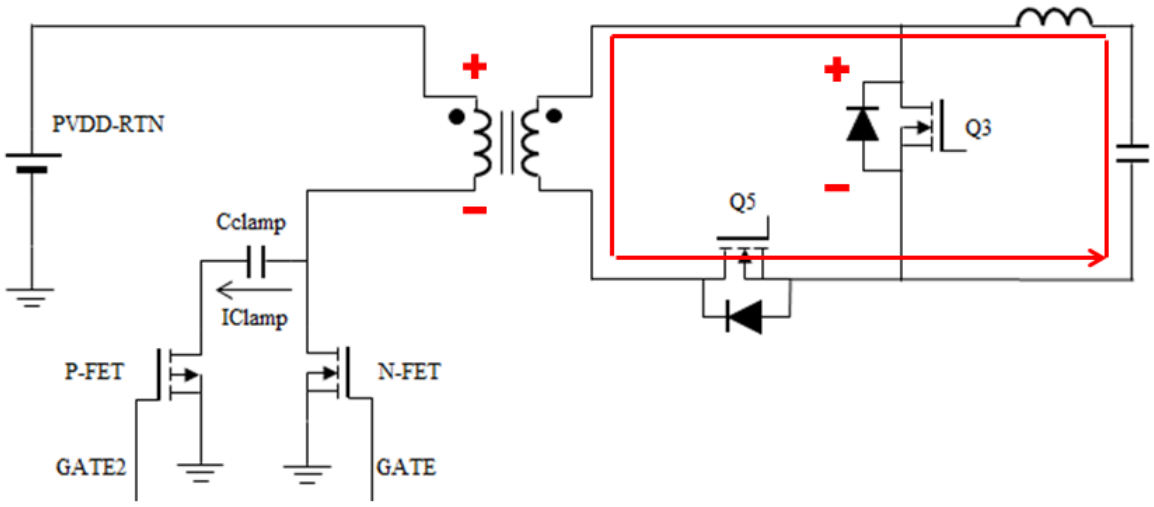

Figure 2-4. Light Load Shutdown When Q3 Turns OFF

This pattern continues until the energy in the circuit is too low to turn on the MOSFETs. In this case, the design may require a 200-V (instead of 150 V) rating with avalanche rating for the N-FET and ≥ 100 V (instead of 60 V) (example: 12-V application) rating for Q5 (in Figure 1-1). This is higher BOM cost. The soft-stop feature reduces or eliminates these spikes, thus leading to lower BOM cost.

3 Operation

To eliminate these potential hazards, the soft-stop mode is triggered on a voltage threshold of the bulk capacitor. The TPS2373X devices use the LINEUV pin to monitor the input bulk capacitance, and this can subsequently be programmed to a user-defined threshold. Once the soft-stop sequence begins, the TPS2373X temporarily turns on the start-up circuit to maintain the input voltage on the bias winding of the transformer, VCC. This ensures the IC remains powered during the soft-stop event. Another important action at the beginning of soft-stop is that the controller lowers the CS voltage threshold to about 50 mV (typically it is 250 mV). This action forces the peak current to be reduced. Then the IC uses the SST capacitor to ramp down the peak current of the switching MOSFETs in a controlled way. Because the IC is still powered, GATE and GAT2 can continue to switch during this time, ensuring there is no lockup. The TPS2373X also maintains dead time between the primary side switching MOSFETs, ensuring that there is no current spike through the P_FET due to the clamp capacitor charge. These actions allow the energy in the output bulk capacitor to be transferred to the input bulk capacitor immediately, regardless of the output voltage load level, see Figure 3-1.

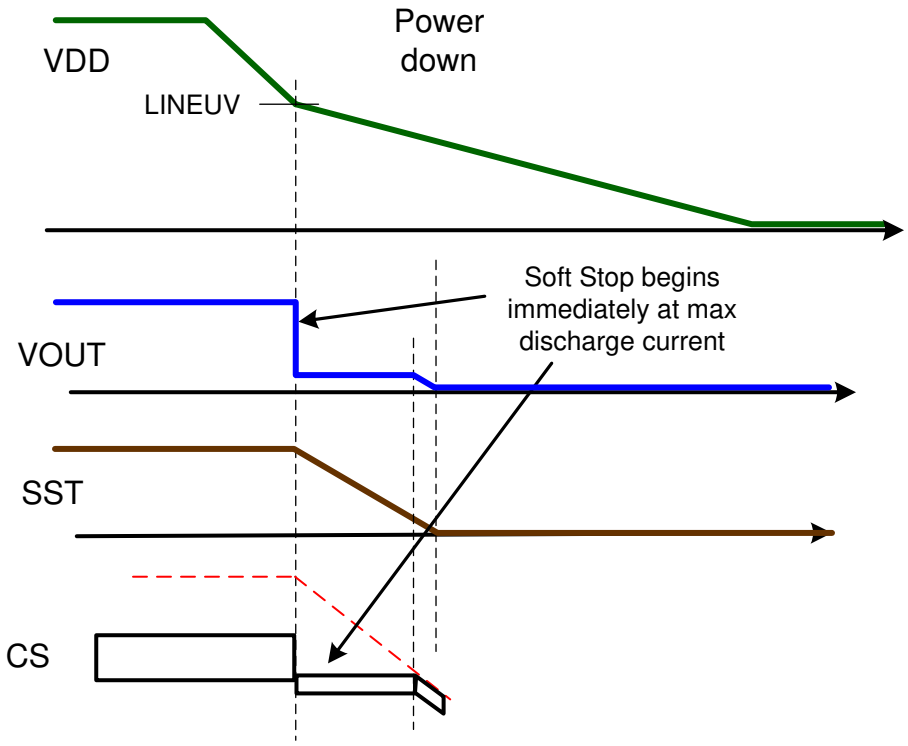

Figure 3-1. Soft-Stop Operation

As Figure 3-2 shows, the results on the TPS23730EVM-093 are identical to the ideal behavior.

Ch1: VDD, **Ch2:** VCC, **Ch3:** SST, **Ch4:** V_{OUT}

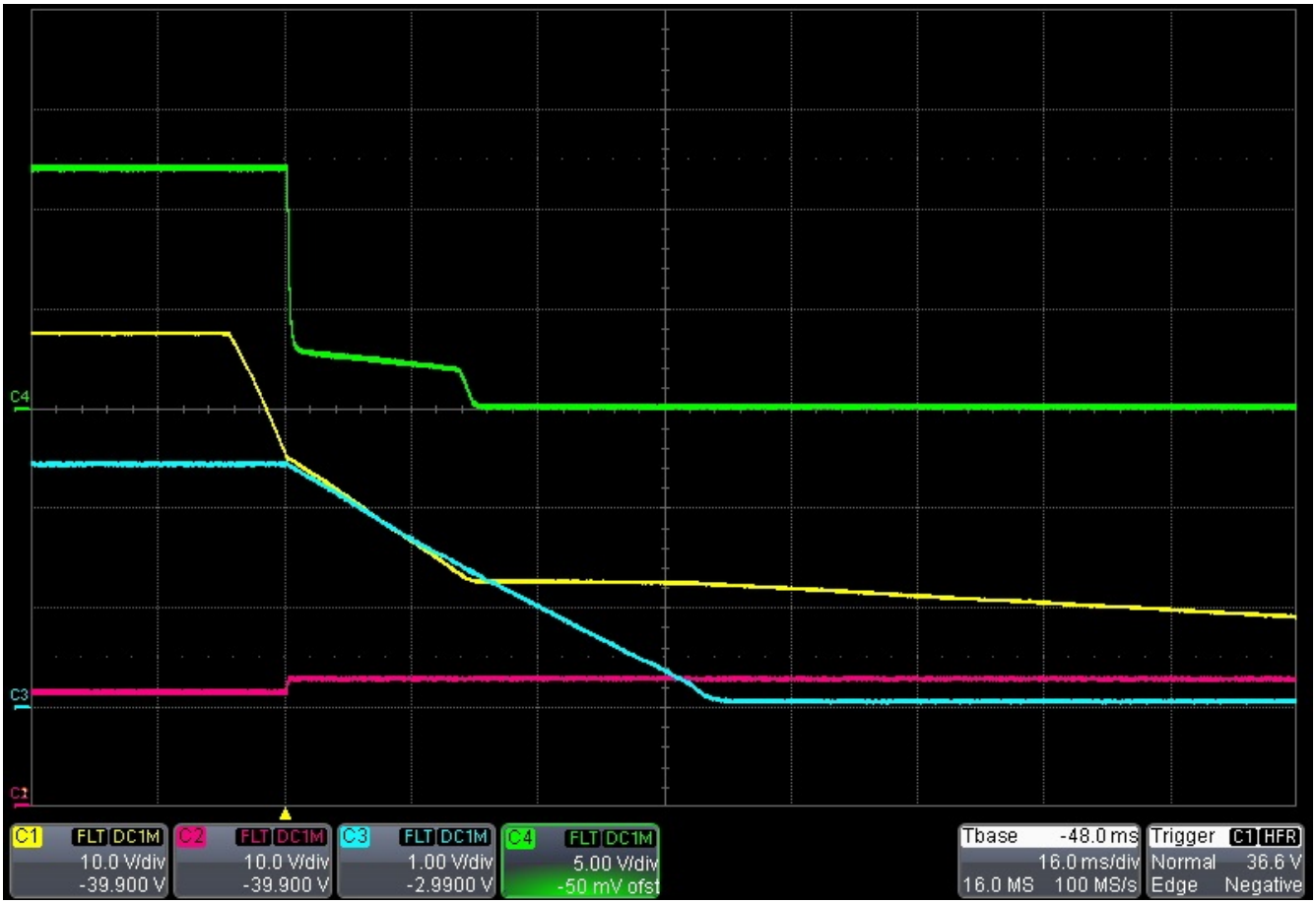

Figure 3-2. PoE Shutdown

Soft-stop is also useful in the case of power interruption. As discussed earlier, if the clamp capacitor is precharged from an unsafe shutdown and then power is reapplied, it can cause an overvoltage event on the MOSFET and potentially damage the part. Figure 3-3 shows a brief power interruption with soft-stop.

Ch1: VDD, **Ch2:** VCC, **Ch3:** SST, **Ch4:** V_{OUT}

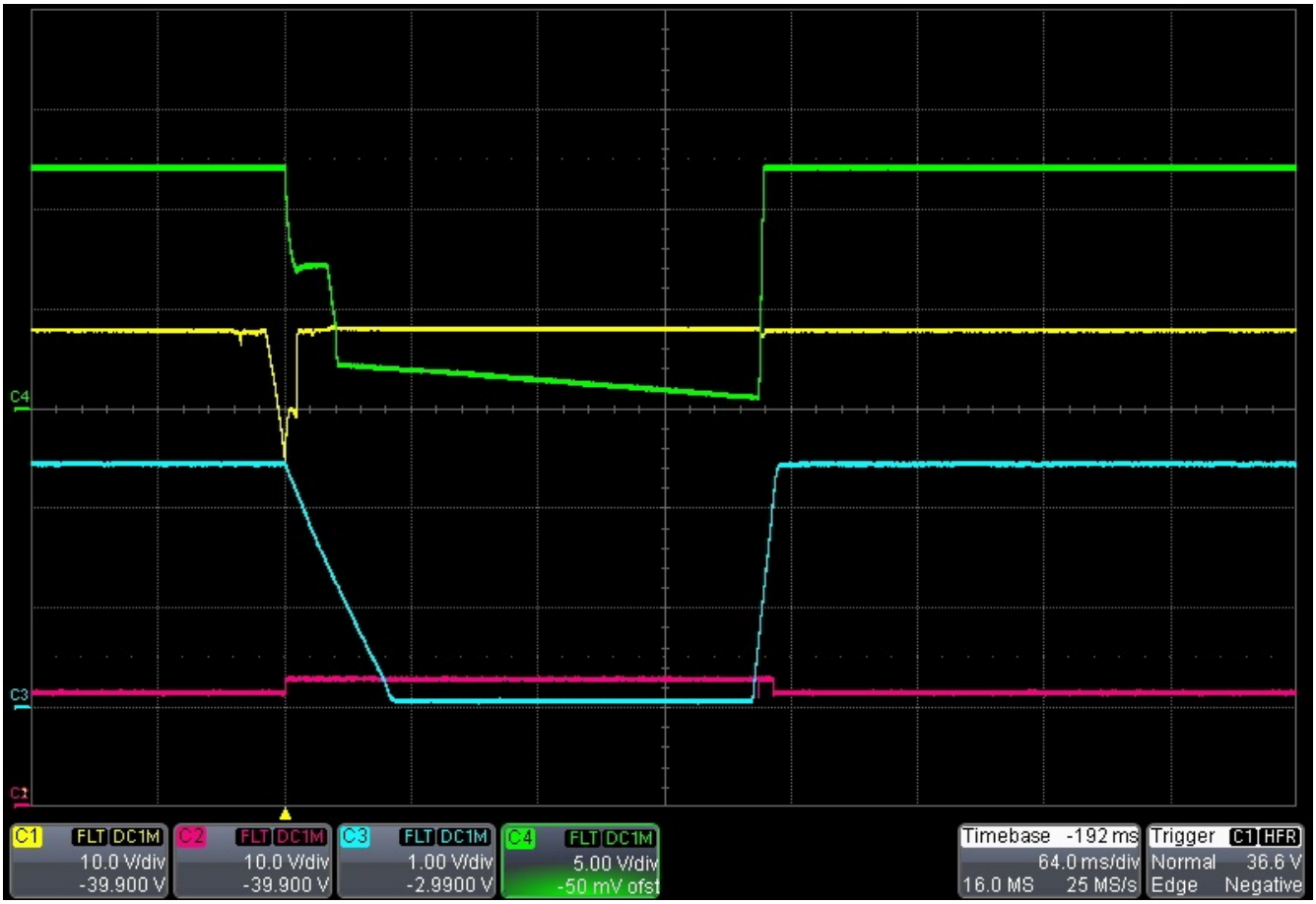

Figure 3-3. PoE Brief Power Interrupt

Finally, a direct comparison follows between a design with soft-stop versus one without. The TPS23730 does allow for the soft-stop to be enabled or disabled. Therefore, a true side-by-side comparison of the feature is demonstrated in Figure 3-4 and Figure 3-5. Figure 3-4 shows the soft-stop feature enabled. The image clearly shows that the VDS voltage of the primary MOSFET (Blue) is well under 150 V. Therefore, 150-V rated MOSFETs are not at risk of damage. Note this is for a 12-V output design. In Figure 3-5, the soft-stop feature is disabled. It is evident that the voltage exceeds 150 V for multiple switching cycles. This would demand high-rated MOSFETs.

Ch1: VDD (Yellow), **Ch2:** Vds P-FET (Pink) **Ch3:** Vds Primary FET (Blue)

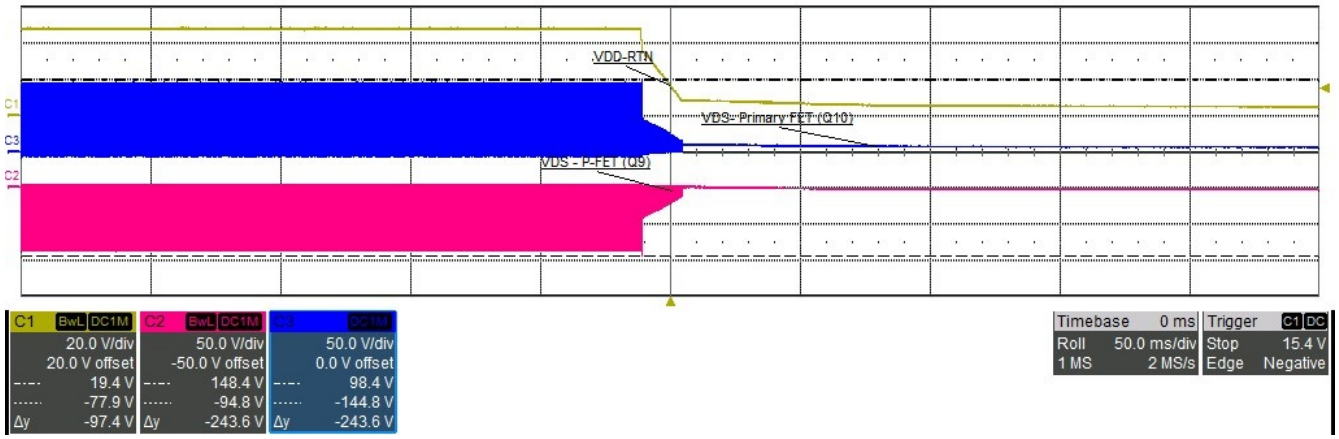

Figure 3-4. Soft-Stop Enabled Full Load for Primary MOSFETs

Ch1: VDD (Yellow), **Ch2:** Vds P-FET (Pink) **Ch3:** Vds Primary FET (Blue)

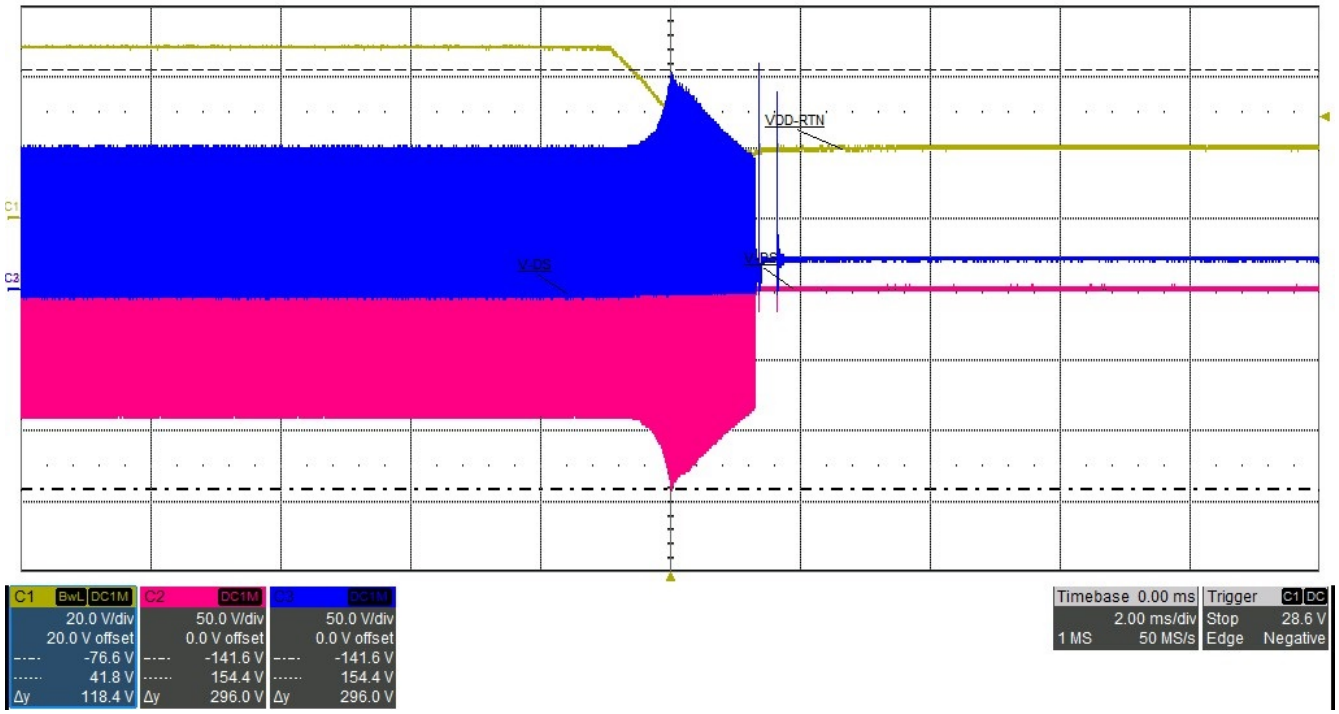

Figure 3-5. Soft-Stop Disabled Full Load for Primary MOSFETs

Figure 3-6 and Figure 3-7 show the same conditions for the secondary-side MOSFETs (Q6 and Q8). Figure 3-6 shows the TPS23730EVM-093 with soft-stop enabled. The spike on the series MOSFET (Q8) is only 53.3 V with soft-stop enabled, versus 88.2 V without soft-stop.

Ch1: VDD (Yellow), **Ch3:** Vds Parallel FET (Blue) **Ch3:** Vds Series FET (Green)

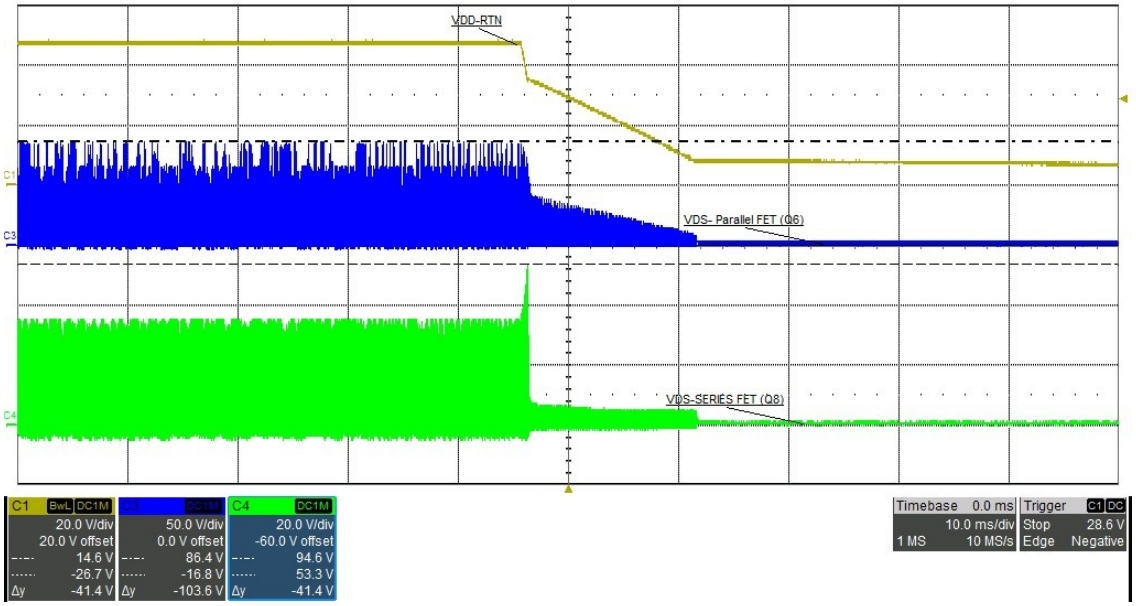

Figure 3-6. Soft-Stop Enabled Full Load for Secondary MOSFETS

Ch1: VDD (Yellow), **Ch3:** Vds Parallel FET (Blue) **Ch3:** Vds Series FET (Green)

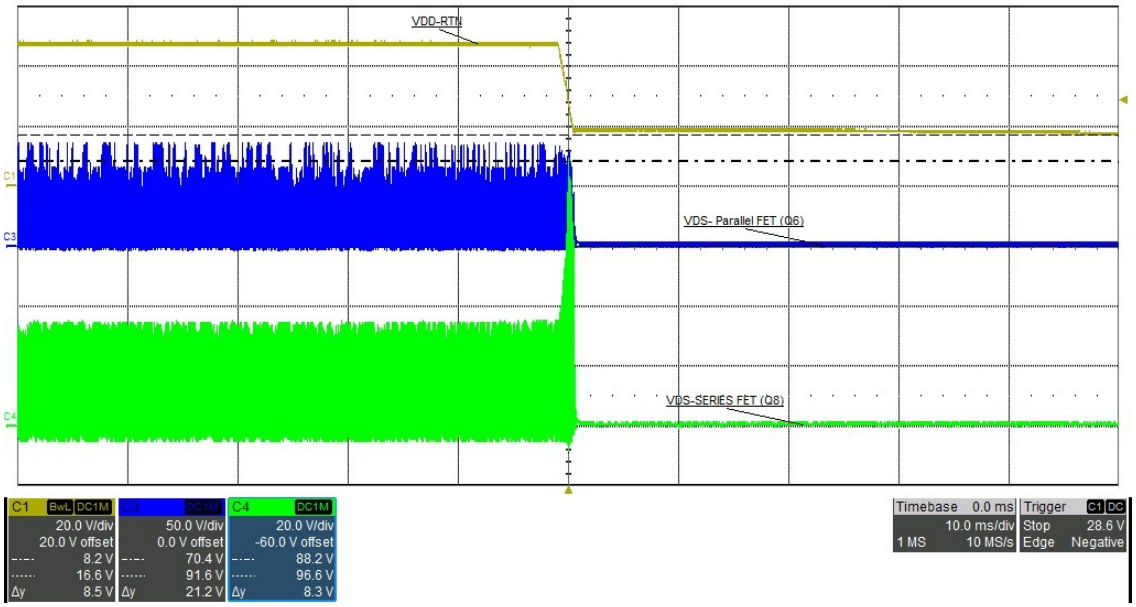

Figure 3-7. Soft-Stop Disabled Full Load for Secondary MOSFETs

It can also be demonstrated in the no load condition. Figure 3-8 and Figure 3-9 display the primary side of theTPS23730EVM-093 during a shutdown with no load on the output of the DC/DC converter. Figure 3-10 and Figure 3-11 show the secondary MOSFETs for the same conditions.

Ch1: VDD (Yellow), **Ch2:** Vds P-FET (Pink) **Ch3:** Vds Primary FET (Blue)

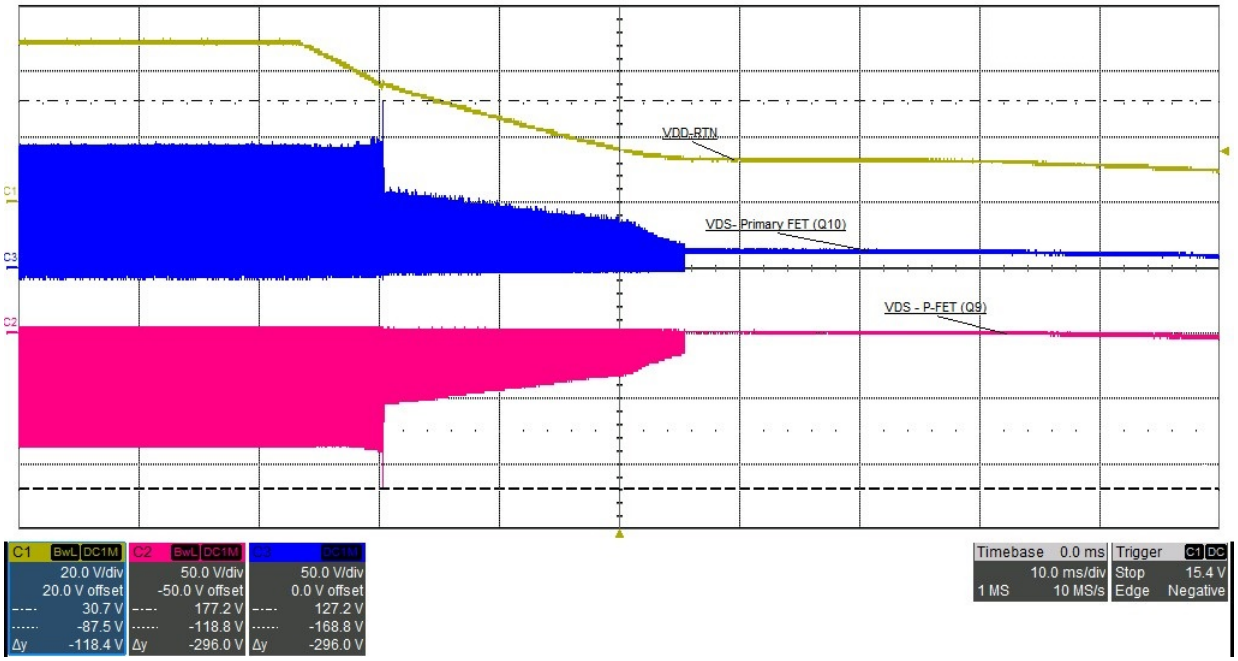

Figure 3-8. Soft-Stop Enabled No Load Primary MOSFETs

Ch1: VDD (Yellow), **Ch2:** Vds P-FET (Pink) **Ch3:** Vds Primary FET (Blue)

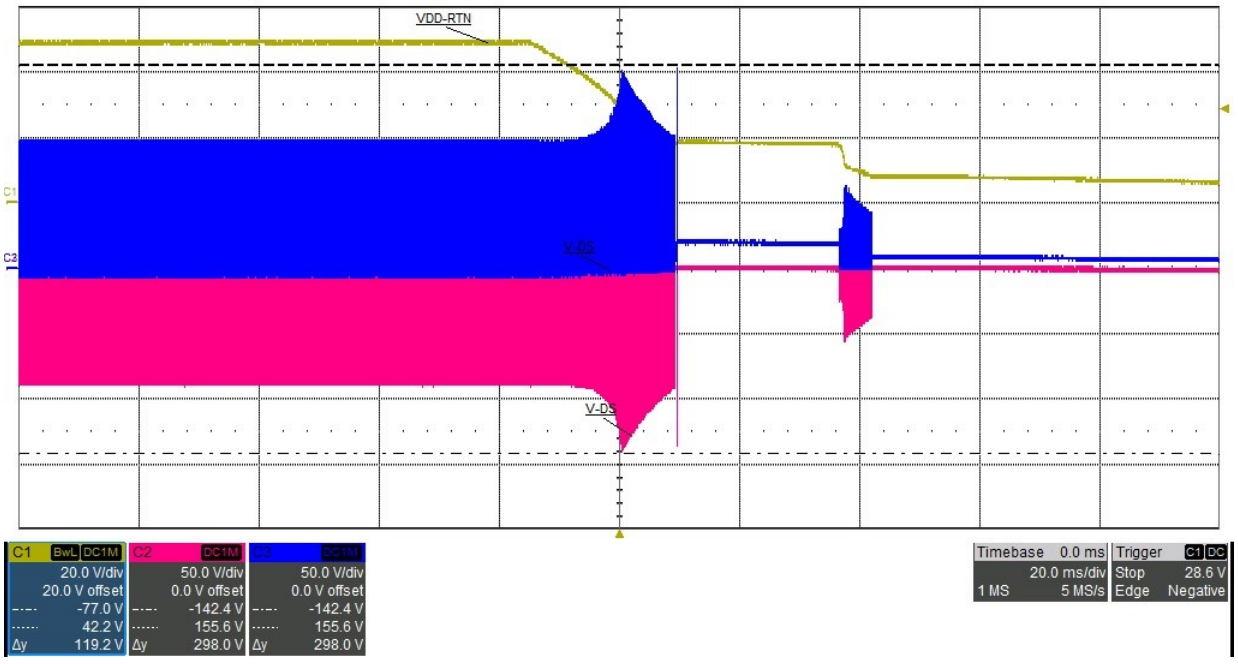

Figure 3-9. Soft-Stop Disabled No Load Primary MOSFETs

Ch1: VDD (Yellow), **Ch3:** Vds Parallel FET (Blue) **Ch3:** Vds Series FET (Green)

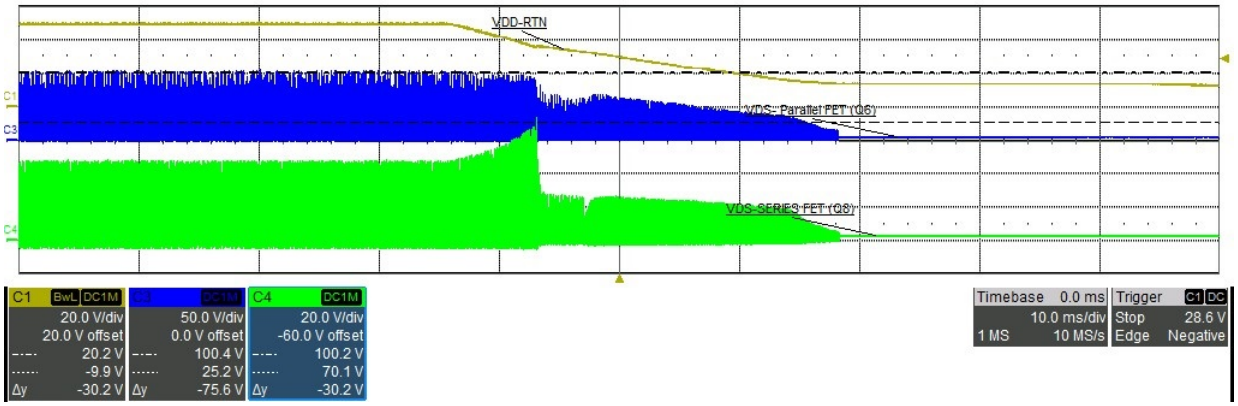

Figure 3-10. Soft-Stop Enabled No Load Secondary MOSFETs

Ch1: VDD (Yellow), **Ch3:** Vds Parallel FET (Blue) **Ch3:** Vds Series FET (Green)

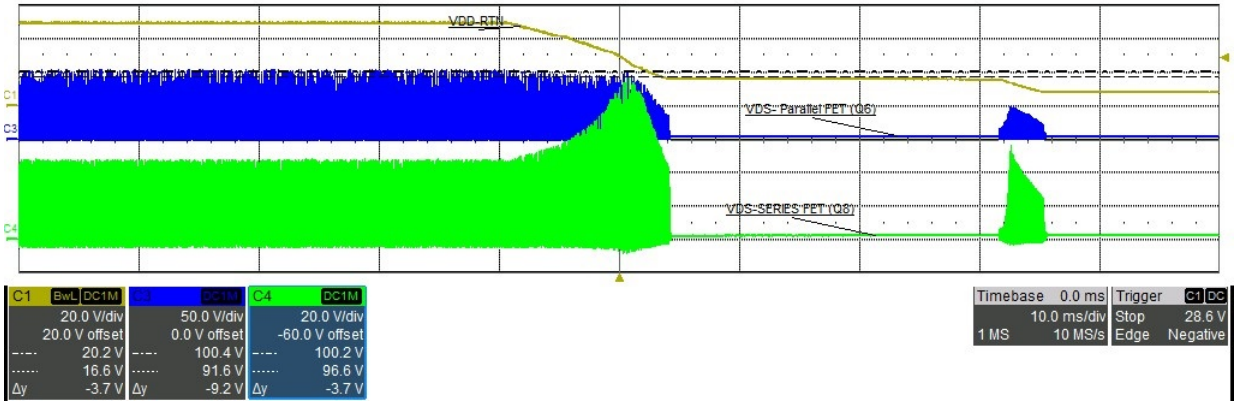

Figure 3-11. Soft-Stop Enabled vs. Disabled Full Load for Secondary MOSFETs

4 Conclusions

Clearly from the scope shots, the soft-stop feature lowers the drain-to-source voltage for all four MOSFETs of an active clamp forward. This completely eliminates the two potential considerations that could cause MOSFET damage, thus allowing lower voltage rated parts to be used. Without soft-stop, designers had to consider the high-voltage spikes in their transformer design. One way to address the spikes is to change the transformer turns ratio, but that sacrifices performance. These conditions are caused by a combination of the input bulk capacitance, the output capacitance, the load during shutdown, and the transformer design. This leads to unpredictability in the design, which causes adjustments to be made after the initial build. Soft-stop eliminates this design consideration because it makes the shutdown predictable, independent of the load. The TPS2373X part allows for the programming of the soft-stop time through the SST and I_STP pins. This feature enables the active clamp forward topology for 12-V output designs, which were previously either costly or unreliable. This topology is highly efficient; the TPS23730EVM-093 can get 92.6% at 5-A load. The TPS2373X gives designers the ability to choose the best topology for their design by overcoming cost and damage barriers.

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