Product Overview

TPS54KB20 Pre-Production to Production Change List

Pre-production samples of the TPS54KB20 are available for customers using orderable PTPS54KB20RZRR. Pre-production samples can not be fully representative of the final revision of the production device. This errata summarizes any known discrepancies that have been identified with pre-production samples and the final product.

The TPS54KB20 device is a high-efficiency, single-channel, small-sized, synchronous-buck converter. The device is an excellent choice for low output voltage point-of-load applications with 25-A or lower output current in server, storage, and similar computing applications. The TPS54KB20 features proprietary D-CAP4 mode control combined with adaptive on-time architecture. This combination is designed for modern low-duty-ratio and ultra-fast load-step-response DC/DC converters. The output voltage set by the feedback voltage divider ranges from the internal voltage reference to 5.5 V. The conversion input voltage ranges from 2.7-V to 16-V, and the VCC input voltage ranges from 3.13 V to 5.3 V. The D-CAP4 modulator uses emulated current information to control the modulation. The D-CAP4 modulator reduces loop gain variation with different output voltages providing better transient response in higher output voltage applications. This control scheme provides multiple advantages. First, this control scheme does not require a phase-compensation network outside, which makes the device easy-to-use and also allows low external component count. This control scheme also supports stable operation with all low ESR output capacitors (such as ceramic capacitors and low ESR polymer capacitors). Lastly adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during load-step transients.

Errata Details

The following table summarizes known errata.

Table 1. TPS54KB20 Errata Summary

Errata Number	Description	Impact	Workaround	Disposition
1	When using internal VCC, there is a possibility of an incorrect internal reading during powerup resulting in the feedback voltage being regulated to 0.5 V instead of 0.9 V. This is more probable when the VCC pin's slew rate is slowed down from external sources. Example scenarios that can slow down the VCC pin's slew rate are: slow VIN slew rate such that the internal VCC LDO goes into dropout during startup or external loading of the VCC pin during startup.	The device operates, but not within the specifications. The output voltage regulates to 0.5/0.9× the target set by the FB resistor divider.	If this is observed during evaluation, a re-read of the internal settings can be triggered by restarting the device. The recommended method is to pull the EN pin low (or float the EN pin) then pull the EN pin high again.	Design fix planned for production release device.

Table 1. TPS54KB20 Errata Summary (continued)

Errata Number	Description	Impact	Workaround	Disposition
2	The switching frequency has more variation across output voltage than desired. A device tested in a 3.3-V output application with the 800-kHz setting had a switching frequency (fsw) within 0.2% of the target and the same device with the 1100-kHz setting had a fsw -5% from the target. Another device tested in a 1.05-V output application with the 800-kHz setting had a fsw +4% from the target and the same device with the 1100-kHz setting had a fsw -11% from the target.	Lower output voltages (such as 1.05 V) have high fsw when the 800-kHz setting is selected and low fsw when 1100-kHz setting is selected.	None	Design change planned for production release device to have more consistent switching frequency across output voltage for the 800-kHz and 1100-kHz settings.
3	The ramp amplitude of RAMP2 selected through the MSEL pin is being adjusted for the production release device. Refer to Table 2 for a summary of the ramp amplitudes.	Pre-production devices have less stability margin and better transient response for RAMP2 as a result of the smaller ramp amplitude. The change to RAMP2 results in more stability margin, but worse transient response in production devices.	None	Design change planned for production release device.
4	TPS54KB20 was designed to retry after thermal shutdown (165°C nominal) if the device's junction temperature reduces to 150°C nominal. However, in typical thermal shutdown scenarios after the device enters thermal shutdown, an under-voltage fault is being tripped causing the device to latch off. As a result, after thermal shutdown, the device needs to be restarted through EN or through VCC UVLO for the device's output to be regulated again.	No impact in normal operation.	None	Design change planned for production release device, for retry response after thermal shutdown.
5	The thermal shutdown threshold of pre-production samples is high, measuring in the range of 180 to 190 °C typical.	No impact in normal operation.	None. Avoid evaluating the device at high temperature extremes.	Design change planned for production release device, to match the data sheet specification of 165°C typical.
6	When there is no input to the device (V_{VIN} = V_{VCC} = V_{EN} = 0 V), the PG pin does not clamp if pulled up to an external 3.3-V source. The voltage exceeds 850 mV if pulled up through a 100-kΩ resistor and exceeds 1000 mV if pulled up through a 10-kΩ resistor.	If testing the device in the scenario in the description, the PG pin floats high indicating the output voltage is in regulation although the output voltage is not in regulation.	Pull the PG pin up using the VCC pin or bias the VCC pin with the same supply being used to pull up the PG pin.	Design change planned for production release device.

Table 2. Pre-Production versus Production Ramp Amplitudes

Ramp Setting	Pre-Production Ramp Amplitude	Production Ramp Amplitude
RAMP1	1×	1×
RAMP2	1.3×	1.8×
RAMP3	1.6×	1.6×
RAMP4	2.1×	2.1×

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