Application Brief

Novel Plating Technology for Wettable-Flank QFN and SON Packages

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Abstract

The Qual-Flat No-leads (QFN) and Small Outline No-leads (SON) packages, offering compactness, cost-effectiveness, and good electrical and thermal performance, are widely used in mobile and automotive industry. However, a challenge for the use of QFN packages in high-reliability industry has been due to the lack of consistent solder fillet formation on the flank of the leads. Thus, one of the key processes to enable QFN and SON in the automotive industry is the wettable flank feature which provides a capability to form solder fillet during the post-SMT assembly to printed circuit board (PCB) effectively. To ensure populated printed circuit boards meet quality standards, it's essential to visually inspect them for flaws and anomalies during assembly. This paper introduces wettable-flank capability with novel immersion Sn plated on lead flank. It creates solderable lead flanks and enhances optical surface mount packaging inspection with a detectable wetting fillet height. Shelf-life studies and solderability tests on ceramic plates demonstrate the capability to meet reliability standards. Board-level reliability (BLR) testing reveals comparable performance to non-wettable flank packages.

Introduction

The automotive industry requires smaller package solution for the reasons of space constraint, weight reduction, heat management, and design flexibility. QFN and SON packages meet the space saving, heat management, and design flexibility needs. However, QFN PCB assembly poses challenges in soldering and inspection. Soldering is a part of the QFN/SON PCB assembly process, where components are mounted after solder paste application through a stencil. Reflow soldering in an oven joins QFN/SON packages to the PCB. A QFN/SON package typically consists of a metal leadframe which is made of copper. The exposed copper flanks of a standard QFN/SON package are prone to oxidation. Oxidized Cu surface is not solderable. With leads being beneath the package, insufficient solder can pose challenges and result in reduced board-level reliability performance from thermomechanical stress and causing electrical failure. For better soldering quality control, inspection process such as optical or X-Ray inspection is needed. X-ray inspection can be costly and time-consuming versus automatic optical inspection (AOI). The solution is to enable side wettable flank terminals with solder wetting for robust solder fillet formation, facilitating AOI for solder defect inspection. The existing industry solutions of wettable flank are step-cut leadframe QFN/SON packages and dimple leadframe QFN/SON packages.

Immersion Tin-Plated Wettable Flanks

In addition to the existing wettable flank options of step-cut leadframe and dimple leadframe QFN/SON packages, TI currently offers wettable flank plated QFN/SON packages from the novel plating technology with Immersion Sn. In general, the packages will go through typical package assembly, mold and cure process. Before package singulation, the lead bottom surfaces will be plated with matte Sn as a solderable surface finish. Then the bare Cu lead flank will be exposed after the mold singulation process. In TI's immersion Sn plating process, any Cu oxidation will be removed during the chemical steps before the immersion Sn is plated to the Cu lead flank. It will ensure a consistent immersion Sn plating outcome. Then the immersion Sn will be plated as a coating of Sn on the exposed Cu lead flank layer. This process doesn't alter the package electrical and reliability performance, but only adding the side wetting capability. Figure 1 shows sawn QFN on PCB board with good solder fillet wetting formed on immersion Sn plated singulated lead.

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The Immersion Sn can be plated on the lead flank effectively with a wide range of leadframe thickness, typically from 0.1mm to 0.2mm. This process enables solder wetting of the side flanks in addition to the bottom leads during SMT reflow for AOI compatibility.

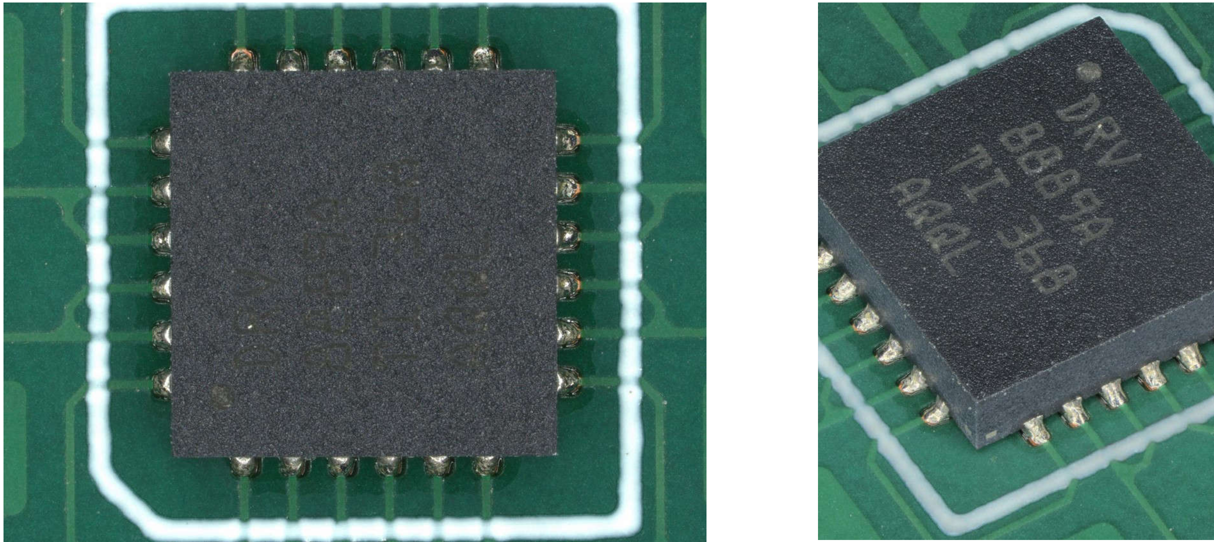

Figure 1. Sawn QFN on PCB Board With Good Solder Fillet Wetting Formed on Immersion Sn Plated Singulated Lead

Solder Joint Fillet and Inspection

The purpose of wettable flank is to form a solder fillet after post SMT on PCB. The fillet which can be detected through AOI (automated optical inspection) system is an indicator of good soldering to the PCB (see Figure 2). AOI system is widely used to inspect the solder fillet. However, AOI system can produce false positives (flagging acceptable joints as defective) and false negatives (missing actual defects or defects escape), affecting production efficiency and quality control. The false positives would lead to yield loss, and the false negatives would result to potential early failure on applications. The effectiveness of AOI systems relies on clear criteria and standards for acceptable solder joints and fillets based on specific automotive requirements (for example, IPC-A-610). In order to meet the AOI system capability, the industry requirement for solder fillet height is approximately 100um with a Cpk = 1.67.

Fillet height is measured from the PCB land to the apex of the fillet after SMT reflow. For an immersion Sn wettable flank QFN/SON package, the immersion Sn plating technology enables a coating of Sn plated on the full surface of the lead flank and the leadframe thickness is typically from 0.1mm to 0.2mm. Thus, the post-SMT fillet height measurement result is guaranteed with minimal 100µm fillet. It increases the AOI process window while inspecting the solder fillet height and result in a very low number of false calls during mass production. Since the QFN/SON leadframe is formed through etching process, the lead flank height can guarantee a Cpk = 1.67, thus the wetting height can achieve a Ckp = 1.67 to meet the requirement during SMT assembly process for AOI systems.

SEM images (see Figure 3) show the post-SMT solder fillet isometric view and cross-section from several different wettable-flank technology approaches. By comparing immersion Sn solution to the other two approaches known as step-cut and dimple leadframe, all three approaches have good wetting formation and solder fillet at the side lead to ensure AOI. The cross-section image of immersion Sn indicates a guarantee of minimal 100µm wetting height during package to PCB assembly. For the immersion Sn wettable flank option, there is no change on the PCB solder mask design, stencil design, type of solder and reflow profile. It can achieve the desired solder fillet formation the same as dimple and step-cut options and without reworking on the board design.

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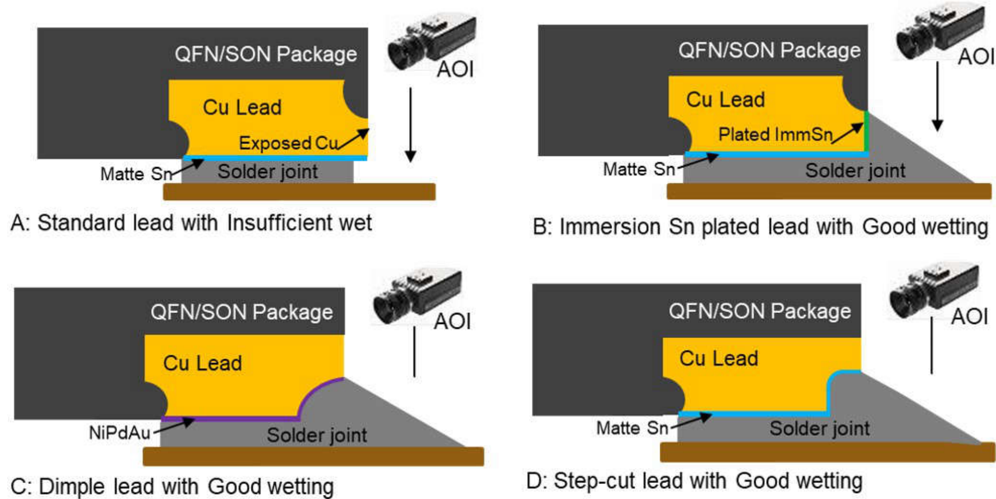

Figure 2. Insufficient Wet on Lead From Standard QFN/SON (A), Good Wetting on Immersion Sn Plated (B); Good Wetting on Step-Cut Lead (C); Good Wetting on Dimple Lead (D)

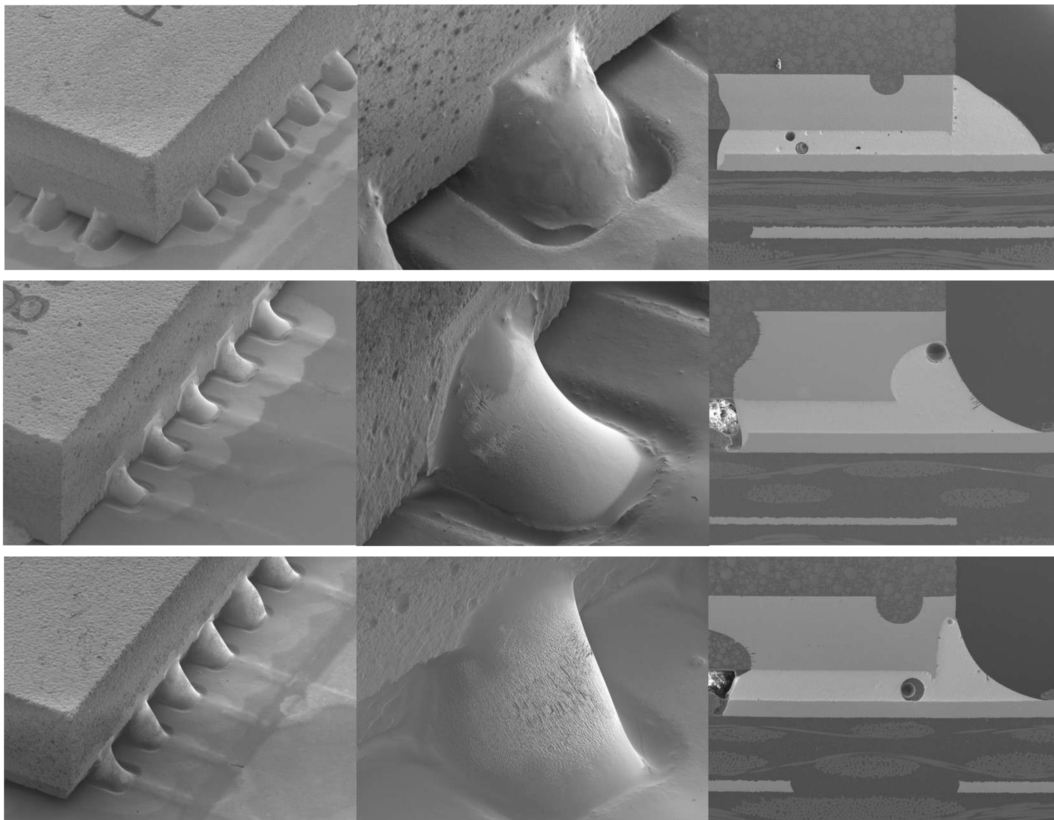

Figure 3. Solder fillet and good wetting in sawn QFN with Immersion Sn (top), sawn QFN with dimple lead (middle), sawn QFN with step-cut lead (bottom)

Solderability and Shelf Life

Solderability testing is essential for robust solder joint formation in electronic packaging and circuit board assembly applications. It assesses if the terminations of a component provide the degree of wetting necessary to form a robust solder connection. Solderability can degrade over time because of contamination or oxidation. Solderability test can also determine whether components left in storage has an adverse effect on the ability to solder to the PCB.

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Solderability testing per J-STD-002 Pb-free solder surface mount test was performed using dry bake preconditioning and a non-wettable ceramic plate substrate. SnAgCu solder paste was used for all testing [1]. Good wetting refers to a relatively uniform, smooth, and unbroken film of solder connection over the surface. The wetting height of the fillet was > 100um and satisfies the fillet height requirements called out in IPC-7093A for robust AOI inspection. Ceramic plate solderability test were conducted to verify the solderability after various pre-conditioning (unstressed post assembly, dry-bake 150ºC 4 hours, steam aging 85ºC 8 hours, respectively prior SMT reflow). Figure 4 demonstratea successful solderability using electroplated Matte Sn on the bottom and Immersion Sn on the flank. There is good wetting on the bottom and side wall flank of all leads. These units also show good wetting height on all electroplated and immersion Sn surfaces.

Additional solderability studies, using the same method as above, were conducted on a variety of aged units that had different Cu-Sn IMC thickness. FIB/cross-section on the aged units indicate the IMC layer and unconsumed Sn layer on the immersion Sn lead flank (see Figure 5). The results show that Immersion Sn units can have a shelf life of over 10 years when stored at 25°C.

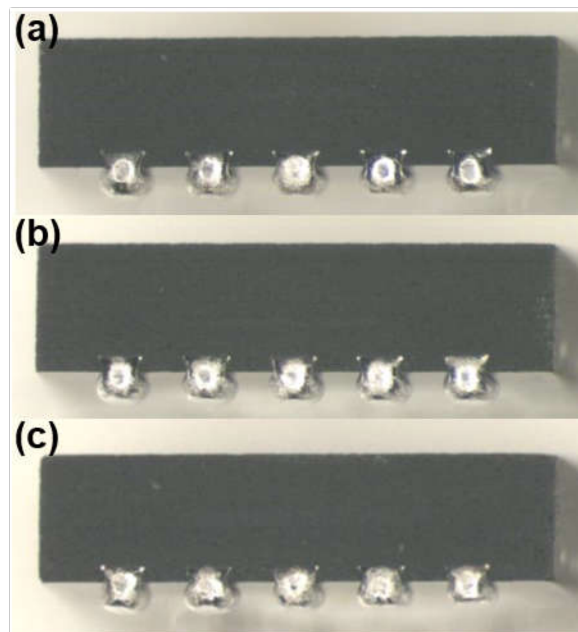

Figure 4. SON Package With Good Wetting on the Side Wall Flank After Preconditioning(a) unstressed, post assembly; (b) dry-bake 150ºC 4hours; (c) steam aging 85ºC 8hours

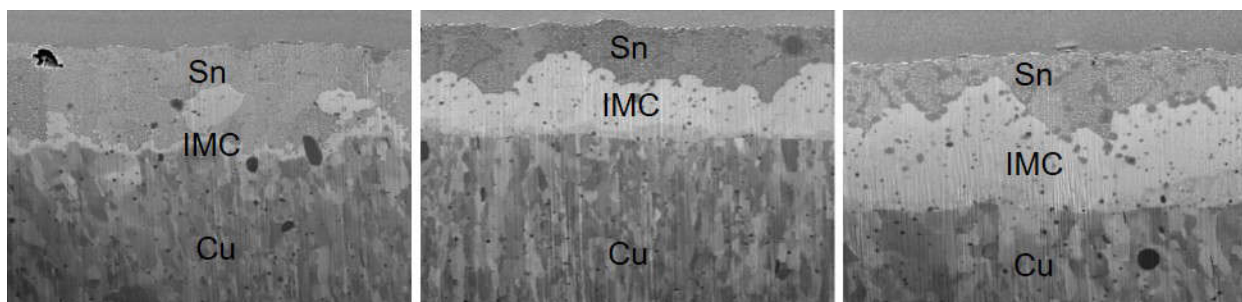

Figure 5. IMC Layer and Unconsumed Sn in FIB/Cross-Section on Immersion Sn QFN Package for Non-Aged Unit (left), Shel Llife Equivalent of 5 Years (middle), Shelf Life Equivalent of 10 Years (right)

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PCB Design

PCB land pad, stencil, and reflow guidelines can be found in the *QFN and SON PCB Attachment*. This application note covers QFN/SON with and without wettable flank. TI's guidelines are based on IPC-7351, which is one of the industry standard guidelines for PCB pad patterns. No special land pattern is needed for a QFN package with wettable flank. Guidelines have a minimum recommendation for the land pad to extend 0.2mm beyond the package to have enough space for good fillet formation. The guidelines allow for the land pad to be extended beyond 0.2mm to give flexibility for wetting angle and AOI optimization. Details are also given for the exposed center thermal pad, if one is present on the device of interest. Each device-specific data sheet provides the package drawing along with the recommended land pattern and stencil drawings.

Rework Procedure

The QFN/SON packages with plated immersion Sn are reworkable and can be removed after board assembly. Reworking QFN/SON packages can be a delicate process. Rework procedures are also covered in detail in *QFN and SON PCB Attachment*. A high level overview of the procedures for QFN packages are below:

1. Preparation of all necessary tools and materials.
   a. Utilize professional rework stations with precise temperature control. When performing the re-work, the PCB needs to be baked out prior to starting rework to reduce the risk of delamination.
   b. In addition, the PCB rework station should incorporate a preheater to reduce thermal shock and improve solder flow without overshooting the peak reflow temperature allowed as stated on the MSL label.
2. Component removal.
   a. Follow a controlled heating profile to minimize thermal stress on the component and the PCB. Avoid rapid temperature changes that could cause damage. Flux will be applied around the QFN/SON package. Use a hot air rework station to evenly heat the QFN package and ensure not to exceed the maximum temperature specified by the device-specific data sheet.
3. Site cleaning.
   a. Ensure no residues remain on the PCB by using a soldering iron and solder wick. Avoid aggressive cleaning agents that could damage the PCB or components.
4. Site preparation.
   a. Apply a layer of flux on the cleaned pads. Use a stencil to apply solder paste accurately on the pads.
5. Component placement.
   a. Place the new packages carefully on the prepared site, ensuring proper alignment.
6. Reflow soldering.
   a. Preheat the PCB to around 150ºC to ensure uniform temperature. Use the hot air rework station to reflow the solder. Gradually increase the temperature to 250°C-260°C, ensuring an even distribution of heat. Allow the solder to reflow and form good joints between the component leads and the PCB pads.
7. Cooling and inspection.
   a. Let the PCB cool down gradually to avoid thermal shock. Inspect the solder joints using a microscope to ensure they are well-formed and free of defects like bridging or insufficient solder. Perform electrical testing to verify the functionality of the reworked component.

By following these procedures and recommendations from Texas Instruments, reliable and high-quality rework of QFN packages can be achieved. For the most up-to-date and specific guidelines always refer to the latest documentation and technical resources provided by Texas Instruments.

Board-Level Reliability

The performance of surface mount packages during BLR temperature cycle test is a critical reliability metric. The purpose of the BLR testing is to determine the lifetime on the solder joint between the package and PCB. TI's standard auto TC test condition is -40°C to +125°C with 60 minutes per cycle. The PCB used for this testing is 1.6mm thick. Two types of BLR units were assembled, standard units with non-wettable flank, units with immersion Sn wettable flank. During the testing, solder connection is monitored for any electrical opens due to solder joint cracking. The target to meet is 1000 cycles without electrical failure. The units on the board will further stressed and generate the BLR data.

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All tested QFN packages are passing the testing criteria. The cross-sections indicate solder joint crack at the IMC interface which is the standard failure mode of non wettable flank QFN/SON packages with Matte Sn plating. The BLR results show that Immersion Sn technology doesn't degrade the BLR cycles to first fail comparing to non-wettable flank QFN packages.

SN Whisker Test

Spontaneous Sn whisker growth is known to occur readily on Sn plating on Cu leadframes. Some of the whiskers can be long enough to cause shorting failure. Though Sn whisker tests are not required for QFN/SON by JEDEC standard JESD201A [2], to be sure that Sn whisker would not grow in the immersion Sn to cause any potential issue, a proprietary anti-whisker agent was added to the plating bath. To verify its effect, Sn whisker tests have been conducted following JEDEC standards JESD201A and JESD22-A121A [3]. The test vehicle was a 24 pin QFN. All three required tests were carried out:

- Thermal cycling: test condition -55°C/85°C, 3 cycles per hour; test duration 1500 cycles; inspection at every 500 cycles.
- Temperature/humidity storage: test condition 30°C/60%RH; test duration 4000 hours; inspection at every 1000 hours.
- High temperature/humidity storage: test condition 55°C/85%RH; test duration 4000 hours; inspection at every 1000 hours.

Samples were pulled out at every reading point for inspection under the optical microscope. No Sn whisker was found on the bottom of the leads that had matte Sn and the sidewall of the lead end that had immersion Sn. It is concluded that Sn whisker is not a concern for QFN packages with matte Sn on the bottom and immersion Sn on the lead end.

Summary

The integration of wettable flanks in leadless automotive packages significantly enhances solder joint inspectability during post SMT PCB assembly and mass production. The novel plating technology enables wettable flank with immersion Sn plated on lead flanks of QFN/SON packages. The solder fillet and fillet height during SMT PCB reflow has been reviewed. The QFN/SON package with immersion Sn plated wettable flank shows the similar solder fillet as alternative wettable flank approach such as dimple leadframe and step-cut. Based on collected reliability testing data, the devices can guarantee a good wettability with AOI compatibility. The current data indicates the components can be kept over 10 years of shelf life at room temperature.

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