Evaluation Module for TPS65150 Low Input Voltage, Compact LCD Bias IC With VCOM

This user's guide describes the characteristics, operation, and use of the TPS65150 evaluation module (EVM). This EVM contains TI's display supply IC TPS65150 with low-input voltage capability of 1.8 V. The user's guide includes EVM specifications, the schematic diagram, the board layouts, and the bill of materials.

All typical characteristics measurements in the TPS65150 datasheet (SLVS576) were done with this evaluation module.

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1 Introduction

TI's TPS65150 evaluation module (EVM) uses a TPS65150 to support three voltages driven for thin-film transistor (TFT), liquid-crystal display (LCD) panels or general dual-power supply applications. The goal of the EVM is to facilitate evaluation of the TPS65150. The device uses a single-inductor scheme in order to provide the smallest solution size possible, as well as high efficiency. With its input voltage range of 1.8 V to 6 V, it is optimized for notebooks powered by a 2.5-V or 3.3-V input rail or monitor applications with a 5-V input voltage rail.

1.1 Requirements

Two regulated adjustable charge pump drivers provide the positive V_{GH} and negative V_{GL} bias voltage for the TFT. This avoids any additional external components to implement application-specific sequencing.

1.1.1 Power Supply

In order to operate this EVM, only a DC power supply capable of delivering between 1.8 V and 6 V at up to 1 A is necessary. The EVM is fully functional, except changing the output voltages with just a power supply connected.

1.2 Applications

- TFT LCD displays for notebooks
- TFT LCD displays for monitors
- Car navigation displays

1.3 Features

- 1.8-V to 6-V input voltage range
- Integrated VCOM buffer
- High voltage switch to isolate V_{GH}
- V_S with 1% output voltage accuracy
- Adjustable power on sequencing
- Adjustable fault detection timing
- Excellent line regulation
- Thermal shutdown
- Double-sided, two-active-layer PCB with all components on top side

2 TPS65150 EVM Electrical and Performance Specifications

Table 1 provides the EVM electrical and performance specifications.

Table 1. TPS65150 EVM Electrical and Performance Specifications

Parameter		Test Conditions	MIN	TYP	MAX	Unit
Supply Current						
V_{IN}	Input voltage range		1.8	5	6.0	V
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		1.6	1.8	V
V_{hys}	Undervoltage lockout threshold	V_{IN} rising		1.7	1.9	V
Main Boost Converter						
V_S	Output voltage range				15	V
I_{LEAK}	Switch leakage current	V_{sw} = 15 V		1	10	µA
V_{OVP}	Output overvoltage protection	V_{OUT} rising	16		20	V
	Line regulation	V_{IN} = 1.8 V to 6.0 V, Iout = 1 mA		0.007		%/V
	Load regulation	V_{IN} = 5 V, Iout = 0 A to 400 mA		0.16		%/A
Negative Charge Pump V_{GL}						
V_{GL}	Output voltage range				–2	V
	Load regulation	V_{GL} = –5 V, Iout = 0 mA to 20 mA		0.016		%/mA
Positive Charge Pump Output						
V_{CPO}	Output voltage range	CTRL = GND, V_{GH} = open			30	V
	Load regulation	V_{GH} = 24 V, Iout = 0 mA to 20 mA		0.07		%/mA
V_{GH} Isolation Switch, Gate Voltage Fall Time Control						
V_{GH}	Minimum output voltage	V_{adj} = 0 V, I_{VGH} = 10 mA		2		V
I_{VGH}	Maximum output current		20			mA
Gate Drive (GD)						
$V_{(GD,\ Vs)}$	Gate drive threshold[1]	V_S rising	–12% of V_S		–4% of V_S	%/V
V_{OL}	Gate drive output low voltage	$I_{(sink)}$ = 500 µA			0.5	V
I_{LKG}	Gate drive output leakage current	V_{GD} = 15 V		0.001	1	µA
VCOM Buffer						
V_{CM}	Common mode input range		2.25		(V_S) –2	V
V_{os}	Input offset voltage	I_{OUT} = 0 mA	–25		25	mV

(1) The GD signal is latched low when the main boost converter output V_S is within regulation. The GD signal is reset when the input voltage or enable of the boost converter is cycled low.

3 TPS65150 EVM Schematic

Figure 1 is for reference only; see the bill of materials in Table 2 for specific values.

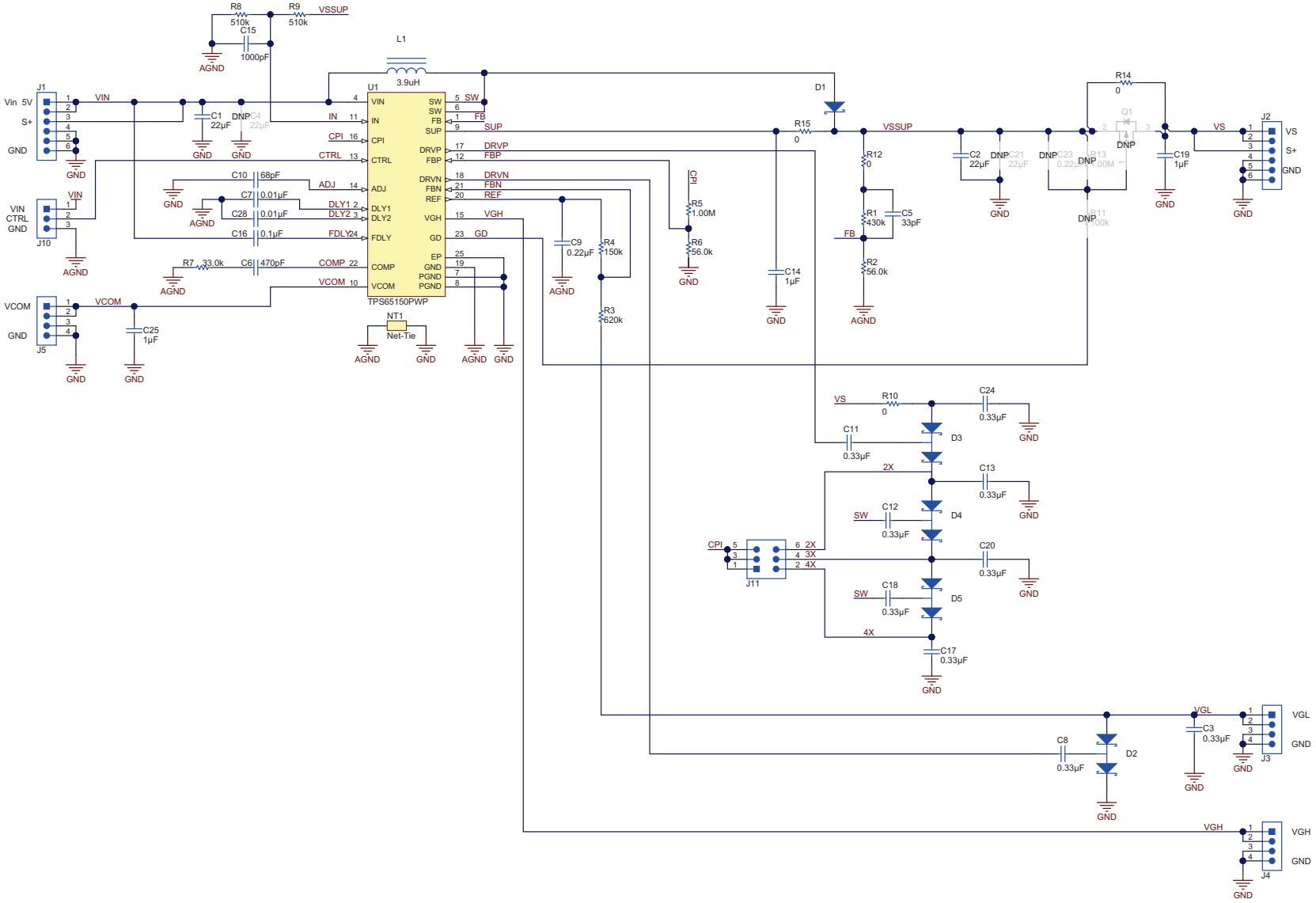

Figure 1. TPS65150 EVM Schematic

4 Connector and Test Point Descriptions

4.1 Input Headers

4.1.1 J1 – VIN, Input Sense and GND Connector

This header is the connection to the input power supply as well as its sense connection. The power supply must be connected between pins 1 and 2 (V_{IN}) and pins 5 and 6 (GND). Twist the leads to the input supply and keep them as short as possible.

The middle 2 pins of this header are intended to measure the input voltage directly on the input capacitor. Therefore, a 4-wire power and sense supply can be connected. Twist the leads to the sensing connector.

4.1.2 J10 -- VIN/CTRL, Input Sense and GND Connector

This header sets V_{GH} and offers to use gate voltage shaping. To set V_{GH}, place a jumper between CTRL and VIN. To enable gate voltage shaping, refer to the TPS65150 datasheet (SLVS576).

4.1.3 J11 -- CPI, Input Sense, and GND Connector

This header sets the charge pump. For normal operation, the charge pump works as a tripler, therefore, the header should be placed between pin 3 and 4. Optionally, the charge pump can be set as a doubler for higher V_S, as well as a quadrupler for lower V_S.

4.2 Output Headers

4.2.1 J2 – VS Output Sense and GND Connector

This header is the connection of the output voltage of the boost converter as well as its sense connection. Connect the boost converter's load between pins 1 and 2 (V_S) and pins 5 and 6 (GND).

The middle 2 pins of this header are intended to measure the output voltage of the boost converter directly on the output capacitors.

4.2.2 J3 – VGL Output Sense and GND Connector

This header is the connection of the output voltage of the positive charge pump. Connect the charge pump's load between pins 1 and 2 (V_{GL}) and pins 3 and 4 (GND).

4.2.3 J4 -- VGH Output Sense and GND Connector

This header is the connection of the output voltage of the positive charge pump. Connect the charge pump's load between pins 1 and 2 (V_{GH}) and pins 3 and 4 (GND).

4.2.4 J5 -- VCOM Output Sense and GND Connector

This header is the connection of the output voltage of the VCOM Buffer. Connect the charge pump's load between pins 1 and 2 (V_{GL}) and pins 3 and 4 (GND).

5 TPS65150 EVM Board Layout

Figure 2 through Figure 3 show the design of the TPS65150 EVM printed-circuit board (PCB). The EVM has been designed using a two-layer, 35-µm (1 oz), copper-clad circuit board. All components are on the top side, and all active traces on the top and bottom layers allow the user to easily view, probe, and evaluate the TPS65150 control IC. Moving components to both sides of the PCB can offer additional size reduction for space-constrained systems.

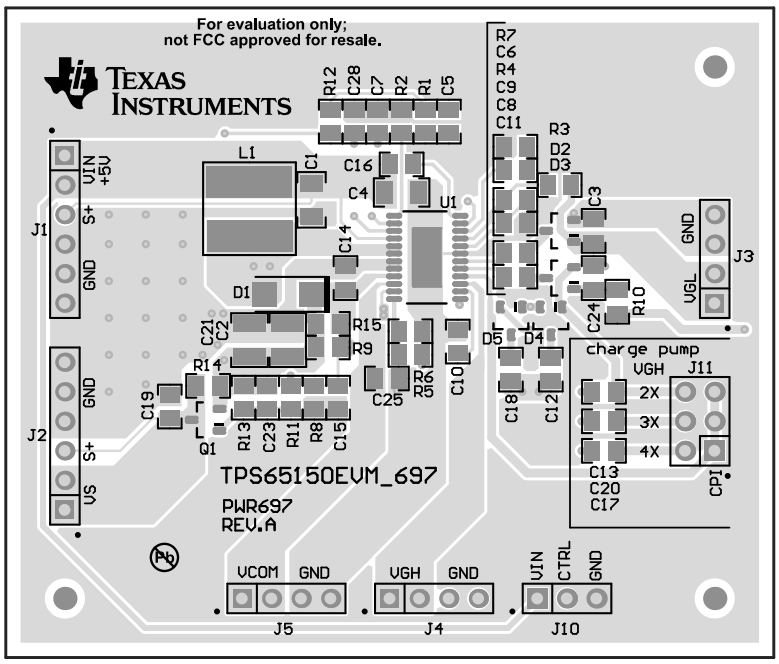

Figure 2. TPS65150 EVM Component Placement, Viewed from Top

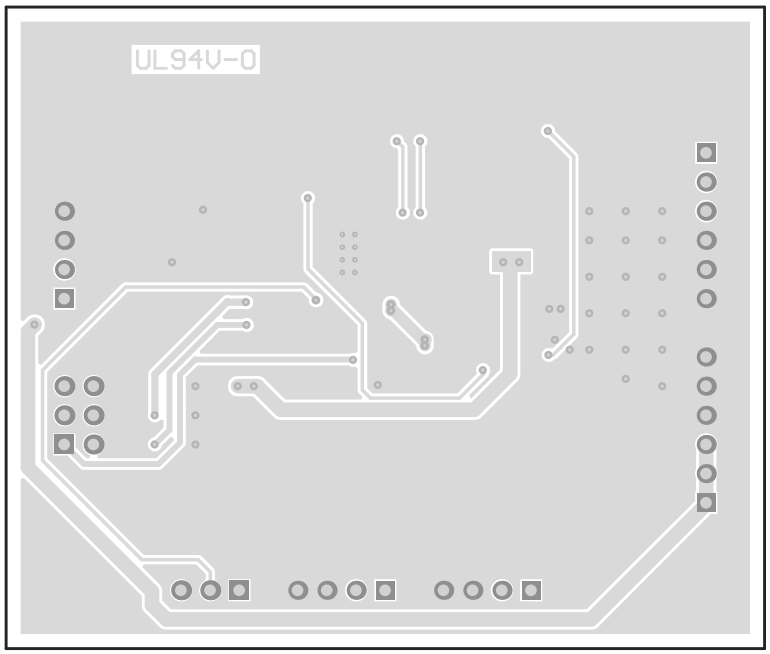

Figure 3. TPS65150 EVM Bottom Copper, Viewed from Bottom

6 List of Materials

Table 2 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 2. TPS65150 EVM Bill of Materials

Designator	Qty	Value	Description	Part Number	Manufacturer
C1	1	22uF	CAP, CERM, 22 µF, 10 V, +/- 10%, X6S, 1206	GRM31CC81A226KE19L	Murata
C2	1	22uF	CAP, CERM, 22 µF, 25 V, +/- 20%, X5R, 1210	12103D226MAT2A	AVX
C3, C8, C11, C12, C13, C17, C18, C20, C24	9	0.33uF	CAP, CERM, 0.33 µF, 50 V, +/- 10%, X7R, 0805	GRM219R71H334KA88D	Murata
C5	1	33pF	CAP, CERM, 33 pF, 50 V, +/- 5%, C0G/NP0, 0805	C0805C330J5GACTU	Kemet
C6	1	470pF	CAP, CERM, 470 pF, 50 V, +/- 1%, C0G/NP0, 0805	08055A471FAT2A	AVX
C7, C28	2	0.01uF	CAP, CERM, 0.01 µF, 50 V, +/- 5%, X7R, 0805	08055C103JAT2A	AVX
C9	1	0.22uF	CAP, CERM, 0.22 µF, 50 V, +/- 10%, X7R, 0805	C2012X7R1H224K	TDK
C10	1	68pF	CAP, CERM, 68 pF, 50 V, +/- 5%, C0G/NP0, 0805	GQM2195C1H680JB01D	Murata
C14, C19, C25	3	1uF	CAP, CERM, 1 µF, 50 V, +/- 10%, X7R, 0805	GRM21BR71H105KA12L	Murata
C15	1	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0805	C0805C102J5GACTU	Kemet
C16	1	0.1uF	CAP, CERM, 0.1 µF, 50 V, +/- 20%, X7R, 0805	C0805C104M5RACTU	Kemet
D1	1	20V	Diode, Schottky, 20 V, 1.5 A, SMA	SL12-E3/61T	Vishay-Semiconductor
D2, D3, D4, D5	4	30V	Diode, Schottky, 30 V, 0.2 A, SOT-23	BAT54S-7-F	Diodes Inc.
L1	1	3.9uH	Inductor, Shielded Drum Core, Ferrite, 3.9 µH, 2.6 A, 0.027 ohm, SMD	CDRH6D28NP-3R9NC	Sumida
R1	1	430k	RES, 430 k, 0.1%, 0.125 W, 0805	RG2012P-434-B-T5	Susumu Co Ltd
R2, R6	2	56.0k	RES, 56.0 k, 0.5%, 0.1 W, 0805	RR1220P-563-D	Susumu Co Ltd
R3	1	620k	RES, 620 k, 0.1%, 0.125 W, 0805	RG2012P-624-B-T5	Susumu Co Ltd
R4	1	150k	RES, 150 k, 1%, 0.125 W, 0805	CRCW0805150KFKEA	Vishay-Dale
R5	1	1.00Meg	RES, 1.00 M, 0.1%, 0.125 W, 0805	RG2012P-105-B-T5	Susumu Co Ltd
R7	1	33.0k	RES, 33.0 k, 0.1%, 0.125 W, 0805	RG2012P-333-B-T5	Susumu Co Ltd
R8, R9	2	510k	RES, 510 k, 0.5%, 0.1 W, 0805	RR1220P-514-D	Susumu Co Ltd
R10, R12, R14, R15	4	0	RES, 0, 5%, 0.125 W, 0805	MCR10EZHJ000	Rohm
U1	1		3-Channel LCD Bias with GPM, VCOM Buffer & Gate Driver for Isolation Switch, 1.8 to 6 V, -40 to 85 degC, 24-pin SOP (PWP24), Green (RoHS & no Sb/Br)	TPS65150PWP	Texas Instruments

Revision History

Changes from Original (July 2015) to A Revision **Page**

- Changed schematic image. 4
- Changed images in *TPS65150 EVM Board Layout* section. 6

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
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Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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