User's Guide

TPS650330-Q1 EVM User's Guide

ABSTRACT

The TPS650330-Q1 EVM is an evaluation board for the TPS65033x-Q1 Power Management Integrated Circuits (PMICs). The EVM includes an onboard USB-to-I^{2}C adapter, power terminals and jumpers for all DC regulator inputs and outputs, and test points for common measurements.

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1 Introduction

The TPS650330-Q1 device is a highly integrated PMIC for automotive camera modules. This device combines three step down converters and one low-dropout (LDO) regulator. The BUCK1 step-down converter has an input voltage range up to 18.3 V for connections to power over coax. All converters operate in a forced fixed-frequency PWM mode. The LDO can supply 300 mA and operate with an input voltage range from 2.2 V to 5.5 V. The step-down converters and the LDO have separate voltage inputs that enable maximum design and sequencing flexibility.

2 Requirements

- Computer with Windows, MacOS, or Linux operating system
- Camera PMIC GUI (Link Here)
- Micro-USB Cable
- TPS650330-Q1 EVM
- DC Power Supply (4.5 V to 19 V)
  - Banana Cables for Power and GND

3 Operation Instructions

1. Ensure USB to I^2C Adapter is configured properly using the jumpers mentioned in Configuring the USB to I^2C Adapter. For most applications, this will be the default configurations defined in the tables.
2. Configure regulator input supply rails for the expected application using the jumpers mentioned in Regulator Input Supplies and Features. Take extra care not to exceed absolute maximum ratings when VSYS supplies BUCK2, BUCK3, or the LDO.
3. Connect Micro-USB to a PC capable of loading the Camera PMIC GUI.
4. Connect VSYS to a power supply capable of supporting the application and enable the supply. Typical supply voltage is 12 V. The PMIC will boot automatically as VSYS is applied.
5. Set the SEQ switch (S1) to *ON* to enable the Buck 1 and Buck 2 regulators.
6. Set GPIO switch (S4) to *ON* to enable the Buck 3 and LDO regulators.
7. Load the Camera PMIC GUI and ensure the adapter has been recognized by the PC. If the GUI says *Hardware not connected*, refer to TPS650330-Q1 EVM Debugging.
8. Step 6: Once the adapter is connected, the GUI will attempt to read all registers and update the register map.

3.1 Configuring the USB to I^2C Adapter

An onboard MCU acts as a USB adapter to the PMIC. This adapter allows I^2C communication to the host PC as well as GPIO assertion and monitoring. By default, the onboard adapter is powered by the USB cable through an onboard dedicated 3.3 V LDO (U4). Additional configurations are allowed by reconfiguring jumpers J18 and J19, shown in Table 3-1 and Table 3-2. The onboard adapter must have power applied through a valid configuration.

Table 3-1. Adapter Power Source (J18)

Selection Jumper Pin	Adapter Supply Bus
Pin 1 (PMIC Buck 1 Output)	Pin 2 (Adapter Input Supply Rail)
Pin 3 (PMIC LDO Output)	Pin 4 (Adapter Input Supply Rail)
Pin 5 (Dedicated 3.3 V LDO Output - *Default*)	Pin 6 (Adapter Input Supply Rail)

Table 3-2. Dedicated LDO Supply for Adapter (J19)

Selection Jumper Pin	Dedicated 3.3V LDO Supply Bus
Pin 1 (PMIC Buck 1 Output)	Pin 2 (Dedicated 3.3 V LDO Input Rail)
Pin 3 (PMIC Buck 1 Input - *Default*)	Pin 4 (Dedicated 3.3 V LDO Input Rail)
Pin 5 (VBUS Rail)	Pin 6 (Dedicated 3.3 V LDO Input Rail)

The following Jumpers in Table 3-3 connect the USB adapter to PMIC functional pins. These can be disconnected for flexibility.

Table 3-3. Adapter PMIC Connections

Jumper	PMIC Pin
J21	nRST
J22	SEQ

3.2 Regulator Input Supplies and Features

The four regulators on the TPS650330-Q1 EVM can be supplied with multiple supplies. The following tables show the possible supply configurations in addition to key specifications and programmable features for each regulator.

3.2.1 Buck 1 Input Supply

Table 3-4. Buck 1 Power Source (J33)

Selection Jumper Pin	Buck1 Supply Bus
Pin 1 (VSYS - *Default*)	Pin 2 (Buck 1 Input Supply Rail)

3.2.2 Mid-Vin Buck1 Features

Table 3-5. Mid-Vin (Buck1) Features

Feature	Specification
Input Voltage Range	4 V to 18.3 V
Operating Current	Maximum of 1.5 A
Current Limiting	1.8 A to 3.6 A
Status Monitoring	UVLO, UV, HOT, OVP, SCG, OCP
Over-Voltage Protection (OVP)	VOUT = 109% to 115%
Short-Circuit Threshold (SCG)	VOUT = 250 mV to 350 mV

Table 3-6. Mid-Vin (Buck1) Configurable Settings

Feature	Configurable Range
Output Voltage	2.5 V to 4.0 V
PVIN_B1 UVLO Rising	3.64 V to 9.36 V
PVIN_B1 UVLO Falling	3.5 V to 9 V
Output Discharge	Disabled, 125 Ω, 250 Ω, and 500 Ω
Sequencing	Enable, Dependencies, and Fault RST
Sequence Delay (Off and On)	0 ms to 20 ms

Note: Over-voltage monitor settings are available for the TPS650331-Q1, TPS650332-Q1, and TPS650333-Q1.

3.2.3 Buck 2 Input Supply

Table 3-7. Buck 2 Power Source (J15)

Selection Jumper Pin	Buck2 Supply Bus
Pin 1 (VSYS)	Pin 2 (Buck 2 Input Supply Rail)
Pin 3 (Buck1 Output Rail - *Default*)	Pin 4 (Buck 2 Input Supply Rail)

3.2.4 Buck 3 Input Supply

Table 3-8. Buck 3 Power Source (J16)

Selection Jumper Pin	Buck3 Supply Bus
Pin 1 (VSYS)	Pin 2 (Buck 3 Input Supply Rail)
Pin 3 (Buck1 Output Rail - *Default*)	Pin 4 (Buck 3 Input Supply Rail)

3.2.5 Low-Vin Buck2 and Buck3 Features

Table 3-9. Low-Vin (Buck2 and Buck3) Features

Feature	Specification
Input Voltage Range	2.5 V to 5.5 V
Operating Current	Maximum of 1.2 A
Current Limiting	1.6 A to 2.8 A
Status Monitoring	UV, HOT, OVP, SCG, OCP
Over-Voltage Protection (OVP)	VOUT = 109% to 115%
Short-Circuit Threshold (SCG)	VOUT = 250 mV to 350 mV

Table 3-10. Low-Vin (Buck2 and Buck3) Configurable Settings

Feature	Configurable Range
Output Voltage	0.9 V to 1.9 V
Under-Voltage Flags (UV)	VOUT = 94.5%, 95%, 95.5%, and 96%
Spread Spectrum	Enable or Disable
Sequencing	Enable, Dependencies, and Fault RST
Sequence Delay (Off and On)	0 ms to 20 ms

Note: Over-voltage monitor settings are available for the TPS650331-Q1, TPS650332-Q1, and TPS650333-Q1.

3.2.6 LDO Input Supply

Table 3-11. PMIC LDO Power Source (J8)

Selection Jumper Pin	PMIC LDO Supply Bus
Pin 1 (VSYS)	Pin 2 (PMIC LDO Input Supply Rail)
Pin 3 (Buck1 Output Rail - *Default*)	Pin 4 (PMIC LDO Input Supply Rail)
Pin 5 (Buck2 Output Rail)	Pin 6 (PMIC LDO Input Supply Rail)
Pin 7 (Buck3 Output Rail)	Pin 8 (PMIC LDO Input Supply Rail)

3.2.7 Low Noise LDO Features

Table 3-12. Low Noise LDO Features

Feature	Specification
Input Voltage Range	2.5 V to 5.5 V
Operating Current	Maximum of 150 mA or 300 mA
Current Limiting	Minimum of 200 mA or 400 mA
Status Monitoring	UV, HOT, OVP, SCG, OCP
Over-Voltage Protection (OVP)	VOUT = 109% to 115%
Short-Circuit Threshold (SCG)	VOUT = 250 mV to 350 mV

Table 3-13. Low Noise LDO Configurable Settings

Feature	Configurable Range
Output Voltage	1.8 V, or 2.7 V to 3.3 V
Under-Voltage Flags (UV)	VOUT = 94.5%, 95%, 95.5%, and 96%
Load Switch Mode	Enable or Disable
Current Limit	200 mA, 400 mA
Sequencing	Enable, Dependencies, and Fault RST
Sequence Delay (Off and On)	0 ms to 20 ms

Note: Over-voltage flag settings are available for the TPS650331-Q1, TPS650332-Q1, and TPS650333-Q1.

3.3 Selecting the Logic Supply Voltage

Table 3-14. VIO Power Source (J8)

Selection Jumper Pin	VIO Supply Bus
Pin 1 (Buck1 Output Rail - *Default*)	Pin 2 (VIO Input Supply Rail)
Pin 3 (Buck2 Output Rail)	Pin 4 (VIO Input Supply Rail)
Pin 5 (Buck3 Output Rail)	Pin 6 (VIO Input Supply Rail)
Pin 7 (PMIC LDO Output Rail)	Pin 8 (VIO Input Supply Rail)
Pin 9 (Dedicated 3.3 V LDO)	Pin 10 (VIO Input Supply Rail)

4 EVM Configurations

The following sections outline how to configure the TPS650330-Q1 EVM for general experimentation.

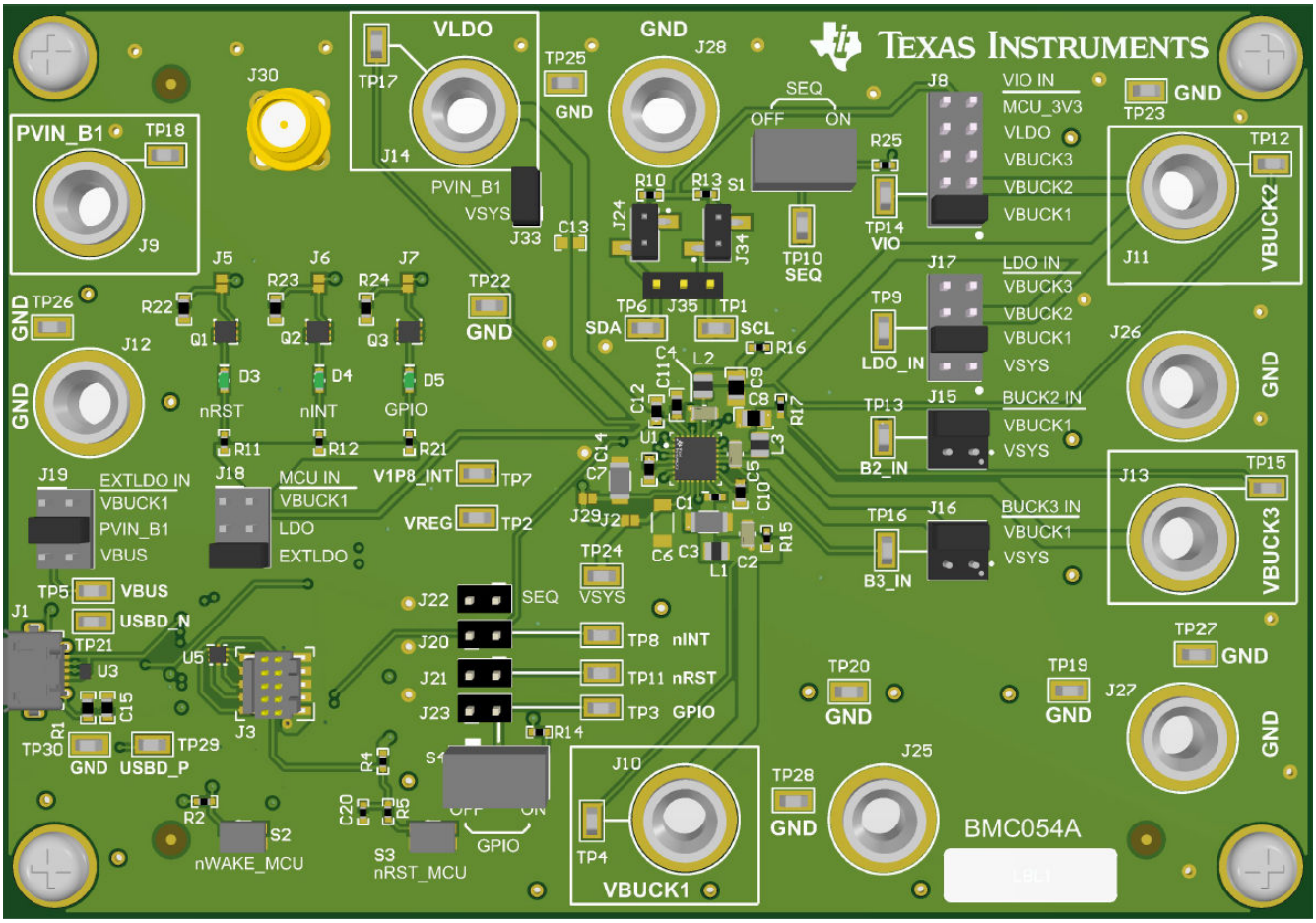


Figure 4-1. TPS650330-Q1 EVM Top View

5 Test Points

5.1 Voltage Test Points

The TPS650330-Q1 EVM contains 30 test points for various measurements. Trace assignments to the test points are shown in Table 5-1. For reference, Figure 5-1 demonstrates the test point locations on the EVM.

Table 5-1. TPS650330-Q1 EVM Test Points

Test Point Number	Associated Trace
TP1	SCL
TP2	VREG
TP3	GPIO
TP4	Buck 1 Output
TP5	VBUS
TP6	SDA
TP7	V1P8_INT
TP8	nINT
TP9	PMIC LDO Input
TP10	SEQ
TP11	nRSTOUT
TP12	Buck 2 Output
TP13	Buck 2 Input
TP14	VIO
TP15	Buck 3 Output
TP16	Buck 3 Input
TP17	PMIC LDO Output
TP18	Buck 1 Input
TP19	GND
TP20	GND
TP21	USBD_N
TP22	GND
TP23	GND
TP24	VSYS
TP25	GND
TP26	GND
TP27	GND
TP28	GND
TP29	USBD_P
TP30	GND

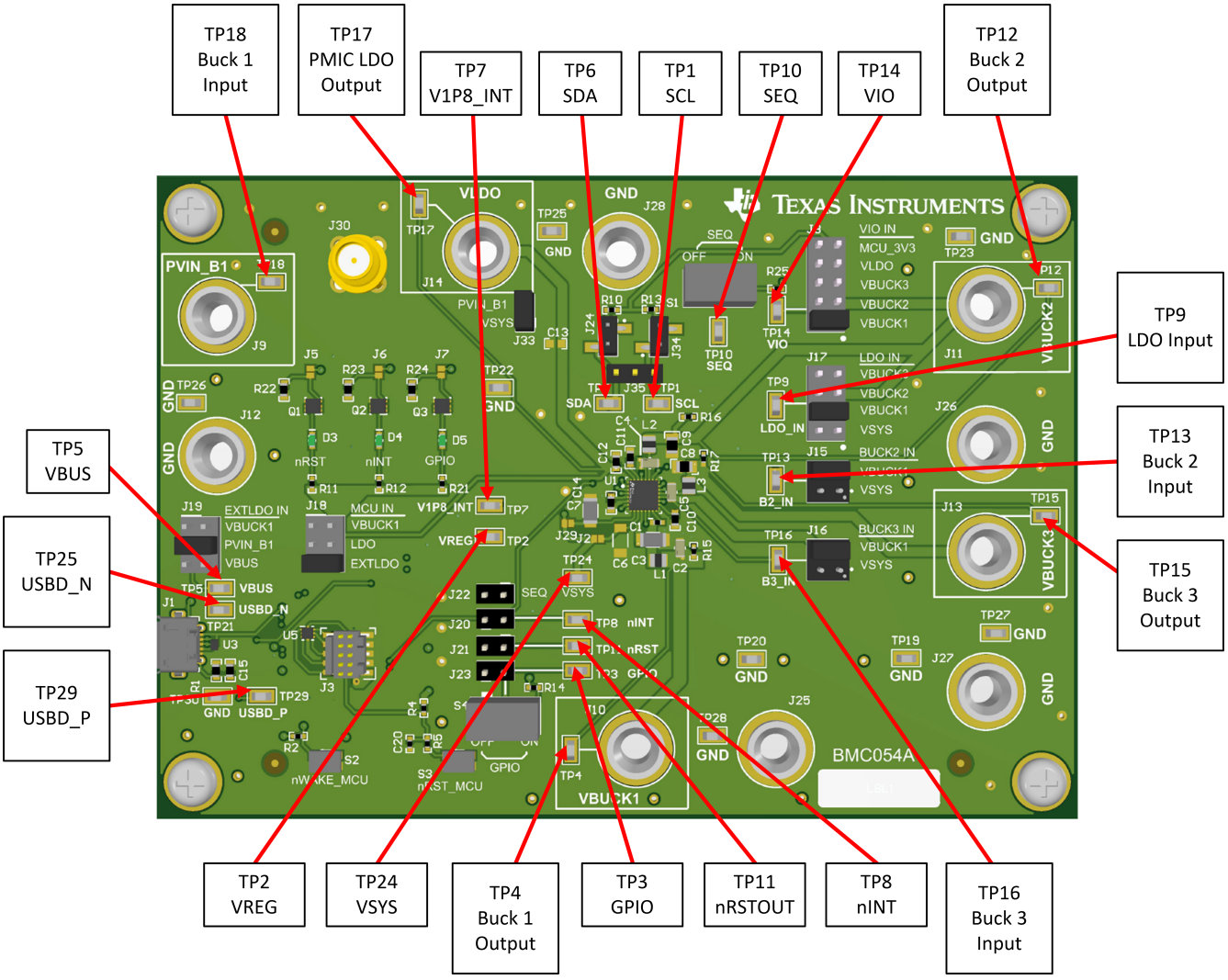


Figure 5-1. TPS650330-Q1 EVM Test Point Locations

6 Graphical User Interface

The Graphical User Interface (GUI) for the EVM can be found in the Gallery at TI DevTools. The GUI can be operated through Google Chrome™ or Mozilla Firefox™ web browsers. To run the GUI in the browser, click the thumbnail and follow the prompted instructions for first time installation. The GUI requires both a browser plugin and the TI Cloud Agent software for access to the local USB ports. The GUI can also be downloaded for offline operation by hovering over the downward arrow in the GUI thumbnail and selecting the desired platform – Windows®, macOS®, or Linux®.

6.1 TPS650330-Q1 EVM Debugging

Refer to Figure 6-1 to debug potential issues while using the TPS650330-Q1 EVM.

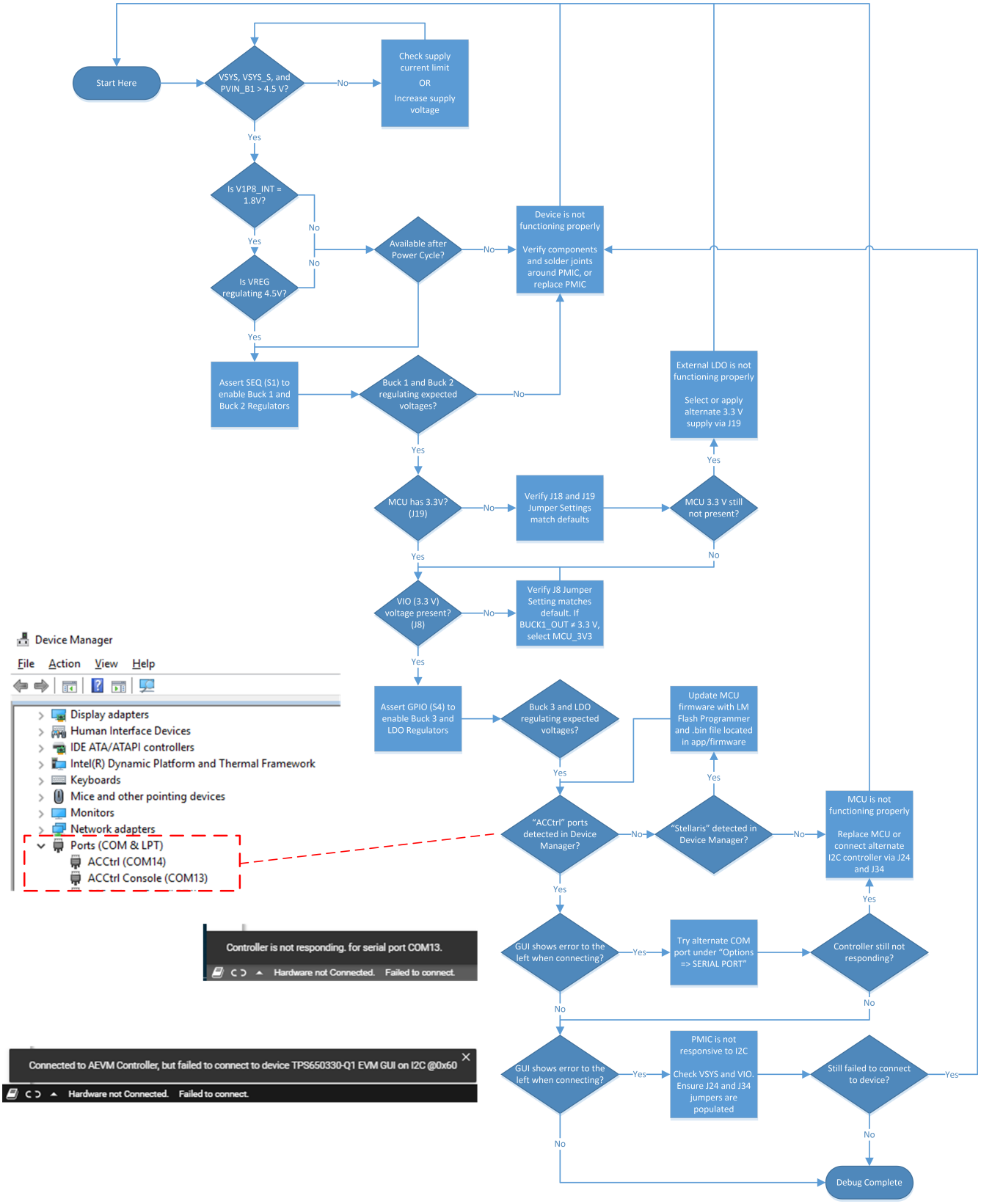


Figure 6-1. TPS650330-Q1 EVM Debugging Flow Chart

6.1.1 I²C Communication Port and Adapter Debugging

By default, the GUI will recognize two serial ports from the EVM adapter, but may not select the I²C bridge automatically. Once the EVM is powered and the USB cable is connected to the computer, click the connect icon at the bottom left of the GUI. If the bottom notification updates to *Hardware Not Selected*:

1. Click the Options menu at the top of the GUI, select *Serial Port*.

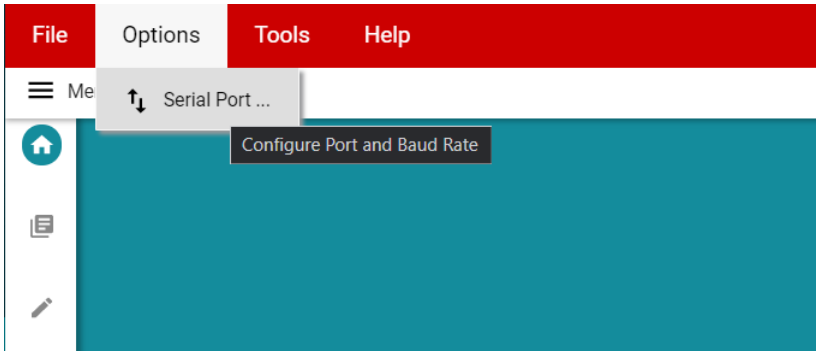


Figure 6-2. Opening Serial Port Options

2. Use the Ports dropdown to select the alternative interface.

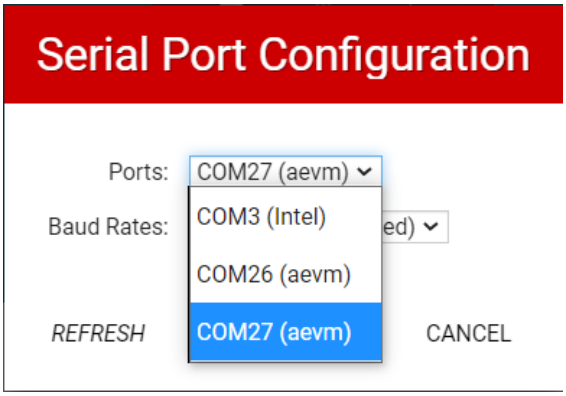


Figure 6-3. Selecting an Alternate Port

After clicking OK, the GUI should connect to the device properly. If communication to the EVM is lost, most issues can be resolved by pressing the nRST_MCU button (S3) on the EVM. Afterwards, further issues can be diagnosed by confirming that MCU_IN (J18) is still present, and that the I²C pull-up domain is still active.

6.1.2 Updating MCU Firmware

If the EVM on-board MCU is showing up under the Device Manager with a *Stellaris...* title, the MCU firmware needs to be updated to communicate with the GUI. One way to do this is with TI's free LM Flash Programmer tool. Once the firmware is updated, the MCU should show up as *ACCtrl...* COM ports in the Device Manager.

1. Download the GUI source files from the Gallery. The EVM firmware is the .bin file located in the install_image_TPS6503xx-Q1_GUI/TPS6503xx-Q1_GUI/app/firmware folder.
2. Open LM Flash Programmer with the EVM connected through USB.
3. Select *USB DFU* in the *Configuration* tab. The Stellaris device should show in the device list box after refreshing.
4. Select the *Program* tab.
5. Browse to the .bin file downloaded from the GUI.
6. Leave all other settings as default.
7. Click *Program*.

6.2 Navigating the GUI

The GUI contains the following five sections, selectable on the left side of the GUI or by clicking the Menu tab in the top left corner.

- Home
- Block Diagram
- Registers
- Device Configuration
- Re-Program PMIC

6.2.1 Home

The Home section is the landing page of the GUI. Here the GUI presents an overview of the EVM and Programming BoosterPack (BOOSTXL-TPS65033), and emphasize navigation to the remaining four sections through the tiles on the bottom of the page.

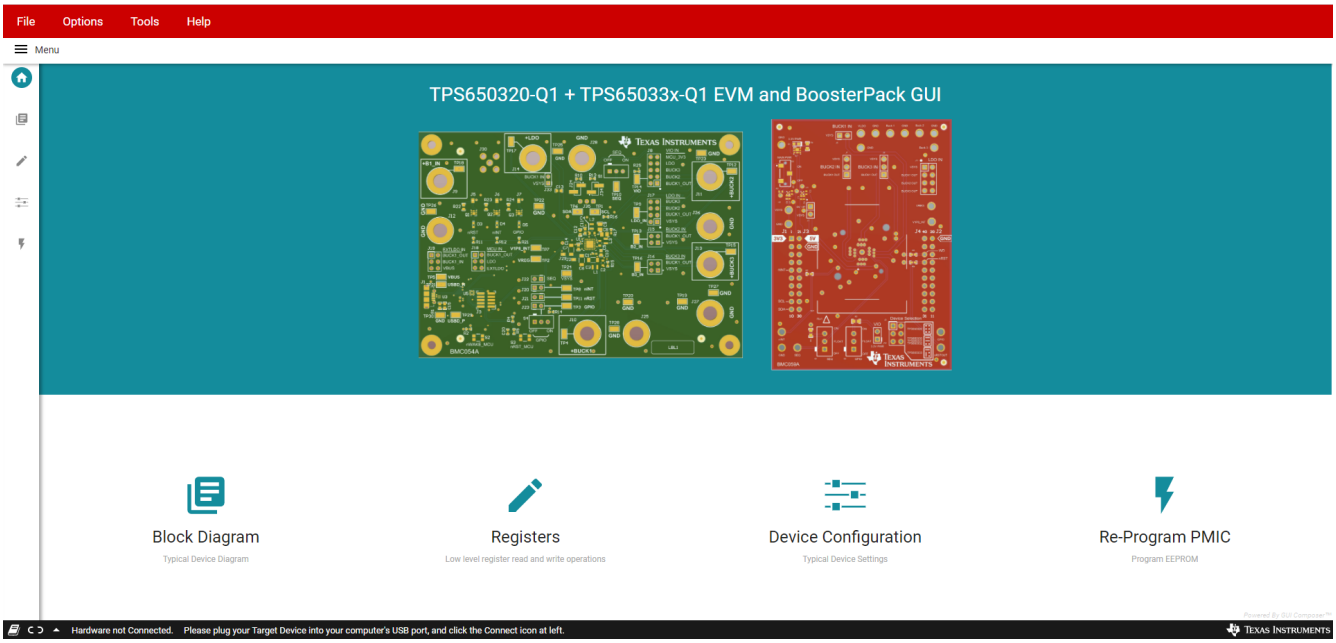


Figure 6-4. TPS6503xx-Q1 GUI Home Screen

6.2.2 Block Diagram

The Block Diagram section displays the typical components and functional blocks of the PMIC. A block diagram for the Programming BoosterPack is also shown.

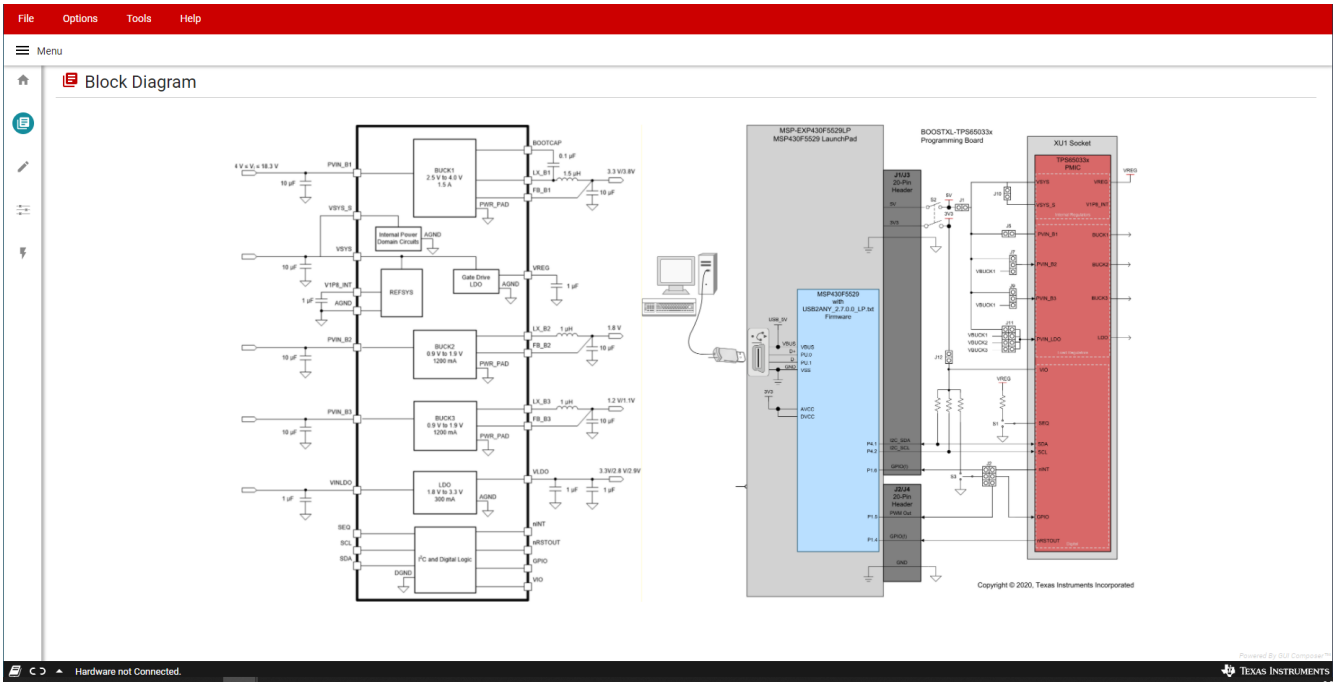


Figure 6-5. TPS6503xx-Q1 GUI Block Diagram Page

6.2.3 Registers

The Registers section provides an overview of the internal register map, and includes basic interfaces for each PMIC register. Figure 6-6 illustrates the register page and the primary interactive regions.

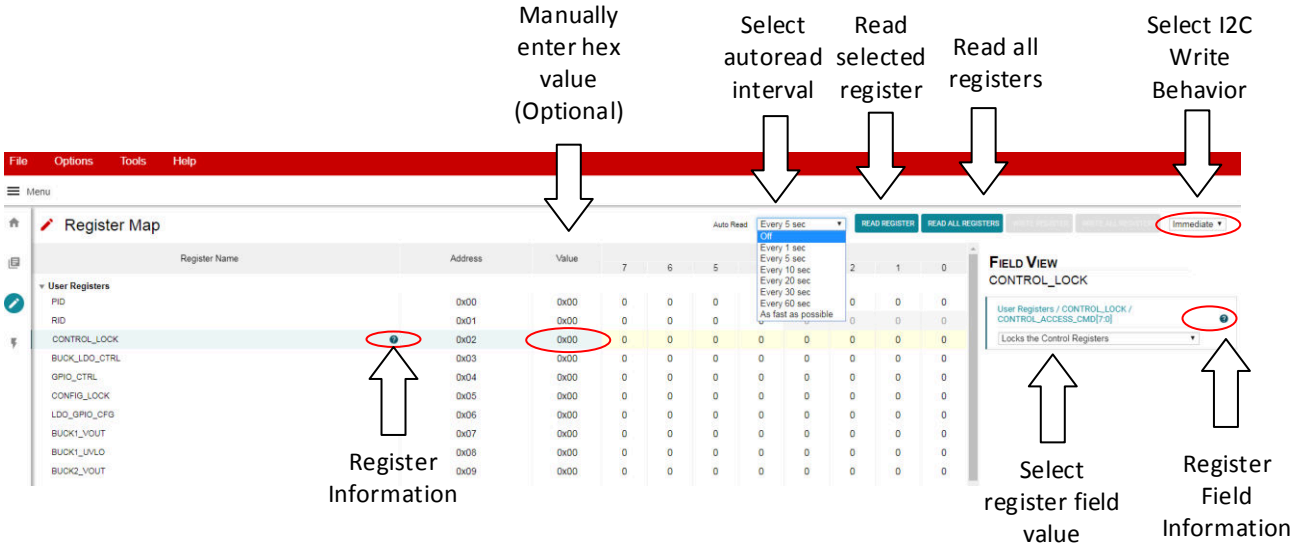


Figure 6-6. Register Page Interfaces

The register table displays each register name, address, last known value from the PMIC, and corresponding bit values. Selecting a title or bit fields in the table will update the Field View column on the right side of the GUI. The Field View displays the individual fields contained within the associated register address. Within the register page, clicking a blue icon containing a question mark (?) will expand additional descriptions if available. The expanded description views can then be closed by clicking the red (x) icon.

This register page can poll the device periodically using the *Auto Read* feature in the top right corner, or allow manual read instructions using the *Read Register* and *Read All Registers* buttons.

A drop-down menu selection at the top right of the register map indicates how the registers are written as the user interacts with the register page. With *Immediate* selected, any update to the register page is automatically sent to the PMIC, whereas *Deferred* will wait for the *Write Register* or *Write All Registers* instructions before communicating with the device. After each write, the register page will automatically read the affected register address to confirm the latest value in the device.

6.2.4 Device Configuration

The Device Configuration section is organized into selectable tabs at the top of the page, where only the contents of the blue tab is actively displayed. Each tab contains categorized visual instruments relating to individual bit fields within the register map. Each instrument is linked to the latest bit values in the register map table, and can be used to alter settings within the PMIC through the dropdown menus or check box features. If the *Auto Read* function in the register map is inactive, the *Read All Registers* button in the top right area of the Device Configuration page can be used to manually refresh the register page, which will then update the instruments with the latest device values.

The PMIC incorporates *Control Lock* and *Configuration Lock* features that can prevent I^2C writes to various registers within the device. The status of these locks will always be displayed in the top right hand corner of the Device Configurations page, and can be toggled by clicking their associated checkbox. When the GUI is properly connected to the EVM and write instructions appear to be ignored by the PMIC, confirm the status of these indicators to verify the device is able to accept new write instructions.

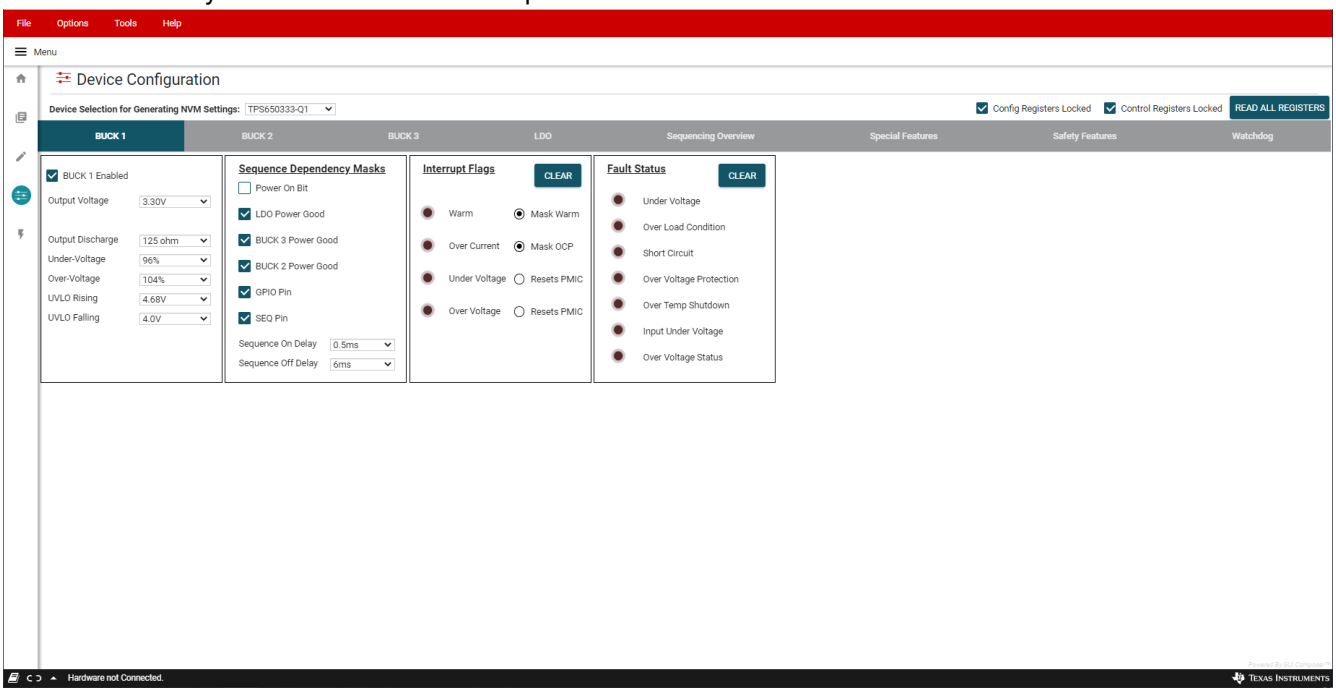


Figure 6-7. TPS6503xx-Q1 GUI Device Configuration Page

6.2.4.1 Using Device Configuration to Define Spin Settings

In some circumstances, TI may provide customized, pre-programmed devices for the camera application. Contact a local TI sales representative for more information.

The Device Configuration tabs in the GUI can be used to define custom settings for TI to pre-program into the device Non-Volatile Memory (NVM). Before beginning the spin definition, see the Camera PMIC Spin Selection Guide to determine if there is an exisiting spin that is already compatible with the target application and the image sensor or both.

Since the visual instruments in the Device Configuration page link directly to the corresponding bits and registers in the Register Map page, the Device Configuration page can be used to quickly define desired OTP register settings.

1. Select the desired camera PMIC from the drop-down menu above the tab indicators to start. The GUI will automatically show, hide, or disable features corresponding to the selected PMIC. This drop down box will not be adjustable if a device is connected to the GUI.

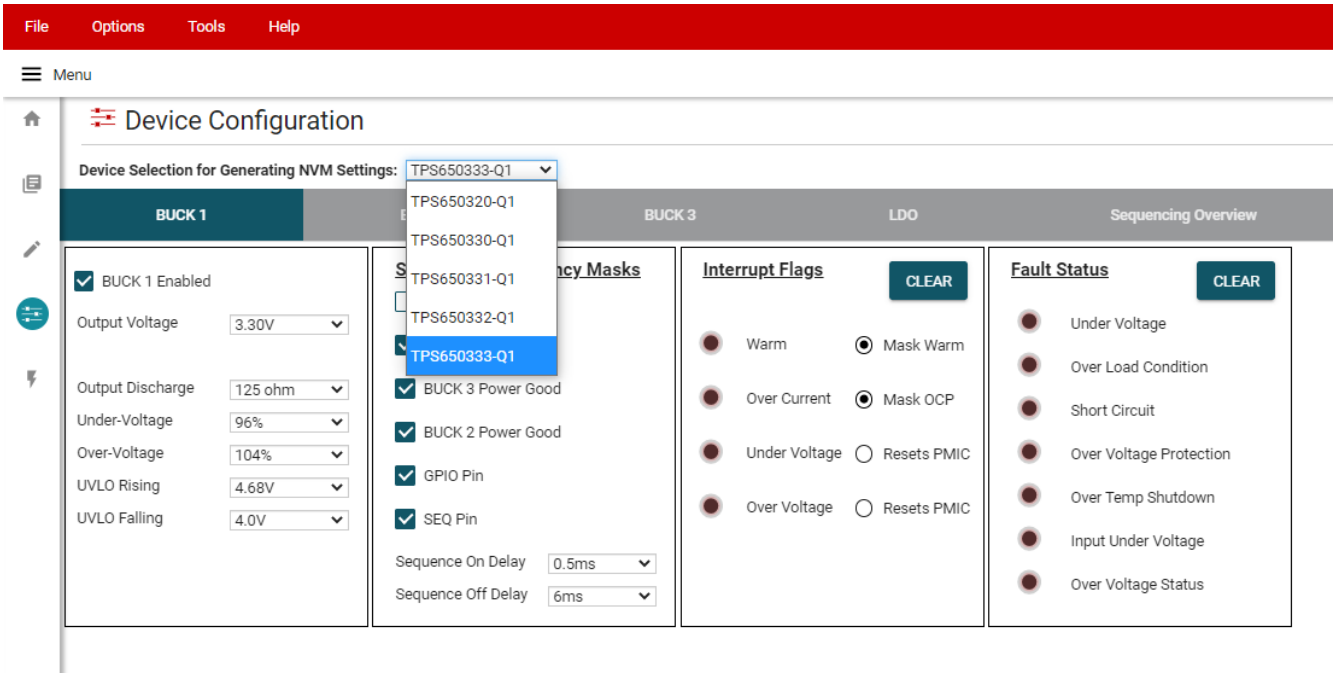


Figure 6-8. Device Selection for Generating NVM Settings

2. Select the desired regulator, sequencing, and additional feature settings in each of the tabs. These changes will be reflected in the Register Map page. For determining the power sequence settings, see Section 6.2.4.2.
3. Click File > Save Settings in the top left corner of the GUI. This exports the register settings in a JSON file that is provided to generate the NVM spin.

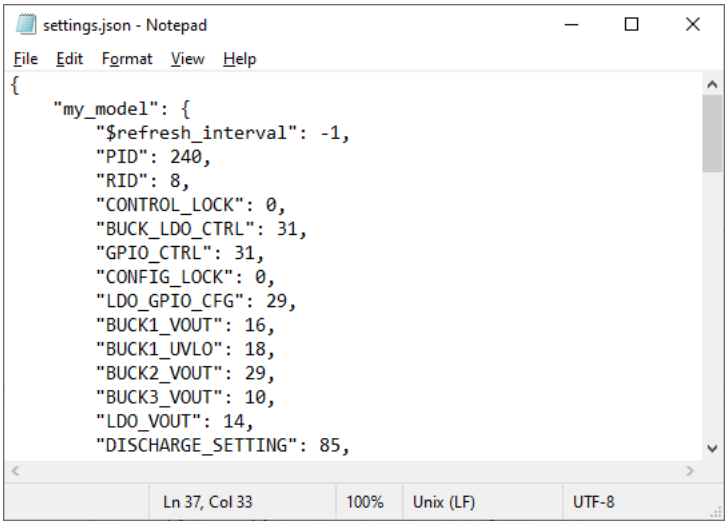


Figure 6-9. Example Settings Output

6.2.4.2 Configuring the Power Sequence

The *Sequencing Overview* tab includes instruments to customize the power sequence of the PMIC. Note that the check boxes are power sequence *masks*. If a particular logic signal needs to be included as part of the regulator or logic power up sequence, leave the box next to the logic signal unchecked. TI recommends to set *Power On Bit* unmasked for each rail that is required in the application.

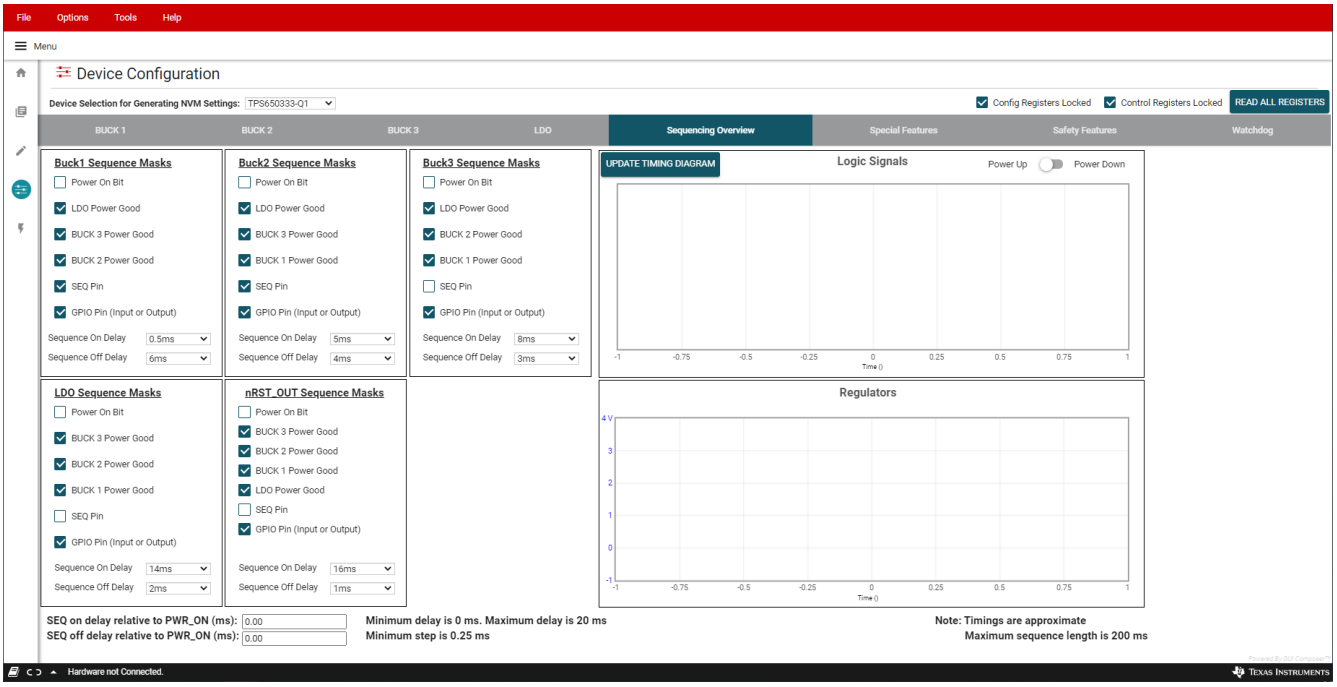


Figure 6-10. Sequencing Overview Tab

When using a TPS65033x-Q1 device, the GPIO pin can also be used for power sequencing of an external regulator or other device. In the *Special Features* tab, configure GPIO as an output to include its sequencing in the *Sequencing Overview* tab. Note that when using GPIO for sequencing, the GPIO Function must be *Enabled*.

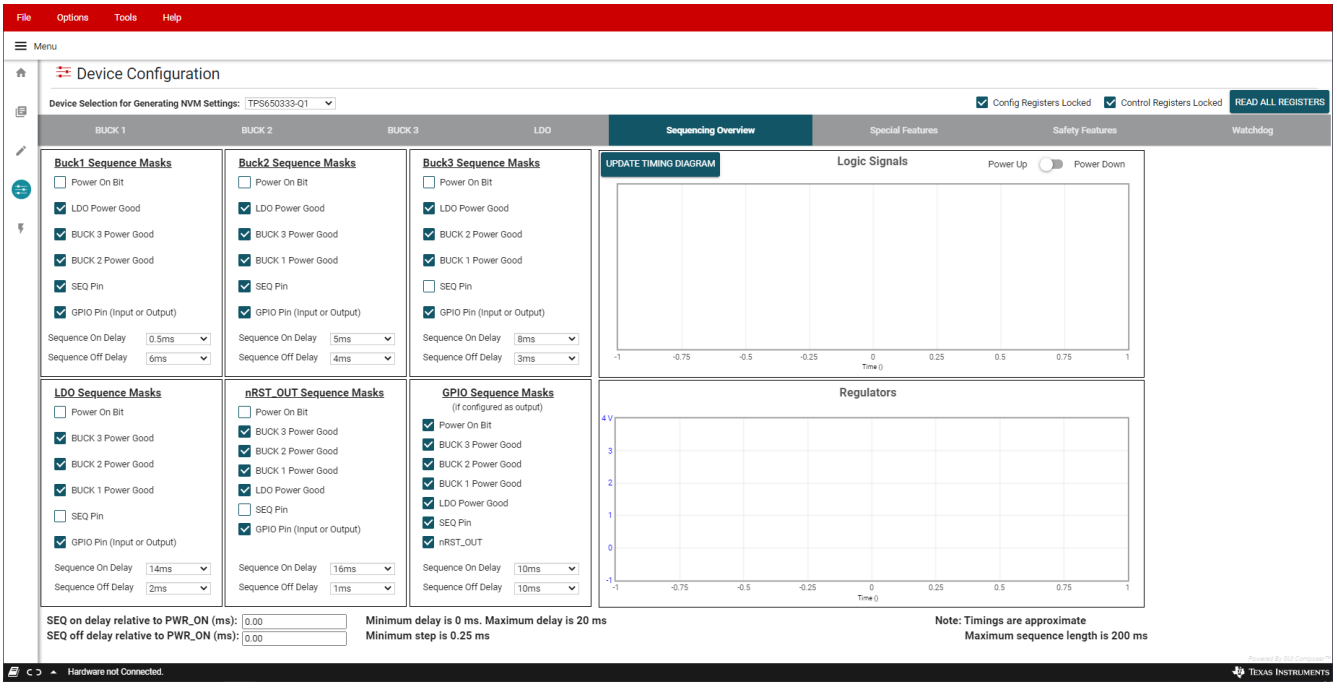


Figure 6-11. Sequencing Overview Including GPIO

For reference, the GUI can generate example power-up and power-down timing diagrams based on the sequence settings present when the *UPDATE TIMING DIAGRAM* button is clicked. As noted, rise and fall times are approximate, and the maximum sequence length is 200 ms. Changes to regulator enable and output discharge settings are reflected in the timing diagram. If the sequence settings are not valid, the GUI will provide a notifying message and the timing diagram will not be updated. For example, if a regulator is enabled but fails to power-up within 200 ms, the sequence settings are not valid.

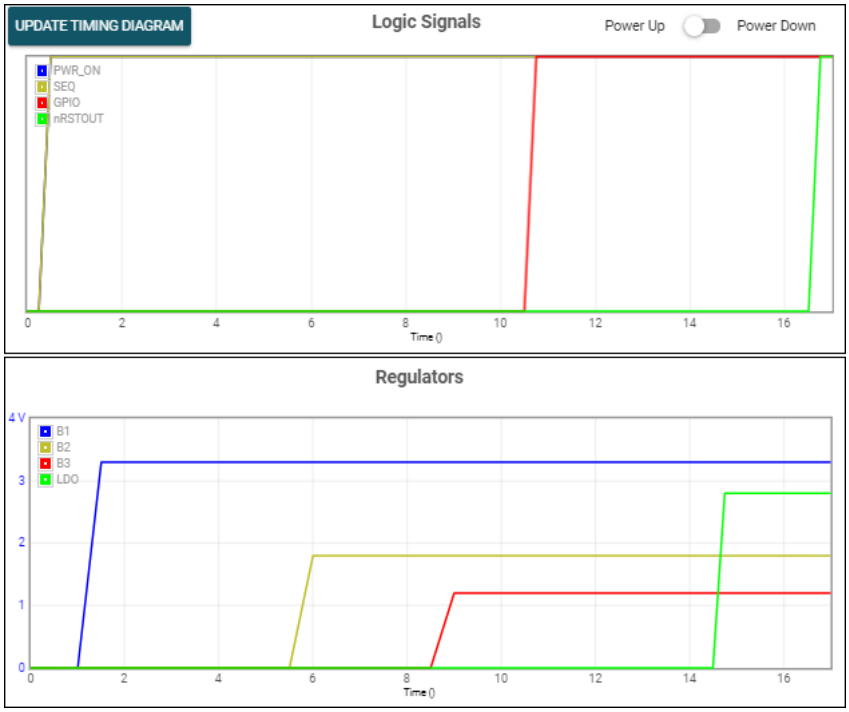


Figure 6-12. GUI Generated Timing Diagram

6.2.5 Re-Program PMIC

The Re-Program PMIC section contains a button for sending the EEPROM Program Command to the device. After the EEPROM Program Command is sent, the device will store the existing register configurations permanently and the PMIC will automatically restart with the latest settings. The device can be re-programmed multiple times to evaluate various configurations.

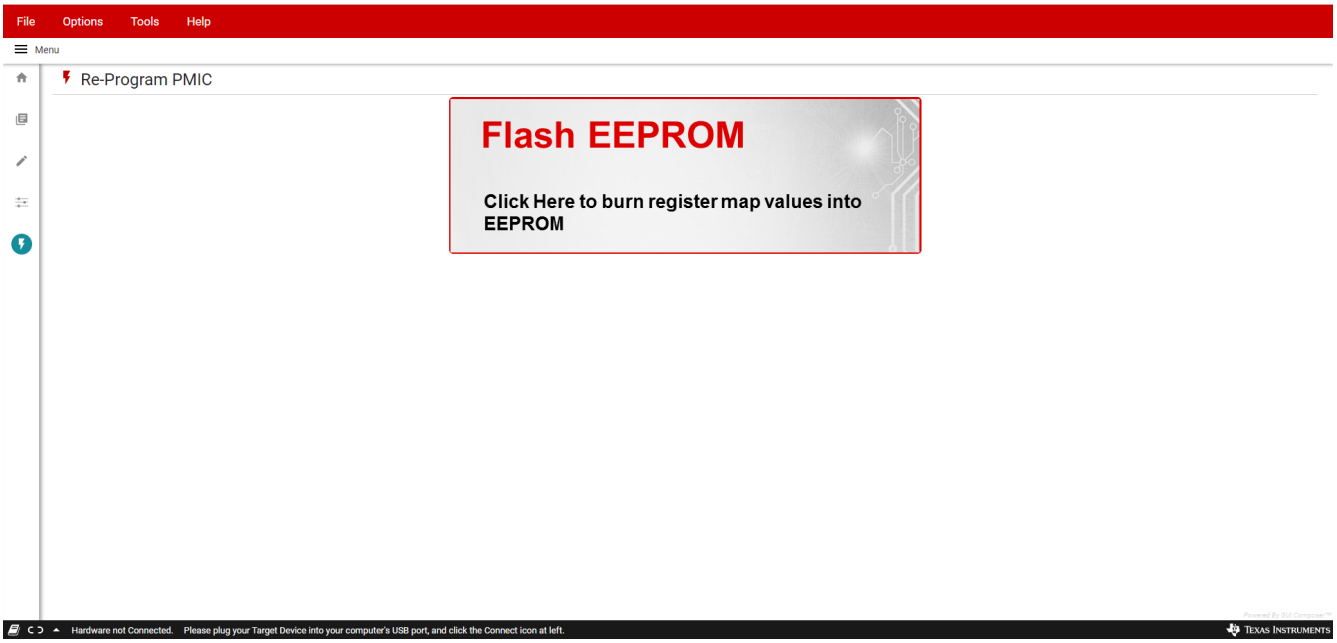


Figure 6-13. TPS6503xx-Q1 GUI Re-Program PMIC Page

6.3 In-Circuit Programming

The TPS650330-Q1 EVM demonstrates the in-circuit programming capabilities of the TPS650330-Q1 PMIC in a typical application. This section provides an example in-circuit programming procedure with application considerations.

1. Verify the desired power and sequence settings using the GUI's Sequencing Overview tools. See Configuring the Power Sequence.
2. Validate the settings with the BOOSTXL-TPS65033. This socketed board provides a quicker way to evaluate device settings.
3. Once settings are verified and validated, configure the TPS650330-Q1 EVM for a typical camera application:
   a. Ensure the I2C pull-up jumpers (J24 and J34) are populated.
   b. Supply the PMIC VIO with either the Buck 1 or Buck 2 output. See Selecting the Logic Supply Voltage.
   c. Tie the PMIC Buck 1 input to VSYS. See Buck 1 Input Supply.
   d. Supply the PMIC Buck 2, Buck 3, and LDO with the Buck 1 output. See Selecting Regulator Input Supplies.
4. Assert SEQ (S1) before applying power.
5. Apply a Buck 1 input voltage (typical is 12 V) to power up the device. By default, the Buck 1 and Buck 2 regulators are enabled, allowing the 3.3 V and 1.8 V rails to power up.
   a. In a typical camera application, this may be sufficient to power up the serializer and enable PMIC programming over the Serializer-Deserializer (SerDes) back-channel.
   b. If additional rails are required, assert GPIO (S4) to enable the Buck 3 and LDO regulators.
6. Unlock the configuration and control registers.
7. Re-program the PMIC settings. If changing a regulator output voltage, TI recommends disabling the regulator first. If doing this in an application setting shuts down a critical component, change the output voltage in small steps to prevent triggering under or over-voltage fault handling.
8. If the device configuration Cyclic Redundancy Check (CRC) is enabled, calculate and write the new configuration CRC by running the GUI's built-in script. For more information on the GUI's capabilities for programming automation, see the BOOSTXL-TPS65033 User's Guide.

Figure 6-14. GUI Configuration CRC Script

9. Burn the final PMIC register settings to EEPROM.
10. Validate the settings on subsequent startups.

7 Typical Performance Plots

7.1 Power Sequence Plots

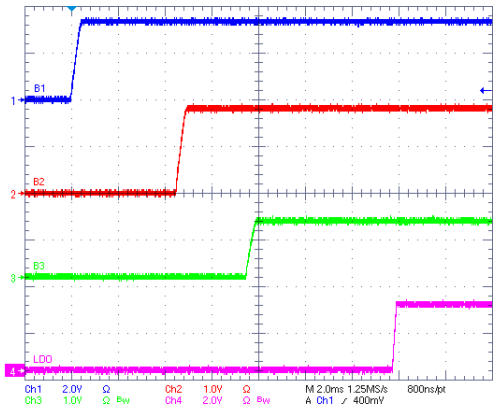


Figure 7-1. TPS650330-Q1 Default Power Up Sequence

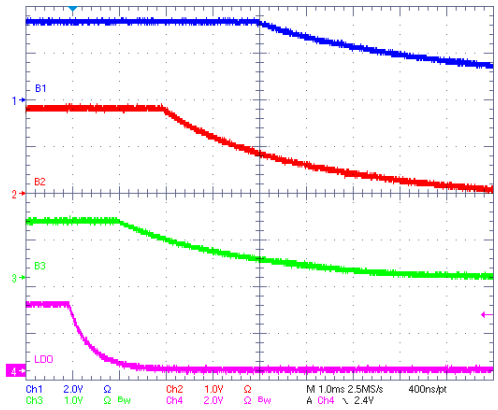
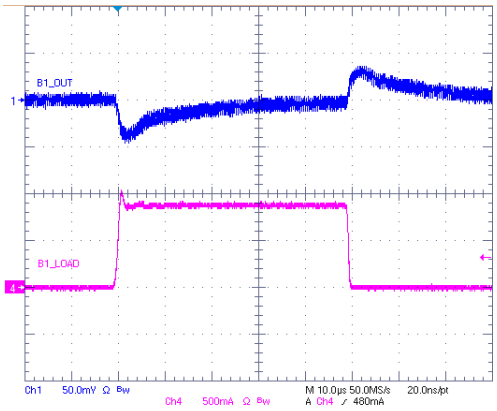


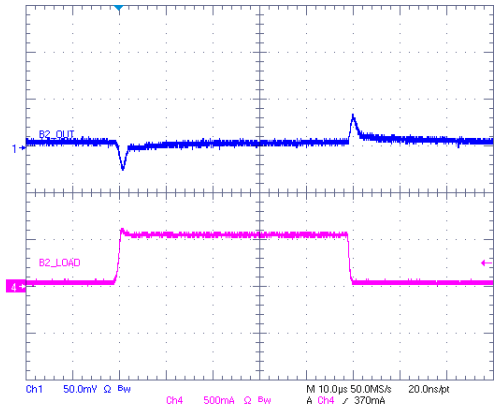
Figure 7-2. TPS650330-Q1 Default Power Down Sequence

7.2 Load Transient Plots



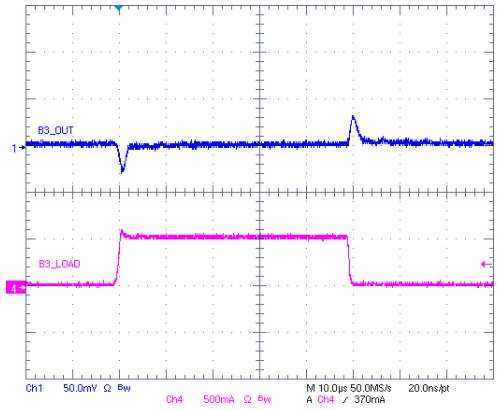
VIN = 12 V VOUT = 3.3 V IOUT = 1 mA to 750 mA in 1 µs

Figure 7-3. Buck 1 Load Transient



VIN = 3.3 V VOUT = 1.8 V IOUT = 1 mA to 300 mA in 1 µs

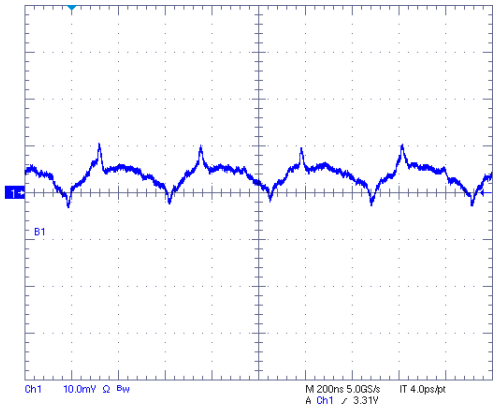
Figure 7-4. Buck 2 Load Transient



VIN = 3.3 V VOUT = 1.2 V IOUT = 1 mA to 300 mA in 1 µs

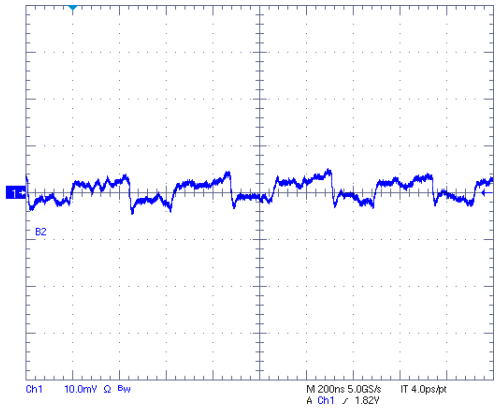
Figure 7-5. Buck 3 Load Transient

7.3 Output Voltage Ripple Plots



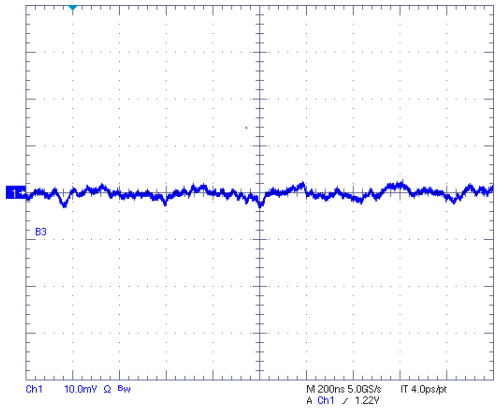
VIN = 12 V VOUT = 3.3 V IOUT = 750 mA

Figure 7-6. Buck 1 Output Voltage Ripple



VIN =3.3 V VOUT = 1.8 V IOUT = 600 mA

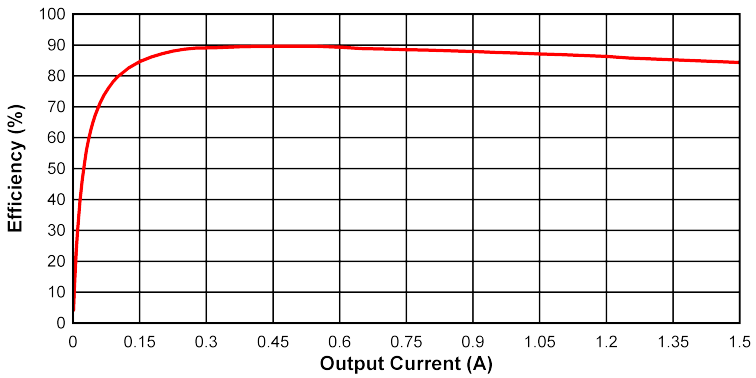
Figure 7-7. Buck 2 Output Voltage Ripple



VIN = 3.3 V VOUT = 1.2 V IOUT = 600 mA

Figure 7-8. Buck 3 Output Voltage Ripple

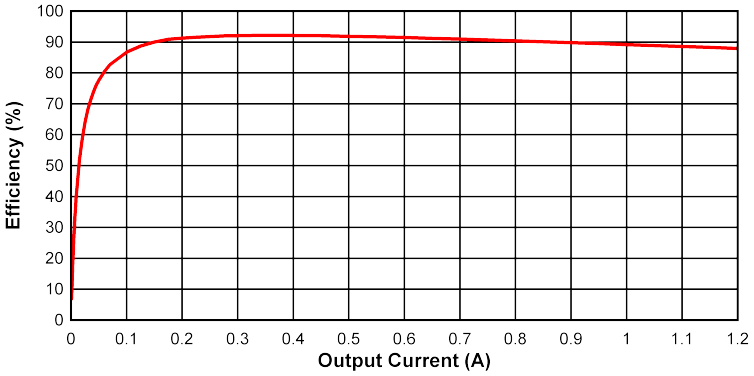
7.4 Efficiency Plots



VIN = 9 V VOUT = 3.3 V Ta = 25°C

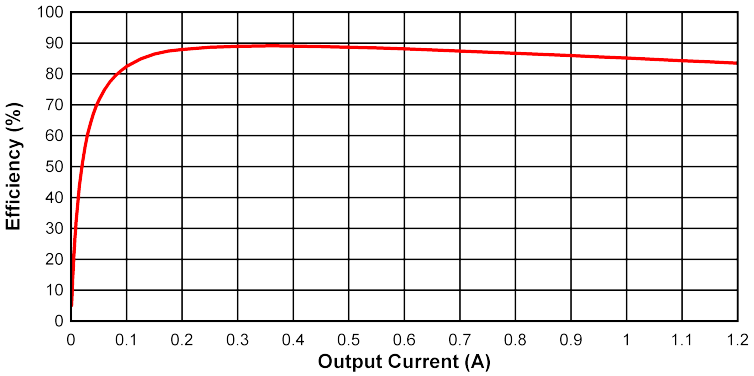
Figure 7-9. Buck 1 Efficiency Curve

7.4 Efficiency Plots



VIN = 3.3 V VOUT = 1.8 V Ta = 25°C

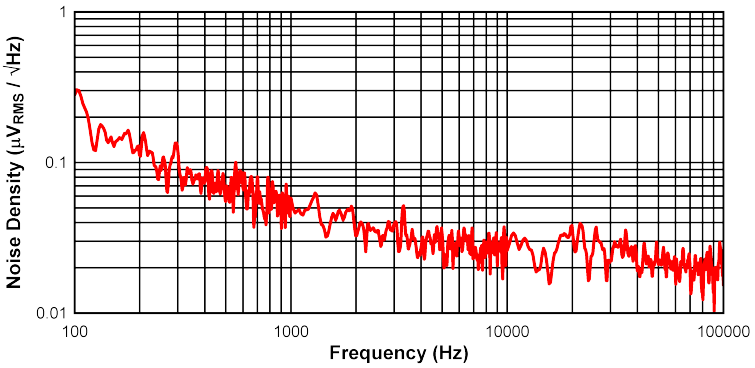
Figure 7-10. Buck 2 Efficiency Curve



VIN = 3.3 V VOUT = 1.2 V Ta = 25°C

Figure 7-11. Buck 3 Efficiency Curve

7.5 LDO Output Noise



VIN = 3.3 V VOUT = 2.8 V IOUT = 300 mA

Figure 7-12. LDO Output Noise Density

8 TPS650330-Q1 EVM Schematic

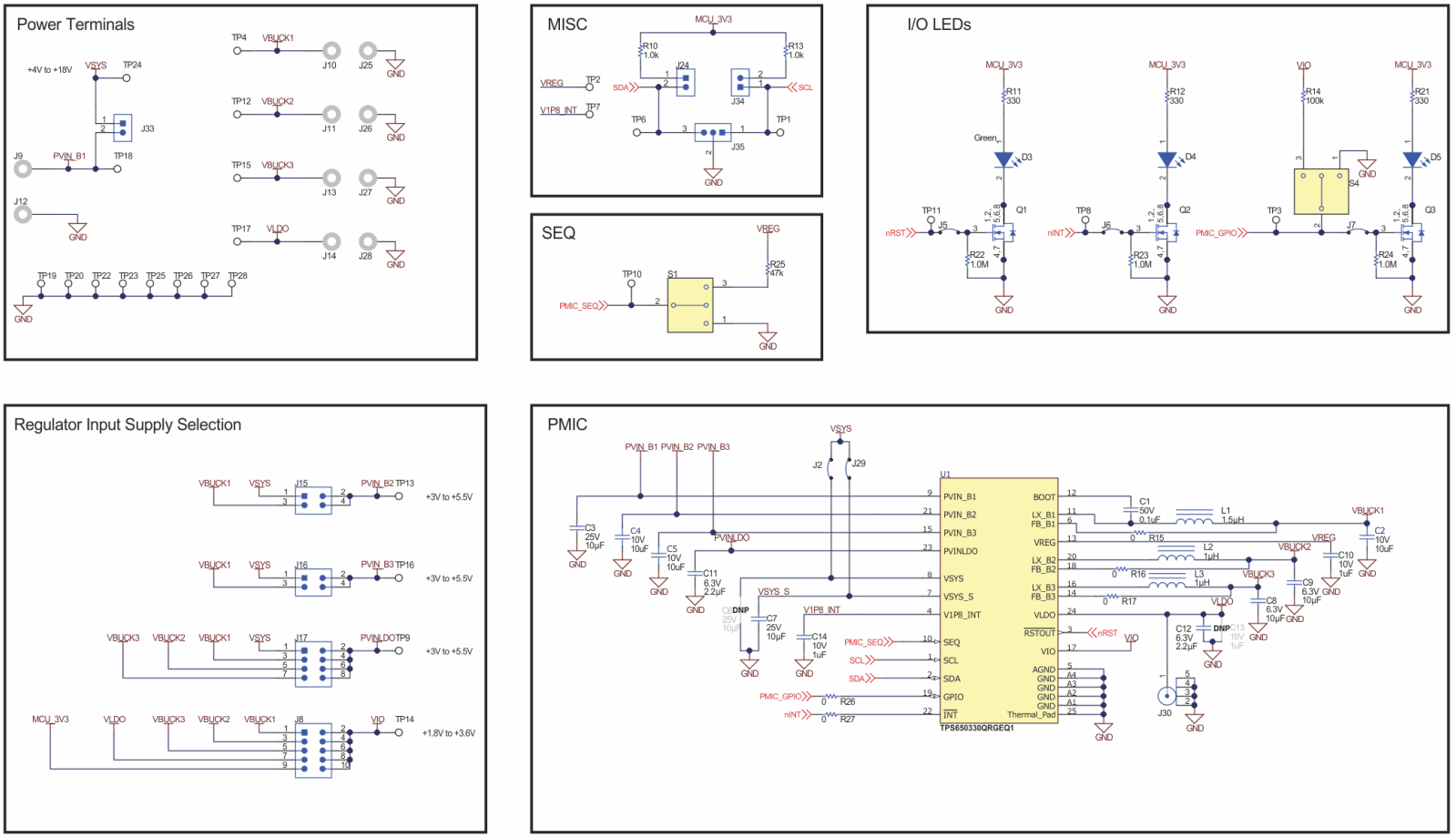


Figure 8-1. TPS650330-Q1 Schematic

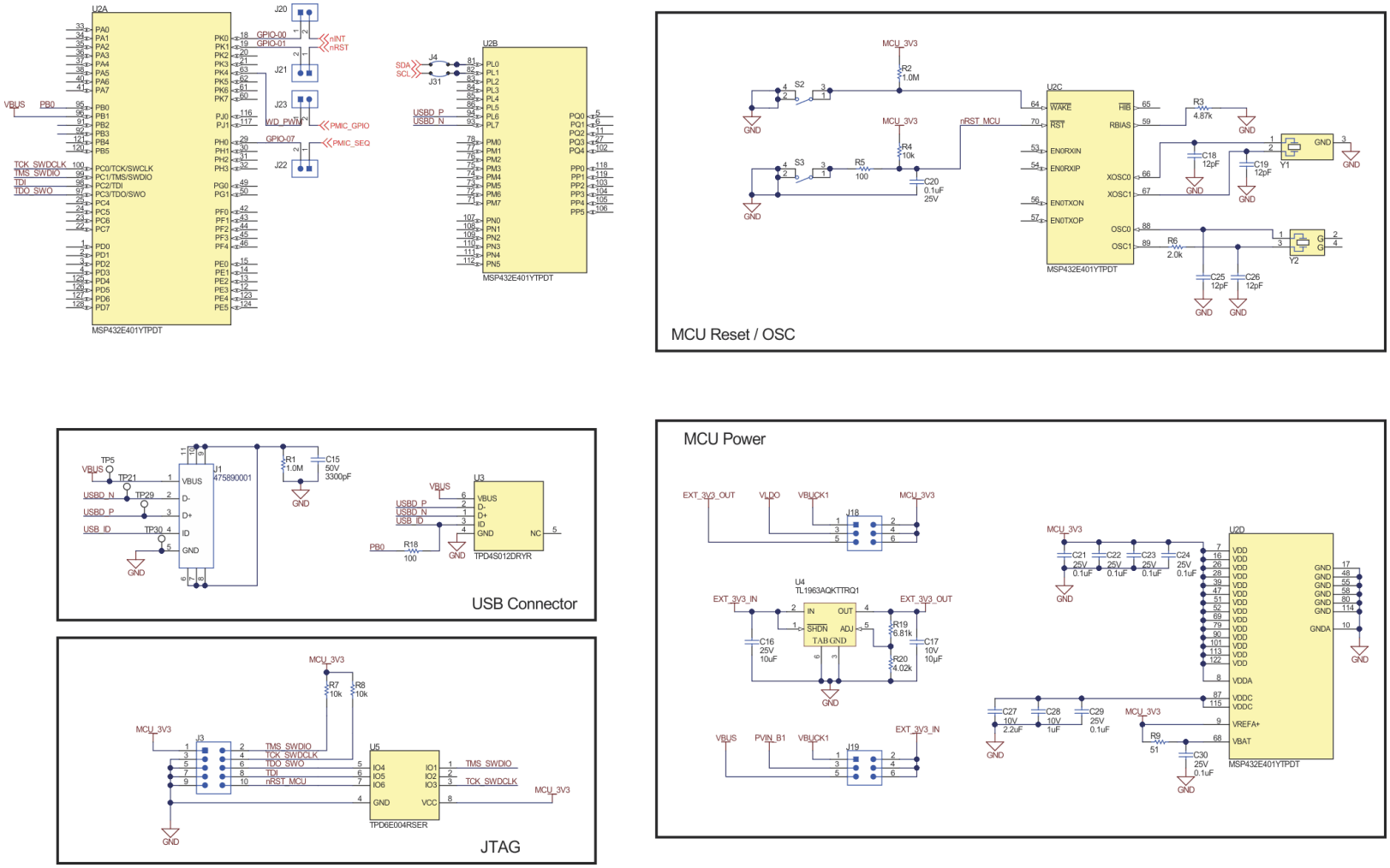


Figure 8-2. MSP432E401Y Schematic

9 TPS650330-Q1 EVM PCB Layers

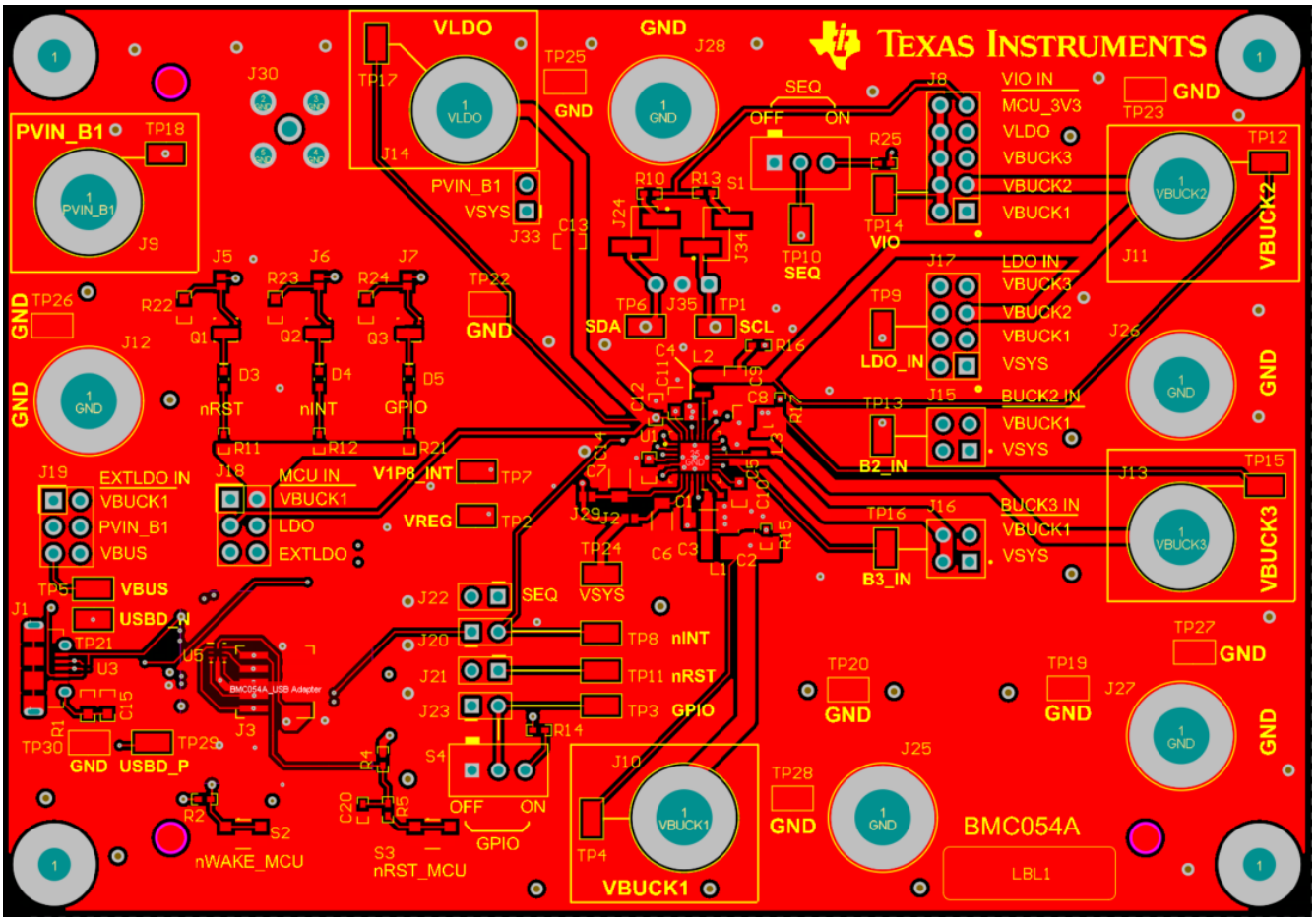


Figure 9-1. Top Layer

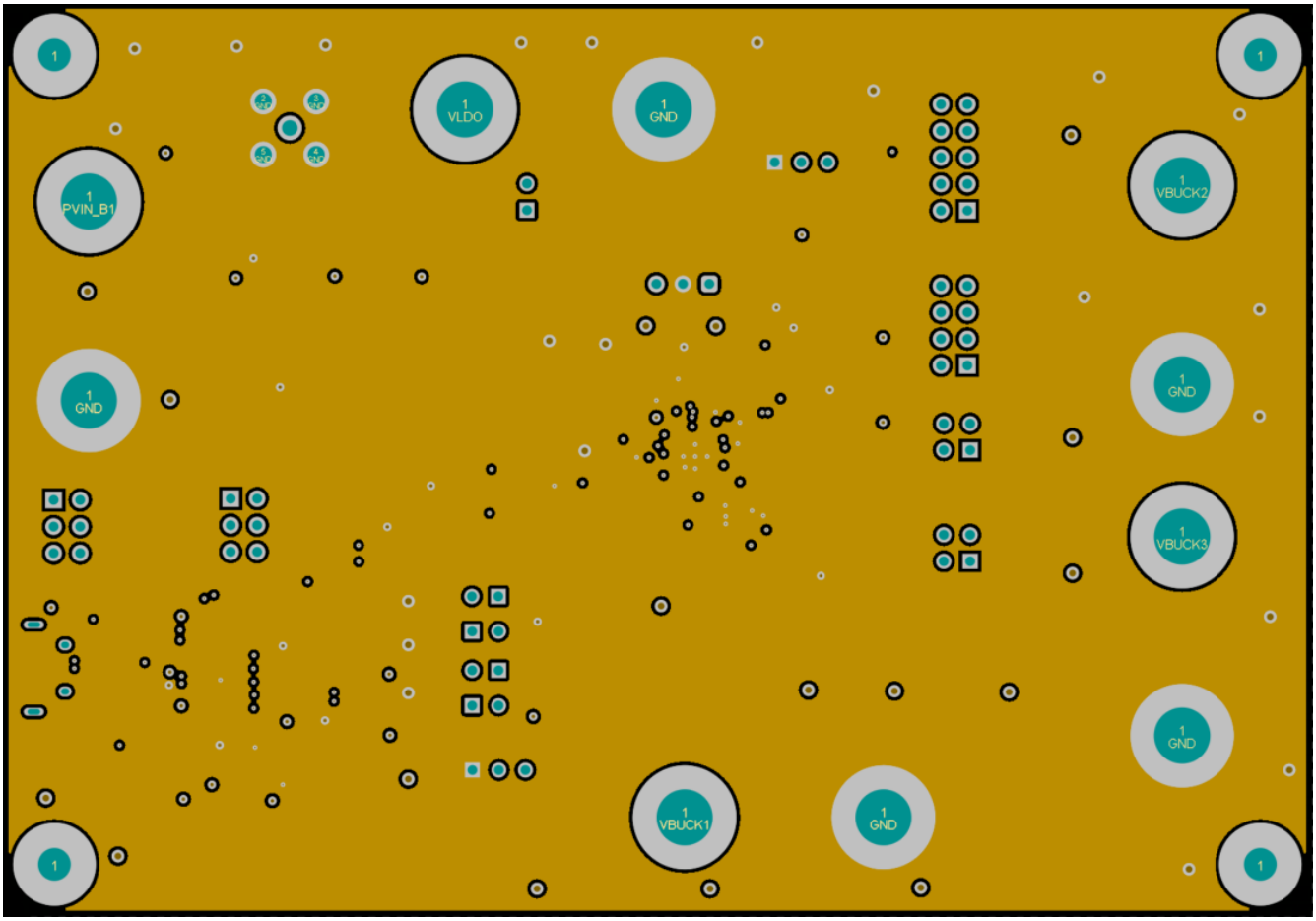


Figure 9-2. Mid-Layer 1

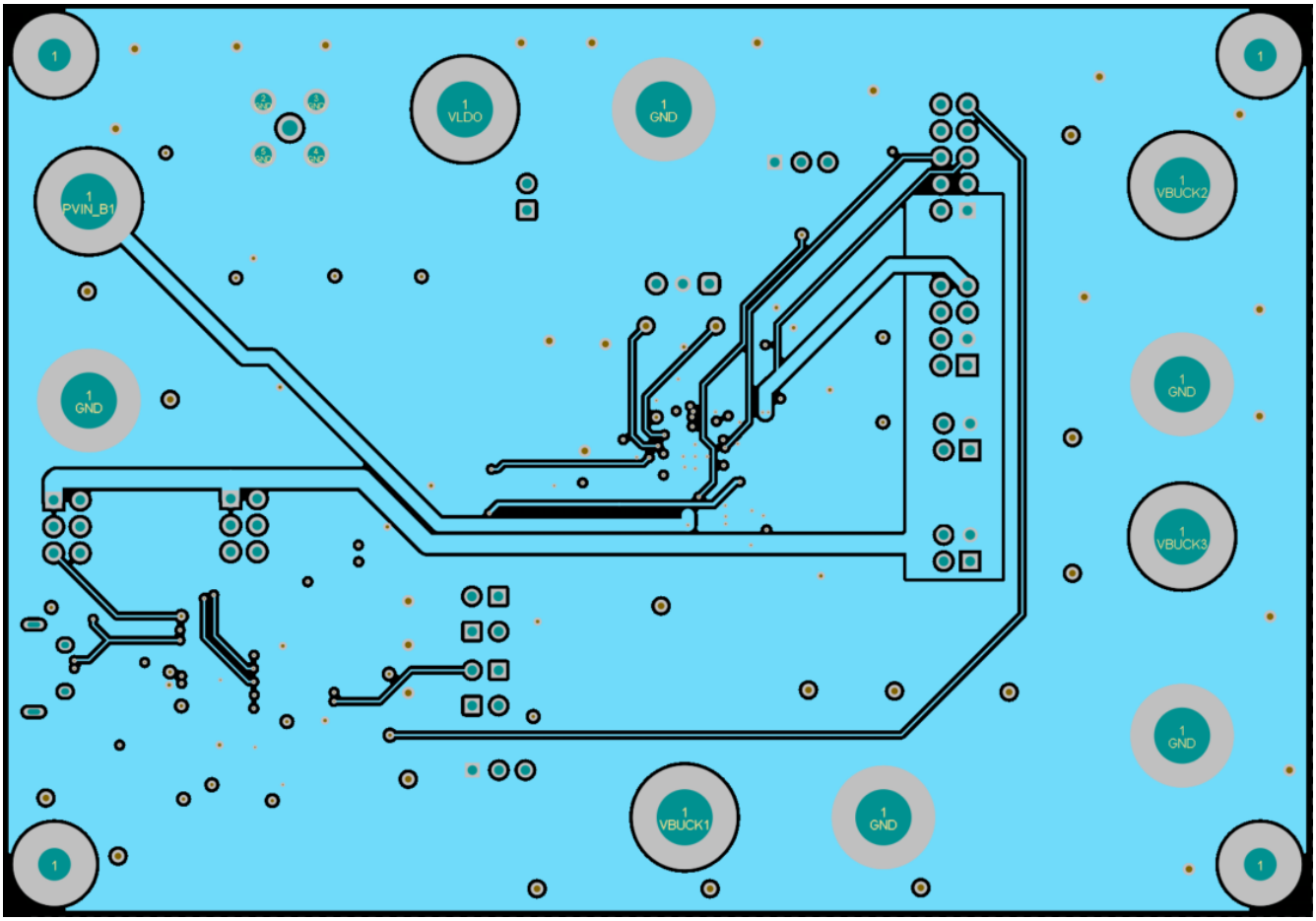


Figure 9-3. Mid-Layer 2

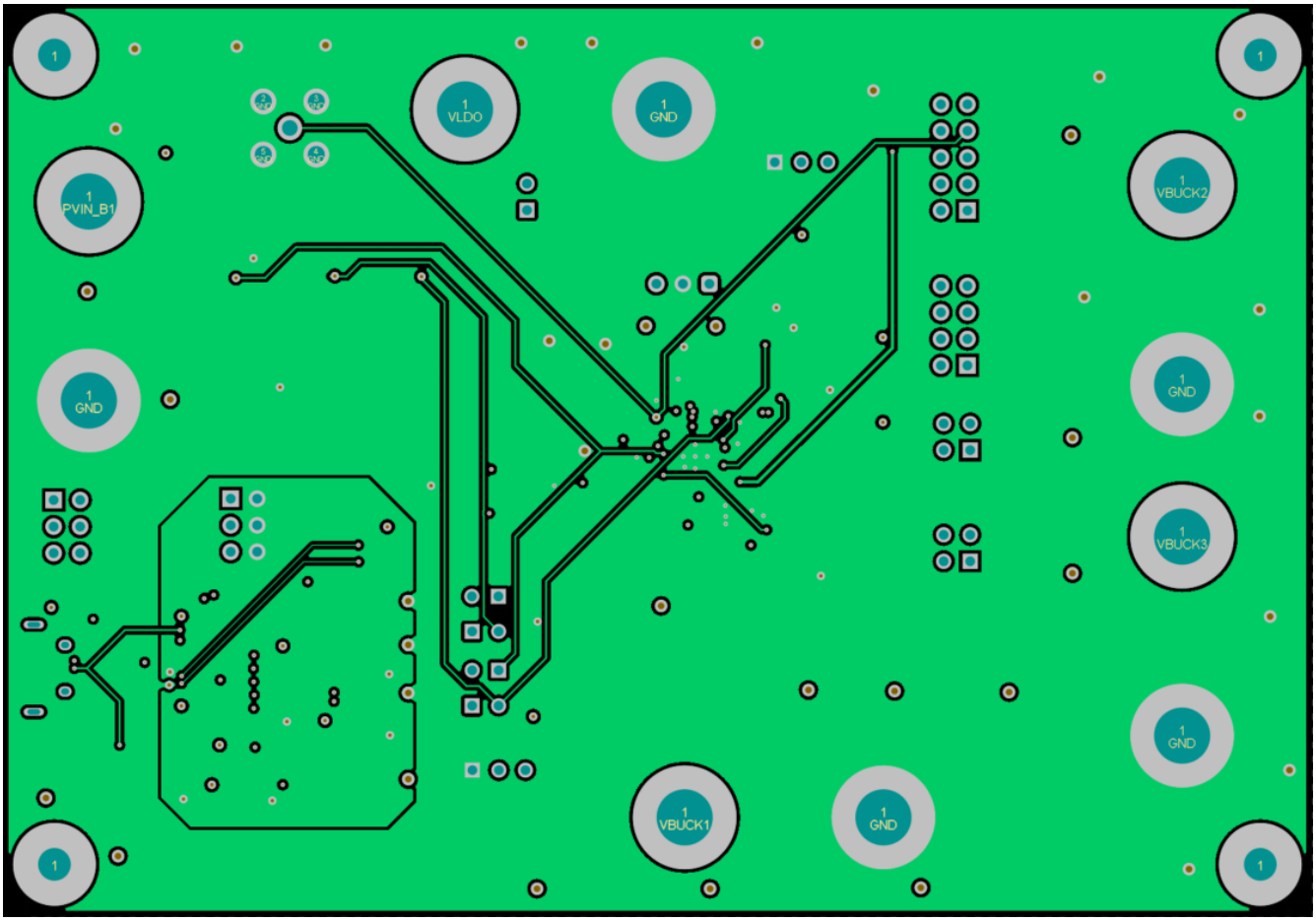


Figure 9-4. Mid-Layer 3

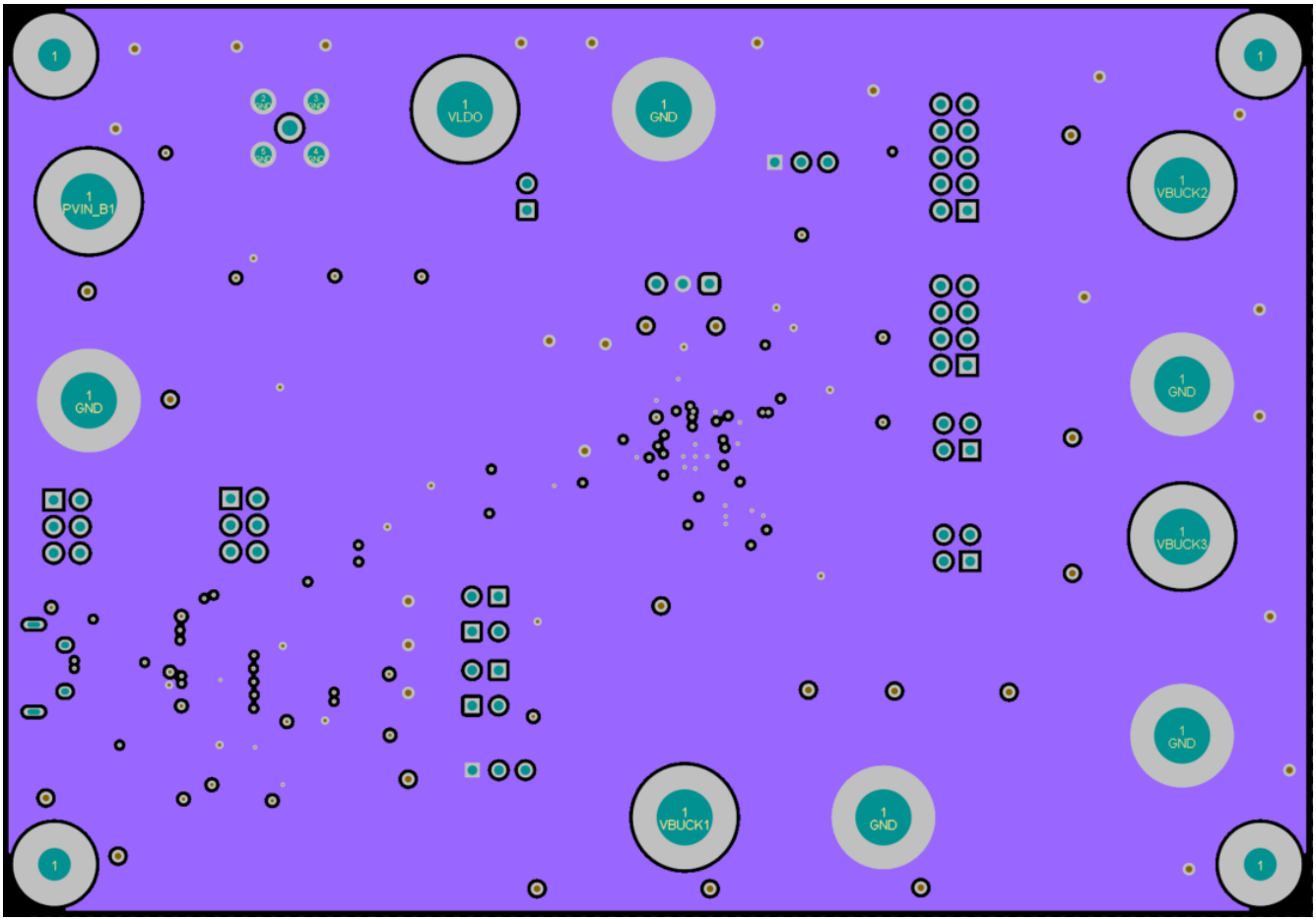


Figure 9-5. Mid-Layer 4

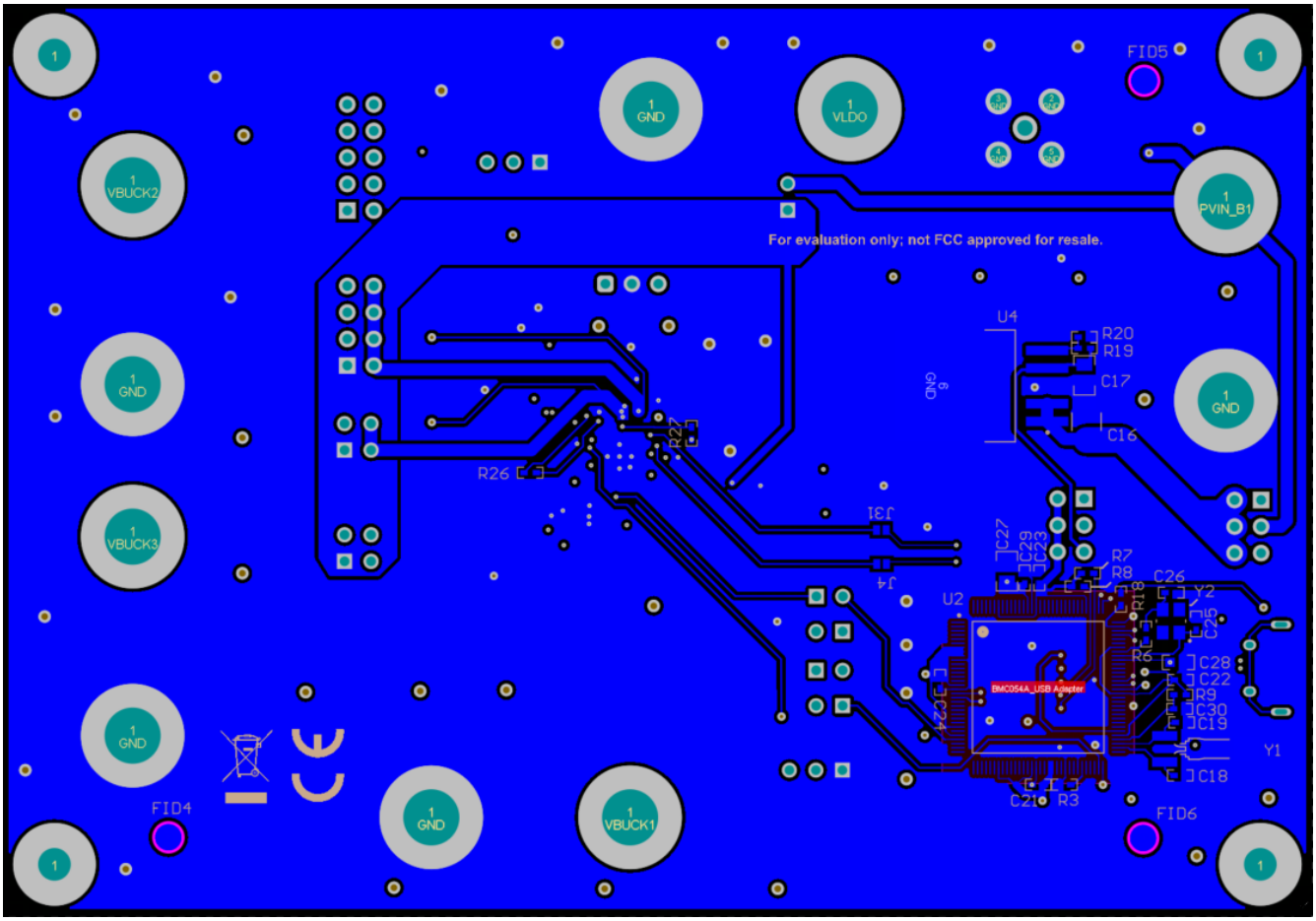


Figure 9-6. Bottom Layer (Mirrored)

10 TPS650330-Q1 EVM Bill of Materials

Table 10-1. TPS650330-Q1 EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		BMC054	Any
C1	1	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ± 20%, X7R, AEC-Q200 Grade 1, 0402	0402	CGA2B3X7R1H104M050BB	TDK
C2, C4, C5	3		10µF ±10% 10V Ceramic Capacitor X7S 0805 (2012 Metric)	0805	CGA4J3X7S1A106K125AE	TDK
C3, C7	2	10 µF	CAP, CERM, 10 µF, 25 V,± 5%, X7R, AEC-Q200 Grade 1, 1206	1206	C1206C106J3RACAUTO	Kemet
C8, C9	2	10µF	CAP, CERM, 10 µF, 6.3 V,± 10%, X7R, AEC-Q200 Grade 1, 0805	0805	JMJ212CB7106KGHT	Taiyo Yuden
C10, C14, C28	3	1 µF	CAP, CERM, 1 µF, 10 V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	0603	LMK107B7105KAHT	Taiyo Yuden
C11, C12	2	2.2 µF	CAP, CERM, 2.2 µF, 6.3 V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	0603	GCM188R70J225KE22D	MuRata
C15	1	3300 pF	CAP, CERM, 3300 pF, 50 V, ± 10%, X7R, 0603	0603	C0603C332K5RACTU	Kemet
C16	1	10 µF	CAP, CERM, 10 µF, 25 V, ± 20%, X7R, AEC-Q200 Grade 1, 1210	1210	CGA6P1X7R1E106M250AC	TDK
C17	1	10 µF	CAP, CERM, 10 µF, 10 V,± 5%, X7R, AEC-Q200 Grade 1, 0805	0805	C0805C106J8RACAUTO	Kemet
C18, C19, C25, C26	4	12 pF	CAP, CERM, 12 pF, 50 V,± 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	0402	GCM1555C1H120JA16J	MuRata
C20, C21, C22, C23, C24, C29, C30	7	0.1 µF	CAP, CERM, 0.1 µF, 25 V, ± 10%, X7R, 0402	0402	GRM155R71E104KE14D	MuRata
C27	1	2.2 µF	CAP, CERM, 2.2 µF, 10 V, ± 10%, X7R, 0805	0805	C0805C225K8RACTU	Kemet
D3, D4, D5	3	Green	LED, Green, SMD	1.7x0.65x0.8 mm	LG L29K-G2J1-24-Z	OSRAM
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5 in L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Connector, Receptacle, Micro-USB Type AB, R/A, Bottom Mount SMT	5.6x2.5x8.2 mm	475890001	Molex
J2, J4, J5, J6, J7, J29, J31	7		Jumper, SMT	shorting jumper, SMT	JMP-36-30X40SMT	Any
J3	1		Header (Shrouded), 1.27 mm, 5x2, Gold, SMT	Header(Shrouded), 1.27 mm, 5x2, SMT	FTSH-105-01-F-DV-K	Samtec
J8	1		Header, 100 mil, 5x2, Tin, TH	Header, 5x2, 100 mil, Tin	PEC05DAAN	Sullins Connector Solutions
J9, J10, J11, J12, J13, J14, J25, J26, J27, J28	10		Standard Banana Jack, Uninsulated, 8.9 mm	Keystone575-8	575-8	Keystone
J15, J16	2		Header, 100 mil, 2x2, Tin, TH	Header, 2x2, 2.54 mm, TH	PEC02DAAN	Sullins Connector Solutions

Table 10-1. TPS650330-Q1 EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
J17	1		Header, 100 mil, 4x2, Tin, TH	Header, 4x2, 100mil, Tin	PEC04DAAN	Sullins Connector Solutions
J18, J19	2		Header, 100 mil, 3x2, Tin, TH	3x2 Header	PEC03DAAN	Sullins Connector Solutions
J20, J21, J22, J23, J33	5		Header, 100 mil, 2x1, Tin, TH	Header, 2 PIN, 100 mil, Tin	PEC02SAAN	Sullins Connector Solutions
J24, J34	2		Header, 100 mil, 2x1, Tin, SMD	SMD, 2-Leads, Body 200x100 mil	TSM-102-01-T-SV-P-TR	Samtec
J30	1		Connector, SMA, TH	SMA	142-0701-201	Cinch Connectivity
J35	1		Header, 100 mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
L1	1	1.5 µH	Inductor, Shielded, Metal Composite, 1.5 µH, 2.3 A, 0.11 Ω, AEC-Q200 Grade 0, SMD	0806	TFM201610ALMA1R5 MTAA	TDK
L2, L3	2	1 µH	Inductor, Shielded, Metal Composite, 1 µH, 3.1 A, 0.06 Ω, AEC-Q200 Grade 0, SMD	0806	TFM201610ALMA1R0 MTAA	TDK
LBL1	1		Thermal Transfer Printable Labels, 0.650 in W x 0.200 in H - 10,000 per roll	PCB Label 0.650 x 0.200 in	THT-14-423-10	Brady
Q1, Q2, Q3	3	25 V	MOSFET, N-CH, 25 V, 5 A, DQK0006C (WSON-6)	DQK0006C	CSD16301Q2	Texas Instruments
R1, R22, R23, R24	4	1.0 Meg	RES, 1.0 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M00JNEA	Vishay-Dale
R2	1	1.0 Meg	RES, 1.0 M, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021M00JNED	Vishay-Dale
R3	1	4.87 k	RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K87FKED	Vishay-Dale
R4, R7, R8	3	10 k	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0JNED	Vishay-Dale
R5, R18	2	100	RES, 100, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402100RJNED	Vishay-Dale
R6	1	2.0 k	RES, 2.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K00JNED	Vishay-Dale
R9	1	51	RES, 51, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040251R0JNED	Vishay-Dale
R10, R13	2	1.0 k	RES, 1.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K00JNED	Vishay-Dale
R11, R12, R21	3	330	RES, 330, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402330RJNED	Vishay-Dale
R14	1	100 k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GEJ104X	Panasonic
R15, R16, R17, R26, R27	5	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R19	1	6.81 k	RES, 6.81 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04026K81FKED	Vishay-Dale
R20	1	4.02 k	RES, 4.02 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K02FKED	Vishay-Dale
R25	1	47 k	RES, 47 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040247K0JNED	Vishay-Dale
S1, S4	2		Switch, Slide, SPDT, On-Off-On, 3 Pos, 0.05 A, 48 V, TH	9.5x5 mm	AS1E-2M-10-Z	Copal Electronics

Table 10-1. TPS650330-Q1 EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
S2, S3	2		Switch, SPST, Off-Mom, 0.05 A, 12 VDC, SMD	3.5x2.9 mm	434153017835	Wurth Elektronik
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9	9	1x2	Shunt, 100 mil, Flash Gold, Black	Closed Top 100 mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30	30		Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone
U1	1		Highly integrated power management IC for automotive camera modules	VQFN24	TPS650330QRGEQ1	Texas Instruments
U2	1		MSP432E401YTPDT, PDT0128A (TQFP-128)	PDT0128A	MSP432E401YTPDT	Texas Instruments
U3	1		USB ESD Solution with Power Clamp, 4 Channels, -40 to +85 °C, 6-pin SON (DRY), Green (RoHS & no Sb/Br)	DRY0006A	TPD4S012DRYR	Texas Instruments
U4	1		Single Output Fast Transient Response LDO, 1.5 A, Adjustable 1.21 to 20 V Output, 2.1 to 20 V Input, 5-pin DDPAK (KTT), -40 to 125 °C, Green (RoHS & no Sb/Br)	KTT0005A	TL1963AQKTTRQ1	Texas Instruments
U5	1		Low-Capacitance 6-Channel ±15 kV ESD Protection Array for High-Speed Data Interfaces, RSE0008A (UQFN-8)	RSE0008A	TPD6E004RSER	Texas Instruments
Y1	1		Crystal, 32.768 kHz, SMD	D1.9xL6 mm	CMR200T-32.768KDZY-UT	Citizen FineDevice
Y2	1		Crystal, 25 MHz, 8pF, SMD	3.2x0.75x2.5 mm	NX3225GA-25.000M-STD-CRG-2	NDK
C6	0	10 µF	CAP, CERM, 10 µF, 25 V, ± 5%, X7R, AEC-Q200 Grade 1, 1206	1206	C1206C106J3RACAUTO	Kemet
C13	0	1 µF	CAP, CERM, 1 µF, 10 V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	0603	LMK107B7105KAHT	Taiyo Yuden

11 TPS650330-Q1 Silicon Revision Changes

The final silicon revision for the TPS65033x-Q1 family of PMICs is denoted *B0*. This corresponds to die revision PG 2.0. Table 11-1 lists the feature changes compared to the first revision of silicon, *A0* or PG 1.0.

Table 11-1. TPS65033x-Q1 Silicon Revision B0 Feature Changes

Item	Design Block	Parameter Impacted	Silicon Revision A0	Silicon Revision B0	Details
1	BUCK1	Output Voltage Settings	3.0 V to 4.0 V	2.5 V to 4.0 V	Maintains 50 mV increments
2	LDO	Output Voltage Settings	2.7 V to 3.3 V	1.8 V, 2.5 V to 3.3 V	1.8 V and 1.825 V settings 2.5 V to 3.2 V settings in 25 mV increments 3.3 V setting
3	BUCK1	PVIN_B1_UVLO	Rising threshold only	Rising and Falling thresholds	Same threshold settings as Rising thesholds with a 4% hysteresis delta betweein rising and falling
4	Digital	Warm Threshold	Exceeding Warm Threshold will keep State Machine from transitioning to the Active state	Option to allow the State Machine to transition to the Active State if the Warm Threshold is exceeded	User programmable in pre-production devices.Factory programmable in production devices.
5	Digital	LDO Pre-Bias Condition	Not applicable	Option to allow the LDO to power on into a pre-bias condition	User programmable in pre-production devices.Factory programmable in production devices.
6	Digital	I2C Bus	Always enabled	Option to disable	Factory programmable only
7	Digital	Configuration CRC	Can be disabled by the user during the configuration process	Can be disabled by the user during the configuration process and programmed to remain disabled	User programmable in pre-production devices.Factory programmable in production devices.
8	Digital	State Transition Control	Not applicable	Option to define the state transition for Priority 2 Faults (either the Reset State or Wait Power Cycle State)	User programmable in pre-production devices.Factory programmable in production devices.Does not apply to the TPS650331-Q1 device.
9	Digital	ABIST Run Time Control	ABIST only runs on power up	ABIST runs on power up or whenever commanded to run	Option is factory programmable only
10	Digital	SEQ Pin Latch	Not applicable	Option to latch the state of the SEQ pin in order to perform a complete power up or power down sequence	Option is factory programmable only
11	Digital	Power Good Status Register	Not applicable	Register bits added to provide the power good status of BUCK1, BUCK2, BUCK3, and the LDO. Status bits also added for nRSTOUT, GPIO, and SEQ pins	Read only register

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2020) to Revision A (October 2020) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Deleted the Hot Surface Warning....3
- Changed the EVM images to EVM Revision A....3
- Removed the J23 Jumper and GPIO PMIC Pin from the *Adapter PMIC Connections* table....3
- Changed the EVM defaults for all regulators....4
- Updated the current limiting feature specifications in the *Low Noise LDO Features* table....5
- Updated the output discharge configurable range in the *Low Noise LDO Configurable Settings* table....5
- Changed the EVM Configurations....6
- Updated the *TPS650330-Q1 EVM Test Points* table....7
- Updated the *Graphical User Interface* section....8
- Updated the *I^2C Communication Port and Adapter Debugging* section....10
- Added the *TPS650330-Q1 EVM Schematic* section....21
- Added the *TPS650330-Q1 EVM PCB Layers* section....23
- Added the *TPS650330-Q1 EVM Bill of Materials* section....29
- Added the *TPS650330-Q1 Silicon Revision Changes* section....32

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