User's Guide

Programmable PMICs: TPS6593-Q1 Default Configuration for TPS6593EVM

ABSTRACT

This User's Guide can be used as a guide for using the TPS6593-Q1 power management integrated circuits (PMICs) into a custom system. This document provides the default non-volatile memory (NVM) settings, state transitions, and power sequencing for the PMIC. Steps for programming this device can be found in Programmable PMICs: Design Guide for Programming in Evaluation and Production.

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Trademarks

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1 Introduction

This guide describes the default NVM settings of the TPS6593-Q1 programmable device. These default settings are intended to support a wide variety of systems, with various interface options and power requirements. This user's guide does not provide information about the electrical characteristics, external components, package, or the functionality of the PMIC. For such information and the full register maps, refer to the datasheet for each device. The data sheet specification will be the definitive source in the event of any inconsistency between the official specification and any user's guide, application report, or other referenced material.

2 Device Versions

The unique NVM settings for each PMIC are distinguishable by the orderable part number for the device. The NVM settings can also be distinguished using the TI_NVM_ID, and TI_NVM_REV values listed in Table 2-1

Table 2-1. TPS6593-Q1 NVM Settings and Orderable Part Numbers

PDN USE CASE	Orderable Part Number	Device Mode	TI_NVM_ID	TI_NVM_REV	Default I2C Address
• Supports I2C or SPI interface • Supports EEPROM programming of desired default settings and sequencing • Power resources are disabled at power up to allow for user to program the device on application board • 1+1+1+1 phase configuration(1) • Default settings of the TPS6593EVM	PTPS65930400RWERQ1	Master(2)	0x00	0x4	0x28

(1) Can be programmed to a different phase configuration.
(2) Can be reprogrammed to slave-mode for multi-PMIC systems.

These NVM settings are also supported in the Scalable PMICs GUI, under the template name *Generic_TPS6593*. For more details on viewing NVM templates in the GUI, see the Scalable PMIC's GUI User's Guide.

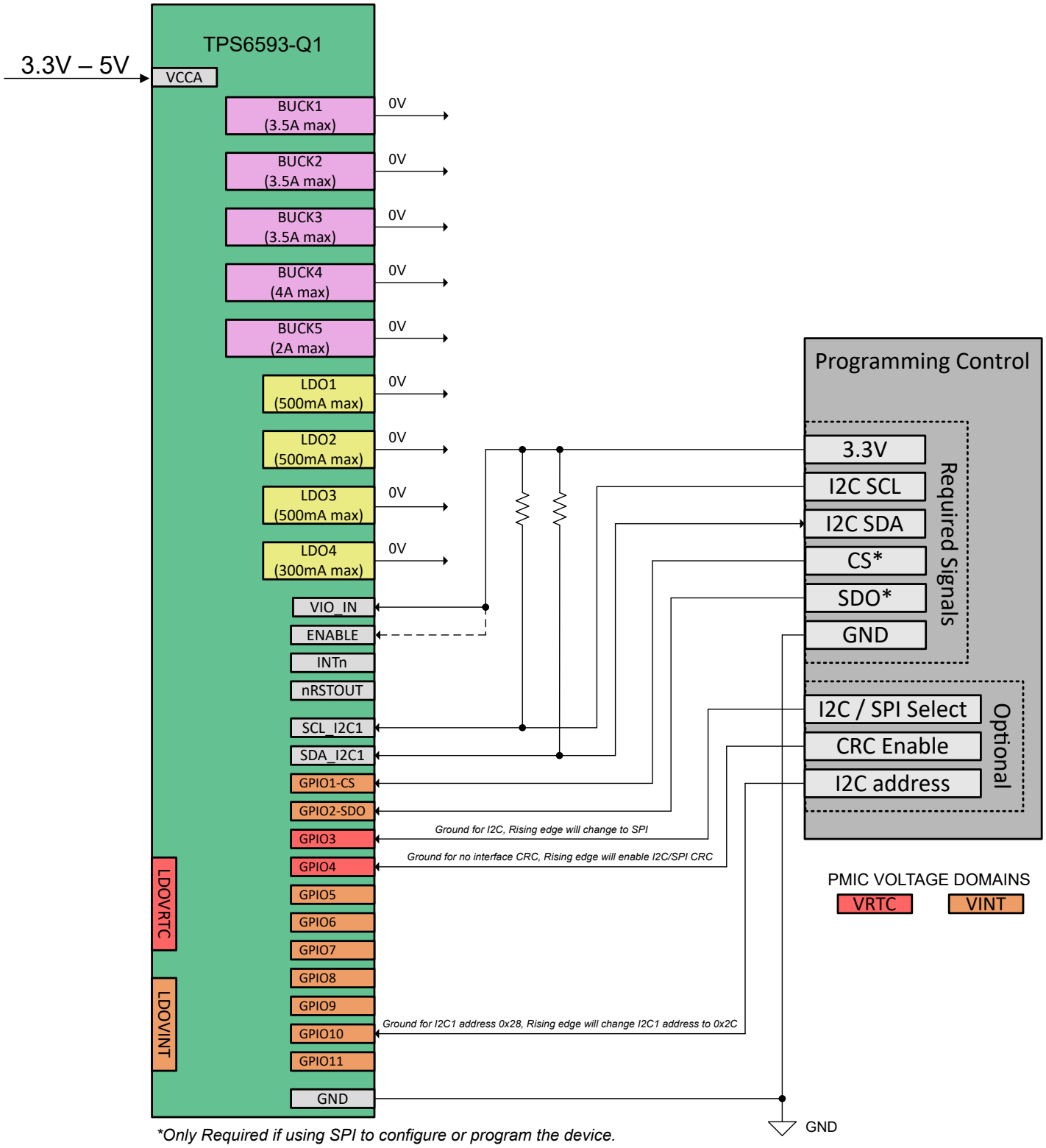
3 Default Configuration

This section details how the TPS6593-Q1 power resources and GPIO signals are configured by default.

Figure 3-1 shows that the PMIC can take 3.3 V through 5 V as its input supply range. Additionally, all BUCKs and LDOs are disabled, with 0 V output by default.

The default phase configuration for this device separates all BUCKs. This phase configuration can be reprogrammed to support multi-phase options if needed. If the system requires updates to the phase configuration, it is recommended that the hardware matches the intended phase configuration for the system, not the default single phase configuration, when programming the device with the custom NVM settings.

The GPIOs are all inputs by default, except GPIO1 and GPIO2. GPIO1 and GPIO2 are configured as CS and SDO pins in the event that a SPI interface is used. All evaluation capabilities and programming capabilities can be equally accessed by using I2C or SPI. GPIO3, GPIO4, and GPIO10 are used to update the interface of the PMIC to match the interface being used to program the PMIC. By default, the PMIC utilizes I2C, with no CRC, and a default I2C1 address of 0x28. If no updates need to be made to these settings, GPIO3, GPIO4, and GPIO10 signals are not required during programming.



*Only Required if using SPI to configure or program the device.

Figure 3-1. Default Configration of TPS6593-Q1

The programming control shown in Figure 3-1 provides all the power and controls that may be needed. The actual number of connections needed will vary by usage. If there is an MCU on the board that is not powered by the PMIC, the programming controls would also depict what signals need to be active when the MCU is updating the PMIC.

To enable SPI interface, by pull GPIO3 high after powering VCCA and VIO_IN.

GPIO4 is available to enable CRC on the I2C or SPI interface. This aids in the scenario when the host MCU or software is expecting a CRC value to be included with register reads and writes.

For multi-PMIC solutions, GPIO10 can be used to change the I2C1 address from 0x28 to 0x2C. If all the I2C lines of multi-PMIC solutions are tied together, it is required that the device being programmed has unique I2C addresses. For this functionality, GPIO10 can be pulled high to update the I2C1 address before a PMIC is programmed. Then, the next PMIC in the system can utilize GPIO10 to update its I2C address to the unique address of 0x2C for programming, and so on until all PMICs are programmed with custom settings and unique I2C addresses. PMICs not in the process of being programmed would keep GPIO10 low, to ensure that they are not being addressed on the 0x2C address.

The ENABLE pin is only required to be pulled high if the default interface settings need to be updated. If no interface settings are required, keep this pin low. It is expected that after the device is programmed with initial custom settings, ENABLE would always remain low during programming to ensure all outputs of the PMIC are disabled.

Lastly, VIO_IN of the PMICs must be supplied to support I2C or SPI communication during programming. If VIO is normally enabled or supplied by an output of the PMIC (either a regulator or GPIO), it is recommended to externally supply VIO while making NVM updates. All regulators and GPIOs, excluding SPI communication on GPIO1 and GPIO2, are automatically disabled during NVM programming.

4 Static NVM Settings

The TPS6593-Q1 device consists of fixed registers and configurable registers that are loaded from NVM. For all NVM registers, the initial NVM settings that load into the registers are provided in this section. Note: these initial NVM settings, unless stated otherwise, can be changed once the PMICs have transitioned into ACTIVE state. The full register map, including default values of fixed registers, is located in the TPS6593-Q1 datasheet.

4.1 Application-Based Configuration Settings

In the TPS6593-Q1 data sheet, there are multiple application-based configurations for each BUCK to operate within. Table 4-1 includes the different configurations available:

Table 4-1. TPS6593-Q1 Use Cases

TPS6593-Q1
2.2 MHz Single Phase for DDR Termination
4.4 MHz Multiphase Configuration
4.4 MHz Single Phase Low Output Voltage
4.4 MHz Single Phase High Output Voltage
2.2 MHz Multiphase with Full Range VIN
2.2 MHz Single Phase with 5.0 V VIN
2.2 MHz Single Phase with Full Range VIN

The seven configurations also have optimal output inductance values that optimize the performance of each buck under these various conditions. Table 4-2 shows the default configurations for the BUCKs. These settings cannot be changed after device startup. These settings can be changed through reprogramming of the NVM.

Table 4-2. Application Use Case Settings

Device	BUCK Rail	Default Application Use Case	Recommended Inductor Value
TPS6593-Q1	BUCK1	2.2 MHz Single Phase with Full Range VIN	470 nH
	BUCK2	2.2 MHz Single Phase with Full Range VIN	470 nH
	BUCK3	2.2 MHz Single Phase with Full Range VIN	470 nH
	BUCK4	2.2 MHz Single Phase with Full Range VIN	470 nH
	BUCK5	2.2 MHz Single Phase with Full Range VIN	470 nH

4.2 Device Identification Settings

These settings are used to distinguish which device is detected in a system. These settings cannot be changed after device startup. Only the phase configuration and CUSTOMER_NVM_ID can be reprogrammed.

Table 4-3. Device Identification NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
DEV_REV	TI_DEVICE_ID	0x2	0x2
NVM_CODE_1	TI_NVM_ID	0x0	0x0
NVM_CODE_2	TI_NVM_REV	0x4	0x4
CUSTOMER_NVM_ID_REG	CUSTOMER_NVM_ID	0x0	0x0
PHASE_CONFIG	MP_CONFIG	0x1	1+1+1+1+1

4.3 BUCK Settings

These settings detail the default voltages, configurations, and monitoring of the BUCK rails. All these settings, except switching frequency, can be changed though I^2C after startup.

Table 4-4. BUCK NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
BUCK1_CTRL	BUCK1_EN(1)	0x0	Disabled; BUCK1 regulator
	BUCK1_FPWM	0x1	PWM operation only.
	BUCK1_FPWM_MP	0x0	Automatic phase adding and shedding.
	BUCK1_VMON_EN	0x0	Disabled; OV, UV, SC, and ILIM comparators.
	BUCK1_VSEL	0x0	BUCK1_VOUT_1
	BUCK1_PLDN	0x1	Enabled; Pull-down resistor
	BUCK1_RV_SEL	0x0	Disabled
BUCK1_CONF	BUCK1_SLEW_RATE	0x3	5.0 mV/µs
	BUCK1_ILIM	0x4	4.5 A
BUCK2_CTRL	BUCK2_EN(1)	0x0	Disabled; BUCK2 regulator
	BUCK2_FPWM	0x1	PWM operation only.
	BUCK2_VMON_EN	0x0	Disabled; OV, UV, SC, and ILIM comparators.
	BUCK2_VSEL	0x0	BUCK2_VOUT_1
	BUCK2_PLDN	0x1	Enabled; Pull-down resistor
	BUCK2_RV_SEL	0x0	Disabled
BUCK2_CONF	BUCK2_SLEW_RATE	0x3	5.0 mV/µs
	BUCK2_ILIM	0x4	4.5 A

Table 4-4. BUCK NVM Settings (continued)

Register Name	Field Name	TPS6593-Q1	
		Value	Description
BUCK3_CTRL	BUCK3_EN(1)	0x0	Disabled; BUCK3 regulator
	BUCK3_FPWM	0x1	PWM operation only.
	BUCK3_FPWM_MP	0x0	Automatic phase adding and shedding.
	BUCK3_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK3_VSEL	0x0	BUCK3_VOUT_1
	BUCK3_PLDN	0x1	Enabled; Pull-down resistor
	BUCK3_RV_SEL	0x0	Disabled
BUCK3_CONF	BUCK3_SLEW_RATE	0x3	5.0 mV/µs
	BUCK3_ILIM	0x4	4.5 A
BUCK4_CTRL	BUCK4_EN(1)	0x0	Disabled; BUCK4 regulator
	BUCK4_FPWM	0x1	PWM operation only.
	BUCK4_VMON_EN	0x0	Disabled; OV, UV, SC, and ILIM comparators.
	BUCK4_VSEL	0x0	BUCK4_VOUT_1
	BUCK4_PLDN	0x1	Enabled; Pull-down resistor
	BUCK4_RV_SEL	0x0	Disabled
BUCK4_CONF	BUCK4_SLEW_RATE	0x3	5.0 mV/µs
	BUCK4_ILIM	0x4	4.5 A
BUCK5_CTRL	BUCK5_EN(1)	0x0	Disabled; BUCK5 regulator
	BUCK5_FPWM	0x1	PWM operation only.
	BUCK5_VMON_EN	0x0	Disabled; OV, UV, SC, and ILIM comparators.
	BUCK5_VSEL	0x0	BUCK5_VOUT_1
	BUCK5_PLDN	0x1	Enable Pull-down resistor
	BUCK5_RV_SEL	0x0	Disabled
BUCK5_CONF	BUCK5_SLEW_RATE	0x3	5.0 mV/µs
	BUCK5_ILIM	0x2	2.5 A
BUCK1_VOUT_1	BUCK1_VSET1	0x0	0.3 V
BUCK1_VOUT_2	BUCK1_VSET2	0x0	0.3 V
BUCK2_VOUT_1	BUCK2_VSET1	0x0	0.3 V
BUCK2_VOUT_2	BUCK2_VSET2	0x0	0.3 V
BUCK3_VOUT_1	BUCK3_VSET1	0x0	0.3 V
BUCK3_VOUT_2	BUCK3_VSET2	0x0	0.3 V
BUCK4_VOUT_1	BUCK4_VSET1	0x0	0.3 V
BUCK4_VOUT_2	BUCK4_VSET2	0x0	0.3 V
BUCK5_VOUT_1	BUCK5_VSET1	0x0	0.3 V
BUCK5_VOUT_2	BUCK5_VSET2	0x0	0.3 V
BUCK1_PG_WINDOW	BUCK1_OV_THR	0x7	+10% / +100 mV
	BUCK1_UV_THR	0x7	-10% / -100 mV
BUCK2_PG_WINDOW	BUCK2_OV_THR	0x7	+10% / +100mV
	BUCK2_UV_THR	0x7	-10% / -100mV
BUCK3_PG_WINDOW	BUCK3_OV_THR	0x7	+10% / +100mV
	BUCK3_UV_THR	0x7	-10% / -100mV
BUCK4_PG_WINDOW	BUCK4_OV_THR	0x7	+10% / +100mV
	BUCK4_UV_THR	0x7	-10% / -100 mV
BUCK5_PG_WINDOW	BUCK5_OV_THR	0x7	+10% / +100 mV
	BUCK5_UV_THR	0x7	-10% / -100 mV

Table 4-4. BUCK NVM Settings (continued)

Register Name	Field Name	TPS6593-Q1	
		Value	Description
BUCK_RESET_REG	BUCK1_RESET	0x0	0x0
	BUCK2_RESET	0x0	0x0
	BUCK3_RESET	0x0	0x0
	BUCK4_RESET	0x0	0x0
	BUCK5_RESET	0x0	0x0
FREQ_SEL	BUCK1_FREQ_SEL	0x0	2.2 MHz
	BUCK2_FREQ_SEL	0x0	2.2 MHz
	BUCK3_FREQ_SEL	0x0	2.2 MHz
	BUCK4_FREQ_SEL	0x0	2.2 MHz
	BUCK5_FREQ_SEL	0x0	2.2 MHz

(1) This NVM default value can change when the device transitions to ACTIVE mode.

4.4 LDO Settings

These settings detail the default voltages, configurations, and monitoring of the LDO rails. All these settings can be changed though I^2C after startup.

Table 4-5. LDO NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
LDO1_CTRL	LDO1_EN(1)	0x0	Disabled; LDO1 regulator.
	LDO1_SLOW_RAMP	0x0	25 mV/µs max ramp up slew rate for LDO output from 0.3 V to 90% of LDOn_VSET
	LDO1_VMON_EN	0x0	Disable OV and UV comparators.
	LDO1_PLDN	0x2	250 Ω
	LDO1_RV_SEL	0x0	Disabled
LDO2_CTRL	LDO2_EN(1)	0x0	Disabled; LDO2 regulator.
	LDO2_SLOW_RAMP	0x0	25 mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
	LDO2_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO2_PLDN	0x2	250 Ω
	LDO2_RV_SEL	0x0	Disabled
LDO3_CTRL	LDO3_EN(1)	0x0	Disabled; LDO3 regulator.
	LDO3_SLOW_RAMP	0x0	25 mV/us max ramp up slew rate for LDO output from 0.3 V to 90% of LDOn_VSET
	LDO3_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO3_PLDN	0x2	250 Ω
	LDO3_RV_SEL	0x0	Disabled
LDO4_CTRL	LDO4_EN(1)	0x0	Disabled; LDO4 regulator.
	LDO4_SLOW_RAMP	0x0	25 mV/us max ramp up slew rate for LDO output from 0.3 V to 90% of LDOn_VSET
	LDO4_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO4_PLDN	0x2	250 Ohm
	LDO4_RV_SEL	0x0	Disabled
LDO1_VOUT	LDO1_VSET	0x4	0.60 V
	LDO1_BYPASS	0x0	Linear regulator mode.
LDO2_VOUT	LDO2_VSET	0x4	0.60 V
	LDO2_BYPASS	0x0	Linear regulator mode.

Table 4-5. LDO NVM Settings (continued)

Register Name	Field Name	TPS6593-Q1	
		Value	Description
LDO3_VOUT	LDO3_VSET	0x4	0.60 V
	LDO3_BYPASS	0x0	Linear regulator mode.
LDO4_VOUT	LDO4_VSET	0x20	1.200 V
LDO1_PG_WINDOW	LDO1_OV_THR	0x7	+10% / +100 mV
	LDO1_UV_THR	0x7	-10% / -100 mV
LDO2_PG_WINDOW	LDO2_OV_THR	0x7	+10% / +100 mV
	LDO2_UV_THR	0x7	-10% / -100 mV
LDO3_PG_WINDOW	LDO3_OV_THR	0x7	+10% / +100 mV
	LDO3_UV_THR	0x7	-10% / -100 mV
LDO4_PG_WINDOW	LDO4_OV_THR	0x7	+10% / +100 mV
	LDO4_UV_THR	0x7	-10% / -100 mV
LDO_RV_TIMEOUT_REG_1	LDO1_RV_TIMEOUT	0xf	16ms
	LDO2_RV_TIMEOUT	0xf	16 ms
LDO_RV_TIMEOUT_REG_2	LDO3_RV_TIMEOUT	0xf	16 ms
	LDO4_RV_TIMEOUT	0xf	16 ms

(1) Note that this NVM default value can change when the device transitions to ACTIVE mode.

4.5 VCCA and VMON Settings

These settings detail the default monitoring enabled on VCCA. All these settings can be changed though I^2C after startup.

Table 4-6. VCCA and VMON NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
GENERAL_REG_0	FAST_VCCA_OVP	0x0	slow, 4us deglitch filter enabled
VCCA_VMON_CTRL	VMON_DEGLITCH_SEL	0x0	4 us
	VCCA_VMON_EN	0x0	Disabled; OV and UV comparators.
VCCA_PG_WINDOW	VCCA_OV_THR	0x7	+10%
	VCCA_UV_THR	0x7	-10%
	VCCA_PG_SET	0x0	3.3 V

4.6 GPIO Settings

These settings detail the default configurations of the GPIO rails. All these settings can be changed though I^2C after startup. Note: the contents of the GPIOx_SEL field determine which other fields in the GPIOx_CONF and GPIO_OUT_x registers are applicable. To understand which NVM fields apply to each GPIOx_SEL option, see the *Digital Signal Descriptions* section in TPS6593-Q1 datasheet.

Table 4-7. GPIO NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
GPIO1_CONF	GPIO1_OD	0x0	Push-pull output
	GPIO1_DIR	0x0	Input
	GPIO1_SEL	0x1	SCL_I2C2/CS_SPI
	GPIO1_PU_SEL	0x0	Pull-down resistor selected
	GPIO1_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO1_DEGLITCH_EN	0x0	No deglitch, only synchronization.

Table 4-7. GPIO NVM Settings (continued)

Register Name	Field Name	TPS6593-Q1	
		Value	Description
GPIO2_CONF	GPIO2_OD	0x0	Push-pull output
	GPIO2_DIR	0x0	Input
	GPIO2_SEL	0x2	SDA_I2C2/SDO_SPI
	GPIO2_PU_SEL	0x0	Pull-down resistor selected
	GPIO2_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO2_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO3_CONF	GPIO3_OD	0x0	Push-pull output
	GPIO3_DIR	0x0	Input
	GPIO3_SEL	0x0	GPIO3
	GPIO3_PU_SEL	0x0	Pull-down resistor selected
	GPIO3_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO3_DEGLITCH_EN	0x1	8 us deglitch time.
GPIO4_CONF	GPIO4_OD	0x0	Push-pull output
	GPIO4_DIR	0x0	Input
	GPIO4_SEL	0x0	GPIO4
	GPIO4_PU_SEL	0x0	Pull-down resistor selected
	GPIO4_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO4_DEGLITCH_EN	0x1	8 µs deglitch time.
GPIO5_CONF	GPIO5_OD	0x0	Push-pull output
	GPIO5_DIR	0x0	Input
	GPIO5_SEL	0x0	GPIO5
	GPIO5_PU_SEL	0x0	Pull-down resistor selected
	GPIO5_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO5_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO6_CONF	GPIO6_OD	0x0	Push-pull output
	GPIO6_DIR	0x0	Input
	GPIO6_SEL	0x0	GPIO6
	GPIO6_PU_SEL	0x0	Pull-down resistor selected
	GPIO6_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO6_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO7_CONF	GPIO7_OD	0x0	Push-pull output
	GPIO7_DIR	0x0	Input
	GPIO7_SEL	0x0	GPIO7
	GPIO7_PU_SEL	0x0	Pull-down resistor selected
	GPIO7_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO7_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO8_CONF	GPIO8_OD	0x0	Push-pull output
	GPIO8_DIR	0x0	Input
	GPIO8_SEL	0x0	GPIO8
	GPIO8_PU_SEL	0x0	Pull-down resistor selected
	GPIO8_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO8_DEGLITCH_EN	0x0	No deglitch, only synchronization.

Table 4-7. GPIO NVM Settings (continued)

Register Name	Field Name	TPS6593-Q1	
		Value	Description
GPIO9_CONF	GPIO9_OD	0x0	Push-pull output
	GPIO9_DIR	0x0	Input
	GPIO9_SEL	0x0	GPIO9
	GPIO9_PU_SEL	0x0	Pull-down resistor selected
	GPIO9_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO9_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO10_CONF	GPIO10_OD	0x0	Push-pull output
	GPIO10_DIR	0x0	Input
	GPIO10_SEL	0x0	GPIO10
	GPIO10_PU_SEL	0x0	Pull-down resistor selected
	GPIO10_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO10_DEGLITCH_EN	0x1	8 µs deglitch time.
GPIO11_CONF	GPIO11_OD	0x0	Push-pull output
	GPIO11_DIR	0x0	Input
	GPIO11_SEL	0x0	GPIO11
	GPIO11_PU_SEL	0x0	Pull-down resistor selected
	GPIO11_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO11_DEGLITCH_EN	0x0	No deglitch, only synchronization.
NPWRON_CONF	NPWRON_SEL	0x0	ENABLE
	ENABLE_PU_SEL	0x0	Pull-down resistor selected
	ENABLE_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	ENABLE_DEGLITCH_EN	0x1	8 us deglitch time when ENABLE, 50 ms deglitch time when NPWRON.
	ENABLE_POL	0x0	Active high
	NRSTOUT_OD	0x1	Open-drain output
GPIO_OUT_1	GPIO1_OUT(1)	0x0	Low
	GPIO2_OUT(1)	0x0	Low
	GPIO3_OUT(1)	0x0	Low
	GPIO4_OUT(1)	0x0	Low
	GPIO5_OUT(1)	0x0	Low
	GPIO6_OUT(1)	0x0	Low
	GPIO7_OUT(1)	0x0	Low
	GPIO8_OUT(1)	0x0	Low
GPIO_OUT_2	GPIO9_OUT(1)	0x0	Low
	GPIO10_OUT(1)	0x0	Low
	GPIO11_OUT(1)	0x0	Low

(1) Note that this NVM default value can change when the device transitions to ACTIVE mode.

4.7 Finite State Machine (FSM) Settings

These settings describe how the PMIC output rails are assigned to various system-level states. Also, the default trigger for each system-level state is described. All these settings can be changed though I^2C after startup.

Table 4-8. FSM NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
RAIL_SEL_1	BUCK1_GRP_SEL	0x0	No group assigned
	BUCK2_GRP_SEL	0x0	No group assigned
	BUCK3_GRP_SEL	0x0	No group assigned
	BUCK4_GRP_SEL	0x0	No group assigned
RAIL_SEL_2	BUCK5_GRP_SEL	0x0	No group assigned
	LDO1_GRP_SEL	0x0	No group assigned
	LDO2_GRP_SEL	0x0	No group assigned
	LDO3_GRP_SEL	0x0	No group assigned
RAIL_SEL_3	LDO4_GRP_SEL	0x0	No group assigned
	VCCA_GRP_SEL	0x0	No group assigned
FSM_TRIG_SEL_1	MCU_RAIL_TRIG	0x2	MCU power error
	SOC_RAIL_TRIG	0x3	SOC power error
	OTHER_RAIL_TRIG	0x1	Orderly shutdown
	SEVERE_ERR_TRIG	0x0	Immediate shutdown
FSM_TRIG_SEL_2	MODERATE_ERR_TRIG	0x1	Orderly shutdown

4.8 Interrupt Settings

These settings detail the default configurations for what is monitored by nINT pin. All these settings can be changed though I^2C after startup.

Table 4-9. Interrupt NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
FSM_TRIG_MASK_1	GPIO1_FSM_MASK	0x0	Not masked
	GPIO1_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO2_FSM_MASK	0x0	Not masked
	GPIO2_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO3_FSM_MASK	0x0	Not masked
	GPIO3_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO4_FSM_MASK	0x0	Not masked
	GPIO4_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
FSM_TRIG_MASK_2	GPIO5_FSM_MASK	0x0	Not masked
	GPIO5_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO6_FSM_MASK	0x0	Not masked
	GPIO6_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO7_FSM_MASK	0x0	Not masked
	GPIO7_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO8_FSM_MASK	0x0	Not masked
	GPIO8_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
FSM_TRIG_MASK_3	GPIO9_FSM_MASK	0x0	Not masked
	GPIO9_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO10_FSM_MASK	0x0	Not masked
	GPIO10_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO11_FSM_MASK	0x0	Not masked
	GPIO11_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'

Table 4-9. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS6593-Q1	
		Value	Description
MASK_BUCK1_2	BUCK1_ILIM_MASK	0x1	Interrupt not generated.
	BUCK1_OV_MASK	0x1	Interrupt not generated.
	BUCK1_UV_MASK	0x1	Interrupt not generated.
	BUCK2_ILIM_MASK	0x1	Interrupt not generated.
	BUCK2_OV_MASK	0x1	Interrupt not generated.
	BUCK2_UV_MASK	0x1	Interrupt not generated.
MASK_BUCK3_4	BUCK3_ILIM_MASK	0x1	Interrupt not generated.
	BUCK3_OV_MASK	0x1	Interrupt not generated.
	BUCK3_UV_MASK	0x1	Interrupt not generated.
	BUCK4_OV_MASK	0x1	Interrupt not generated.
	BUCK4_UV_MASK	0x1	Interrupt not generated.
	BUCK4_ILIM_MASK	0x1	Interrupt not generated.
MASK_BUCK5	BUCK5_ILIM_MASK	0x1	Interrupt not generated.
	BUCK5_OV_MASK	0x1	Interrupt not generated.
	BUCK5_UV_MASK	0x1	Interrupt not generated.
MASK_LDO1_2	LDO1_OV_MASK	0x1	Interrupt not generated.
	LDO1_UV_MASK	0x1	Interrupt not generated.
	LDO2_OV_MASK	0x1	Interrupt not generated.
	LDO2_UV_MASK	0x1	Interrupt not generated.
	LDO1_ILIM_MASK	0x1	Interrupt not generated.
	LDO2_ILIM_MASK	0x1	Interrupt not generated.
MASK_LDO3_4	LDO3_OV_MASK	0x1	Interrupt not generated.
	LDO3_UV_MASK	0x1	Interrupt not generated.
	LDO4_OV_MASK	0x1	Interrupt not generated.
	LDO4_UV_MASK	0x1	Interrupt not generated.
	LDO3_ILIM_MASK	0x1	Interrupt not generated.
	LDO4_ILIM_MASK	0x1	Interrupt not generated.
MASK_VMON	VCCA_OV_MASK	0x1	Interrupt not generated.
	VCCA_UV_MASK	0x1	Interrupt not generated.
MASK_GPIO1_8_FALL	GPIO1_FALL_MASK	0x0	Interrupt generated
	GPIO2_FALL_MASK	0x0	Interrupt generated
	GPIO3_FALL_MASK	0x0	Interrupt generated
	GPIO4_FALL_MASK	0x0	Interrupt generated
	GPIO5_FALL_MASK	0x0	Interrupt generated
	GPIO6_FALL_MASK	0x0	Interrupt generated
	GPIO7_FALL_MASK	0x0	Interrupt generated
	GPIO8_FALL_MASK	0x0	Interrupt generated
MASK_GPIO1_8_RISE	GPIO1_RISE_MASK	0x0	Interrupt generated
	GPIO2_RISE_MASK	0x0	Interrupt generated
	GPIO3_RISE_MASK	0x0	Interrupt generated
	GPIO4_RISE_MASK	0x0	Interrupt generated
	GPIO5_RISE_MASK	0x0	Interrupt generated
	GPIO6_RISE_MASK	0x0	Interrupt generated
	GPIO7_RISE_MASK	0x0	Interrupt generated
	GPIO8_RISE_MASK	0x0	Interrupt generated

Table 4-9. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS6593-Q1	
		Value	Description
MASK_GPIO9_11 / MASK_GPIO9_10	GPIO9_FALL_MASK	0x0	Interrupt generated
	GPIO9_RISE_MASK	0x0	Interrupt generated
	GPIO10_FALL_MASK	0x0	Interrupt generated
	GPIO11_FALL_MASK	0x0	Interrupt generated
	GPIO10_RISE_MASK	0x0	Interrupt generated
	GPIO11_RISE_MASK	0x0	Interrupt generated
MASK_STARTUP	NPWRON_START_MASK	0x1	Interrupt not generated.
	ENABLE_MASK	0x0	Interrupt generated
	FSD_MASK	0x1	Interrupt not generated.
	SOFT_REBOOT_MASK	0x1	Interrupt not generated.
MASK_MISC	TWARN_MASK	0x0	Interrupt generated
	BIST_PASS_MASK	0x1	Interrupt not generated.
	EXT_CLK_MASK	0x0	Interrupt generated
MASK_MODERATE_ERR	BIST_FAIL_MASK	0x1	Interrupt not generated.
	REG_CRC_ERR_MASK	0x1	Interrupt not generated.
	SPMI_ERR_MASK	0x1	Interrupt not generated.
	NPWRON_LONG_MASK	0x1	Interrupt not generated.
	PFSM_ERR_MASK	0x0	Interrupt generated
MASK_FSM_ERR	IMM_SHUTDOWN_MASK	0x0	Interrupt generated
	MCU_PWR_ERR_MASK	0x0	Interrupt generated
	SOC_PWR_ERR_MASK	0x0	Interrupt generated
	ORD_SHUTDOWN_MASK	0x0	Interrupt generated
MASK_COMM_ERR	COMM_FRM_ERR_MASK	0x1	Interrupt not generated.
	COMM_CRC_ERR_MASK	0x1	Interrupt not generated.
	COMM_ADR_ERR_MASK	0x1	Interrupt not generated.
	I2C2_CRC_ERR_MASK	0x1	Interrupt not generated.
	I2C2_ADR_ERR_MASK	0x1	Interrupt not generated.
MASK_READBACK_ERR	EN_DRV_READBACK_ MASK	0x1	Interrupt not generated.
	NINT_READBACK_MASK	0x0	Interrupt generated
	NRSTOUT_READBACK_ MASK	0x0	Interrupt generated
	NRSTOUT_SOC_ READBACK_MASK	0x1	Interrupt not generated.
MASK_ESM	ESM_SOC_PIN_MASK	0x1	Interrupt not generated.
	ESM_SOC_RST_MASK	0x1	Interrupt not generated.
	ESM_SOC_FAIL_MASK	0x1	Interrupt not generated.
	ESM_MCU_PIN_MASK	0x1	Interrupt not generated.
	ESM_MCU_RST_MASK	0x1	Interrupt not generated.
	ESM_MCU_FAIL_MASK	0x1	Interrupt not generated.

4.9 POWERGOOD Settings

These settings detail the default configurations for what is monitored by PGOOD pin. All these settings can be changed though I^2C after startup.

Table 4-10. POWERGOOD NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
PGOOD_SEL_1	PGOOD_SEL_BUCK1	0x0	Masked
	PGOOD_SEL_BUCK2	0x0	Masked
	PGOOD_SEL_BUCK3	0x0	Masked
	PGOOD_SEL_BUCK4	0x0	Masked
PGOOD_SEL_2	PGOOD_SEL_BUCK5	0x0	Masked
PGOOD_SEL_3	PGOOD_SEL_LDO1	0x0	Masked
	PGOOD_SEL_LDO2	0x0	Masked
	PGOOD_SEL_LDO3	0x0	Masked
	PGOOD_SEL_LDO4	0x0	Masked
PGOOD_SEL_4	PGOOD_SEL_VCCA	0x0	Masked
	PGOOD_SEL_TDIE_WARN	0x0	Masked
	PGOOD_SEL_NRSTOUT	0x0	Masked
	PGOOD_SEL_NRSTOUT_ SOC	0x0	Masked
	PGOOD_POL	0x0	PGOOD signal is high when monitored inputs are valid
	PGOOD_WINDOW	0x0	Only undervoltage is monitored

4.10 Miscellaneous Settings

These settings detail the default configurations of additional settings, such as spread spectrum, BUCK frequency, and LDO timeout. All these settings can be changed though I^2C after startup.

Table 4-11. Miscellaneous NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
PLL_CTRL	EXT_CLK_FREQ	0x0	1.1 MHz
CONFIG_1	TWARN_LEVEL	0x0	130C
	TSD_ORD_LEVEL	0x0	140C
	I2C1_HS	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code.
	I2C2_HS	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code.
	EN_ILIM_FSM_CTRL	0x0	Buck/LDO regulators ILIM interrupts do not affect FSM triggers.
	NSLEEP1_MASK	0x0	NSLEEP1(B) affects FSM state transitions.
	NSLEEP2_MASK	0x0	NSLEEP2(B) affects FSM state transitions.
CONFIG_2	BB_CHARGER_EN	0x0	Disabled
	BB_VEOC	0x0	2.5 V
	BB_ICHR	0x0	100 µA
RECOV_CNT_REG_2	RECOV_CNT_THR	0xf	0xf
SPREAD_SPECTRUM_1	SS_EN	0x0	Spread spectrum disabled
	SS_DEPTH	0x0	No modulation
FSM_STEP_SIZE	PFSM_DELAY_STEP	0xb	0xb
USER_SPARE_REGS	USER_SPARE_1	0x0	0x0
	USER_SPARE_2	0x0	0x0
	USER_SPARE_3	0x0	0x0
	USER_SPARE_4	0x0	0x0
ESM_MCU_MODE_ CFG	ESM_MCU_EN	0x0	ESM_MCU disabled.
ESM_SOC_MODE_ CFG	ESM_SOC_EN	0x0	ESM_SoC disabled.

Table 4-11. Miscellaneous NVM Settings (continued)

Register Name	Field Name	TPS6593-Q1	
		Value	Description
RTC_CTRL_2	XTAL_EN	0x0	Crystal oscillator is disabled
	LP_STANDBY_SEL	0x0	LDOINT is enabled in standby state.
	FAST_BIST	0x1	Only analog BIST is run at BOOT BIST.
	STARTUP_DEST	0x3	ACTIVE
	XTAL_SEL	0x0	6 pF
RTS_SPARE_REG	RTC_SPARE_3	0x0	0x0
	RTC_SPARE_2	0x0	0x0
	RTC_SPARE_1	0x0	0x0
	RTC_SPARE_0	0x0	0x0
PFSM_DELAY_REG_1	PFSM_DELAY1	0x0	0x0
PFSM_DELAY_REG_2	PFSM_DELAY2	0x0	0x0
PFSM_DELAY_REG_3	PFSM_DELAY3	0x0	0x0
PFSM_DELAY_REG_4	PFSM_DELAY4	0x0	0x0

4.11 Interface Settings

These settings detail the default interface, interface configurations, and device addresses. These settings cannot be changed through software writes. The device must be reprogrammed to update these settings.

Table 4-12. Interface NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
SERIAL_IF_CONFIG	I2C_SPI_SEL	0x0	I2C
	I2C1_SPI_CRC_EN	0x0	CRC disabled
	I2C2_CRC_EN	0x0	CRC disabled
I2C1_ID_REG	I2C1_ID	0x28	0x28
I2C2_ID_REG	I2C2_ID	0x12	0x12

4.12 Multi-Device Settings

These settings detail whether the device is a operating as a master or slave in the system. These settings cannot be changed after device startup.

Table 4-13. Multi-Device NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
SPMI_ID	SPMI_SID	0x5	0x5
	SPMI_MID	0x0	0x0
SPMI_SLAVE_COUNT	SPMI_SLAVE_CNT	0x1	0x1

4.13 Watchdog Settings

These settings detail the default watchdog settings. These settings can be changed though I^2C after startup.

Table 4-14. Watchdog NVM Settings

Register Name	Field Name	TPS6593-Q1	
		Value	Description
WD_LONGWIN_CFG	WD_LONGWIN		
WD_THR_CFG	WD_EN		

5 Pre-Configurable Finite State Machine (PFSM) Settings

This section describes the default PFSM settings of the TPS6593-Q1 device. These settings cannot be changed after device startup. They are only changed through reprogramming of the device.

5.1 Configured States

In this PDN, the following three power states are configured into the PMIC devices:

- Standby
- Active
- Safe

In Figure 5-1, the configured power states are described, along with the transition conditions required to move between configured states. Additionally, the transitions to hardware states, such as SAFE RECOVERY, are described.

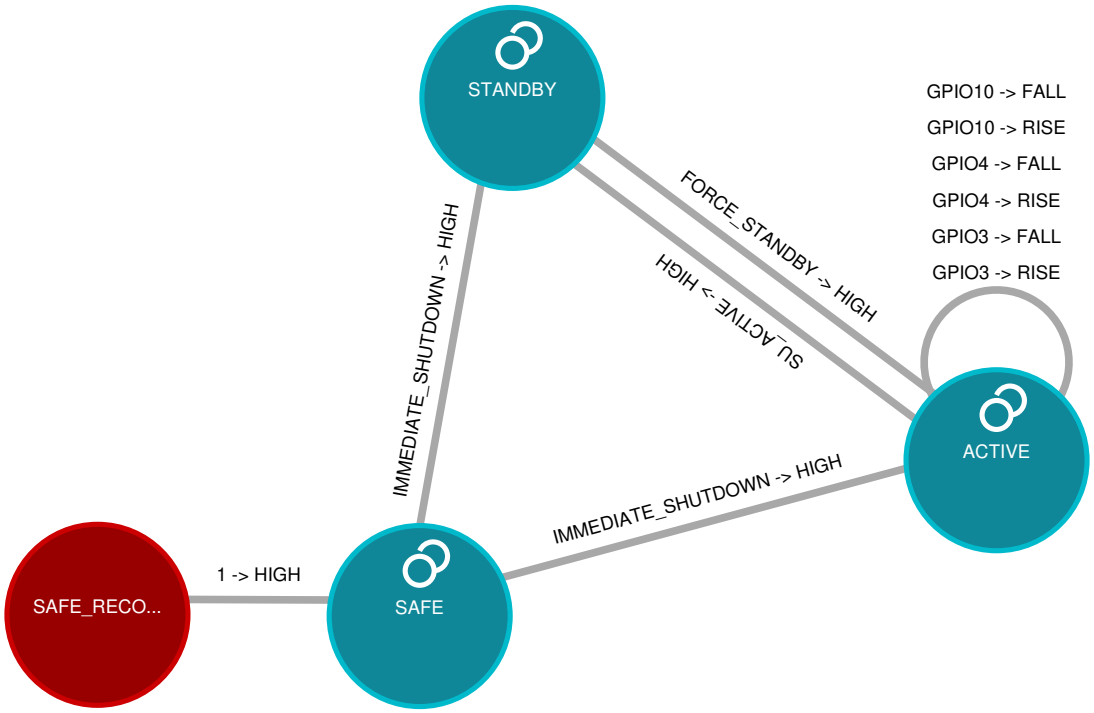


Figure 5-1. Pre-Configurable State Machine (PFSM) States and Transitions

The definition for each power state is described below:

STANDBY The PMIC is powered by a valid supply on the system power rail (VCCA > VCCA_UV) and waiting for a start-up event or condition. All device resources are powered down in the STANDBY state. If no changes are needed from the default interface settings, then the device can be re-programmed in STANDBY state.

ACTIVE The PMIC is powered by a valid supply and has received a start-up event, such as ENABLE pin asserted high. The PMIC will keep the outputs of all resources off, but is now ready to be programmed. The device must be programmed from ACTIVE state if needing to enable SPI or CRC, or change the default I2C address. If programming is not required, the PMIC is now ready for I2C or SPI commands (based on GPIO configuration) to configure and enable the output rails of the PMIC.

SAFE In the event of a severe power error, such as a short circuit or thermal event, the SAFE state provides a controlled way to shut down all resources safely and quickly before transitioning to SAFE RECOVERY.

5.2 State Transitions

As shown in Figure 5-1, there are various triggers that can enable a state transition between configured states and hardware states. Table 5-1 describes each trigger and its associated state transition from highest priority to lowest priority.

Table 5-1. State Transition Triggers

Trigger	PFSM Current State	PFSM Destination State	Power Sequence Executed
Immediate Shutdown	STANDBY, ACTIVE	SAFE	TO_SAFE_SEVERE
OFF Request(1)	ACTIVE	STANDBY	TO_STANDBY
ON Request(2)	STANDBY	ACTIVE	TO_ACTIVE
GPIO3 Rises	ACTIVE	ACTIVE	EN_SPI
GPIO3 Falls	ACTIVE	ACTIVE	DIS_SPI
GPIO4 Rises	ACTIVE	ACTIVE	EN_CRC
GPIO4 Falls	ACTIVE	ACTIVE	DIS_CRC
GPIO10 Rises	ACTIVE	ACTIVE	UPDATE_I2C1_2C
GPIO10 Falls	ACTIVE	ACTIVE	UPDATE_I2C1_28
Always True(3)	SAFE	SAFE_RECOVERY	No sequence is excuted, device exits PFSM

(1) OFF Request trigger is named FORCE_STANDBY.
(2) ON Request trigger is named SU_ACTIVE.
(3) Trigger from SAFE to SAFE RECOVERY always occurs once transitioned to SAFE state. This allows the device to exit the PFSM and transition to the hardware states and check that the error is removed before the next startup.

5.3 Power Sequences

Since this NVM is intended as a starting point for programmable applications, none of the power sequences include any change of output resources, except for the TO_SAFE_SEVERE sequence. As shown in Figure 3, this sequence will shut down all power rails in the event that any were enabled through I2C or SPI.

All other power sequences consist of register writes only to enable or disable interface features. In the case of the TO_ACTIVE and TO_STANDBY sequences, the device is activating and deactivating internal components, clocks, etc. Details on *Activate* and *Deactivate* commands can be found in the Scalable PMIC's GUI User's Guide.

When a severe error causes the TO_SAFE_SEVERE sequence to execute, the immediate shutdown will disable the clocks and switching of the BUCKs first and rely on the pulldown resistors of the BUCKs and LDOs to discharge the rails. This is to prevent any damage of the PMICs in case of over voltage on VCCA or thermal shutdown. The sequence is shown in Figure 5-2.

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
BUCK1	TPS6593-Q1		0 us	BUCK1
BUCK2	TPS6593-Q1		0 us	BUCK2
BUCK3	TPS6593-Q1		0 us	BUCK3
BUCK4	TPS6593-Q1		0 us	BUCK4
BUCK5	TPS6593-Q1		0 us	BUCK5
LDO1	TPS6593-Q1		0 us	LDO1
LDO2	TPS6593-Q1		0 us	LDO2
LDO3	TPS6593-Q1		0 us	LDO3
LDO4	TPS6593-Q1		0 us	LDO4

Figure 5-2. TO_SAFE_SEVERE Sequence

6 References

- Texas Instruments, *Programmable PMICs: Design Guide for Programming TPS6593-Q1 in Evaluation and Production*user's guide
- Texas Instruments, *Scalable PMIC's GUI* user's guide
- Texas Instruments, *TPS6593-Q1 Power Management IC (PMIC) for Processors with 5 Bucks and 4 LDOs* user's guide
- Texas Instruments, *TPS6594-BOOSTXL* user’s guide
- Texas Instruments, *TPS6594-Q1 Schematic PCB Checklist*
- Texas Instruments, *TPS6594EVM and TPS6593EVM* user’s guide

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