User's Guide

TPS65941212-Q1 and TPS65941111-Q1 PMIC User Guide for Jacinto™ 7 J721E, PDN-0B

ABSTRACT

This user's guide can be used as a guide for integrating the TPS65941212-Q1 and TPS65941111-Q1 power management integrated circuits (PMICs) into a system powering the Automotive Jacinto™ 7 DRA829 or TDA4VM processor.

Table of Contents

Trademarks

Jacinto™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

This user's guide describes a power distribution network (PDN), PDN-0B, between two TPS6594-Q1 devices and either DRA829V or TDA4VM processor with independent MCU and Main power rails. This PDN enables board level isolation of the processor MCU and Main voltage resources as required to leverage the processor architecture in implementing two desirable end product features:

1. MCU processor acts as independent safety monitor (MCU Safety Island) over the Main processing resources to ensure safe system operations.
2. MCU processor maintains minimum system operations (MCU Only) to significantly reduce processor power dissipation thereby extending battery life during stand-by use cases and reducing component temperature.

This description includes the following to clarify platform system operation:

1. PDN power resource connections
2. PDN digital control connections
3. Primary and secondary PMIC default NVM contents
4. PMIC sequencing settings to support different PDN power state transitions for an advanced processor system

PMIC and processor data manuals describe recommended operation, electrical characteristics, external components, package details, register maps, and overall component functionality. In the event of any inconsistency between any user's guide, application report, or other referenced material, the data sheet specification is the definitive source.

2 Device Versions

There are different orderable part numbers (PNs) of the TPS6594-Q1 device available with unique NVM settings to support different end product use cases and processor types. The unique NVM settings for each PMIC device is optimized per PDN design to support different processors, processing loads, SDRAM types, system functional safety levels, and end product features (such as low power modes, processor voltages, and memory subsystems). The NVM settings can be identified by both NVM_ID and NVM_REV registers. Each PMIC device is distinguished by the part number, NVM_ID, and NVM_REV values listed in Table 2-1.

Table 2-1. Dual TPS6594-Q1 Orderable Part Numbers for Independent MCU and Main PDN System

PDN USE CASE	PDN	Orderable Part Number	TI_NVM_ID (TI_NVM_REV)	Orderable Part Number	TI_NVM_ID (TI_NVM_REV)	Error Signal Monitoring
• Up to 9 A(1) on the Primary PMIC 3-phase CPU rail • Up to 12 A1 on the Secondary PMIC 4-phase CORE rail • Up to 3.4 A(1) on the SDRAM, with support for LPDDR4 • Supports Processor 2 GHz maximum clock with high-speed SERDES operations • Supports 32 Gb of LPDDR4 SDRAM with 4266MTs data rate • Supports Functional Safety up to ASIL-D level with MCU Safety Island • Supports MCU-only and DDR_Retention low power modes • Supports I/O level of 3.3 V or 1.8 V • Supports optional end product features: – Compliant high-speed SD Card memory – Compliant USB 2.0 Interface – On-board Efuse programming of high security processors	0B	TPS65941212RWERQ1	0x12 (0x03)	TPS65941111RWERQ1	0x11 (0x03)	Combined MCU and SOC
	0C	TPS65941213RWERQ1	0x13 (0x04)	TPS65941111RWERQ1	0x11 (0x03)	Dedicated MCU and SOC

(1) TI recommends having 15% margin between the maximum expected load current and the maximum current allowed per each PMIC output rail.

Note

PDN-0C is recommended for all new designs and designs needing the additional functional safety coverage provided afforded by the GPIO optimizations found in PDN-0C. This document describes PDN-0B.

3 Processor Connections

This section details how the dual TPS6594-Q1 power resources and GPIO signals are connected to the processor and other peripheral components in order to support the PDN use case.

3.1 Power Mapping

Figure 3-1 shows the power mapping between the dual TPS6594-Q1 PMIC power resources and processor voltage domains required to support independent MCU and Main power rails. In this configuration, both PMICs use a 3.3 V input voltage. For Functional Safety applications, there is a protection FET before VCCA that connects to the OVPGDRV pin of the primary PMIC, allowing voltage monitoring of the input supply to the PMICs.

The VCCA voltage must be the first voltage applied to the PMIC devices. VIO_IN of the PMICs must not be supplied before VCCA. A load switch supplies VIO_IN in this PDN. This load switch also supplies the VDDSHVx_MCU voltage domain of the processor. This allows PMIC GPIO control signals referenced to VIO_IN to remain active during MCU Only low power mode and to be disabled during DDR Retention (aka Suspend-to-RAM) to reduce PMIC power.

For SD card dual-voltage I/O support (3.3 V and 1.8 V), LDO1 of the TPS659411-Q1 device can be used. A processor GPIO control signal with a logic high default value is used to set SD VIO to 3.3 V initially. During processor power up, the boot loader SW can set GPIO signal low to select 1.8 V level as needed for high-speed card operation per SD specification. This allows control of the LDO1 voltage without the need for the MCU processor to establish I2C communication with the PMICs during boot from SD card operations.

This PDN uses four discrete power components with three being required and one is optional depending upon end product features. The two TPS22965-Q1 Load Switches connect VCCA_3V3 power rail to supply OV protected 3.3 V to processor I/O domains. Two load switches are required in order to enable isolation between MCU and Main processor sub-sections for MCU Safety Island or MCU Only low power operations. The TPS62813-Q1 Buck Converter supplies LPDDR4 SDRAM component with required 1.1V supply. The unused primary PMIC FB pin, FB_B3, has been configured per NVM settings, Table 5-3, to provide voltage monitoring for VDD_DDR_1V1 power rail if an end product OV/UV monitoring requirements include this supply. The one optional discrete power component is TLV73318-Q1 LDO that can be used if an end product uses a high security processor type and desires the capability to program Efuse values on-board. If this feature is not desired, then this LDO can be omitted and processor VPP pins treated per data manual recommendations.

Note

The PMIC voltage monitor on FB_B3 must be connected to 1.1 V. The VMON_ABIST_EN=1 for both the primary and secondary PMICs. If 1.1 V is not connected to FB_B3 when the monitor is enabled then the self-test fails and the BIST_FAIL_INT interrupt is set and the device goes to the safe state and main processor voltages are disabled.

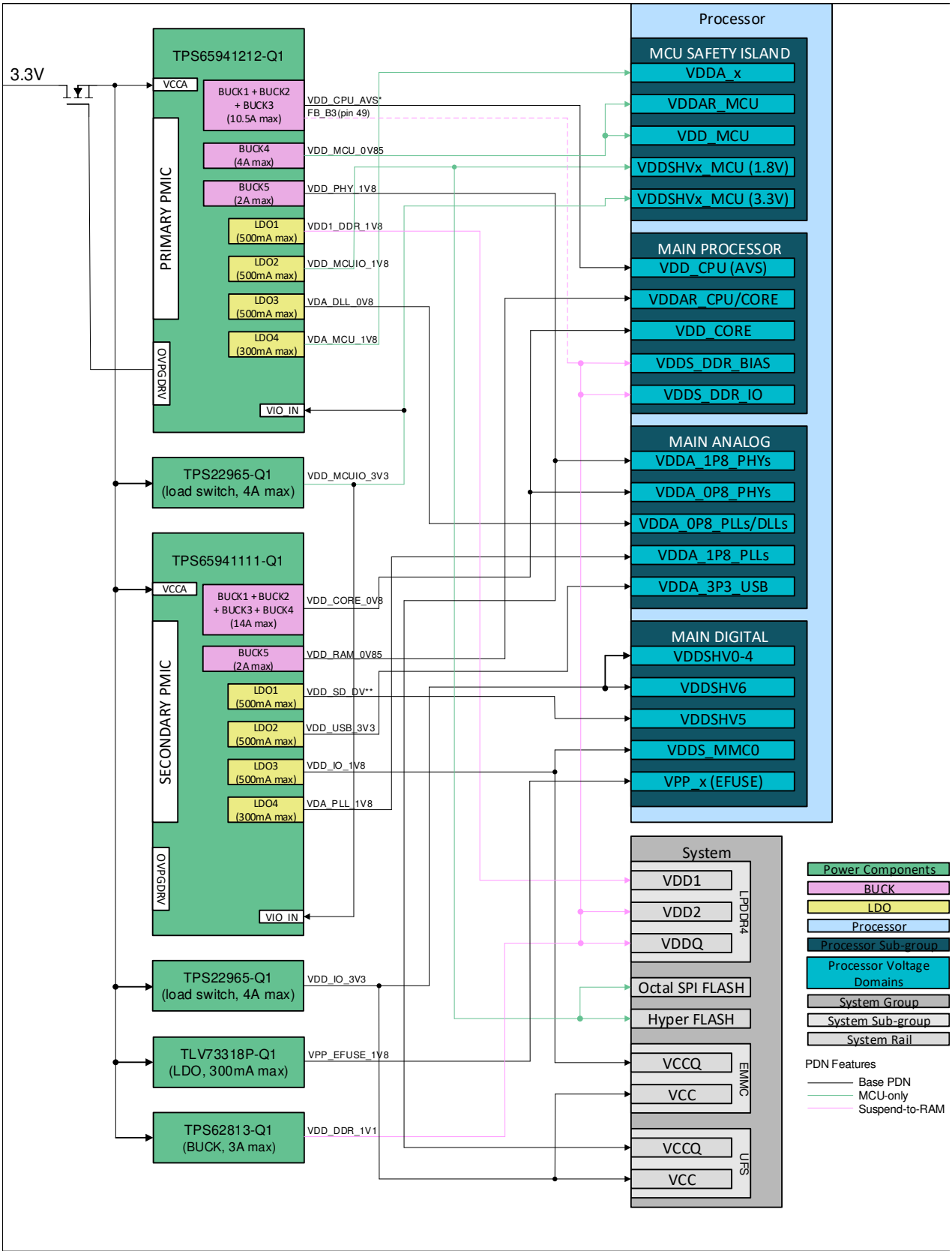

Figure 3-1. Power Connections

- * VDD_CPU_AVS, boot voltage of 0.8 V then software sets device specific AVS; 0.68 V – 0.72 V.
- ** VDD_SD_DV, 3.3 V then software changes to 1.8 V per HS-SD.

Table 3-1 identifies which power resources are required to support different system features. If the system feature listed is not required, the power resource connection can be removed and the processor voltage domains need to be grouped into alternative power rails.

Table 3-1. PDN Power Mapping and System Features

Power Mapping				System Features				
Device	**Power Resource**	**Power Rails**	**Processor and Memory Domains**	**Active SoC**	**MCU - only**	**Suspend-to-RAM**	**SD Card**	**USB Interface**
TPS65941212-Q1	BUCK123	VDD_CPU_AVS	VDD_CPU	Required				
	FB_B3		VDDS_DDR_BIAS, VDDS_DDR_IO, LPDDR4	Required		Required		
	BUCK4	VDD_MCU_0V85	VDDAR_MCU, VDD_MCU	Required	Required			
	BUCK5	VDD_PHY_1V8	VDDA_1P8_PHYs	Required				
	LDO1	VDD1_DDR_1V8	Mem: VDD1	Required	Optional	Required		
	LDO2	VDD_MCUIO_1V8	VDDSHVx_MCU (1.8 V) Mem: VCC	Required	Required			
	LDO3	VDA_DLL_0V8	VDDA_0P8_PLLs/DLLs	Required				
	LDO4	VDA_MCU_1V8	VDDA_x	Required	Required			
TPS65941111-Q1	BUCK1234	VDD_CORE_0V8	VDD_CORE, VDDA_0P8_PHYs	Required				
	BUCK5	VDD_RAM_0V85	VDDAR_CPU/CORE	Required				
	LDO1	VDD_SD_DV	VDDSHV5				Required	
	LDO2	VDD_USB_3V3	VDDA_3P3_USB					Required
	LDO3	VDD_IO_1V8	VDDS_MMC0 Mem: VCCQ	Required				
	LDO4	VDA_PLL_1V8	VDDA_1P8_PLLs	Required				
TPS22965-Q1	Load Switch	VDD_MCUIO_3V3	VDDSHVx_MCU (3.3 V)	Required	Required			
TPS22965-Q1	Load Switch	VDD_IO_3V3	VDDSHV0-4,VDDSHV6 (3.3 V)	Required	Required			
TLV73318P-Q1	LDO	VPP_EFUSE_1V8	VPP_x(EFUSE)	Optional				
TPS62813-Q1	BUCK	VDD_DDR_1V1	VDDS_DDR_BIAS, VDDS_DDR_IO Mem: VDD2	Required	Optional	Required		

3.2 Control Mapping

Figure 3-2 shows the digital control signal mapping between processor and PMIC devices. For the two PMIC devices to work together, the primary PMIC and secondary PMIC must establish an SPMI communication channel. This allows the two TPS6594-Q1 to synchronize their internal Pre-Configurable State Machines (PFSM) so that they operate as one PFSM across all power and digital resources. The GPIO_5 and GPIO_6 pins on the TPS6594-Q1 are assigned for this functionality. In addition, the primary PMIC LDOVINT pin is connected to the secondary PMIC ENABLE input to correctly initiate the PFSM.

Other digital connections from the TPS6594-Q1 devices to the processor provide error monitoring, processor reset, processor wake up, and system low-power modes. Specific GPIO pins have been assigned to key signals in order to ensure proper operation during low power modes when only a few GPIO pins remain operational.

The digital connections shown in Figure 3-2 allow system features including MCU-only MCU Safety Island and suspend-to-RAM low power modes, functional safety up to ASIL-D, compliant dual voltage SD card operation, and LPDDR4x integration.

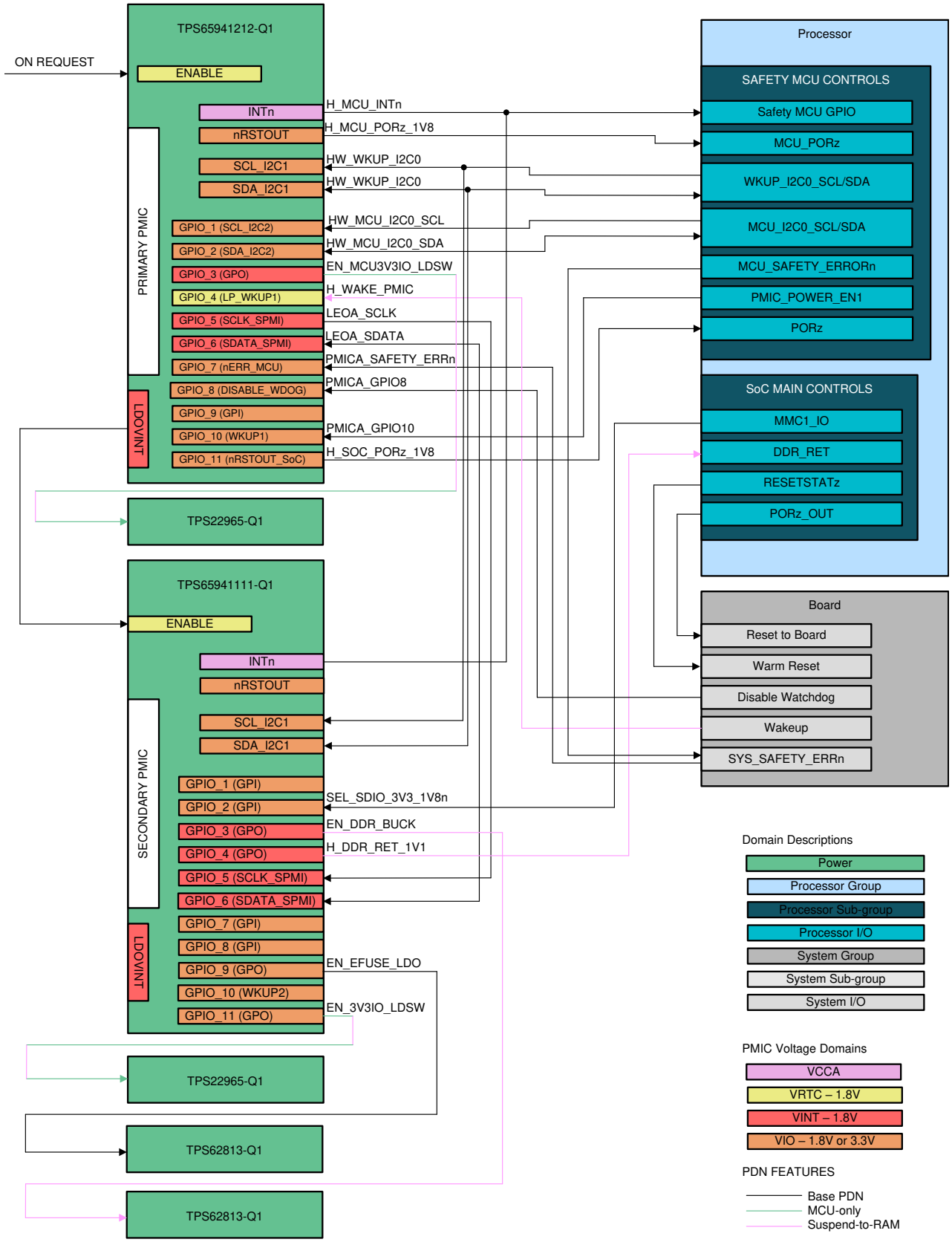

Figure 3-2. TPS6594-Q1 Digital Connections

Note

The PMIC voltage domain of an IO can be different depending upon configuration. When configured as an input GPIO3 and GPIO4 are in the VRTC domain. When configured as an output, GPIO3 and GPIO4 are in the VINT domain.

Note

In addition to the I2C signals, four additional signals are open-drain outputs and require a pullup to a specific power rail. Please refer to Table 3-2 for a list of the signals and the specific power rail.

Table 3-2. Open-drain signals and Power Rail

PDN Signal	Pullup Power Rail
H_MCU_INTn	VDD_MCUIO_3V3
H_MCU_PORz_1V8	VDA_MCU_1V8
H_SOC_PORz_1V8	VDA_MCU_1V8
H_DDR_RET_1V1	VDD_DDR_1V1_REG
H_WKUP_I2C0	VDD_MCUIO_3V3
H_MCU_I2C0_SCL/SDA	VDD_MCUIO_3V3

Please use Table 3-3 as a guide to understand GPIO assignments required for each PDN system feature. If the feature listed is not required, the digital connection can be removed; however, the GPIO pin is still configured per NVM defined default function shown. After the processor has booted up, system software can potentially reconfigure an unused GPIO to support a new function. This is possible as long as that function is only needed after boot and default function does not cause any conflicts with normal operations (for example, two outputs driving same net). For details on how functional safety related connections help achieve functional safety system-level goals, see Section 4.

Table 3-3. Digital Connections by System Feature

Device	GPIO Mapping			System Features				
	PMIC Pin	NVM Function	PDN Signals	Active SoC	Functional Safety	MCU - only and MCU-Safety Island	Suspend-to-RAM	SD Card
TPS6594112-Q1	nPWRON/ ENABLE	Enable	SOC_PWR_ON	Required				
	INT	INT	H_MCU_INTn		Required			
	nRSTOUT	nRSTOUT	H_MCU_PORz_1V8	Required		Required		
	SCL_I2C1	SCL_I2C1	H_WKUP_I2C0	Required				
	SDA_I2C1	SDA_I2C1	H_WKUP_I2C0	Required				
	GPIO_1	SCL_I2C2	H_MCU_I2C0_SCL		Required			
	GPIO_2	SDA_I2C2	H_MCU_I2C0_SDA		Required			
	GPIO_3	GPO	EN_MCU3V3IO_LDSW				Required	
	GPIO_4	LP_WKUP1	H_WAKE_PMIC				Required	
	GPIO_5	SCLK_SPMI	LEOA_SCLK	Required				
	GPIO_6	SDATA_SPMI	LEOA_SDATA	Required				
	GPIO_7	nERR_MCU	PMICA_SAFETY_ERRn		Required			
	GPIO_8	DISABLE_WDOG	PMICA_GPIO8	(2)	(2)			
	GPIO_9	GPI	PMICA_GPIO9(3)					
	GPIO_10	WKUP1	PMIC_POWER_EN1	Required				
	GPIO_11	nRSTOUT_SOC	H_SOC_PORz_1V8			Required		

Table 3-3. Digital Connections by System Feature (continued)

Device	GPIO Mapping			System Features				
	PMIC Pin	NVM Function	PDN Signals	Active SoC	Functional Safety	MCU - only and MCU-Safety Island	Suspend-to-RAM	SD Card
TPS65941111-Q1	nPWRON/ ENABLE	ENABLE	VINT_LEOA_1V8		Required			
	nINT	nINT	H_MCU_INTn					
	nRSTOUT	nRSTOUT	Unused					
	SCL_I2C1	SCL_I2C1	H_WKUP_I2C0	Required				
	SDA_I2C1	SCL_I2C1	H_WKUP_I2C0	Required				
	GPIO_1	GPI	Unused(3)					
	GPIO_2	GPI	SEL_SDIO_3V3_1V8n(1)					Required
	GPIO_3	GPO	EN_DDR_BUCK					
	GPIO_4	GPO	H_DDR_RET_1V1				Required	
	GPIO_5	SCLK_SPMI	LEOA_SCLK	Required				
	GPIO_6	SDATA_SPMI	LEOA_SDATA	Required				
	GPIO_7	GPI	Unused(3)					
	GPIO_8	GPI	Unused(3)					
	GPIO_9	GPO	EN_EFUSE_LDO(3)					
	GPIO_10	WKUP2	Unused(3)					
	GPIO_11	GPO	EN_3V3IO_LDSW			Required		

(1) This pin is an input with an internal pulldown enabled. A rising edge on this GPI initiates the FSM trigger and associated sequence. The sequence configures LDO1 to bypass mode, supplying 3.3 V. A falling edge triggers an alternate sequence which configures LDO1 to LDO mode, supplying 1.8 V. See also Table 6-1

(2) If it is desired to disable the watchdog through hardware, GPIO_8 is required and must be set high by the time nRSTOUT goes high. After nRSTOUT is high, the watchdog state is latched and the pin can be configured for other functions through software.

(3) This GPIO is not required for power sequencing or PMIC functionality and can be configured by software for a different purpose if desired.

4 Supporting Functional Safety Systems

By using the dual TPS6594-Q1 solution to power the DRA829V or TDA4VM processor, the system can leverage the following PMIC functional safety features:

- Independent Power Control of MCU and Main Rails
- Independent Monitoring and Reset for MCU and Main Rails
- Input Supply Monitoring
- Output Voltage and Current Monitoring
- Question and Answer Watchdog
- Fault Reporting Interrupts
- Enable Drive Pin that provides an independent path to disable system actuators
- Error Pin Monitoring
- Internal Diagnostics including voltage monitoring, temperature monitoring, and Built-In Self-Test

Refer to the Safety Manual of the TPS6594-Q1 device for full descriptions and analysis of the PMIC functional safety features. These functional safety features can assist in achieving up to ASIL-D rating for a system. Additionally, these features help in achieving the functional safety assumptions utilized by the processor to achieve up to ASIL-D rating. See the DRA829/TDA4VM Safety Manual for Jacinto™ 7 Processors for a complete list of functional safety system assumptions.

4.1 Achieving ASIL-B System Requirements

To achieve a system functional safety level of ASIL-B, the following PDN features are available:

- PMIC over voltage and under voltage monitoring on the power resource voltage outputs
- PMIC over-voltage monitoring and protection on the input to the PMIC (VCCA)
- Watchdog monitoring of safety processor
- MCU error monitoring
- MCU reset
- I^2C communication
- Error indicator for driving external circuitry (optional)

The PDN has an in-line, external power FET, as shown in Figure 3-1, between the input supply and PMICs. The voltage before and after the FET is monitored by the PMIC, and the PMIC controls the FET through the OVPGDRV pin. The FET can quickly isolate the PMICs when an over-voltage event greater than 6 V is detected on the input supply to protect the system from being damaged. This includes all power rails sourced from the FET output. Any power connected upstream from the FET is not protected from over voltage events. In Figure 3-1 the load switches that supply power to the MCU and Main I/O domains, the discrete buck supplying the DDR, and the discrete LDO supplying EFUSE are all connected after the FET to extend the over voltage protection to these processor domains and discrete power resources.

The PMIC internal over voltage and under voltage monitoring and their respective monitoring threshold levels are enabled by default and can be updated through I2C after startup. PMIC power rails connected directly to the processor are monitored by default. Rails supplied through the load switches are not monitored directly. To monitor the load switch output voltage that supplies the MCU I/O of the processor, it is recommended to use the POK monitor built into the VDDSHV0_MCU voltage domain of the processor. The unused feedback pin of BUCK3 on TPS65941212-Q1, FB_B3, is assigned to monitor the VDD_DDR_1V1 voltage supplied by the external BUCK regulator. For monitoring the load switch voltage that supplies the Main I/O, an unused feedback pin of the TPS65941111- Q1 (FB_B3 or FB_B4) can be configured through I2C and connected to the output of the load switch to enable monitoring.

The internal Q&A Watchdog is enabled by default on the primary TPS6594-Q1 device. Once the device is in ACTIVE state, the trigger or Q&A watchdog settings can be configured through the secondary I2C in the device. The primary and secondary I2C CRC is not enabled by default but must be enabled with the I2C_2 trigger described in Table 6-1. Once enabled the secondary I2C is disabled for 2ms. It is recommended to enable I2C CRC and wait a minimum of 2ms before starting the Q&A Watchdog. The steps for configuring and starting the watchdog can be found in the TPS6594-Q1 datasheet. Setting the DISABLE_WDOG signal high on primary TPS6594-Q1 GPIO_8 disables the watchdog timer if this feature needs to be suspended during initial development or is not required in the system.

GPIO_7 of the primary TPS6594-Q1 PMIC is configured as the MCU error signal monitor, and must be enabled though the ESM_MCU_EN register bit. MCU reset is supported through the connection between the primary PMIC nRSTOUT pin and the MCU_PORz of the processor. Lastly, there are two I2C ports between the TPS6594-Q1 and the processor. The first is used for all non-watchdog communication, such as voltage level control, and the second allows the watchdog monitoring to be on an independent communication channel.

There is an option to use the primary TPS6594-Q1 EN_DRV pin to indicate an error has been detected and the system is entering SAFE state. This signal can be utilized if the system has some additional external circuitry that needs to be driven by an error event. In this PDN, the EN_DRV is not utilized, but still available.

4.2 Achieving up to ASIL-D System Requirements

For ASIL-C or ASIL-D systems, the following features in addition to the ones described in Section 4.1 can be used:

- PMIC current monitoring on all output power rails
- Isolation of processor MCU and Main power domains
- SoC error monitoring
- SoC reset

The current monitoring is enabled by default for all BUCKs and LDOs for the TPS6594-Q1 devices. Additionally, Figure 3-1 shows that the MCU domain of the processor is powered by different power resources of the PMICs than the main power domain of the processor. SoC error signal monitoring can be utilized if GPIO_3 of TPS65941111-Q1 is available to be reconfigured as nERR_SoC. This feature is enabled through I^2C using the ESM_SOC_EN register bit. The SoC reset functionality is supported through the connection of GPIO_11 on the primary TPS6594-Q1, configured as nRSTOUT_SoC, to the PORz pin of the processor.

Table 4-1. System Level Safety Features

ASIL-B						**ASIL-D**
Safety Monitoring Processor	External SW Wdog	External Wdog COMM & INTn	Safety MCU Processing ESM Safety MCU Reset	Safety Status Signal	System Input Voltage Monitoring	SoC Main Processing ESM SoC Main Reset
SoC: MCU Island R5 Cores	TPS65941212-Q1: Q&A Watchdog	TPS65941212-Q1: I2C2 TPS65941212-Q1 and TPS65941111-Q1: nINT	TPS65941212-Q1: nERR_MCU connected to SOC:MCU_SAFETY_ERRz TPS65941212-Q1: nRSTOUT connected to MCU_PORz_1V8	TPS65941212-Q1: ENDRV	TPS65941212-Q1: VSYS_SENSE - OV with Safety FET OVPGDRV TPS65941212-Q1 and TPS65941111-Q1 with VCCA OV & UV and SoC (VMON1) -UV	TSP65941212-Q1: nERR_MCU connected to SOC: SOC_SAFETY_ERRz TPS65941212-Q1: nRSTOUT_SOC connected to SOC_PORz_1V8

Table 4-2. Monitoring Safety Features

				ASIL-B	**ASIL-D Adds**
Device	Power Resource	PDN Power Rail	Safe State Power Group1	Supply Voltage Monitoring	Supply Current Monitoring
TPS65941212-Q1 (PMIC-A)	BUCK1-3	VDD_CPU_AVS	SOC	PMIC-A - OV & UV	PMIC-A -CM
	BUCK4	VDD_MCUIO_0V8	MCU	PMIC-A - OV & UV	PMIC-A -CM
	BUCK5	VDD_PHY_1V8	SOC	PMIC-A - OV & UV	PMIC-A -CM
	LDO1	VDD1_LPDDR4_1V8	SOC	PMIC-A - OV & UV	PMIC-A -CM2
	LDO2	VDD_MCUIO_1V8	MCU	PMIC-A - OV & UV	PMIC-A -CM
	LDO3	VDA_DLL_0V8	SOC	PMIC-A - OV & UV	PMIC-A -CM
	LDO4	VDA_MCU_1V8	MCU	PMIC-A - OV & UV	PMIC-A -CM
TPS65941111-Q1 (PMIC-B)	BUCK1-4	VDD_CORE_0V8	SOC	PMIC-B - OV & UV	PMIC-B -CM
	BUCK5	VDD_RAM_0V85	SOC	PMIC-B - OV & UV	PMIC-B -CM
	LDO1	VDD_SD_DV	SOC	PMIC-B - OV & UV	PMIC-B -CM
	LDO2	VDA_USB_3V3	SOC	PMIC-B - OV & UV	PMIC-B -CM
	LDO3	VDD_IO_1V8	SOC	PMIC-B - OV & UV	PMIC-B -CM
	LDO4	VDA_PLL_1V8	SOC	PMIC-B - OV & UV	PMIC-B -CM
TPS22965W-Q1	Ld Sw A	VDD_MCUIO_3V3	MCU	SoC (VDDSHV0_MCU) - OV & UV	NA
TPS22965W-Q1	Ld Sw B	VDD_IO_3V3	SOC	PMIC-B (FB_B4) - OV & UV7	NA3 4
TPS62813-Q1	Buck A	VDD_LPDDR4_1V1	None	PMIC-A (FB_B3) - OV & UV5	NA2
TLV73318P-Q1	LDO-A	VDD_EFUSE_1V8	None	NA6	NA6

1. Rail Group settings for the TPS65941212-Q1 and TPS65941111-Q1 are found in Table 5-7.
2. Power rails VDD_DDR_1V1 and VDD1_LPDDR4_1V8 are *safety critical* but do not required direct voltage or current monitoring since other means are available (for example, SoC internal *timeout gaskets* and *ECC checkers*) provide diagnostic coverage to detect faults in the DDR voltage.

3. Power rails VDD_IO_1V8/3V3 and VDD_GPIORET_1V8/3V3 are typically *not safety critical* since other means are available (for example, *black-channel checkers*) to provide diagnostic coverage to detect faults in SoC signaling interfaces (for example, CAN, UART, and SPI).
4. If an SoC GPIO control signal is used in a *safety critical* interface, then adding voltage and current monitoring to specific VIO power rail may be needed per customer's end product design.
5. PMIC resource, FB_B3 is used to monitor both OV and UV of VDD_DDR_1V1. This PMIC monitor is not associated with a Power group, but can be added to a group by software.
6. Power rail VPP_EFUSE_1V8 is *not safety critical* since Efuse programming does not occur during safety critical processing.
7. PMIC-B, Buck3 and 4 have unused remote sense feedback inputs that can be assigned to provide OV and UV voltage monitoring after SoC SW boot for 2x external power rails per desired functional safety needs. Optional OV/UV monitoring of VDD_DDR_1V1 and VDD_IO_3V3 power rails are examples.

5 Static NVM Settings

The TPS6594-Q1 devices consist of fixed registers and configurable registers that are loaded from the NVM. For all NVM registers, the initial NVM settings that load into the registers are provided in this section. Note: these initial NVM settings can be changed during state transitions, such as moving from STANDBY to ACTIVE mode. The register map, including default values of fixed registers, is located in the TPS6594-Q1 datasheet.

5.1 Application-Based Configuration Settings

In the TPS6594-Q1 datasheet, there are seven application-based configurations for each BUCK to operate within. The following list includes the different configurations available:

- 2.2 MHz Single Phase for DDR Termination
- 4.4 MHz VOUT Less than 1.9 V, Multiphase or High COUT Single Phase
- 4.4 MHz VOUT Less than 1.9 V, Low COUT, Single Phase Only
- 4.4 MHz VOUT Greater than 1.7 V, Single Phase Only
- 2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase
- 2.2 MHz Full VOUT Range and VIN Greater than 4.5 V, Single Phase Only
- 2.2 MHz Full VOUT and Full VIN Range, Single Phase Only

The seven configurations also have optimal output inductance values that optimize the performance of each buck under these various conditions. Table 5-1 shows the default configurations for the BUCKs. These settings cannot be changed after device startup.

Table 5-1. Application Use Case Settings

Device	BUCK Rail	Default Application Use Case	Recommended Inductor Value
TPS65941212-Q1	BUCK1	2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase	470 nH
	BUCK2	2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase	470 nH
	BUCK3	2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase	470 nH
	BUCK4	2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase	470 nH
	BUCK5	2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase	470 nH
TPS65941111-Q1	BUCK1	2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase	470 nH
	BUCK2	2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase	470 nH
	BUCK3	2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase	470 nH
	BUCK4	2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase	470 nH
	BUCK5	2.2 MHz VOUT Less than 1.9 V Multiphase or Single Phase	470 nH

5.2 Device Identification Settings

These settings are used to distinguish which device is detected in a system. These settings cannot be changed after device startup.

Table 5-2. Device Identification NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
DEV_REV	DEVICE_ID	0x82		0x82	
NVM_CODE_1	TI_NVM_ID	0x12		0x11	
NVM_CODE_2	TI_NVM_REV	0x3		0x3	
PHASE_CONFIG	MP_CONFIG	0x3	3+1+1	0x0	4+1

5.3 BUCK Settings

These settings detail the default voltages, configurations, and monitoring of the BUCK rails. All these settings can be changed though I^2C after startup.

Table 5-3. BUCK NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
BUCK1_CTRL	BUCK1_EN	0x0	Disabled; BUCK1 regulator	0x0	Disabled; BUCK1 regulator
	BUCK1_FPWM	0x0	PFM and PWM operation (AUTO mode).	0x0	PFM and PWM operation (AUTO mode).
	BUCK1_FPWM_MP	0x0	Automatic phase adding and shedding.	0x0	Automatic phase adding and shedding.
	BUCK1_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK1_VSEL	0x0	BUCK1_VOUT_1	0x0	BUCK1_VOUT_1
	BUCK1_PLDN	0x1	Enabled; Pull-down resistor	0x1	Enabled; Pull-down resistor
	BUCK1_RV_SEL	0x1	Enabled	0x1	Enabled
BUCK1_CONF	BUCK1_SLEW_RATE	0x3	5.0 mV/µs	0x3	5.0 mV/µs
	BUCK1_ILIM	0x5	5.5 A	0x5	5.5 A
BUCK2_CTRL	BUCK2_EN	0x0	Disabled; BUCK2 regulator	0x0	Disabled; BUCK2 regulator
	BUCK2_FPWM	0x0	PFM and PWM operation (AUTO mode).	0x0	PFM and PWM operation (AUTO mode).
	BUCK2_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK2_VSEL	0x0	BUCK2_VOUT_1	0x0	BUCK2_VOUT_1
	BUCK2_PLDN	0x1	Enabled; Pull-down resistor	0x1	Enabled; Pull-down resistor
	BUCK2_RV_SEL	0x1	Enabled	0x1	Enabled
BUCK2_CONF	BUCK2_SLEW_RATE	0x3	5.0 mV/µs	0x3	5.0 mV/µs
	BUCK2_ILIM	0x5	5.5 A	0x5	5.5 A
BUCK3_CTRL	BUCK3_EN	0x0	Disabled; BUCK3 regulator	0x0	Disabled; BUCK3 regulator
	BUCK3_FPWM	0x0	PFM and PWM operation (AUTO mode).	0x0	PFM and PWM operation (AUTO mode).
	BUCK3_FPWM_MP	0x0	Automatic phase adding and shedding.	0x0	Automatic phase adding and shedding.
	BUCK3_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK3_VSEL	0x0	BUCK3_VOUT_1	0x0	BUCK3_VOUT_1
	BUCK3_PLDN	0x1	Enabled; Pull-down resistor	0x1	Enabled; Pull-down resistor
	BUCK3_RV_SEL	0x0	Disabled	0x0	Disabled

Table 5-3. BUCK NVM Settings (continued)

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
BUCK3_CONF	BUCK3_SLEW_RATE	0x7	0.31 mV/µs	0x2	10 mV/µs
	BUCK3_ILIM	0x5	5.5 A	0x4	4.5 A
BUCK4_CTRL	BUCK4_EN	0x0	Disabled; BUCK4 regulator	0x0	Disabled; BUCK4 regulator
	BUCK4_FPWM	0x0	PFM and PWM operation (AUTO mode).	0x0	PFM and PWM operation (AUTO mode).
	BUCK4_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK4_VSEL	0x0	BUCK4_VOUT_1	0x0	BUCK4_VOUT_1
	BUCK4_PLDN	0x1	Enabled; Pull-down resistor	0x1	Enabled; Pull-down resistor
	BUCK4_RV_SEL	0x1	Enabled	0x0	Disabled
BUCK4_CONF	BUCK4_SLEW_RATE	0x3	5.0 mV/µs	0x2	10 mV/µs
	BUCK4_ILIM	0x5	5.5 A	0x4	4.5 A
BUCK5_CTRL	BUCK5_EN	0x0	Disabled; BUCK5 regulator	0x0	Disabled; BUCK5 regulator
	BUCK5_FPWM	0x0	PFM and PWM operation (AUTO mode).	0x0	PFM and PWM operation (AUTO mode).
	BUCK5_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK5_VSEL	0x0	BUCK5_VOUT_1	0x0	BUCK5_VOUT_1
	BUCK5_PLDN	0x1	Enable Pull-down resistor	0x1	Enable Pull-down resistor
	BUCK5_RV_SEL	0x1	Enabled	0x1	Enabled
BUCK5_CONF	BUCK5_SLEW_RATE	0x3	5.0 mV/µs	0x3	5.0 mV/µs
	BUCK5_ILIM	0x3	3.5 A	0x3	3.5 A
BUCK1_VOUT_1	BUCK1_VSET1	0x37	0.800 V	0x37	0.800 V
BUCK1_VOUT_2	BUCK1_VSET2	0x37	0.800 V	0x0	0.3 V
BUCK2_VOUT_1	BUCK2_VSET1	0x37	0.800 V	0x37	0.800 V
BUCK2_VOUT_2	BUCK2_VSET2	0x37	0.800 V	0x0	0.3 V
BUCK3_VOUT_1	BUCK3_VSET1	0x73	1.10 V	0x0	0.3 V
BUCK3_VOUT_2	BUCK3_VSET2	0x73	1.10 V	0x0	0.3 V
BUCK4_VOUT_1	BUCK4_VSET1	0x41	0.850 V	0x0	0.3 V
BUCK4_VOUT_2	BUCK4_VSET2	0x41	0.850 V	0x0	0.3 V
BUCK5_VOUT_1	BUCK5_VSET1	0xb2	1.80 V	0x41	0.850 V
BUCK5_VOUT_2	BUCK5_VSET2	0x0	0.3 V	0x0	0.3 V
BUCK1_PG_WINDOW	BUCK1_OV_THR	0x3	+5% / +50 mV	0x3	+5% / +50 mV
	BUCK1_UV_THR	0x3	-5% / -50 mV	0x3	-5% / -50 mV
BUCK2_PG_WINDOW	BUCK2_OV_THR	0x3	+5% / +50 mV	0x3	+5% / +50 mV
	BUCK2_UV_THR	0x3	-5% / -50 mV	0x3	-5% / -50 mV
BUCK3_PG_WINDOW	BUCK3_OV_THR	0x3	+5% / +50 mV	0x0	+3% / +30mV
	BUCK3_UV_THR	0x3	-5% / -50 mV	0x0	-3% / -30mV
BUCK4_PG_WINDOW	BUCK4_OV_THR	0x3	+5% / +50 mV	0x0	+3% / +30mV
	BUCK4_UV_THR	0x3	-5% / -50 mV	0x0	-3% / -30mV
BUCK5_PG_WINDOW	BUCK5_OV_THR	0x3	+5% / +50 mV	0x3	+5% / +50 mV
	BUCK5_UV_THR	0x3	-5% / -50 mV	0x3	-5% / -50 mV

5.4 LDO Settings

These settings detail the default voltages, configurations, and monitoring of the LDO rails. All these settings can be changed though I^2C after startup. Note: only TPS65941212-Q1 device contains LDO outputs.

Table 5-4. LDO NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
LDO1_CTRL	LDO1_EN	0x0	Disabled; LDO1 regulator.	0x0	Disabled; LDO1 regulator.
	LDO1_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
	LDO1_PLDN	0x1	125 Ohm	0x1	125 Ohm
	LDO1_VMON_EN	0x0	Disable OV and UV comparators.	0x0	Disable OV and UV comparators.
	LDO1_RV_SEL	0x1	Enabled	0x1	Enabled
LDO2_CTRL	LDO2_EN	0x0	Disabled; LDO2 regulator.	0x0	Disabled; LDO2 regulator.
	LDO2_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
	LDO2_PLDN	0x1	125 Ohm	0x1	125 Ohm
	LDO2_VMON_EN	0x0	Disabled; OV and UV comparators.	0x0	Disabled; OV and UV comparators.
	LDO2_RV_SEL	0x1	Enabled	0x1	Enabled
LDO3_CTRL	LDO3_EN	0x0	Disabled; LDO3 regulator.	0x0	Disabled; LDO3 regulator.
	LDO3_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
	LDO3_PLDN	0x1	125 Ohm	0x1	125 Ohm
	LDO3_VMON_EN	0x0	Disabled; OV and UV comparators.	0x0	Disabled; OV and UV comparators.
	LDO3_RV_SEL	0x1	Enabled	0x1	Enabled
LDO4_CTRL	LDO4_EN	0x0	Disabled; LDO4 regulator.	0x0	Disabled; LDO4 regulator.
	LDO4_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
	LDO4_PLDN	0x1	125 Ohm	0x1	125 Ohm
	LDO4_VMON_EN	0x0	Disabled; OV and UV comparators.	0x0	Disabled; OV and UV comparators.
	LDO4_RV_SEL	0x1	Enabled	0x1	Enabled
LDO1_VOUT	LDO1_VSET	0x1c	1.80 V	0x3a	3.30 V
	LDO1_BYPASS	0x0	Linear regulator mode.	0x1	Bypass mode.
LDO2_VOUT	LDO2_VSET	0x1c	1.80 V	0x3a	3.30 V
	LDO2_BYPASS	0x0	Linear regulator mode.	0x1	Bypass mode.
LDO3_VOUT	LDO3_VSET	0x8	0.80 V	0x1c	1.80 V
	LDO3_BYPASS	0x0	Linear regulator mode.	0x0	Linear regulator mode.
LDO4_VOUT	LDO4_VSET	0x38	1.800 V	0x38	1.800 V
LDO1_PG_WINDOW	LDO1_OV_THR	0x3	+5% / +50 mV	0x3	+5% / +50 mV
	LDO1_UV_THR	0x3	-5% / -50 mV	0x3	-5% / -50 mV

Table 5-4. LDO NVM Settings (continued)

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
LDO2_PG_WINDOW	LDO2_OV_THR	0x3	+5% / +50 mV	0x3	+5% / +50 mV
	LDO2_UV_THR	0x3	-5% / -50 mV	0x3	-5% / -50 mV
LDO3_PG_WINDOW	LDO3_OV_THR	0x3	+5% / +50 mV	0x3	+5% / +50 mV
	LDO3_UV_THR	0x3	-5% / -50 mV	0x3	-5% / -50 mV
LDO4_PG_WINDOW	LDO4_OV_THR	0x3	+5% / +50 mV	0x3	+5% / +50 mV
	LDO4_UV_THR	0x3	-5% / -50 mV	0x3	-5% / -50 mV

5.5 VCCA Settings

These settings detail the default monitoring enabled on VCCA. All these settings can be changed though I^2C after startup.

Table 5-5. VCCA NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
VCCA_VMON_CTRL	VMON_DEGLITCH_SEL	0x1	20 us	0x1	20 us
	VCCA_VMON_EN	0x1	Enabled; OV and UV comparators.	0x1	Enabled; OV and UV comparators.
VCCA_PG_WINDOW	VCCA_OV_THR	0x7	+10%	0x7	+10%
	VCCA_UV_THR	0x7	-10%	0x7	-10%
	VCCA_PG_SET	0x0	3.3 V	0x0	3.3 V
GENERAL_REG_1	FAST_VCCA_OVP	0x0	slow, 4us deglitch filter enabled	0x0	slow, 4us deglitch filter enabled
GENERAL_REG_3	LPM_EN_DISABLES_VCCA_VMON	0x1	VCCA_VMON enabled if VCCA_VMON_EN=1 and LPM_EN=0	0x1	VCCA_VMON enabled if VCCA_VMON_EN=1 and LPM_EN=0

5.6 GPIO Settings

These settings detail the default configurations of the GPIO rails. All these settings can be changed though I^2C after startup. Note that the contents of the GPIOx_SEL field determine which other fields in the GPIOx_CONF and GPIO_OUT_x registers are applicable. To understand which NVM fields apply to each GPIOx_SEL option, see the *Digital Signal Descriptions* section in TPS6594-Q1 data sheet.

Table 5-6. GPIO NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
GPIO1_CONF	GPIO1_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO1_DIR	0x0	Input	0x0	Input
	GPIO1_SEL	0x1	SCL_I2C2/CS_SPI	0x0	GPIO1
	GPIO1_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO1_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO1_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x0	No deglitch, only synchronization.

Table 5-6. GPIO NVM Settings (continued)

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
GPIO2_CONF	GPIO2_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO2_DIR	0x0	Input	0x0	Input
	GPIO2_SEL	0x2	SDA_I2C2/SDO_SPI	0x0	GPIO2
	GPIO2_PU_SEL	0x0	Pull-down resistor selected	0x1	Pull-up resistor selected
	GPIO2_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO2_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x1	8 us deglitch time.
GPIO3_CONF	GPIO3_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO3_DIR	0x1	Output	0x1	Output
	GPIO3_SEL	0x0	GPIO3	0x0	GPIO3
	GPIO3_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO3_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO3_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x0	No deglitch, only synchronization.
GPIO4_CONF	GPIO4_OD	0x0	Push-pull output	0x1	Open-drain output
	GPIO4_DIR	0x0	Input	0x1	Output
	GPIO4_SEL	0x6	LP_WKUP1	0x0	GPIO4
	GPIO4_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO4_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO4_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x0	No deglitch, only synchronization.
GPIO5_CONF	GPIO5_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO5_DIR	0x1	Output	0x0	Input
	GPIO5_SEL	0x1	SCLK_SPMI	0x1	SCLK_SPMI
	GPIO5_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO5_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO5_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x0	No deglitch, only synchronization.
GPIO6_CONF	GPIO6_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO6_DIR	0x0	Input	0x0	Input
	GPIO6_SEL	0x1	SDATA_SPMI	0x1	SDATA_SPMI
	GPIO6_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO6_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO6_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x0	No deglitch, only synchronization.
GPIO7_CONF	GPIO7_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO7_DIR	0x0	Input	0x0	Input
	GPIO7_SEL	0x1	NERR_MCU	0x0	GPIO7
	GPIO7_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO7_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO7_DEGLITCH_EN	0x1	8 us deglitch time.	0x1	8 us deglitch time.

Table 5-6. GPIO NVM Settings (continued)

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
GPIO8_CONF	GPIO8_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO8_DIR	0x0	Input	0x0	Input
	GPIO8_SEL	0x3	DISABLE_WDOG	0x0	GPIO8
	GPIO8_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO8_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO8_DEGLITCH_EN	0x1	8 us deglitch time.	0x0	No deglitch, only synchronization.
GPIO9_CONF	GPIO9_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO9_DIR	0x0	Input	0x1	Output
	GPIO9_SEL	0x0	GPIO9	0x0	GPIO9
	GPIO9_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO9_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO9_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x0	No deglitch, only synchronization.
GPIO10_CONF	GPIO10_OD	0x0	Push-pull output	0x0	Push-pull output
	GPIO10_DIR	0x0	Input	0x0	Input
	GPIO10_SEL	0x6	WKUP1	0x7	WKUP2
	GPIO10_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO10_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO10_DEGLITCH_EN	0x1	8 us deglitch time.	0x1	8 us deglitch time.
GPIO11_CONF	GPIO11_OD	0x1	Open-drain output	0x0	Push-pull output
	GPIO11_DIR	0x1	Output	0x1	Output
	GPIO11_SEL	0x2	NRSTOUT_SOC	0x0	GPIO11
	GPIO11_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	GPIO11_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO11_DEGLITCH_EN	0x0	No deglitch, only synchronization.	0x0	No deglitch, only synchronization.
NPWRON_CONF	NPWRON_SEL	0x0	ENABLE	0x0	ENABLE
	ENABLE_PU_SEL	0x0	Pull-down resistor selected	0x0	Pull-down resistor selected
	ENABLE_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.	0x1	Enabled; Pull-up/pull-down resistor.
	ENABLE_DEGLITCH_EN	0x1	8 us deglitch time when ENABLE, 50 ms deglitch time when NPWRON.	0x1	8 us deglitch time when ENABLE, 50 ms deglitch time when NPWRON.
	ENABLE_POL	0x0	Active high	0x0	Active high
	NRSTOUT_OD	0x1	Open-drain output	0x1	Open-drain output
GPIO_OUT_1	GPIO1_OUT	0x0	Low	0x0	Low
	GPIO2_OUT	0x0	Low	0x0	Low
	GPIO3_OUT	0x0	Low	0x0	Low
	GPIO4_OUT	0x0	Low	0x0	Low
	GPIO5_OUT	0x0	Low	0x0	Low
	GPIO6_OUT	0x0	Low	0x0	Low
	GPIO7_OUT	0x0	Low	0x0	Low
	GPIO8_OUT	0x0	Low	0x0	Low

Table 5-6. GPIO NVM Settings (continued)

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
GPIO_OUT_2	GPIO9_OUT	0x0	Low	0x0	Low
	GPIO10_OUT	0x0	Low	0x0	Low
	GPIO11_OUT	0x0	Low	0x0	Low

5.7 Finite State Machine (FSM) Settings

These settings describe how the PMIC output rails are assigned to various system-level states. Also, the default trigger for each system-level state is described. All these settings can be changed though I^2C after startup.

Table 5-7. FSM NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
RAIL_SEL_1	BUCK1_GRP_SEL	0x2	SOC rail group	0x2	SOC rail group
	BUCK2_GRP_SEL	0x2	SOC rail group	0x2	SOC rail group
	BUCK3_GRP_SEL	0x0	No group assigned	0x0	No group assigned
	BUCK4_GRP_SEL	0x1	MCU rail group	0x0	No group assigned
RAIL_SEL_2	BUCK5_GRP_SEL	0x2	SOC rail group	0x2	SOC rail group
	LDO1_GRP_SEL	0x1	MCU rail group	0x0	No group assigned
	LDO2_GRP_SEL	0x1	MCU rail group	0x2	SOC rail group
	LDO3_GRP_SEL	0x2	SOC rail group	0x2	SOC rail group
RAIL_SEL_3	LDO4_GRP_SEL	0x1	MCU rail group	0x2	SOC rail group
	VCCA_GRP_SEL	0x1	MCU rail group	0x1	MCU rail group
FSM_TRIG_SEL_1	MCU_RAIL_TRIG	0x2	MCU power error	0x2	MCU power error
	SOC_RAIL_TRIG	0x3	SOC power error	0x3	SOC power error
	OTHER_RAIL_TRIG	0x1	Orderly shutdown	0x1	Orderly shutdown
	SEVERE_ERR_TRIG	0x0	Immediate shutdown	0x0	Immediate shutdown
FSM_TRIG_SEL_2	MODERATE_ERR_TRIG	0x1	Orderly shutdown	0x1	Orderly shutdown

5.8 Interrupt Settings

These settings detail the default configurations for what is monitored by nINT pin. All these settings can be changed though I^2C after startup.

Table 5-8. Interrupt NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
FSM_TRIG_MASK_1	GPIO1_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO1_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO2_FSM_MASK	0x1	Masked	0x0	Not masked
	GPIO2_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO3_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO3_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO4_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO4_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'

Table 5-8. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
FSM_TRIG_MASK_2	GPIO5_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO5_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO6_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO6_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO7_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO7_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO8_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO8_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
FSM_TRIG_MASK_3	GPIO9_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO9_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO10_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO10_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
	GPIO11_FSM_MASK	0x1	Masked	0x1	Masked
	GPIO11_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'	0x0	Low; Masking sets signal value to '0'
MASK_BUCK1_2	BUCK1_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK1_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK1_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK2_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK2_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK2_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
MASK_BUCK3_4	BUCK3_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK3_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK3_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK4_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK4_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK4_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
MASK_BUCK5	BUCK5_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK5_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BUCK5_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
MASK_LDO1_2	LDO1_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	LDO1_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	LDO2_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	LDO2_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	LDO1_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	LDO2_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
MASK_LDO3_4	LDO3_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	LDO3_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	LDO4_OV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	LDO4_UV_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	LDO3_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	LDO4_ILIM_MASK	0x0	Interrupt generated	0x0	Interrupt generated

Table 5-8. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
MASK_VMON	VCCA_OV_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	VCCA_UV_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
MASK_GPIO1_8_FALL	GPIO1_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO2_FALL_MASK	0x1	Interrupt not generated.	0x0	Interrupt generated
	GPIO3_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO4_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO5_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO6_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO7_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO8_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
MASK_GPIO1_8_RISE	GPIO1_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO2_RISE_MASK	0x1	Interrupt not generated.	0x0	Interrupt generated
	GPIO3_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO4_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO5_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO6_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO7_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO8_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
MASK_GPIO9_11 / MASK_GPIO9_10	GPIO9_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO9_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO10_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO11_FALL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO10_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	GPIO11_RISE_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
MASK_STARTUP	NPWRON_START_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	ENABLE_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	FSD_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
MASK_MISC	TWARN_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	BIST_PASS_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	EXT_CLK_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
MASK_MODERATE_ERR	BIST_FAIL_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	REG_CRC_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	SPMI_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	NPWRON_LONG_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	NINT_READBACK_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	NRSTOUT_READBACK_ MASK	0x0	Interrupt generated	0x1	Interrupt not generated.
MASK_FSM_ERR	IMM_SHUTDOWN_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	MCU_PWR_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	SOC_PWR_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	ORD_SHUTDOWN_MASK	0x0	Interrupt generated	0x0	Interrupt generated

Table 5-8. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
MASK_COMM_ERR	COMM_FRM_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	COMM_CRC_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	COMM_ADR_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated
	I2C2_CRC_ERR_MASK	0x0	Interrupt generated	0x1	Interrupt not generated.
	I2C2_ADR_ERR_MASK	0x0	Interrupt generated	0x1	Interrupt not generated.
MASK_READBACK_ERR	EN_DRV_READBACK_MASK	0x0	Interrupt generated	0x1	Interrupt not generated.
	NRSTOUT_SOC_READBACK_MASK	0x0	Interrupt generated	0x1	Interrupt not generated.
MASK_ESM	ESM_SOC_PIN_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	ESM_SOC_RST_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	ESM_SOC_FAIL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	ESM_MCU_PIN_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	ESM_MCU_RST_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
	ESM_MCU_FAIL_MASK	0x1	Interrupt not generated.	0x1	Interrupt not generated.
GENERAL_REG_1	PFSM_ERR_MASK	0x0	Interrupt generated	0x0	Interrupt generated

5.9 POWERGOOD Settings

These settings detail the default configurations for what is monitored by PGOOD pin. All these settings can be changed though I^2C after startup.

Table 5-9. POWERGOOD NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
PGOOD_SEL_1	PGOOD_SEL_BUCK1	0x0	Masked	0x0	Masked
	PGOOD_SEL_BUCK2	0x0	Masked	0x0	Masked
	PGOOD_SEL_BUCK3	0x0	Masked	0x0	Masked
	PGOOD_SEL_BUCK4	0x0	Masked	0x0	Masked
PGOOD_SEL_2	PGOOD_SEL_BUCK5	0x0	Masked	0x0	Masked
PGOOD_SEL_3	PGOOD_SEL_LDO1	0x0	Masked	0x0	Masked
	PGOOD_SEL_LDO2	0x0	Masked	0x0	Masked
	PGOOD_SEL_LDO3	0x0	Masked	0x0	Masked
	PGOOD_SEL_LDO4	0x0	Masked	0x0	Masked

Table 5-9. POWERGOOD NVM Settings (continued)

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
PGOOD_SEL_4	PGOOD_SEL_VCCA	0x0	Masked	0x0	Masked
	PGOOD_SEL_TDIE_WARN	0x0	Masked	0x0	Masked
	PGOOD_SEL_NRSTOUT	0x0	Masked	0x0	Masked
	PGOOD_SEL_NRSTOUT_ SOC	0x0	Masked	0x0	Masked
	PGOOD_POL	0x0	PGOOD signal is high when monitored inputs are valid	0x0	PGOOD signal is high when monitored inputs are valid
	PGOOD_WINDOW	0x0	Only undervoltage is monitored	0x0	Only undervoltage is monitored

5.10 Miscellaneous Settings

These settings detail the default configurations of additional settings, such as spread spectrum, BUCK frequency, and LDO timeout. All these settings can be changed though I^2C after startup.

Table 5-10. Miscellaneous NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
PLL_CTRL	EXT_CLK_FREQ	0x0	1.1 MHz	0x0	1.1 MHz
CONFIG_1	TWARN_LEVEL	0x0	130C	0x0	130C
	I2C1_HS	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode controller code.	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode controller code.
	I2C2_HS	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode controller code.	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode controller code.
	EN_ILIM_FSM_CTRL	0x0	Buck/LDO regulators ILIM interrupts do not affect FSM triggers.	0x0	Buck/LDO regulators ILIM interrupts do not affect FSM triggers.
	NSLEEP1_MASK	0x0	NSLEEP1(B) affects FSM state transitions.	0x0	NSLEEP1(B) affects FSM state transitions.
	NSLEEP2_MASK	0x0	NSLEEP2(B) affects FSM state transitions.	0x0	NSLEEP2(B) affects FSM state transitions.
CONFIG_2	BB_CHARGER_EN	0x0	Disabled	0x0	Disabled
	BB_VEOC	0x0	2.5V	0x0	2.5V
	BB_ICHR	0x0	100uA	0x0	100uA
RECOV_CNT_REG_2	RECOV_CNT_THR	0xf	0xf	0xf	0xf
BUCK_RESET_REG	BUCK1_RESET	0x0	0x0	0x0	0x0
	BUCK2_RESET	0x0	0x0	0x0	0x0
	BUCK3_RESET	0x0	0x0	0x0	0x0
	BUCK4_RESET	0x0	0x0	0x0	0x0
	BUCK5_RESET	0x0	0x0	0x0	0x0
SPREAD_SPECTRUM_1	SS_EN	0x0	Spread spectrum disabled	0x0	Spread spectrum disabled
	SS_MODE	0x1	Mixed dwell	0x1	Mixed dwell
	SS_DEPTH	0x0	No modulation	0x0	No modulation
SPREAD_SPECTRUM_2	SS_PARAM1	0x7	0x7	0x7	0x7
	SS_PARAM2	0xc	0xc	0xc	0xc

Table 5-10. Miscellaneous NVM Settings (continued)

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
FREQ_SEL	BUCK1_FREQ_SEL	0x0	2.2 MHz	0x0	2.2 MHz
	BUCK2_FREQ_SEL	0x0	2.2 MHz	0x0	2.2 MHz
	BUCK3_FREQ_SEL	0x0	2.2 MHz	0x0	2.2 MHz
	BUCK4_FREQ_SEL	0x0	2.2 MHz	0x0	2.2 MHz
	BUCK5_FREQ_SEL	0x0	2.2 MHz	0x0	2.2 MHz
FSM_STEP_SIZE	PFSM_DELAY_STEP	0xb	0xb	0xb	0xb
LDO_RV_TIMEOUT_REG_1	LDO1_RV_TIMEOUT	0xf	16ms	0xf	16ms
	LDO2_RV_TIMEOUT	0xf	16ms	0xf	16ms
LDO_RV_TIMEOUT_REG_2	LDO3_RV_TIMEOUT	0xf	16ms	0xf	16ms
	LDO4_RV_TIMEOUT	0xf	16ms	0xf	16ms
USER_SPARE_REGS	USER_SPARE_1	0x0	0x0	0x0	0x0
	USER_SPARE_2	0x0	0x0	0x0	0x0
	USER_SPARE_3	0x0	0x0	0x0	0x0
	USER_SPARE_4	0x0	0x0	0x0	0x0
ESM_MCU_MODE_CFG	ESM_MCU_EN	0x0	ESM_MCU disabled.	0x0	ESM_MCU disabled.
ESM_SOC_MODE_CFG	ESM_SOC_EN	0x0	ESM_SoC disabled.	0x0	ESM_SoC disabled.
CUSTOMER_NVM_ID_REG	CUSTOMER_NVM_ID	0x0	0x0	0x0	0x0
RTC_CTRL_2	XTAL_EN	0x0	Crystal oscillator is disabled	0x0	Crystal oscillator is disabled
	LP_STANDBY_SEL	0x1	Low power standby state is used as standby state (LDOINT is disabled).	0x1	Low power standby state is used as standby state (LDOINT is disabled).
	FAST_BIST	0x0	Logic and analog BIST is run at BOOT BIST.	0x0	Logic and analog BIST is run at BOOT BIST.
	STARTUP_DEST	0x3	ACTIVE	0x3	ACTIVE
	XTAL_SEL	0x0	6 pF	0x0	6 pF
PFSM_DELAY_REG_1	PFSM_DELAY1	0x58	0x58	0x0	0x0
PFSM_DELAY_REG_2	PFSM_DELAY2	0x9d	0x9d	0x1d	0x1d
PFSM_DELAY_REG_3	PFSM_DELAY3	0x0	0x0	0x0	0x0
PFSM_DELAY_REG_4	PFSM_DELAY4	0x0	0x0	0x0	0x0

5.11 Interface Settings

These settings detail the default interface, interface configurations, and device addresses. These settings cannot be changed after device startup.

Table 5-11. Interface NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
SERIAL_IF_CONFIG	I2C_SPI_SEL	0x0	I2C	0x0	I2C
	I2C1_SPI_CRC_EN	0x0	CRC disabled	0x0	CRC disabled
	I2C2_CRC_EN	0x0	CRC disabled	0x0	CRC disabled
I2C1_ID_REG	I2C1_ID	0x48	0x48	0x4c	0x4C
I2C2_ID_REG	I2C2_ID	0x12	0x12	0x13	0x13

5.12 Multi-Device Settings

These settings detail whether the device is operating as a primary or secondary in the system. These settings cannot be changed after device startup.

Table 5-12. Multi-Device NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
SPMI_CONFIG_1	SPMI_CRC_EN	0x1	SPMI CRC check enabled	0x1	SPMI CRC check enabled
	BIT 1	0x1	Primary mode	0x0	Secondary mode
	SPMI_CLK_SEL	0x2	5MHz	0x2	5MHz
SPMI_CONFIG_2	SPMI_IF_SEL	0x0	Debug feature and uses primary logic to implement logical secondary.	0x0	Debug feature and uses primary logic to implement logical secondary.
	SPMI_RETRY_LIMIT	0x3	Three retries in case of error detected	0x3	Three retries in case of error detected
	SPMI_WD_AUTO_BOOT	0x1	SPMI auto boot enabled	0x1	SPMI auto boot enabled
	SPMI_EN	0x1	SPMI enabled	0x1	SPMI enabled
	SPMI_WD_EN	0x1	SPMI WD enabled	0x1	SPMI WD enabled
SPMI_CONFIG_3	SPMI_WD_BOOT_INTERVAL	0x8	0x8	0x8	0x8
	SPMI_WD_RUNTIME_INTERVAL	0x8	0x8	0x8	0x8
SPMI_CONFIG_4	SPMI_WD_RESPONSE_ TIMEOUT	0x8	0x8	0x8	0x8
	SPMI_PFSM_RESPONSE_ TIMEOUT	0x8	0x8	0x8	0x8
SPMI_CONFIG_5	SPMI_WD_RUNTIME_BIST_ TIMEOUT	0x8	0x8	0x8	0x8
	SPMI_WD_BOOT_BIST_ TIMEOUT	0x8	0x8	0x8	0x8
SPMI_CONFIG_6	BOOT_DELAY	0x0	0x0	0x0	0x0
SPMI_ID	SPMI_SID	0x5	0x5	0x3	0x3
	SPMI_MID	0x0	0x0	0x0	0x0

5.13 Watchdog Settings

These settings detail the default watchdog addresses. These settings can be changed though I^2C after startup.

Table 5-13. Watchdog NVM Settings

Register Name	Field Name	TPS65941212-Q1		TPS65941111-Q1	
		Value	Description	Value	Description
WD_LONGWIN_CFG	WD_LONGWIN	0xff	0xff	0xff	0xff
WD_THR_CFG	WD_EN	0x1	Watchdog enabled.	0x0	Watchdog disabled.

6 Pre-Configurable Finite State Machine (PFSM) Settings

This section describes the default PFSM settings of the TPS6594-Q1 devices. These settings cannot be changed after device startup.

6.1 Configured States

In this PDN, the PMIC devices have the following four configured power states:

- Standby
- Active
- MCU Only
- Suspend-to-RAM

In Figure 6-1, the configured PDN power states are shown, along with the transition conditions to move between the states. Additionally, the transitions to hardware states, such as SAFE RECOVERY and LP_STANDBY are shown. The hardware states are part of the Fixed Device Power Finite State Machine (FSM) and described in the TPS6594-Q1 data sheet, see Section 8.

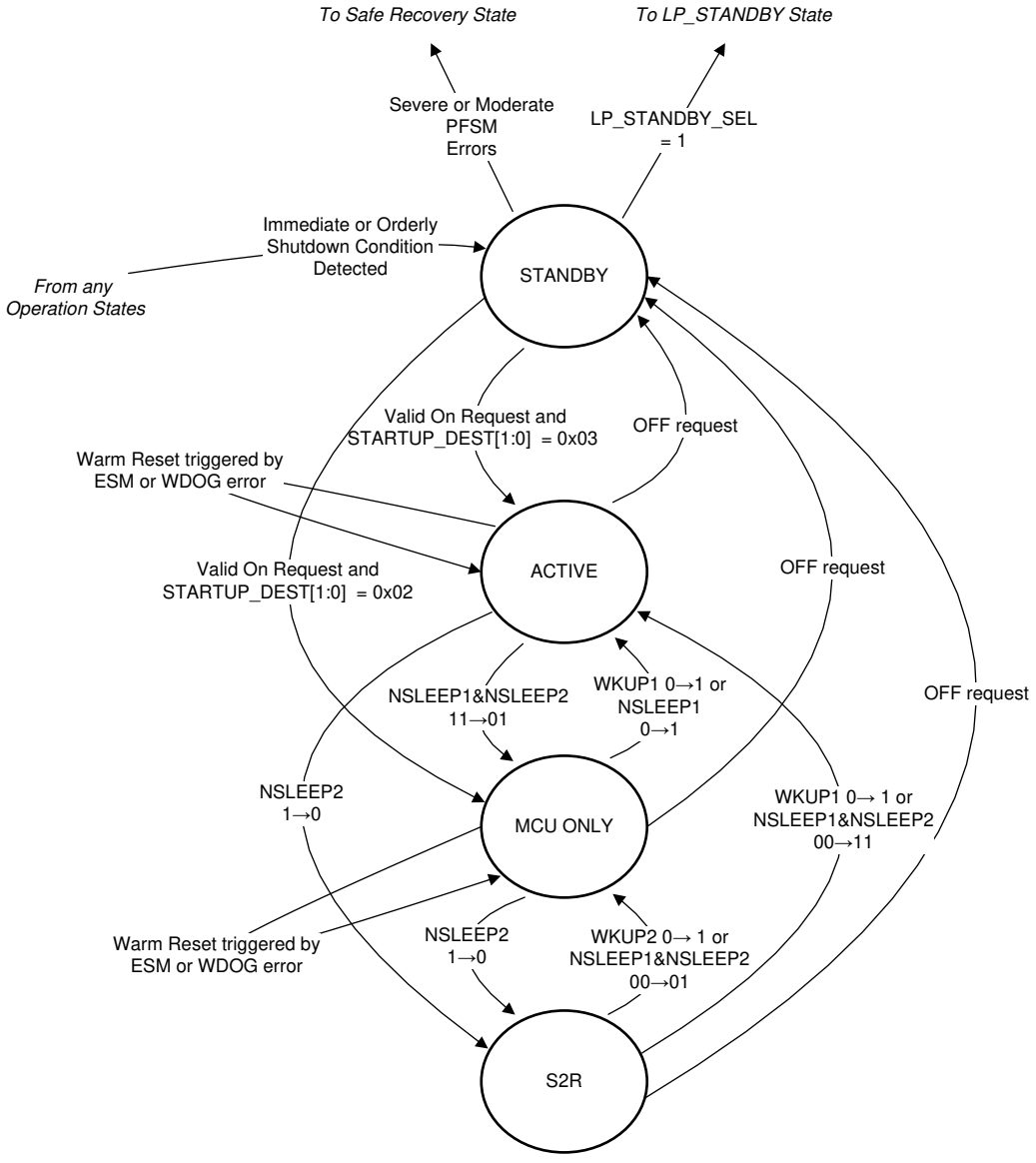

Figure 6-1. Pre-Configurable Mission Finite State Machine (PFSM) States and Transitions

When the PMICs transition from the FSM to the PFSM, several initialization instructions are performed to disable the residual voltage checks on both the BUCK and LDO regulators and set the FIRST_STARTUP_DONE bit. After these instructions are executed the PMICs wait for a valid ON Request (SU_ACTIVE trigger) before entering the ACTIVE state. The definition for each power state is described below:

STANDBY The PMICs are powered by a valid supply on the system power rail (VCCA > VCCA_UV). All device resources are powered down in the STANDBY state. EN_DRV is forced low in this state. The processor is in the Off state, no voltage domains are energized. Refer to the Section 6.3.2 sequence description.

ACTIVE The PMICs are powered by a valid supply. The PMICs are fully functional and supply power to all PDN loads. The processor has completed a recommended power up sequence with all voltage domains energized in both MCU and Main processor sections. Refer to the Section 6.3.8 sequence description.

MCU ONLY The PMICs are powered by a valid supply. Only the power resources assigned to the processor MCU rails are on. Refer to the Section 6.3.7 sequence description.

A special case of the MCU ONLY mode is when the state is entered due to an SOC power error. In this case the, the PMICs cannot transition to the ACTIVE or other states until the PMICs are intentionally moved to the MCU ONLY state by the processor. After this triggering of the TO_MCU sequence and 'reentery' into the MCU ONLY state can the PMICs transition back to the ACTIVE state.

Suspend-to-RAM (S2R) The PMICs are powered by a valid supply. Only 3 SoC voltage domains (vdds_ddr_bias, vdds_ddr, and vdds_ddr_c) remain energized while all other domains are off to minimize total system power. EN_DRV is forced low in this state. Refer to the Section 6.3.9 sequence description.

6.2 PFSM Triggers

As shown in Figure 6-1, there are various triggers that can enable a state transition between configured states. Table 6-1 describes each trigger and its associated state transition from highest priority (Immediate Shutdown) to lowest priority (I2C_3). Active triggers of higher priority block triggers of lower priority and the associated sequence.

Table 6-1. State Transition Triggers

ID	Trigger	Immediate (IMM)	REENTERANT	PFSM Current State	PFSM Destination State	Power Sequence or Function Executed
0	Immediate Shutdown	True	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	SAFE(1)	TO_SAFE_SEVERE
1	MCU Power Error	True	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	SAFE(1)	TO_SAFE
2(7)	Orderly Shutdown	True	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	SAFE(1)	TO_SAFE_ORDERLY
4	OFF Request	False	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	STANDBY(2)	TO_STANDBY
5	WDOG Error	False	True	ACTIVE	ACTIVE	ACTIVE_TO_WARM
6	ESM MCU Error	False	True	ACTIVE	ACTIVE	
7	ESM SOC Error	False	True	ACTIVE	ACTIVE	ESM_SOC_ERROR
8	WDOG Error	False	True	MCU ONLY	MCU ONLY	MCU_TO_WARM
9	ESM MCU Error	False	True	MCU ONLY	MCU ONLY	
10	SOC Power Error	False	False	ACTIVE	MCU ONLY(8)	PWR_SOC_ERR
11	I2C_1 bit is high(3)	False	True	ACTIVE, MCU ONLY	No State Change	Execute RUNTIME BIST
12	I2C_2 bit is high(3)	False	True	ACTIVE, MCU ONLY	No State Change	Enable I^2C CRC on I^2C1 and I^2C2 on all devices.(4)
13	GPIO Falling Edge(1)	False	False	ACTIVE	No State Change	TPS65941111-Q1 LDO1 output is 3.3 V in BYPASS mode

Table 6-1. State Transition Triggers (continued)

ID	Trigger	Immediate (IMM)	REENTERANT	PFSM Current State	PFSM Destination State	Power Sequence or Function Executed
14	GPIO2 Rising Edge(1)	False	False	ACTIVE	No State Change	TPS65941111-Q1 LDO1 output is 1.8 V in LDO mode
15	ON Request	False	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	ACTIVE	TO_ACTIVE
16	WKUP1 goes high	False	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	ACTIVE	
17	NSLEEP1 and NSLEEP2 are high(5)	False	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	ACTIVE	
18	MCU ON Request	False	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	MCU ONLY	TO_MCU
19	WKUP2 goes high	False	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	MCU ONLY	
20	NSLEEP1 goes low and NSLEEP2 goes high(5)	False	False	ACTIVE, MCU ONLY, Suspend-to-RAM	MCU ONLY	
21	NSLEEP1 goes low and NSLEEP2 goes low(5)	False	False	ACTIVE, MCU ONLY	Suspend-to-RAM	TO_S2R
22	NSLEEP1 goes high and NSLEEP2 goes low(5)	False	False	ACTIVE, MCU ONLY	Suspend-to-RAM	
23	I2C_0 bit goes high(3)	False	False	STANDBY, ACTIVE, MCU ONLY	STANDBY	TO_STANDBY
24	I2C_3 bit goes high(3)	False	False	ACTIVE, MCU ONLY	No State Change	Devices are prepared for OTA NVM update. (6)

(1) From the SAFE state, the PFSM automatically transitions to the hardware FSM state of SAFE_RECOVERY. From the SAFE_RECOVERY state, the recovery counter is incremented and compared to the recovery count threshold (see RECOV_CNT_REG_2, in Table 5-10). If the recovery count threshold is reached, then the PMICs halt recovery attempts and require a power cycle. Refer to the datasheet for more details.
(2) If the LP_STANDBY_SEL bit is set, then the PFSM transitions to the hardware FSM state of LP_STANDBY. When LP_STANDBY is entered, then please use the appropriate mechanism to wakeup the device as determined by the means of entering LP_STANDBY. Refer to the datasheet for more details.
(3) I2C_0, I2C_1, I2C_2 and I2C_3 are self-clearing triggers.
(4) Enabling the I^2C CRC, enables the CRC on both I2C1 and I2C2, however, the I2C2 is disabled for 2ms after the CRC is enabled. Care should be taken when using the watchdog Q&A before enabling I^2C CRC. The recommendation is to enable the I^2C CRC first, and then after 2ms, start the watchdog Q&A.
(5) NSLEEP1 and NSLEEP2 of the primary PMIC can be accessed through the GPIO pin or through a register bit. If either the register bit or the GPIO pin is pulled high, the NSLEEPx value is read as a *high* logic level.
(6) After completion of an OTA update, a reset of the PMICs is required to apply the new NVM settings.
(7) Trigger IDs 3, 25, and 26 are not described. These triggers are helper functions and transparent to the application.
(8) The PWR_SOC_ERR sequence results in the same regulator configuration as the TO_MCU sequence. However, in the event of an SOC power error the triggers to execute the TO_ACTIVE and TO_S2R sequences are masked. The processor must trigger the TO_MCU using trigger 20, as well as clearing relevant interrupts, before attempting to return to the ACTIVE state.

6.3 Power Sequences

6.3.1 TO_SAFE_SEVERE and TO_SAFE

The TO_SAFE_SEVERE and TO_SAFE are distinct sequences which occur when transition to the SAFE state. Both sequences shut down all rails without delay. The TO_SAFE_SEVERE sequence immediately ceases

BUCK switching and enables the pulldown resistors of the BUCKs and LDOs. This is to prevent any damage of the PMICs in case of over voltage on VCCA or thermal shutdown. The timing is illustrated in Figure 6-2. The TO_SAFE sequence does not reset the BUCK regulators until after the regulators are turned off as shown in Figure 6-2.

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
nRSTOUT	TPS65941212-Q1		0 us	MCU_PORZ
nRSTOUT_SOC	TPS65941212-Q1		0 us	PORZ
BUCK3 Monitor	TPS65941212-Q1		0 us	mVDDS_DDR_x
LDO3	TPS65941212-Q1		0 us	VDDA_0P8_PLLs/DLLs
BUCK1_2_3	TPS65941212-Q1		0 us	VDD_CPU (AVS)
BUCK4	TPS65941212-Q1		0 us	VDD/VDDAR_MCU
BUCK5	TPS65941212-Q1		0 us	VDDA_1P8_PHYs
LDO2	TPS65941212-Q1		0 us	VDDSHVx_MCU (1.8V)
LDO4	TPS65941212-Q1		0 us	VDDA_x
LDO1	TPS65941212-Q1		0 us	VDD1
GPIO3	TPS65941212-Q1		0 us	EN_MCU3V3IO_LDSW
GPIO3	TPS65941111-Q1		0 us	EN_DDR_BUCK
BUCK5	TPS65941111-Q1		0 us	VDDAR_CPU/CORE
LDO3	TPS65941111-Q1		0 us	VDDS_MMC0
BUCK1_2_3_4	TPS65941111-Q1		0 us	VDD_CORE/VDDA_0P8_PHYs
LDO4	TPS65941111-Q1		0 us	VDDA_1P8_PLLs
LDO1	TPS65941111-Q1		0 us	VDDSHV5
LDO2	TPS65941111-Q1		0 us	VDDA_3P3_USB
GPIO11	TPS65941111-Q1		0 us	EN_3V3IO_LDSW

Figure 6-2. TO_SAFE_SEVERE and TO_SAFE Power Sequence

After the power sequence shown in Figure 6-2, the TO_SAFE sequence delays the TPS65941212 by 16 ms and the TPS65941111 by 3 ms. This ensures that the primary PMIC finishes after the secondary. After these delays, the following instructions are executed on both PMICs:

```
//TPS65941212 and TPS65941111
// Clear AMUXOUT_EN, CLKMON_EN, set LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xE3
// Reset all BUCK regulators
REG_WRITE_MASK_IMM ADDR=0x87 DATA=0x1F MASK=0xE0
```

The TO_SAFE_SEVERE sequence executes the following instruction after the power sequence:

```
//TPS65941212 and TPS65941111
// Clear AMUXOUT_EN, CLKMON_EN, set LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xE3
```

The TPS65941212 has an additional delay of 500 ms at the end of the TO_SAFE_SEVERE sequence.

6.3.2 TO_SAFE_ORDERLY and TO_STANDBY

If a moderate error occurs, an orderly shutdown trigger is generated. The sequence following the trigger, disables the PMIC regulators using the recommended power down sequence for the processor and moves the PMICs to the SAFE_RECOVERY state.

If an OFF request occurs, such as the ENABLE pin of the primary TPS6594-Q1 device being pulled low, the same power down sequence occurs, except that the PMICs goes to STANDBY (LP_STANDBY_SEL=0) or LP_STANDBY (LP_STANDBY_SEL=1) states, rather than going to the SAFE_RECOVERY state. The power sequence for both of these events is shown in Figure 6-3.

Both the TO_SAFE_ORDERLY and TO_STANDBY sequences set the SPMI_LP_EN and FORCE_EN_DRV_LOW in the TPS65941212 while only the SPMI_LP_EN is set in the TPS65941111.

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
nRSTOUT	TPS65941212-Q1		0 us	MCU_PORZ
nRSTOUT_SOC	TPS65941212-Q1		0 us	PORZ
BUCK3 Monitor	TPS65941212-Q1		500 us	mVDDS_DDR_x
GPIO3	TPS65941111-Q1		500 us	EN_DDR_BUCK
BUCK5	TPS65941111-Q1		500 us	VDDAR_CPU/CORE
LDO3	TPS65941111-Q1		500 us	VDDS_MMC0
LDO3	TPS65941212-Q1		2500 us	VDDA_0P8_PLLs/DLLs
BUCK1_2_3	TPS65941212-Q1		2500 us	VDD_CPU(AVS)
BUCK4	TPS65941212-Q1		2500 us	VDD/VDDAR_MCU
BUCK1_2_3_4	TPS65941111-Q1		2500 us	VDD_CORE/VDDA_0P8_PHYs
BUCK5	TPS65941212-Q1		3000 us	VDDA_1P8_PHYs
LDO2	TPS65941212-Q1		3000 us	VDDSHV1_MCU
LDO4	TPS65941212-Q1		3000 us	VDDA_x
LDO1	TPS65941212-Q1		3000 us	VDD1
LDO4	TPS65941111-Q1		3000 us	VDDA_1P8_PLLs
GPIO3	TPS65941212-Q1		3500 us	EN_MCU3V3IO_LDSW
LDO1	TPS65941111-Q1		3500 us	VDDSHV5
LDO2	TPS65941111-Q1		3500 us	VDDA_3P3_USB
GPIO11	TPS65941111-Q1		3500 us	EN_3V3IO_LDSW

Figure 6-3. TO_SAFE_ORDERLY and TO_STANDBY Power Sequence

At the end of the TO_SAFE_ORDERLY both PMICs wait approximately 16 ms before executing the following instructions:

```
//TPS65941212
// Clear AMUXOUT_EN and CLKMON_EN and set LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xE3
// Reset all BUCKs
REG_WRITE_MASK_IMM ADDR=0x87 DATA=0x1F MASK=0xE0
//TPS65941111
// Clear AMUXOUT_EN and CLKMON_EN and set LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xE3
// Reset all BUCKs
REG_WRITE_MASK_IMM ADDR=0x87 DATA=0x1F MASK=0xE0
```

The resetting of the BUCK regulators is done before to transitioning to the SAFE_RECOVERY state. This means that the PMIC leaves the mission state. The SAFE_RECOVERY state is where the recovery mechanism increments the recovery counter and determine if the recovery count threshold (see Table 5-10) was achieved before attempting to recover.

At the end of the TO_STANDBY sequence, the 16 ms delay is found in the TPS65941212 device only and the same AMUXOUT_EN, CLKMON_EN, and LPM_EN bit manipulations are made in both PMICs. The BUCKs are not reset. After these instructions, the TPS65941212 performs an additional check to determine if the LP_STANDBY_SEL (see Table 5-10) is true. If true then the PMICs enters the LP_STANDBY state and leave the mission state. If the LP_STANDBY_SEL is false, then the PMICs remains in the mission state defined by STANDBY in Configured States.

6.3.3 ACTIVE_TO_WARM

The ACTIVE_TO_WARM sequence can be triggered by either a watchdog or ESM_MCU error. In the event of a trigger, the nRSTOUT and nRSTOUT_SOC signals are driven low and the recovery count (register RECOV_CNT_REG_1) increments. Then, all BUCKs and LDOs are reset to their default voltages. The PMICs remain in the ACTIVE state. Note that the GPIOs do not reset during the sequence as shown in Figure 6-4.

At the beginning of the sequence the following instructions are executed:

```
//TPS65941212
// Set FORCE_EN_DRV_LOW
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x08 MASK=0xF7
// Clear nRSTOUT and nRSTOUT_SOC
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x00 MASK=0xFC
// Increment the recovery counter
REG_WRITE_MASK_IMM ADDR=0xa5 DATA=0x01 MASK=0xFE
```

Note

The watchdog or ESM error is an indication of a significant error which has taken place outside of the PMIC. The PMIC does not actually transition through the safe recovery as with an MCU_POWER_ERR, however, in order to maintain consistency all of the regulators are returned to the values stored in NVM and the recovery counter is incremented.

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
nRSTOUT	TPS65941212-Q1		0 us	MCU_PORZ
nRSTOUT_SOC	TPS65941212-Q1		0 us	PORZ
LDO1	TPS65941212-Q1		0 us	VDD1
LDO4	TPS65941212-Q1		0 us	VDDA_x
LDO2	TPS65941212-Q1		0 us	VDDSHV1_MCU
BUCK5	TPS65941212-Q1		0 us	VDDA_1P8_PHYs
BUCK4	TPS65941212-Q1		0 us	VDD/VDDAR_MCU
BUCK1_2_3	TPS65941212-Q1		0 us	VDD_CPU(AVS)
LDO3	TPS65941212-Q1		0 us	VDDA_0P8_PLLs/DLLs
LDO2	TPS65941111-Q1		0 us	VDDA_3P3_USB
LDO1	TPS65941111-Q1		0 us	VDDSHV5
LDO4	TPS65941111-Q1		0 us	VDDA_1P8_PLLs
BUCK1_2_3_4	TPS65941111-Q1		0 us	VDD_CORE/VDDA_0P8_PHYs
LDO3	TPS65941111-Q1		0 us	VDDS_MMC0
BUCK5	TPS65941111-Q1		0 us	VDDAR_CPU/CORE
nRSTOUT	TPS65941212-Q1		2000 us	MCU_PORZ
nRSTOUT_SOC	TPS65941212-Q1		2000 us	PORZ

Figure 6-4. ACTIVE_TO_WARM Power Sequence

Note

The regulator transitions do not represent enabling of the regulators but the time at which the voltages are restored to their default values. Since this sequence originates from the ACTIVE state all of the regulators are on.

6.3.4 ESM_SOC_ERROR

In the event of an ESM_SOC error, the nRSTOUT_SOC signal is driven low and then driven high again after 200 µs. There is no change to the power rails. The sequence is shown in Figure 6-5.

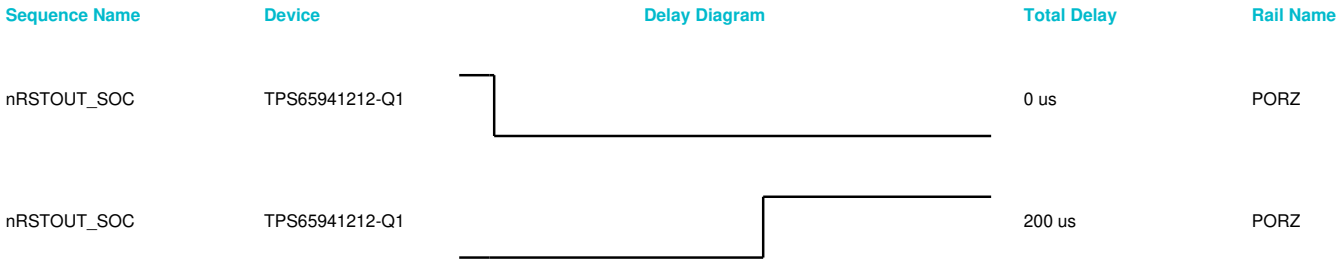

Figure 6-5. ESM_SOC_ERROR Sequence

6.3.5 PWR_SOC_ERROR

In the event of an error on any of the power rails which are part of the SOC power rail group, the PWR_SOC_ERROR sequence is performed. The nRSTOUT_SOC pin is pulled low and the SOC power rails execute a normal processor power down sequence except the MCU power group remains energized as shown in Figure 6-6. The state of the I2C_7 trigger determines whether the DDR supplies and control signal remains energized (I2C_7=1) or disabled (I2C_7=0), as shown in Figure 6-7.

In the start of the sequence the following instructions are executed:

```
// TPS65941212
// Set AMUXOUT_EN and CLKMON_EN, clear LPM_EN and nRSTOUT_SOC
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x18 MASK=0xE1
// Clear SPMI_LPM_EN
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x00 MASK=0xEF
//TPS65941111
// Set AMUXOUT_EN and CLKMON_EN, clear LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x18 MASK=0xE3
// Clear SPMI_LPM_EN
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x00 MASK=0xEF
```

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
nRSTOUT_SOC	TPS65941212-Q1		0 us	PORZ
BUCK5	TPS65941111-Q1		500 us	VDDAR_CPU/CORE
LDO3	TPS65941111-Q1		500 us	VDDS_MMC0
LDO3	TPS65941212-Q1		2500 us	VDDA_0P8_PLLs/DLLs
BUCK1_2_3_4	TPS65941111-Q1		2500 us	VDD_CORE/VDDA_0P8_PHYs
BUCK1_2_3	TPS65941212-Q1		2500 us	VDD_CPU(AVS)
BUCK5	TPS65941212-Q1		3000 us	VDDA_1P8_PHYs
LDO4	TPS65941111-Q1		3000 us	VDDA_1P8_PLLs
LDO1	TPS65941111-Q1		3500 us	VDDSHV5
LDO2	TPS65941111-Q1		3500 us	VDDA_3P3_USB

Figure 6-6. PWR_SOC_ERROR with I2C_7 High

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
nRSTOUT_SOC	TPS65941212-Q1		0 us	PORZ
BUCK3 Monitor	TPS65941212-Q1		500 us	mVDDS_DDR_x
GPIO3	TPS65941111-Q1		500 us	EN_DDR_BUCK
BUCK5	TPS65941111-Q1		500 us	VDDAR_CPU/CORE
LDO3	TPS65941111-Q1		500 us	VDDS_MMC0
LDO3	TPS65941212-Q1		2500 us	VDDA_0P8_PLLs/DLLs
BUCK1_2_3_4	TPS65941111-Q1		2500 us	VDD_CORE/VDDA_0P8_PHYs
BUCK1_2_3	TPS65941212-Q1		2500 us	VDD_CPU(AVS)
BUCK5	TPS65941212-Q1		3000 us	VDDA_1P8_PHYs
LDO4	TPS65941111-Q1		3000 us	VDDA_1P8_PLLs
LDO1	TPS65941212-Q1		3000 us	VDD1
LDO1	TPS65941111-Q1		3500 us	VDDSHV5
LDO2	TPS65941111-Q1		3500 us	VDDA_3P3_USB

Figure 6-7. PWR_SOC_ERROR with I2C_7 is Low

6.3.6 MCU_TO_WARM

The MCU_TO_WARM sequence is triggered by a WATCHDOG or ESM_MCU error. The MCU_TO_WARM, similar to the ACTIVE_TO_WARM sequence does not result in a state change. The event and sequence originate from the MCU_ONLY state and stays in the MCU_ONLY state. In the sequence, the recover counter (found in register, RECOV_CNT_REG_1) is incremented and the nRSTOUT (MCU_PORz) signal is driven low. The MCU relevant BUCK and LDOs are reset to their default voltages at the time indicated in Figure 6-8, and finally the MCU_PORz signal is set high.

Note

GPIOs do not reset during the MCU warm reset event

Also, at the beginning of the sequence the following instructions are executed to increment the recovery counter and configure the PMICs:

```
// TPS65941212
// Set FORCE_EN_DRV_LOW
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x08 MASK=0xF7
// Clear nRSTOUT
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x00 MASK=0xFE
// Increment Recovery Counter
REG_WRITE_MASK_IMM ADDR=0xa5 DATA=0x01 MASK=0xFE
```

Note

The watchdog or ESM error is an indication of a significant error which has taken place outside of the PMIC. The PMIC does not actually transition through the safe recovery as with an MCU_POWER_ERR, however, in order to maintain consistency all of the regulators are returned to the values stored in NVM and the recovery counter is incremented.

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
nRSTOUT	TPS65941212-Q1		0 us	MCU_PORZ
LDO1	TPS65941212-Q1		0 us	VDD1
LDO4	TPS65941212-Q1		0 us	VDDA_x
LDO2	TPS65941212-Q1		0 us	VDDSHV1_MCU
BUCK4	TPS65941212-Q1		0 us	VDD/VDDAR_MCU
nRSTOUT	TPS65941212-Q1		2000 us	MCU_PORZ

Figure 6-8. MCU_TO_WARM Sequence

6.3.7 TO_MCU

The TO_MCU sequence first turns off rails and GPIOs which are assigned to the SOC power group. The sequence then enables the MCU rails, in the event that they are not already active (when transitioning from STANDBY to MCU_ONLY for example). There are two cases for this sequence, based off the value stored in the I2C_7 register bit of primary TPS65941212-Q1. If the bit is low, then VDD1, EN_DDR_BUCK and mVDDS_DDR_x, are disabled; Figure 6-9. If the I2C_7 bit is high, then VDD1, EN_DDR_BUCK and mVDDS_DDR_x are enabled; Figure 6-10.

The first instructions of the TO_MCU sequence perform writes to the MISC_CTRL and ENABLE_DRV_STAT registers.

```
// TPS65941212Q1
// Set AMUXOUT_EN, CLKMON_EN
```

```
// Clear LPM_EN, NRSTOUT_SOC
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x18 MASK=0xE1
// Clear SPMI_LP_EN
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x00 MASK=0xEF
// TPS65941111Q1
// Set AMUXOUT_EN, CLKMON_EN
// Clear LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x18 MASK=0xE3
// Clear SPMI_LP_EN
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x00 MASK=0xEF
```

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
nRSTOUT_SOC	TPS65941212-Q1		0 us	PORZ
BUCK5	TPS65941111-Q1		500 us	VDDAR_CPU/CORE
LDO3	TPS65941111-Q1		500 us	VDDS_MMC0
BUCK1_2_3_4	TPS65941111-Q1		2500 us	VDD_CORE/VDDA_0P8_PHYs
LDO3	TPS65941212-Q1		2500 us	VDDA_0P8_PLLs/DLLs
BUCK1_2_3	TPS65941212-Q1		2500 us	VDD_CPU(AVS)
LDO4	TPS65941111-Q1		2500 us	VDDA_1P8_PLLs
BUCK5	TPS65941212-Q1		3000 us	VDDA_1P8_PHYs
LDO1	TPS65941111-Q1		3000 us	VDDSHV5
LDO2	TPS65941111-Q1		3000 us	VDDA_3P3_USB
GPIO11	TPS65941111-Q1		3000 us	EN_3V3IO_LDSW
GPIO3	TPS65941212-Q1		3000 us	EN_MCU3V3IO_LDSW
LDO1	TPS65941212-Q1		4700 us	VDD1
GPIO3	TPS65941111-Q1		4700 us	EN_DDR_BUCK
LDO4	TPS65941212-Q1		6400 us	VDDA_x
LDO2	TPS65941212-Q1		6400 us	VDDSHV1_MCU
BUCK4	TPS65941212-Q1		7400 us	VDD/VDDAR_MCU
BUCK3 Monitor	TPS65941212-Q1		8400 us	mVDDS_DDR_x
nRSTOUT	TPS65941212-Q1		17400 us	MCU_PORZ

Figure 6-9. TO_MCU with I2C_7 HIGH; VDD1 is Unchanged in Sequence

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
nRSTOUT_SOC	TPS65941212-Q1		0 us	PORZ
BUCK3 Monitor	TPS65941212-Q1		500 us	mVDDS_DDR_x
GPIO3	TPS65941111-Q1		500 us	EN_DDR_BUCK
BUCK5	TPS65941111-Q1		500 us	VDDAR_CPU/CORE
LDO3	TPS65941111-Q1		500 us	VDDS_MMC0
BUCK1_2_3_4	TPS65941111-Q1		2500 us	VDD_CORE/VDDA_0P8_PHYs
LDO3	TPS65941212-Q1		2500 us	VDDA_0P8_PLLs/DLLs
BUCK1_2_3	TPS65941212-Q1		2500 us	VDD_CPU(AVS)
LDO4	TPS65941111-Q1		2500 us	VDDA_1P8_PLLs
BUCK5	TPS65941212-Q1		3000 us	VDDA_1P8_PHYs
LDO1	TPS65941111-Q1		3000 us	VDDSHV5
LDO2	TPS65941111-Q1		3000 us	VDDA_3P3_USB
GPIO11	TPS65941111-Q1		3000 us	EN_3V3IO_LDSW
LDO1	TPS65941212-Q1		3000 us	VDD1
GPIO3	TPS65941212-Q1		3000 us	EN_MCU3V3IO_LDSW
LDO4	TPS65941212-Q1		6400 us	VDDA_x
LDO2	TPS65941212-Q1		6400 us	VDDSHV1_MCU
BUCK4	TPS65941212-Q1		7400 us	VDD/VDDAR_MCU
nRSTOUT	TPS65941212-Q1		17400 us	MCU_PORZ

Figure 6-10. TO_MCU with I2C_7 LOW, VDD1 is Disabled in Sequence

The last instructions of the TO_MCU sequence also perform writes to the MISC_CTRL and ENABLE_DRV_STAT registers after the delay defined in the PFSM_DELAY_REG_1.

```
// TPS65941212Q1
SREG_READ_REG ADDR=0xCD REG=R1
DELAY_SREG R1
// Clear SPMI_LPM_EN and FORCE_EN_DRV_LOW
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x00 MASK=0xE7
// Set NRSTOUT (MCU_PORZ)
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x01 MASK=0xFE
```

6.3.8 TO_ACTIVE

When a trigger causes the TO_ACTIVE sequence to execute, all rails of the PMICs power up in the recommended processor power up sequence as shown in Figure 6-11.

At the beginning of the TO_ACTIVE sequence both PMICs clear SPMI_LP_EN and LPM_EN and set AMUXOUT_EN and CLKMON_EN.

Note

BUCK3 Monitor, mVDDS_DDR_X, monitors the external regulator controlled by GPIO3, EN_DDR_BUCK. Although these occur at the same time, the analog BIST, which first checks the actual voltage being monitored, occurs approximately 3.7 ms after the monitor is enabled. This is a function of the voltage and slew rate of BUCK3 as described in Table 5-3.

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
GPIO3	TPS65941212-Q1		0 us	EN_MCU3V3IO_LDSW
GPIO11	TPS65941111-Q1		0 us	EN_3V3IO_LDSW
LDO2	TPS65941111-Q1		0 us	VDDA_3P3_USB
LDO1	TPS65941111-Q1		0 us	VDDSHV5
LDO1	TPS65941212-Q1		1700 us	VDD1
LDO4	TPS65941212-Q1		1700 us	VDDA_x
LDO2	TPS65941212-Q1		1700 us	VDDSHV1_MCU
BUCK5	TPS65941212-Q1		1700 us	VDDA_1P8_PHYs
LDO4	TPS65941111-Q1		1700 us	VDDA_1P8_PLLs
BUCK4	TPS65941212-Q1		2700 us	VDD/VDDAR_MCU
BUCK1_2_3	TPS65941212-Q1		2700 us	VDD_CPU(AVS)
LDO3	TPS65941212-Q1		2700 us	VDDA_0P8_PLLs/DLLs
BUCK1_2_3_4	TPS65941111-Q1		2700 us	VDD_CORE/VDDA_0P8_PHYs
BUCK3 Monitor	TPS65941212-Q1		3700 us	mVDDS_DDR_x
LDO3	TPS65941111-Q1		3700 us	VDDS_MMC0
BUCK5	TPS65941111-Q1		3700 us	VDDAR_CPU/CORE
GPIO3	TPS65941111-Q1		3700 us	EN_DDR_BUCK
nRSTOUT	TPS65941212-Q1		12700 us	MCU_PORZ
nRSTOUT_SOC	TPS65941212-Q1		12700 us	PORZ

Figure 6-11. TO_ACTIVE Sequence

6.3.9 To Suspend-to-RAM (TO_S2R)

The C and D triggers, defined by the NSLEEPx bits or pins, trigger the S2R sequence. This sequence disables all power rails and GPIOs that are not supplying the retention rails, as described in Table 3-1. The sequence can be modified using the I2C_7 bit found in register FSM_I2C_TRIGGERS. These bits need to be set by I2C in both PMICs before a trigger for the retention state occurs. If the I2C_7 bit is set high in both PMICs, they enter the DDR retention state as shown in . The BUCK3 Monitor (mVDDS_DDR_x) as well as the LDO1 (VDD1) are not disabled and the GPIO3 of the TPS6591111 (EN_DDR_BUCK) is also unchanged. If I2C_7 is set low, these components associated with DDR do not remain active, as shown in Figure 6-12.

Note

The I2C_7 bits need to be set or cleared by I2C in both PMICs before a trigger to the retention state occurs. The I2C_7 trigger is not self-clearing and need to be updated manually.

The following instructions are used to configure the PMICs at the beginning of the sequence:

```
// TPS65941212
// Set LPM_EN, Clear NRSTOUT_SOC and NRSTOUT
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xF8
// Set SPMI_LP_EN and FORCE_EN_DRV_LOW
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x18 MASK=0xE7
//TPS6594l111
// Set SPMI_LP_EN
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x10 MASK=0xEF
```

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
nRSTOUT	TPS65941212-Q1		0 us	MCU_PORZ
nRSTOUT_SOC	TPS65941212-Q1		0 us	PORZ
BUCK3 Monitor	TPS65941212-Q1		500 us	mVDDS_DDR_x
GPIO3	TPS65941111-Q1		500 us	EN_DDR_BUCK
BUCK5	TPS65941111-Q1		500 us	VDDAR_CPU/CORE
LDO3	TPS65941111-Q1		500 us	VDDS_MMC0
LDO3	TPS65941212-Q1		2500 us	VDDA_0P8_PLLs/DLLs
BUCK1_2_3	TPS65941212-Q1		2500 us	VDD_CPU(AVS)
BUCK4	TPS65941212-Q1		2500 us	VDD/VDDAR_MCU
BUCK1_2_3_4	TPS65941111-Q1		2500 us	VDD_CORE/VDDA_0P8_PHYs
BUCK5	TPS65941212-Q1		3000 us	VDDA_1P8_PHYs
LDO2	TPS65941212-Q1		3000 us	VDDSHV1_MCU
LDO4	TPS65941212-Q1		3000 us	VDDA_x
LDO4	TPS65941111-Q1		3000 us	VDDA_1P8_PLLs
LDO1	TPS65941212-Q1		3000 us	VDD1
LDO1	TPS65941111-Q1		3500 us	VDDSHV5
LDO2	TPS65941111-Q1		3500 us	VDDA_3P3_USB
GPIO11	TPS65941111-Q1		3500 us	EN_3V3IO_LDSW
GPIO3	TPS65941212-Q1		3500 us	EN_MCU3V3IO_LDSW

Figure 6-12. TO_S2R and I2C_7 is Low on Both PMICs

Sequence Name	Device	Delay Diagram	Total Delay	Rail Name
nRSTOUT	TPS65941212-Q1		0 us	MCU_PORZ
nRSTOUT_SOC	TPS65941212-Q1		0 us	PORZ
BUCK5	TPS65941111-Q1		500 us	VDDAR_CPU/CORE
LDO3	TPS65941111-Q1		500 us	VDDS_MMC0
LDO3	TPS65941212-Q1		2500 us	VDDA_0P8_PLLs/DLLs
BUCK1_2_3	TPS65941212-Q1		2500 us	VDD_CPU(AVS)
BUCK4	TPS65941212-Q1		2500 us	VDD/VDDAR_MCU
BUCK1_2_3_4	TPS65941111-Q1		2500 us	VDD_CORE/VDDA_0P8_PHYs
BUCK5	TPS65941212-Q1		3000 us	VDDA_1P8_PHYs
LDO2	TPS65941212-Q1		3000 us	VDDSHV1_MCU
LDO4	TPS65941212-Q1		3000 us	VDDA_x
LDO4	TPS65941111-Q1		3000 us	VDDA_1P8_PLLs
LDO1	TPS65941111-Q1		3500 us	VDDSHV5
LDO2	TPS65941111-Q1		3500 us	VDDA_3P3_USB
GPIO11	TPS65941111-Q1		3500 us	EN_3V3IO_LDSW
GPIO3	TPS65941212-Q1		3500 us	EN_MCU3V3IO_LDSW

Figure 6-13. To S2R and I2C_7 is High in Both PMICs

At the end of the sequence, both PMICs set the LPM_EN and clear the CLKMON_EN and AMUXOUT_EN. The TPS65941212 device also performs an additional 16 ms delay based upon the contents of the register (PFSM_DELAY_REG_2) to ensure that the TPS65941212 sequence finishes last.

7 Impact of NVM Changes

Table 7-1. NVM Changes from revision 2 to revison 3

Change	Impact of change
Update NVM revision to 3, see Table 5-2.	None.
VCCA overvoltage and undervoltage monitors are masked in the static configuration, see Table 5-8.	None. The monitors are unmasked in the PFSM once the enable pin goes high.
BUCK and LDO overvoltage and undervoltage monitors are masked before the monitor is transitioned from the disabled to the enabled state. The corresponding monitors are unmasked just before release of the nRSTOUT/nRSTOUT_SOC.	None. These instructions are performed during the power sequences and have no impact on the timing. Additionally, the monitors are unmasked before the system can perform safety relevant functions.
Logic and analog BIST is run at BOOT BIST, see Table 5-10.	BIST time is extended to include the logic BIST.
For the TPS65941111, the readback interrupt for the nINT pin is unmasked. Table 5-8	In the event of a readback error on the nINT pin, a MODERATE_ERR_INT occurs resulting in the transition to SAFE_RECOVERY.

8 References

For additional information regarding the PMIC or processor devices, use the following:

- Texas Instruments, *TPS65941213-Q1 and TPS65941111-Q1 User Guide for Jacinto™ 7 DRA829 and TDA4VM PDN-0C*
- Texas Instruments, *DRA829 Jacinto™ Processors Silicon Revisions 1.0 and 1.1* data sheet
- Texas Instruments, DRA829 Safety Manual Jacinto™ 7 Processors (request through mySecure)
- Texas Instruments, *DRA829/TDA4VM/AM752x Technical Reference Manual (Rev. B)* reference model
- Texas Instruments, *TPS6594-Q1 Power Management IC (PMIC) with 5 Bucks and 4 LDOs for Safety-Relevant Automotive Applications* data sheet
- Texas Instruments, TPS6594-Q1 Safety Manual (request through mySecure)
- Texas Instruments, *TPS6594-Q1 Schematic PCB Checklist* application note

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2022) to Revision B (February 2022)	Page
• Updated title	0
• Updated abstract	1

Changes from Revision * (June 2021) to Revision A (January 2022)	Page
• Changed all instances of legacy terminology to controller and peripheral where I^2C is mentioned	1
• Changed all instances of legacy terminology to primary and secondary where SPMI is mentioned	1
• Updated NVM revision	2
• Updated Power Connections figure	4
• Updated PDN Power Mapping and System Features table	4
• Included description of impact to the I2C2 in the event that the I2C CRC is enabled	11
• Added TPS65941111-Q1 nINT in System Level Safety Feastures Table	11
• Updated Device ID NVM settings	14
• Added FAST_VCCA_OVP and LPM_EN_DISABLES_VCCA_VMON	17
• Updated Interrupt Settings for nINT readback and VCCA over-voltage and undervoltage	20
• Updated location of NINT_READBACK_MASK, NRSTOUT_READBACK_MASK, and PFSM_ERR_MASK.	20
• Updated FAST_BIST	24
• Added CUSTOMER_NVM_ID_REG	24
• Added note to State Transition Triggers for I2C_2	28
• Added Section 7	49
• Added reference to PDN-0C	50

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265