User's Guide

TPS629210-Q1EVM User's Guide

ABSTRACT

The TPS629210-Q1EVM is designed to help user easily evaluate the performance of the TPS629210-Q1. The user's guide includes the performance characteristics, EVM configuration, test setup, test result, PCB layout, schematic diagram and a bill of materials.

Table of Contents

Trademarks

1 Introduction

TPS629210-Q1 is a high efficiency and high flexible synchronous step-down buck converter in a small 1.6 × 2.1 mm SOT583 package. TPS629210-Q1 can be configured to run at 2.5 MHz or 1 MHz in either forced PWM mode or auto PFM mode. In 2.5-MHz auto PFM mode, TI AEE™ mode automatically adjusts the switching frequency based on both input and output voltage to hold a high efficiency through the whole operation range without the need of using different inductors. The device includes a smart-Config/Mode input to select different combinations of external/internal feedback dividers, max switching frequencies, output discharge enable/disable and auto PFM/forced PWM operations.

2 Performance Specification

Table as below provides a summary of TPS629210-Q1EVM performance specifications. All the specifications are given for an ambient temperature of 25°C.

Table 2-1. EVM Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	UNIT
Input Voltage		3	12	17	V
Output Voltage			3.3		V
Output Current		0		1	A
Input Current	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, Forced PWM, 2.5 MHz		6.1		mA
	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, Forced PWM, 2.5 MHz		0.307		A
Switching frequency	Set by Mode/S-CONF pin		2.5		MHz
Line Regulation	V_{IN} = 5 V–17 V, V_{OUT}= 3.3 V, I_{OUT} = 1 A, Forced PWM, 2.5 MHz		+/-0.15		%
Load Regulation	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A–1 A, Forced PWM and Auto PFM with AEE, 2.5 MHz		+/-0.15		%
Output Ripple	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, Forced PWM, 2.5 MHz		10.6		mV
Peak Efficiency	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A–1 A, Forced PWM, 2.5 MHz		90.8		%
	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A–1 A, Auto PFM/PWM with AEE, 2.5 MHz		91.2		%
	V_{IN} = 12 V, V_{OUT} = 3.3 V,I_{OUT} = 10 mA, Auto PFM/PWM with AEE, 2.5 MHz		87.11		%
Output Rise time	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, Forced PWM, 2.5 MHz		520		us
Load Transient	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0.5 A–1 A, Slew rate: 1 A/us, Forced PWM, Internal FB, 2.5 MHz		+/-42		mV
Loop Bandwidth	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, Forced PWM, Internal FB,2.5 MHz		139		kHz
Phase Margin	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, Forced PWM, Internal FB, 2.5 MHz		86		deg
IC case temperature	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, Forced PWM, 2.5 MHz, 10 minutes soaking		34.5		°C

3 EVM Configuration and Modification

The EVM is designed to provide access to features of TPE629210-Q1. The EVM also provides jumpers for different configurations. Jumper selections must be made prior to enabling the TPS629120-Q1. Additional input and output capacitors can be added. The input voltage at which the IC turns on can be programmed with a voltage divider. The TPS629210-Q1EVM allows multiple MODE/S-CONF pin configurations for switching frequency, auto PFM/PWM with AEE, forced PWM and output discharge setting as well as internal and external feedback options. The loop response can also be measured.

3.1 Input and Output Capacitors

C2 is provided for additional input capacitance. This capacitor is not required for proper operation but can be used to reduce the input voltage ripple. C6, C7, C8, and C9 are provided for additional output capacitors. These capacitors are not required for proper operation but can be used to reduce the output voltage ripple. The total output capacitance must remain within the recommended range in the TPS629210-Q1.

3.2 Configurable Enable Threshold Voltage

JP1 is provided as option for Enable pin with precise threshold voltage. R4 and R5 can be adjusted to set a user-selectable input voltage at which the IC turns on. The EVM pre-configured R4 and R5 to have 6.5-V rising and 5.85-V falling threshold voltage.

3.3 MODE/S-CONF Setting

JP2 is used to set different MODE/S-CONF configurations. MODE/S-CONF can be connected to VIN and GND as a traditional HIGH or LOW level. R6 and R7 select the other device configurations including internal/external feedback, switching frequency, output discharge, Auto PFM or Forced PWM options. The values of R6 and R7 can be changed per user's requirement.

- While using the internal feedback (VSET) configuration for the output voltage setting, either float the FB pin by cutting the net tie (NT1) included on the back of the board or remove both R1 and R2 for 3.3-V output voltage. Other output voltage can be programmed by removing R1 and changing the value of R2. Ensure the JP2 jumper is removed for proper operation with internal feedback.

  WARNING
  Ensure not to set the MODE pin for external feedback if either the net tie (NT1) is cut or R1 and R2 are removed. This could cause damage to the device due to lack of external feedback control.

- Dynamic mode option is an advance feature which allows MODE pin to actively switch between Forced PWM and Auto PFM/PWM during operation, but this is only possible by driving the mode pin between Vin and GND. This feature provides user with the option of controlling when/if the device enters power save mode (DCM).

3.4 Power Good

JP3 is provided as an option for power good test point. If power good is not used, it is recommended to tie to GND or leave open.

3.5 Power Good Pull Up Voltage

JP4 is provided as an option for power good pull up voltage. Either V_{IN} or V_{OUT} with 100-kΩ pull up resistor.

3.6 Feedforward Capacitor Option

C10 is provided as an optional of feedforward capacitor (Cff). It helps to improve the loop stability if needed. More detailed discussion on the optimization for stability versus transient response can be found in Optimizing Transient Response of Internally Compensated dc-dc Converter With Feedforward Capacitor and Feedforward Capacitor to Improve Stability and Bandwidth With the TPS621-Family and TPS821-Family.

3.7 Output Voltage Setting

The TPS629210-Q1EVM is configured for external feedback as default with an output voltage of 3.3 V set by R1 and R2. Additionally, if the internal feedback (VSET) configuration is used, the user can cut net tie NT1 located on the back of the board. This modification is shown in Figure 3-1. This will float the FB pin resulting in a 3.3-V

output voltage using the internal VSET. Resistors R1 and R2 can also be changed to set the output voltage between 0.6 V and 5.5 V. See the TPS629210 data sheet for recommended values. R2 was populated with 34 k such that if the internal (VSET) is chosen while R1 is removed, the device will regulate to 1.8-V output voltage.

WARNING

If the output voltage is increased, make sure the voltage rating of output capacitor C5 is sized appropriately.

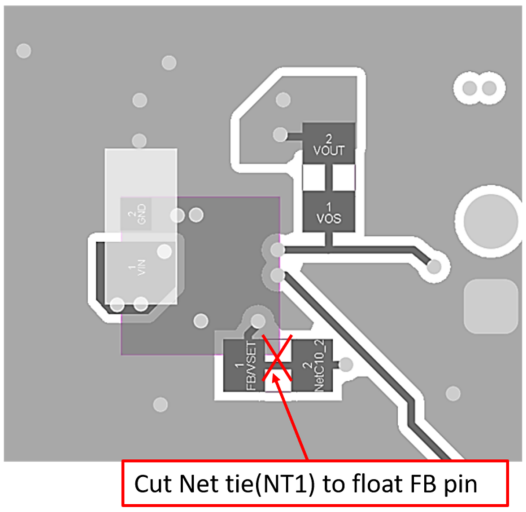

Figure 3-1. Internal feedback (VSET) Configuration Board Modification

3.8 Loop Response Measurement

The loop response can be measured after simple changing to the board. First, cut net tie (NT2) and install a 10-Ω 0603 resistor on the bottom of board. The change is show as below. An AC signal (10-mV, peak-to-peak amplitude recommended) can be injected into the control loop across the added 10-Ω resistor.

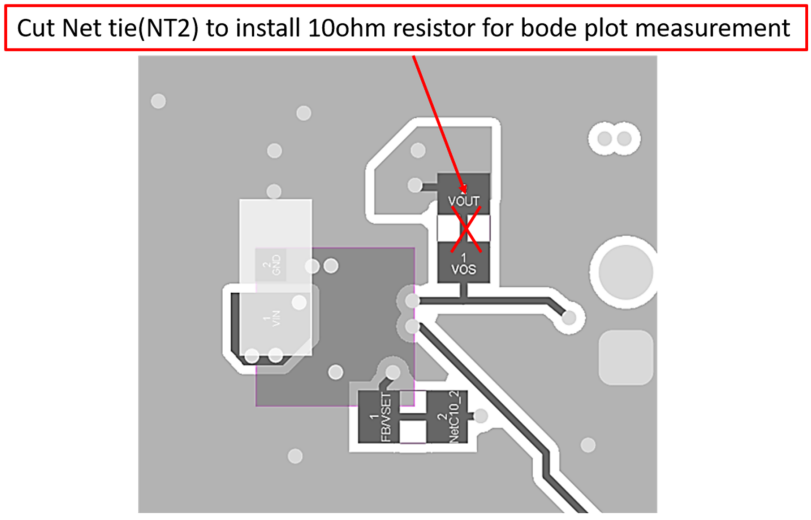

Figure 3-2. Bode Plot Measurement Board Modification

4 EVM Test Set Up

This section describes how to properly test the EVM

4.1 Input and Output Connectors

Table 4-1. Input and Output Connector

Connector	Pins	Description
J1	Pin1 and Pin2	V_{IN} positive input for input supply.
	Pin3 and Pin4	S+ and S- input voltage sense. Input voltage measure point.
	Pin5 and Pin6	GND return for input supply.
J2	Pin1 and Pin2	V_{OUT} Output voltage connection.
	Pin3 and Pin4	S+ and S- output voltage sense. Output voltage measure point.
	Pin5 and Pin6	GND Output return connection.

4.2 Jumper Configuration

4.2.1 JP1 Enable

Table 4-2. Enable Pin Configuration

Jumper Short Location	Description
Pin2 and Pin3	Turn on device
Pin3 and Pin4	Turn off device as default
Pin1 and Pin2, Pin3 and Pin4	Set programmable Enable threshold voltage with R4 and R5
Pin3 and Pin4	Pin1 can be used for external supply voltage with R4 and R5 resistor divider

4.2.2 JP2 MODE/S-CONF

Table 4-3. MODE/S-CONF Pin Configuration

Jumper Short Location	Description
Pin1 and Pin3	Forced PWM, 2.5 MHz, external FB, output discharge enabled
Pin3 and Pin5	Auto PFM/PWM with AEE, 2.5 MHz. external FB, output discharge enabled
Pin2 and Pin4	52.3 k to GND, forced PWM, 2.5 MHz, internal FB (VSET), output discharge disabled
Pin4 and Pin6	42.2 k to GND, auto PFM/PWM with AEE, 2.5 MHz, internal FB(VSET), output discharge disabled

4.2.3 JP3 Power Good

The PGOOD output is on pin 1 of this header with a convenient ground on pin 2. If PG is not used, short pin1 and pin2 by a jumper

4.2.4 JP4 PG Pull Up Voltage

Table 4-4. PG pull Up Voltage Option

Jumper Short Location	Description
Pin1 and Pin2	PG pulls up to output voltage.
Pin2 and Pin3	PG pulls up to input voltage.
No jumper	JP4 pin2 can pull up to different external voltage. This external voltage must remain below 18 V.

5 Test Results

This section provides the test results of TPS629210-Q1EVM.

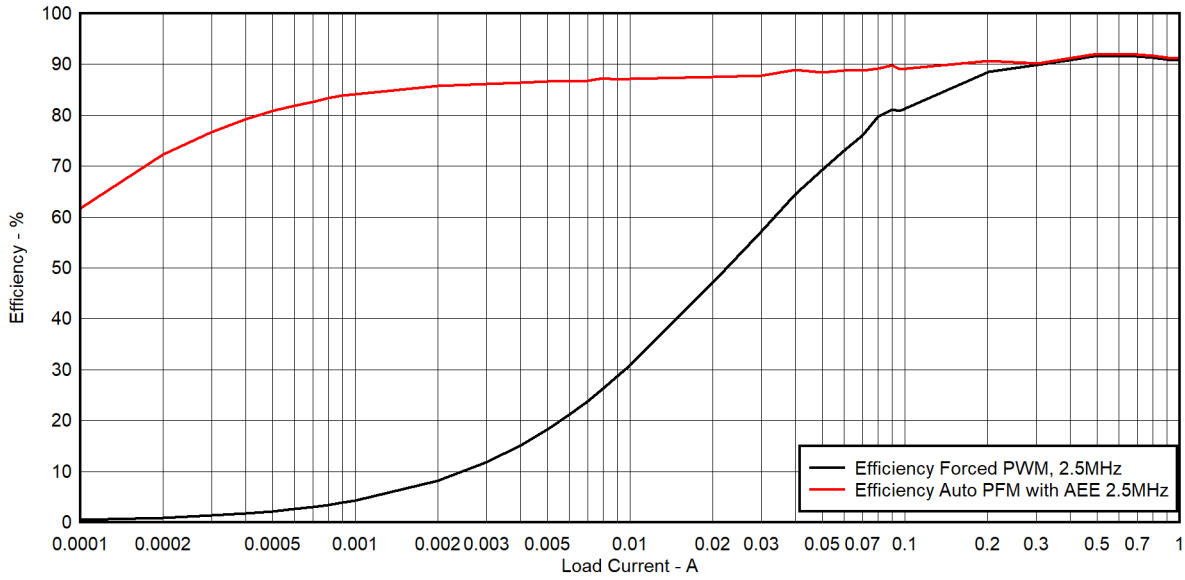

Figure 5-1. Efficiency V_{IN}= 12 V V_{OUT} = 3.3 V F_{SW}=2.5 MHz

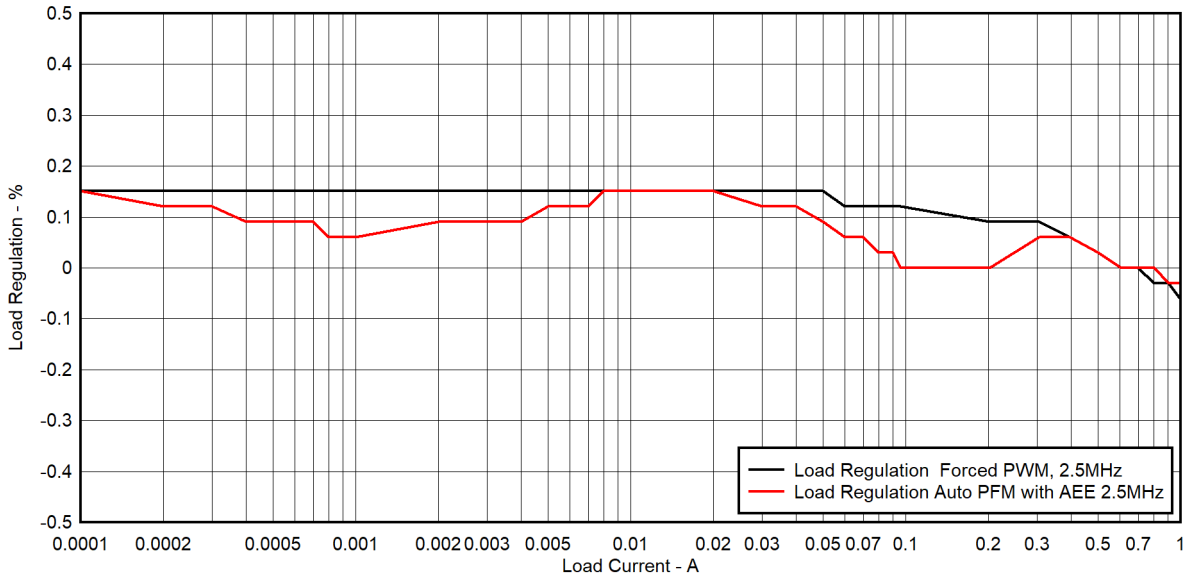

Figure 5-2. Load Regulation V_{IN} = 12 V V_{OUT} = 3.3 V F_{SW}=2.5 MHz

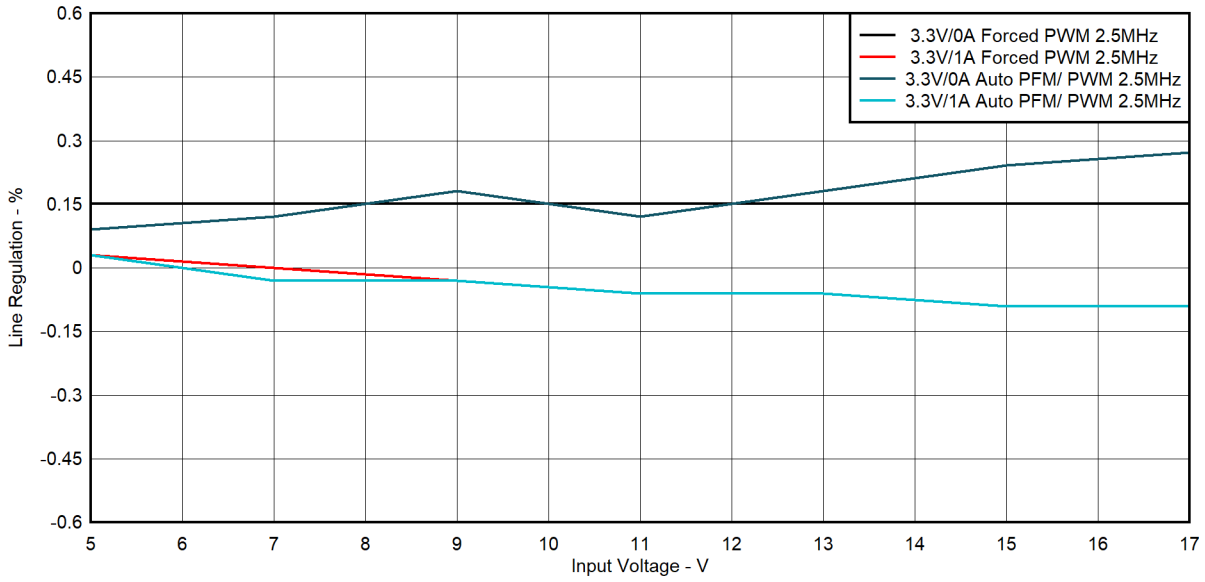

Figure 5-3. Line Regulation V_{IN} = 5 V–17 V V_{OUT} = 3.3 V I_{OUT} = 0 A and 1 A

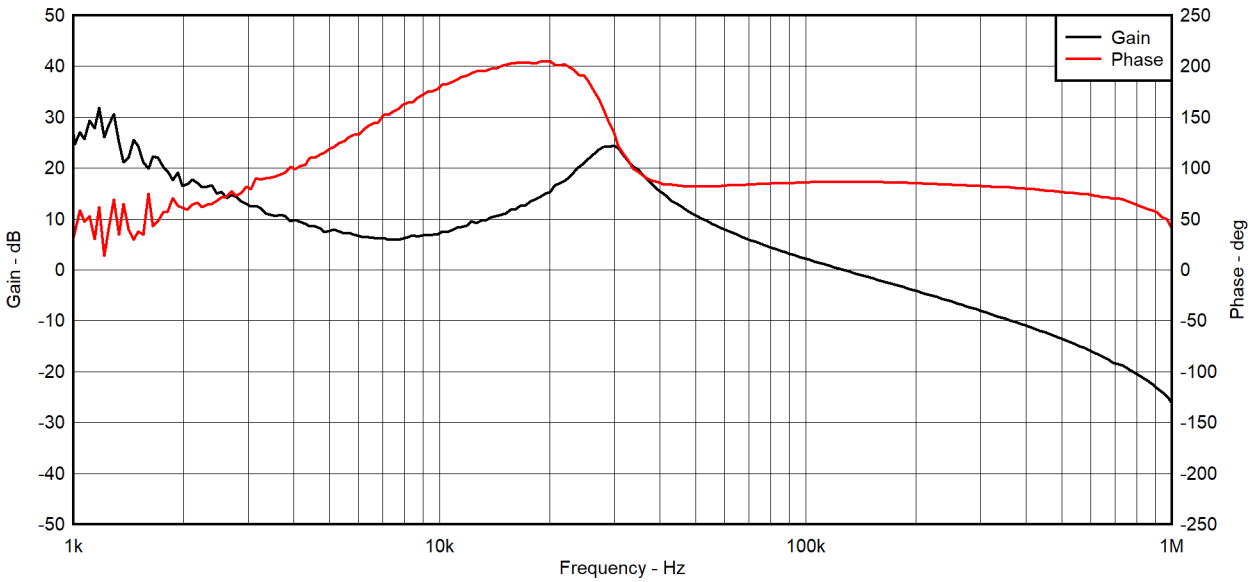

Figure 5-4. Loop Response Forced PWM Internal FB (VSET) V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 1 A

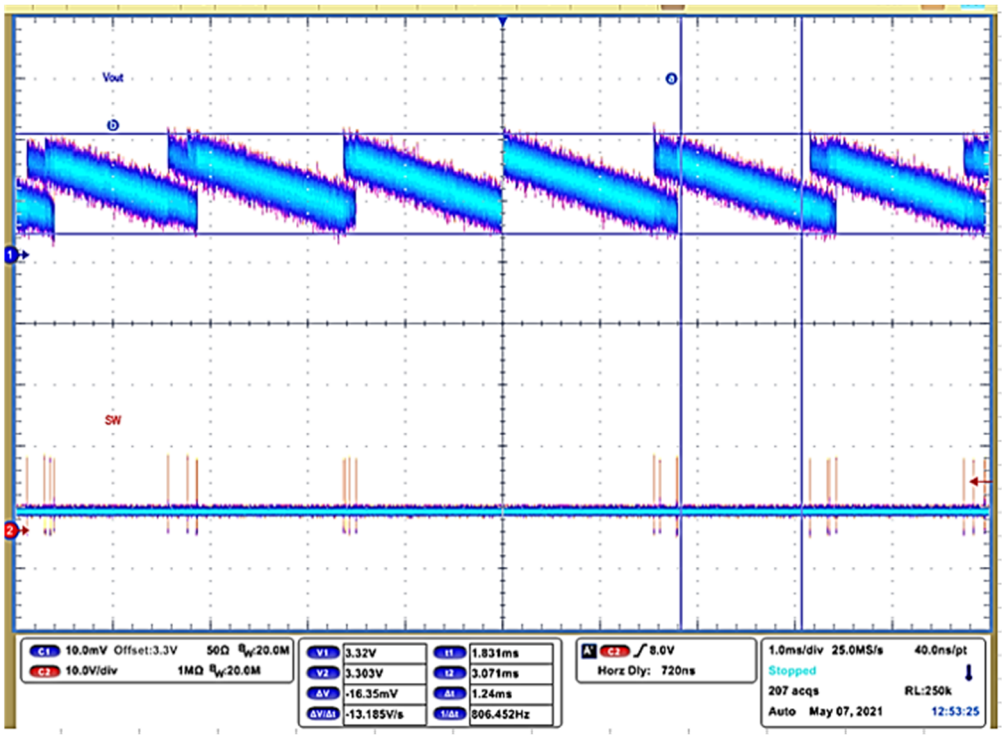

Figure 5-5. Output Voltage Ripple Auto PFM V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 0 A

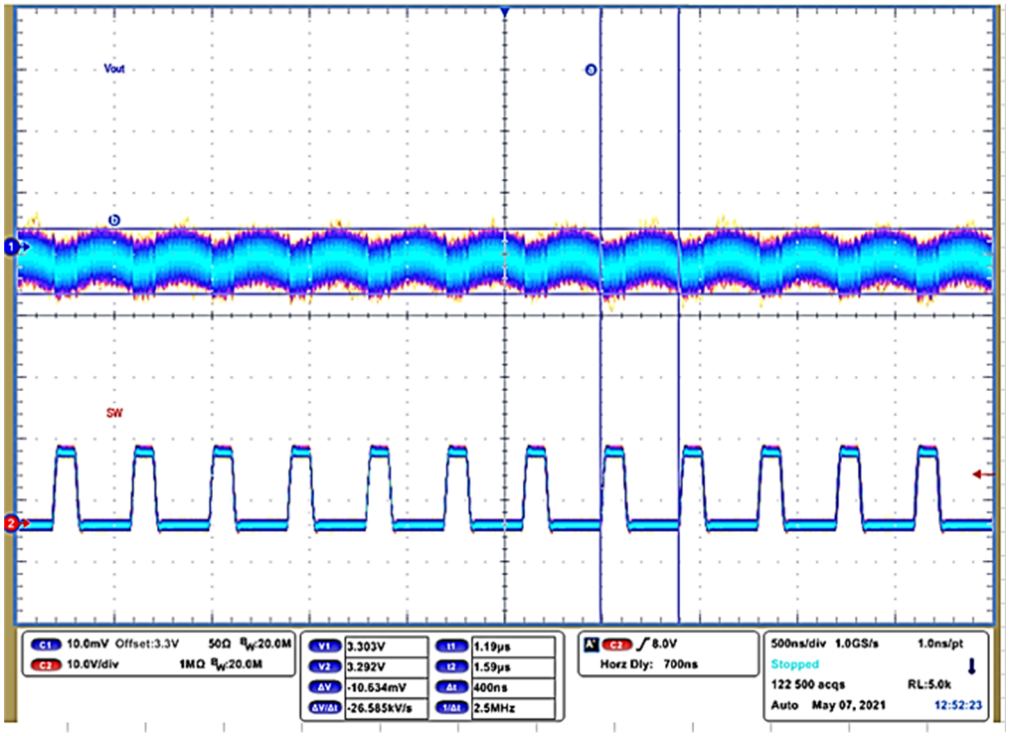

Figure 5-6. Output Voltage Ripple Forced PWM V_{IN} = 12 V, V_{OUT} = 3.3 V I_{OUT} = 1 A

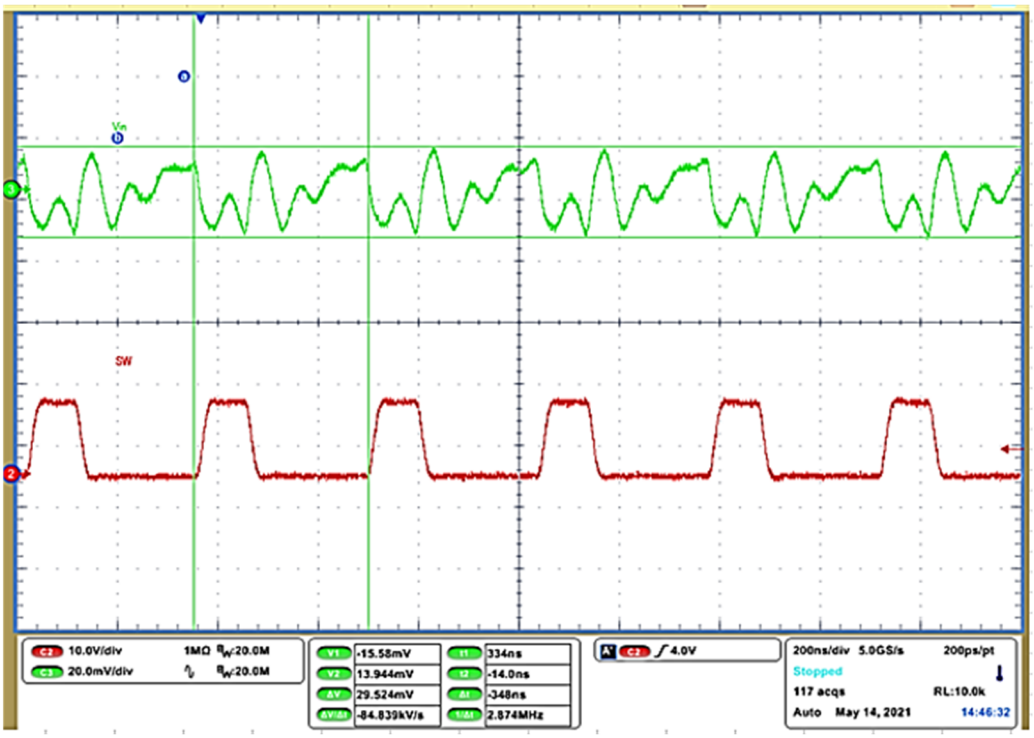

Figure 5-7. Input Voltage Ripple Forced PWM V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 1 A

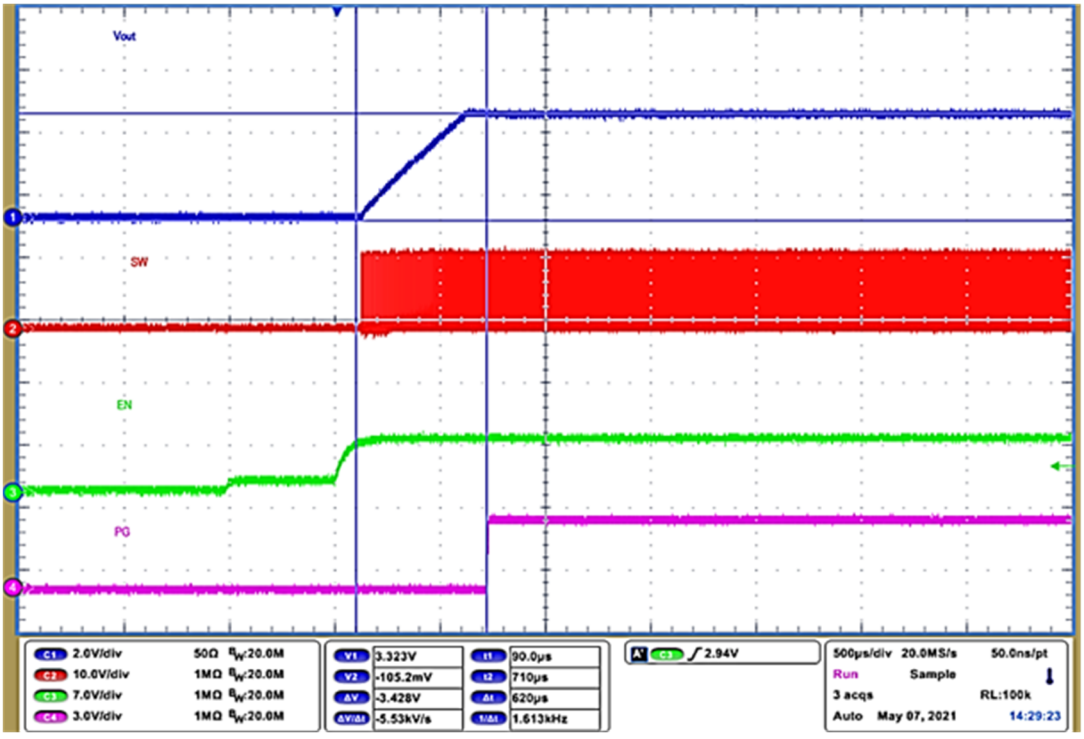

Figure 5-8. Enable Start Up Forced PWM V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 1 A

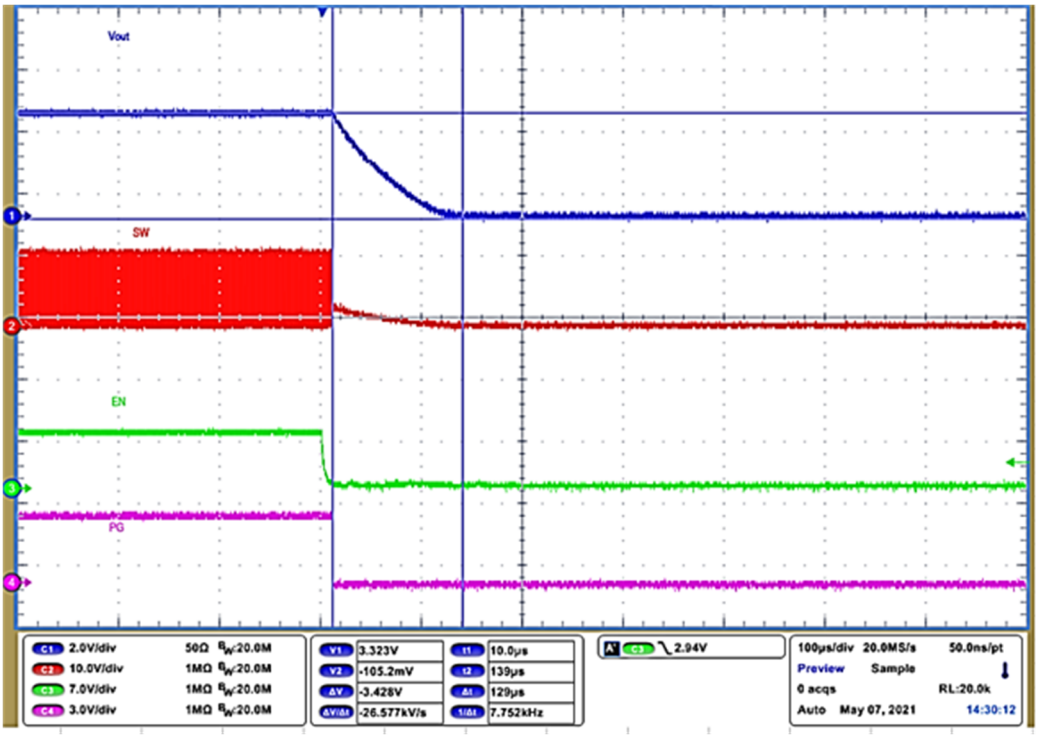

Figure 5-9. Enable Shutdown Forced PWM V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 1 A

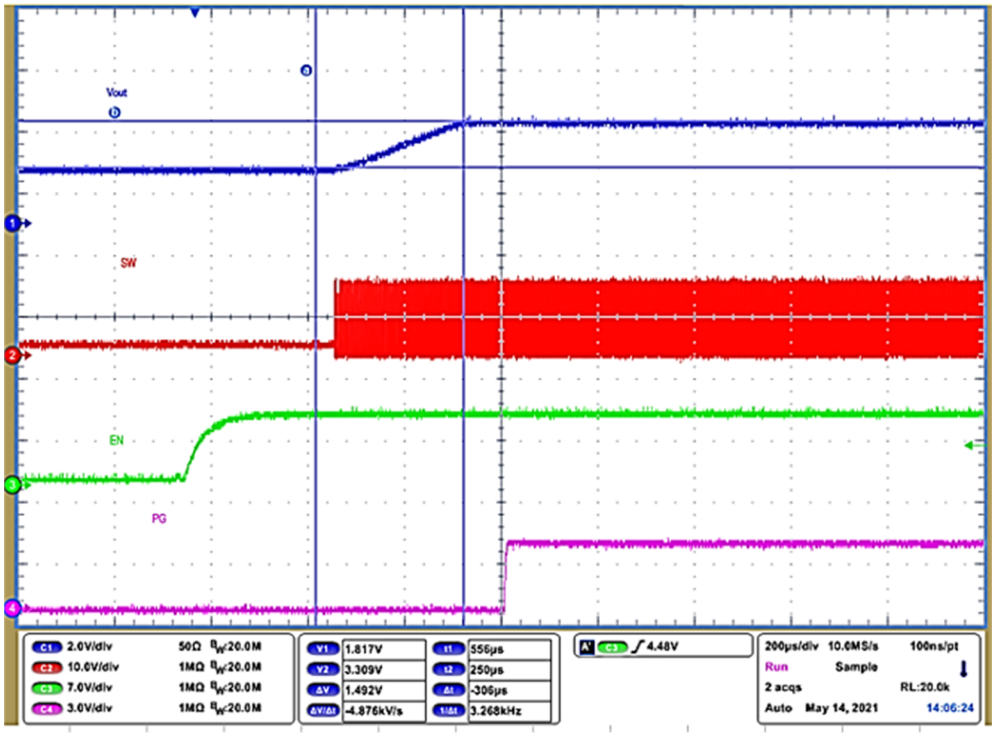

Figure 5-10. Enable Pre-Bias Start Up Forced PWM V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 0 A

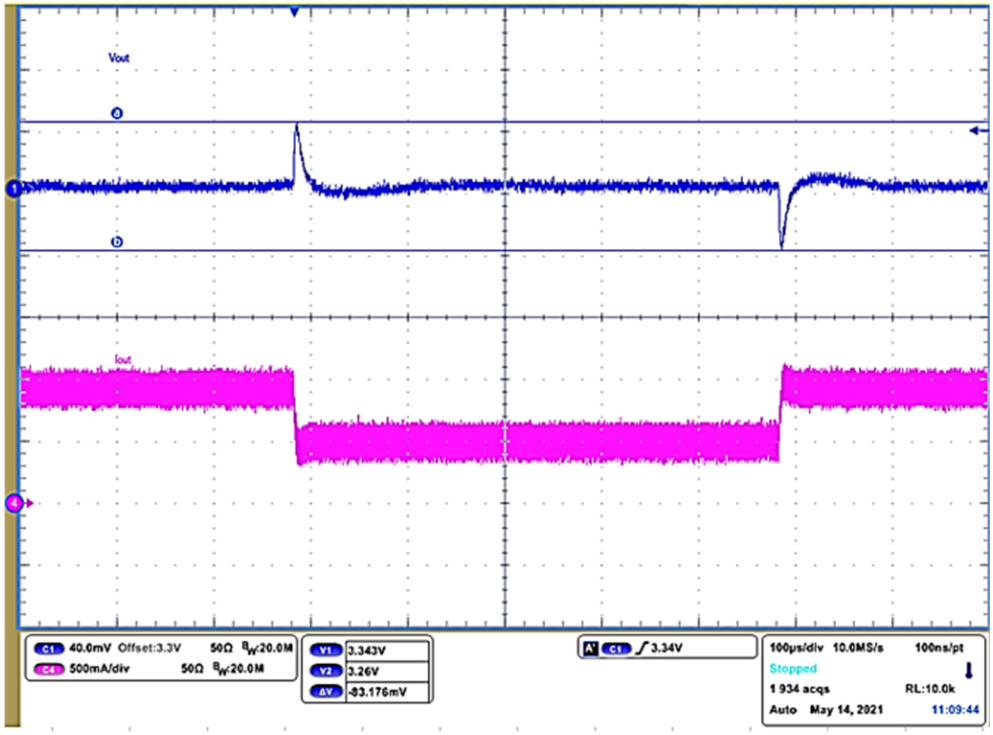

Figure 5-11. Load Transient Response Forced PWM Internal FB (VSET) V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT}= 0.5 A–1 A Slew Rate = 1 A/us

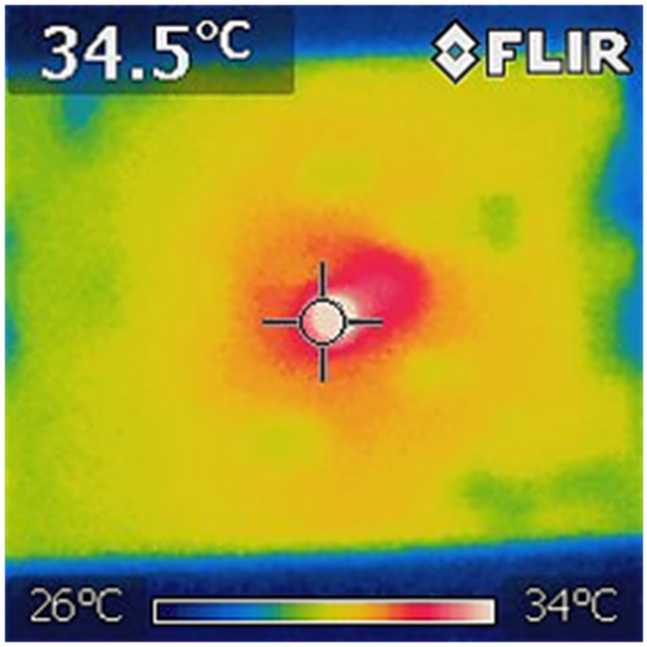

Figure 5-12. Thermal Performance Forced PWM V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 1 A F_{SW}=2.5 MHz

6 Board Layout

This section provides the EVM board layout and illustrations.

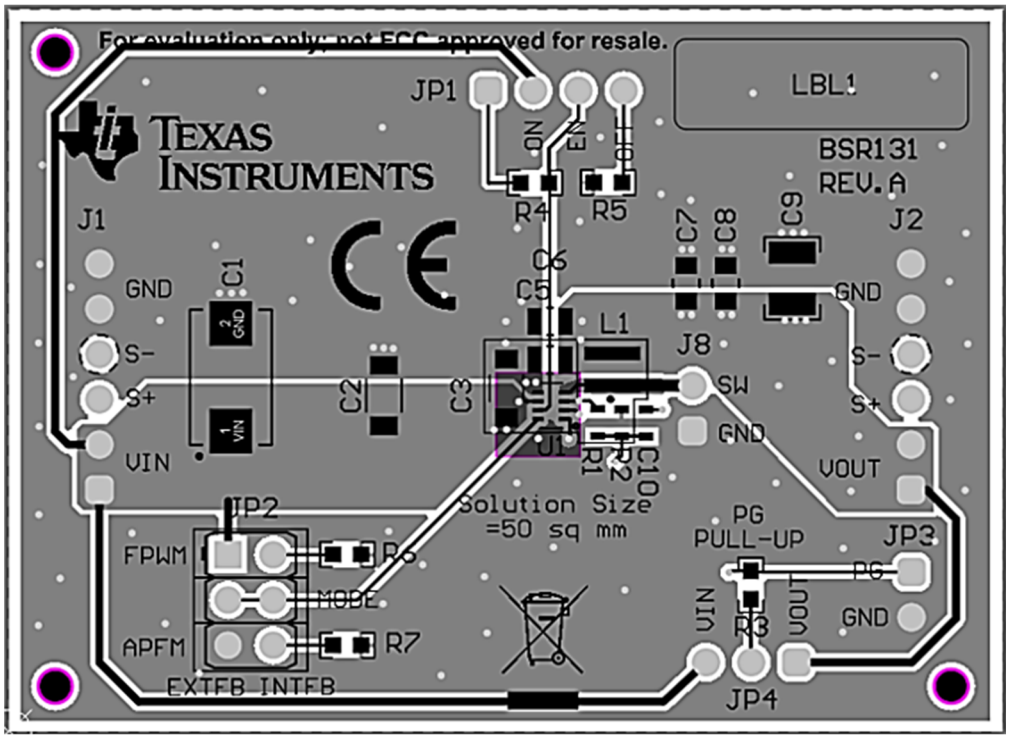

Figure 6-1. Top Assembly

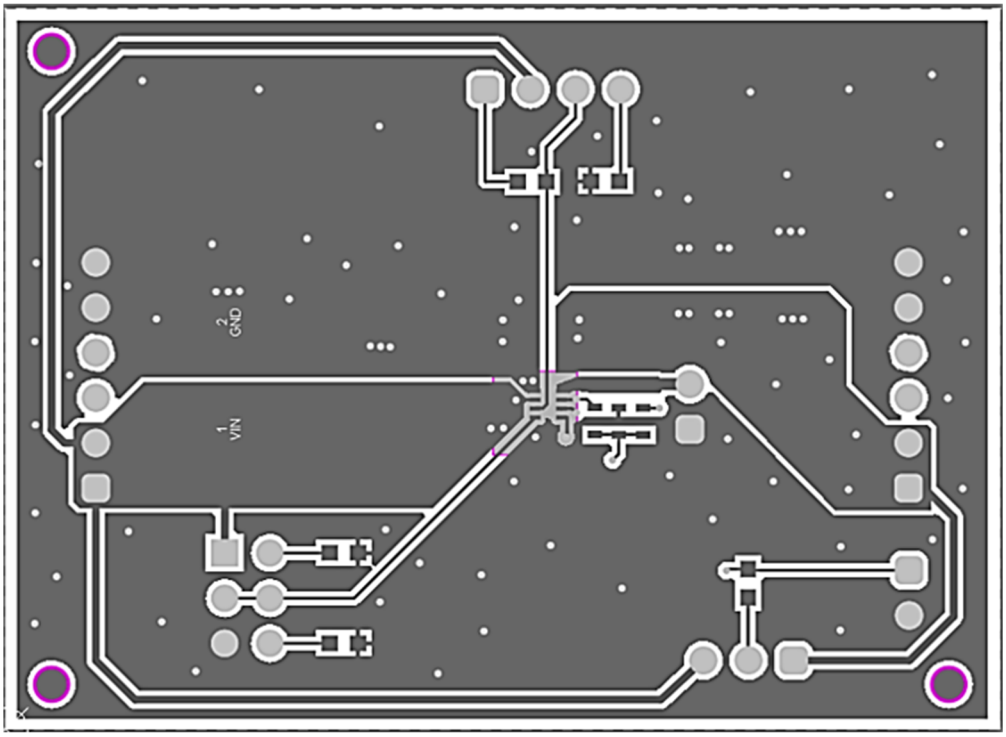

Figure 6-2. Top Layer

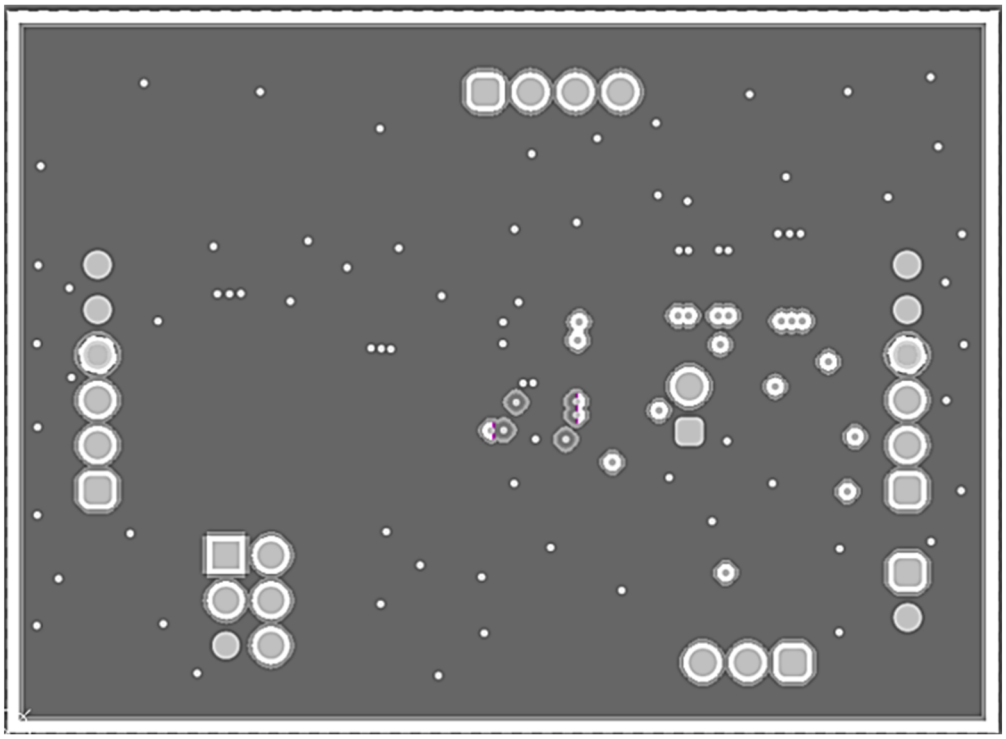

Figure 6-3. Internal Layer 1

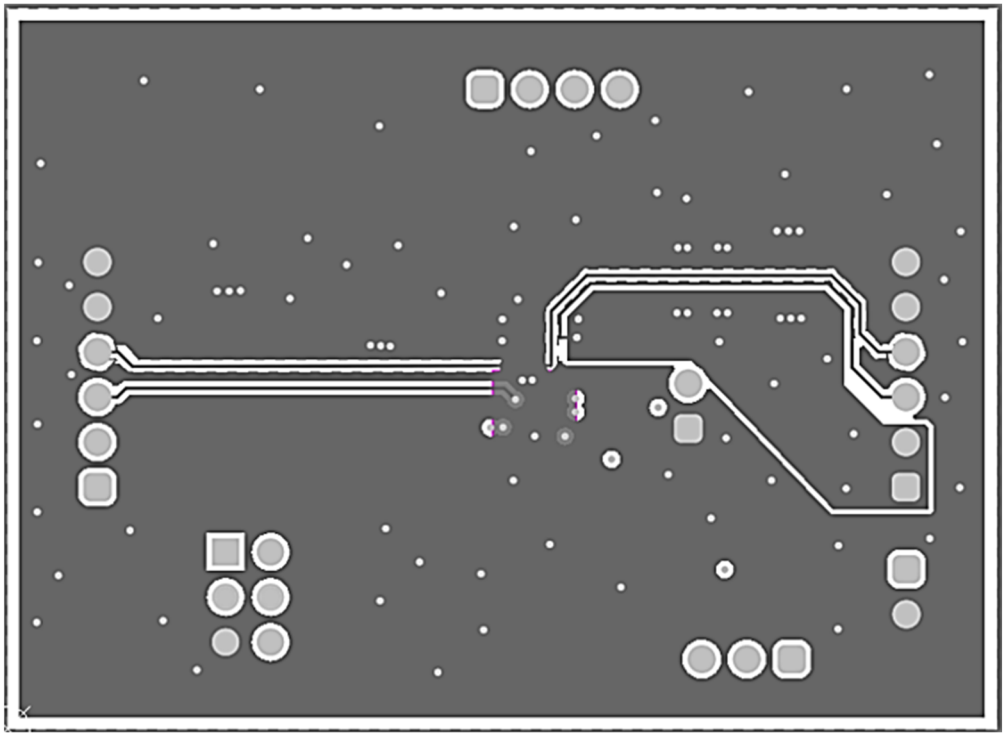

Figure 6-4. Internal Layer 2

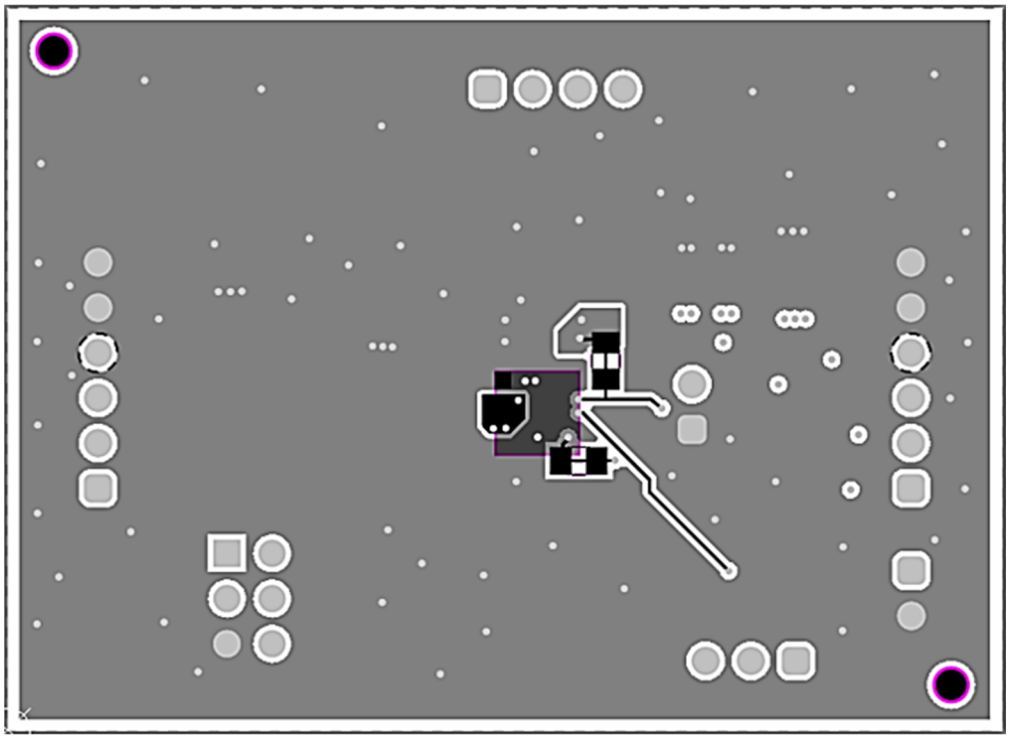

Figure 6-5. Bottom Layer

7 Schematic and Bill of Materials

This section provides the EVM schematic and bill of materials (BOM).

7.1 Schematic

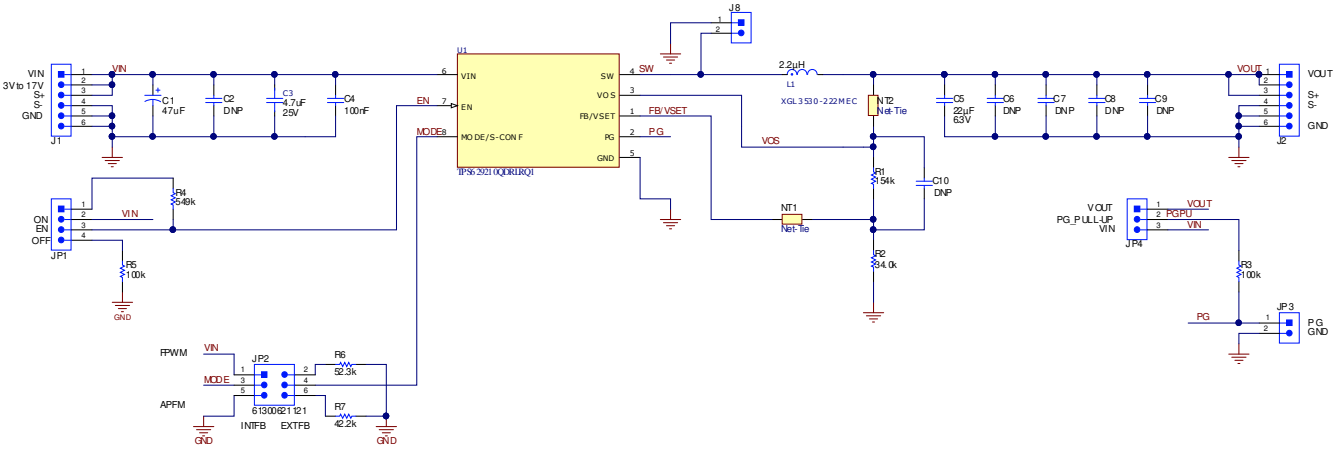

Figure 7-1. TPS629210-Q1EVM Schematic

7.2 Bill of Materials

Table 7-1. EVM Bill of Materials

Designator	Qty	Value	Description	Package	Part Number	Manufacturer
C1	1	47µF	CAP, TA, 47 uF, 35 V, +/- 10%, 0.3 ohm, SMD	7343-43	T495X476K035ATE300	Kemet
C3	1	4.7µF	Cap Ceramic 4.7uF 25V X7R 10% Pad SMD 1206 +125°C Automotive T/R	1206	CGA5L1X7R1E475K160AC	TDK
C4	1	0.1µF	CAP, CERM, 0.1uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C104K3RACTU	Kemet
C5	1	22µF	CAP, CERM, 22 uF, 6.3 V, +/- 20%, X7T, AEC-Q200 Grade 1, 0805	0805	GCM21BD70J226ME36L	MuRata
J1, J2	2		Header, 2.54 mm, 6x1, Gold, TH	Header, 2.54mm, 6x1, TH	61300611121	Wurth Elektronik
JP1	1		Header, 2.54 mm, 4x1, Gold, TH	Header, 2.54mm, 4x1, TH	61300411121	Wurth Elektronik
JP2	1		Header, 2.54 mm, 3x2, Gold, TH	Header, 2.54mm, 3x2, TH	61300621121	Wurth Elektronik
JP3	1		Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH	61300211121	Wurth Elektronik
JP4	1		Header, 2.54 mm, 3x1, Gold, TH	Header, 2.54mm, 2x1, TH	61300311121	Wurth Elektronik
L1	1	2.2µH	Molded Power Inductor, Shielded, 2.2uH 20%, 7.2A, 23mOhm DCR Max, AEC-Q200, T/R	SMT_IND_3MM2_3MM5	XGL3530-222MEC	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1	1	154k	RES, 154 k, 1%, 0.1 W, 0603	0603	RC0603FR-07154KL	Yageo
R2	1	34.0k	RES, 34.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0734KL	Yageo
R3, R5	2	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo
R4	1	549k	RES, 549 k, 1%, 0.1 W, 0603	0603	RC0603FR-07549KL	Yageo

Table 7-1. EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Package	Part Number	Manufacturer
R6	1	52.3k	RES, 52.3 k, 1%, 0.1 W, 0603	0603	RC0603FR-0752K3L	Yageo
R7	1	42.2k	RES, 42.2 k, 1%, 0.1 W, 0603	0603	RC0603FR-0742K2L	Yageo
U1	1		3-V to 17-V, Synchronous Buck Converters in 1.6 mm x 2.1 mm SOT583 Package	SOT583	TPS629210QDRLRQ1	Texas Instruments
C2	0	10µF	CAP, CERM, 10 uF, 25 V, +/- 20%, X7R, 1206_190	1206_190	C3216X7R1E106M160AE	TDK
C6	0	22µF	CAP, CERM, 22 µF, 6.3 V,+/- 20%, X7T, AEC-Q200 Grade 1, 0805	0805	CGA4J1X7T0J226M	TDK
C7, C8	0	22µF	CAP, CERM, 22 uF, 10 V, +/- 20%, X7S, 0805	0805	C2012X7S1A226M125AC	TDK
C9	0	47µF	CAP, CERM, 47 uF, 6.3 V, +/- 20%, X7R, 1210	1210	GRM32ER70J476ME20L	MuRata
C10	0	22pF	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H220JA01D	MuRata
J8	0		Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH	61300211121	Wurth Elektronik

8 References

TPS629210-Q1 data sheet, TPS629210-Q1 3 V to 17 V, 1-A Low Iq Buck Converter in SOT583 Package (SLVSFS6)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265