User's Guide

TPS65219 Evaluation Module

ABSTRACT

This user's guide describes the characteristics, operation, and use of the TPS65219 evaluation module (EVM). The TPS65219EVM is a fully assembly platform for evaluating the performance and functionality of the TPS65219 power management IC (PMIC). The EVM includes an onboard USB-to-I^{2}C adapter, power terminals, and jumpers for all DC regulator inputs and outputs, as well as test points for common measurements.

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Trademarks

1 Caution

	**Caution**	**Read the user's guide before use**
	**Caution**	**Caution hot surface** **Contact can cause burns** **Do not touch!**

2 Introduction

The TPS65219 PMIC is a highly integrated power management design for Arm® Cortex®-A53 Processors and FPGAs. This device combines three step down converters and four low-dropout (LDO) regulators. The Buck1 step down converter can support a load current of up to 3.5A, designed for the core rail of a processor. All three step down converters support non-fixed switching frequency or fixed frequency mode. LDO1 and LDO2 are configurable in both load switch and bypass-mode to support SD-Card configuration. All LDO voltage inputs can be cascaded off the step down converter outputs or use the same system power to enable maximum design and sequencing functionality. Complete with three GPIOs and three Multi-Function-Pins (MFPs), TPS65219 offers the complete package for full control of the power and sequencing of a System on Chip (SoC).

3 Requirements

3.1 Hardware

This section lists the minimum hardware requirements needed to operate the EVM.

- **EVM**
- **Host Computer**
  - A computer with an available USB port is required to make use of the EVM software. The EVM software runs on the computer and communicates with the EVM via a USB-A to micro-B cable.
- **Power Supply**

3.2 Software

- **TPS65219-GUI (PMIC graphical user interface)**
  - The TPS65219-GUI can be used in your browser or as a standalone application. This software provides a simple way to communicate with the device via I2C using the built-in USB2ANY utilizing an MSP430. For details on the GUI installation and setup process, please see Section 6 of this guide. Note that the EVM can power up and operate without use of software.

4 TPS65219 Resources Overview

The TPS65219 PMIC contains seven regulators; 3 Buck regulators and 4 Low Drop-out Regulators (LDOs). The Buck converters are capable of supporting up to 3.5 A for Buck1, and 2 A each for the remaining buck regulators. LDO1 and LDO2 (2×400 mA) can be configured as load switch and bypass mode. LDO3 and LDO4 (2×300 mA) can be configured as load switches. With a VIN range of 2.5 V to 5.5 V, the PMIC can support a common 3.3 V or 5 V system voltage. Table 4-1 shows a summary of the voltage and current capabilities for each of the analog resources. With an I2C interface, three GPIO pins, and three multi-function-pins, the TPS65219 PMIC provides the full power package to meet the requirements of a variety of SoCs.

This PMIC has two versions, TPS65219 supports industrial applications with a temperature range of -40°C to +105°C ambient and TPS65219-Q1 supports automotive applications that requires an extended temperature range of -40°C to +125°C ambient. Table 4-2 shows the differences between the industrial and automotive PMIC variants.

Table 4-1. TPS65219 Power Resources

	Input Voltage	Output Voltage	Current Capability	Comments
BUCK1	2.5 V - 5.5 V	0.6 V - 3.4 V	3.5 A	• 2.3 MHz switching frequency • Dynamic voltage scaling • Programmable power sequencing and default voltages. • Integrated voltage supervisor for undervoltage.
BUCK2	2.5 V - 5.5 V	0.6 V - 3.4 V	2 A	
BUCK3	2.5 V - 5.5 V	0.6 V - 3.4 V	2 A	
LDO1	1.5 V - 5.5 V (LDO, Load-Switch) 1.5 V - 3.4 V (Bypass)	0.6 V - 3.4 V (LDO) 1.5 V - 3.4 V (Bypass)	400 mA	• Programmable power sequencing and default voltages. • Configurable as load switch and bypass-mode. • Integrated voltage supervisor for undervoltage
LDO2	1.5 V - 5.5 V (LDO, Load-Switch) 1.5 V - 3.4 V (Bypass)	0.6 V - 3.4 V (LDO) 1.5 V - 3.4 V (Bypass)	400 mA	
LDO3	2.2 V - 5.5 V	1.2 V - 3.3 V	300 mA	• Programmable power sequencing and default voltages. • Configurable as load switch • Integrated voltage supervisor for undervoltage
LDO4	2.2 V - 5.5 V	1.2 V - 3.3 V	300 mA	

Table 4-2. TPS65219 vs TPS65219-Q1

Feature	TPS65219 (Industrial)	TPS65219-Q1 (Automotive)
Target Processor	AM62x 13 mm x 13 mm, 0.5-mm pitch, 425-pin FCCSP BGA (ALW)	AM62x-Q1 17.2 mm x 17.2 mm, 0.8-mm pitch, 441-pin FCBGA (AMC)
Switching Frequency	Up to 2.3 MHz Quasi-fixed frequency • Auto-PFM • Forced-PWM	Up to 2.3MHz . Capable of either quasi-fixed frequency or fixed-frequency depending on device configuration Quasi-fixed frequency • Auto-PFM • Forced-PWM Fixed-frequency • Spread spectrum available
Operating Free-Air Temp TA	40C to 105C	40C to 125C
Operating Junction Temp TJ	-40C to 125C	-40C to 150C
Functional Safety Capable	No	Functional Safety Capable (TI Quality managed process, Functional safety FIT rate calculation, and Failure Mode Distribution is available)
Package	Two package options • 4 mm × 4 mm, 0.4 mm pitch VQFN • 5 mm × 5 mm, 0.5 mm pitch VQFN	One package option • 5 mm × 5 mm, 0.5 mm pitch VQFN • (Wettable-Flank)

5 EVM Configuration

The TPS65219EVM can be configured as follows. The following sections outline how to configure the TPS65219EVM for general experimentation.

1. Configure regulator input supply rails for the expected application using the jumpers indicated in the *Supply Voltage Setup*.
2. Configure the multi-function pins externally using the mode configuration descriptions indicated in *Multi-Function pin setup*. Please note that the default configuration for regulator choice in SD or DDR voltage selection can differ for each individual NVM configuration (polarity is configurable).
3. Connect VSYS to a power supply capable of supporting the application and enable the supply.
4. If using a version of TPS65219 configured for First Supply Detection (FSD), then the power-up sequence is executed as soon as a valid supply is connected to VSYS.

5.1 Default EVM Configuration

This section describes the default configuration programmed on the TPS6521901 PMIC.

The TPS65219EVM comes with the TPS6521901 PMIC installed which is one of the orderable part numbers of the TPS65219 device family. The default output voltages for the Bucks and LDOs is shown in Figure 5-1. This information is based on the programmed default configuration on the TPS6521901 EVM. The EVM can be used to evaluate other TPS65219 variants by reprogramming the PMIC NVM memory. External passive components and jumper configuration can need to be changed if the PMIC is reprogrammed or replaced with a different orderable. For more information about the settings that can be re configured and the I2C registers associated, refer to the device data sheet and technical reference manual (TRM).

Note

The TPS65219EVM is designed to demonstrate some of the potential uses of the PMIC family. The EVM has more limitations than the TPS65219x device.

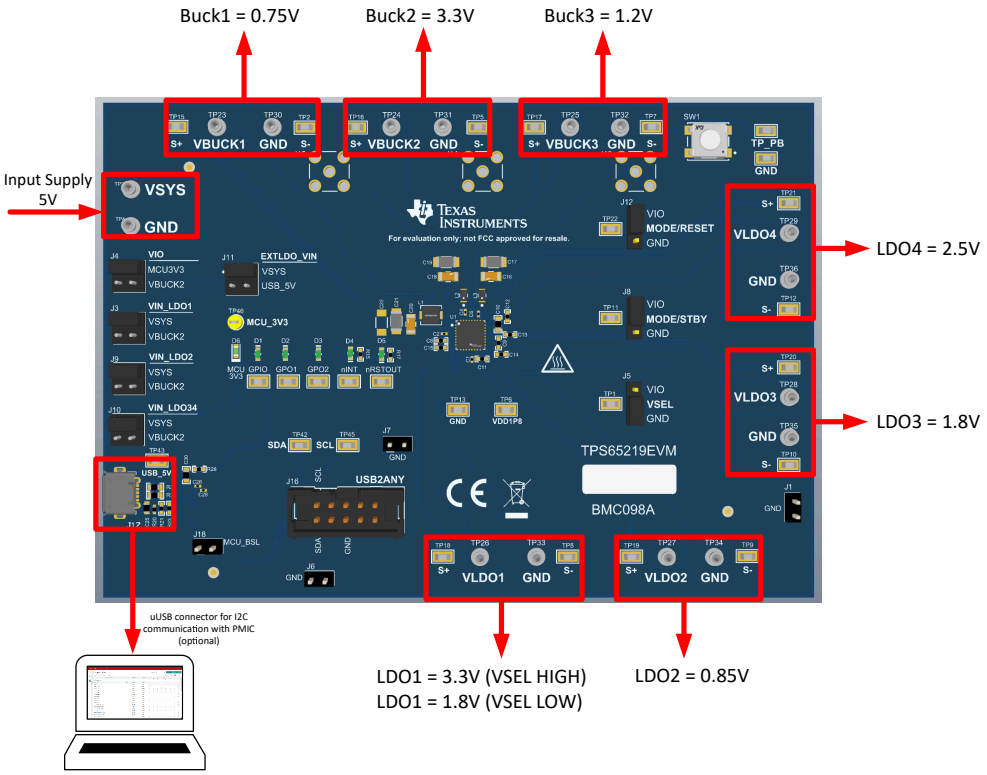


Figure 5-1. TPS65219EVM Default Configuration - Output Voltages

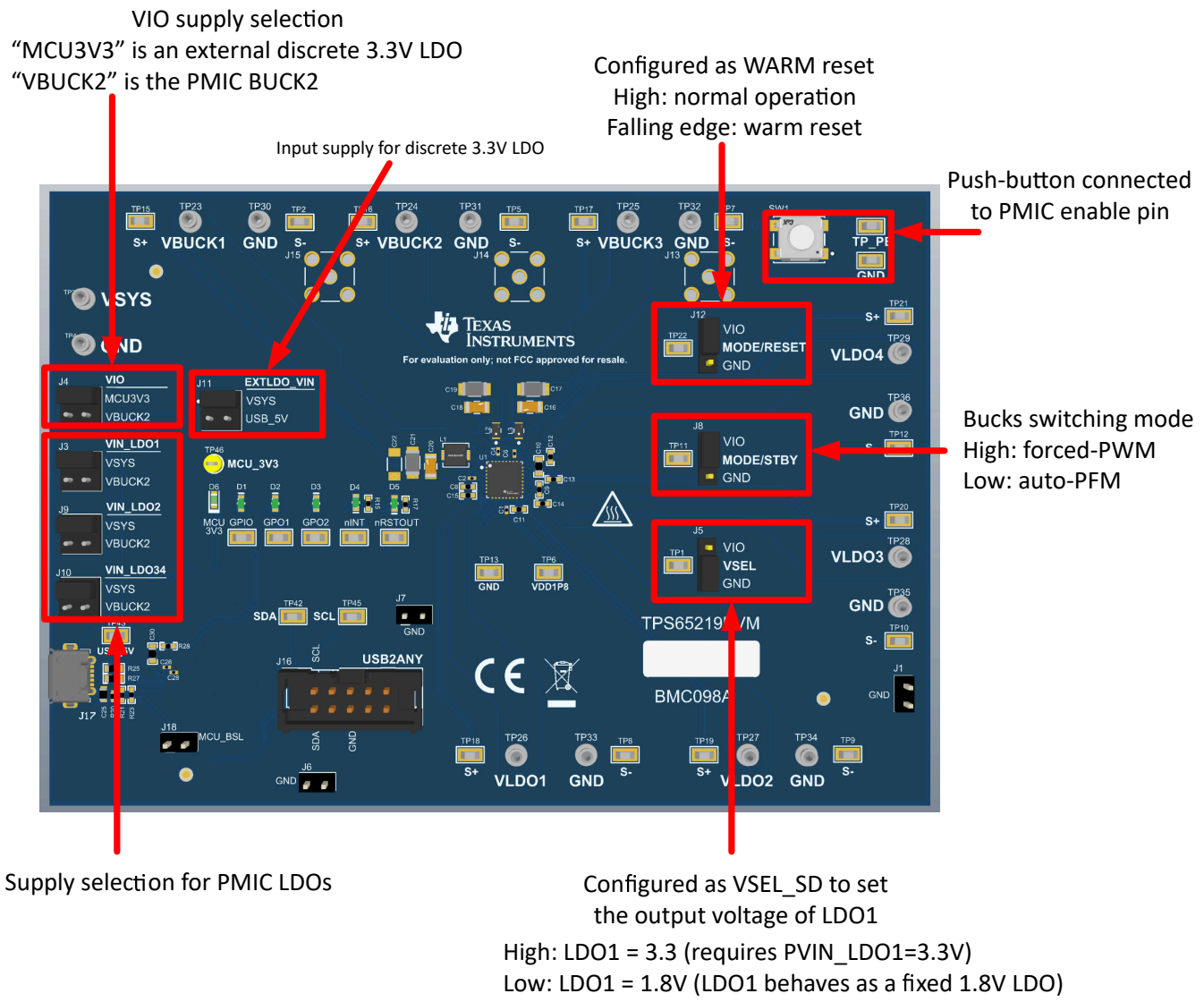


Figure 5-2. TPS65219EVM Default Configuration - Jumpers

Table 5-1. TPS65219EVM Default Jumper Configuration

	Header		Jumper Default Position
Supply voltage setup	J3	VIN_LDO1	Supply selection for LDO1 Default: setup to supply LDO1 with BUCK2
	J9	VIN_LDO2	Supply selection for LDO2 Default: setup to supply LDO2 with VSYS
	J10	VIN_LDO34	Supply selection for LDO3 and LDO4 Default: setup to supply LDO3/4 with VSYS
	J11	EXTLDO_VIN	Supply selection for the external discrete LDO. Default: setup to supply the discrete 3.3V LDO with VSYS
	J4	VIO	VIO supply selection Default: setup to use external 3.3V discrete LDO as the pull-up supply for the I2C pins and digital input pins)

Table 5-1. TPS65219EVM Default Jumper Configuration (continued)

	Header		Jumper Default Position
Multi-Function pin setup	J5	VSEL	High = sets 3.3V output voltage on LDO1 if the LDO is supplied by a 3.3V source. Low = sets 1.8V output voltage on LDO1 (default EVM config)
	J8	MODE/STBY	Bucks switching mode High = forced-PWM (default EVM config) Low = auto-PFM
	J12	MODE_RESET	High = normal operation (default EVM config) Low = performs a warm reset (reset target voltage and Bypass mode configs to the default NVM values)

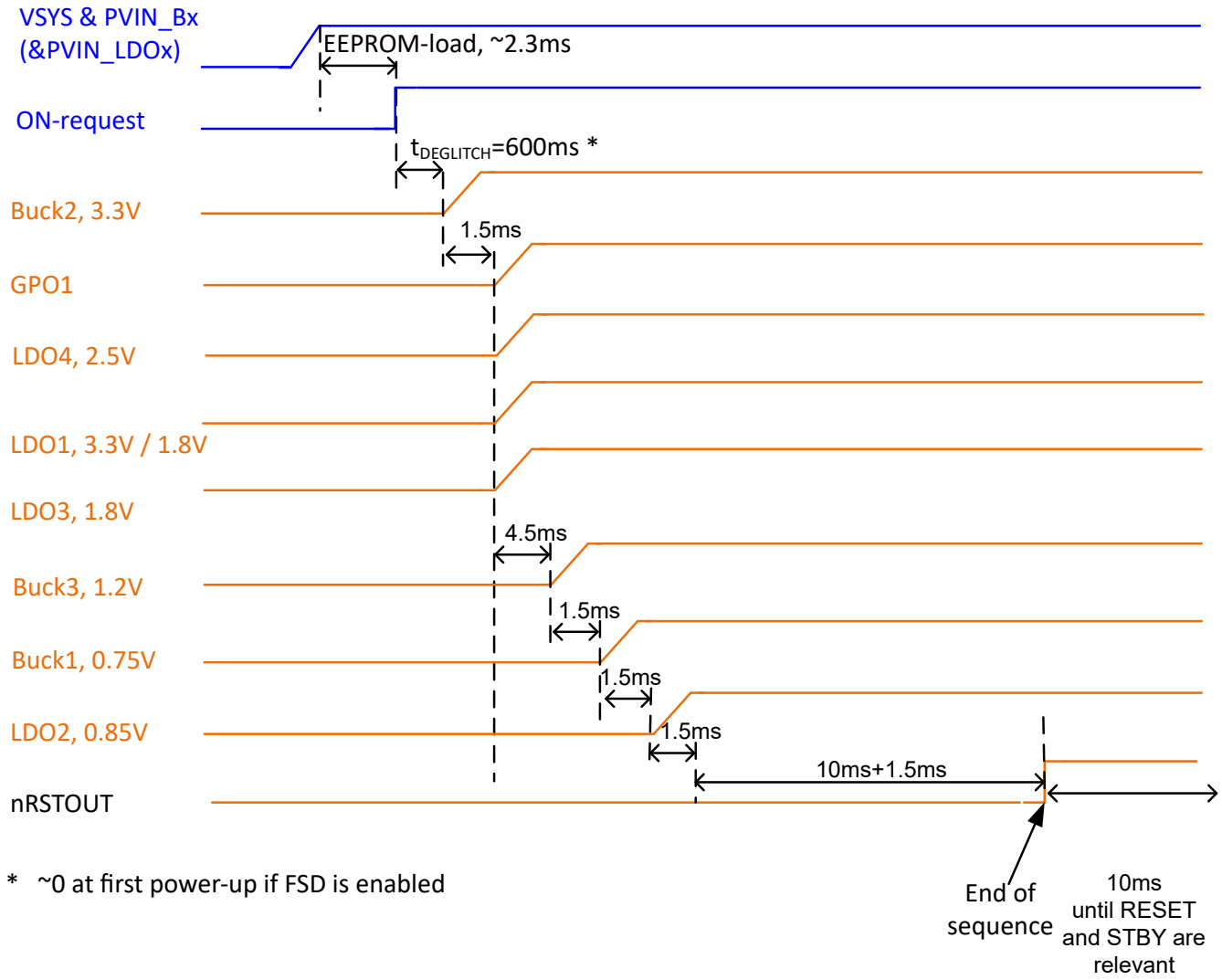
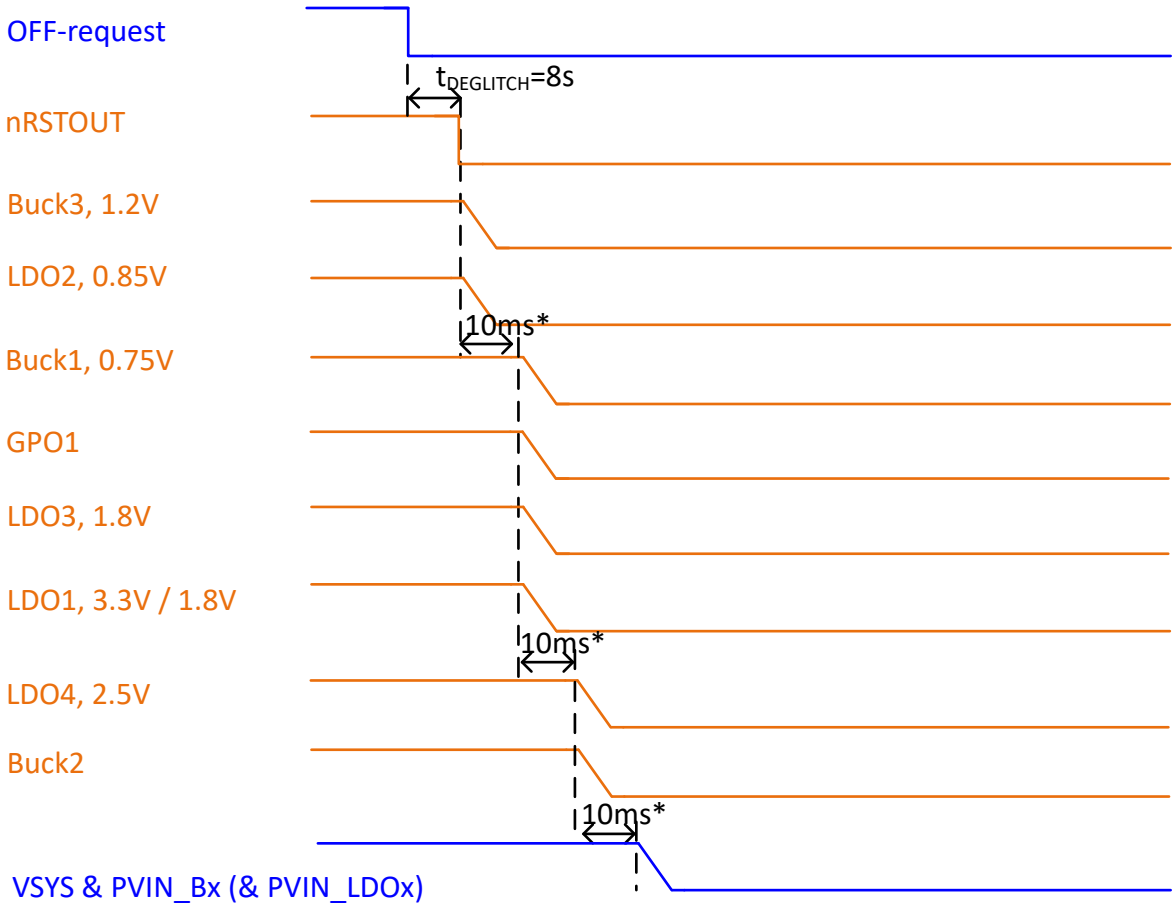


Figure 5-3. TPS6521901 Power-Up Sequence



* discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt. Slot-duration extends up to 8x its configured value.

Figure 5-4. TPS6521901 Power-Down Sequence

5.2 Configuration Headers

The TPS65219EVM has multiple headers that can be used to change the input supply for some of the power rails. The PCB also includes headers that allows changing specific functions of the PMIC using the multi-function pins. An overview of the jumper options for each header is shown in Figure 5-5. All the headers and the expected configuration for each selection is listed in Table 5-2.

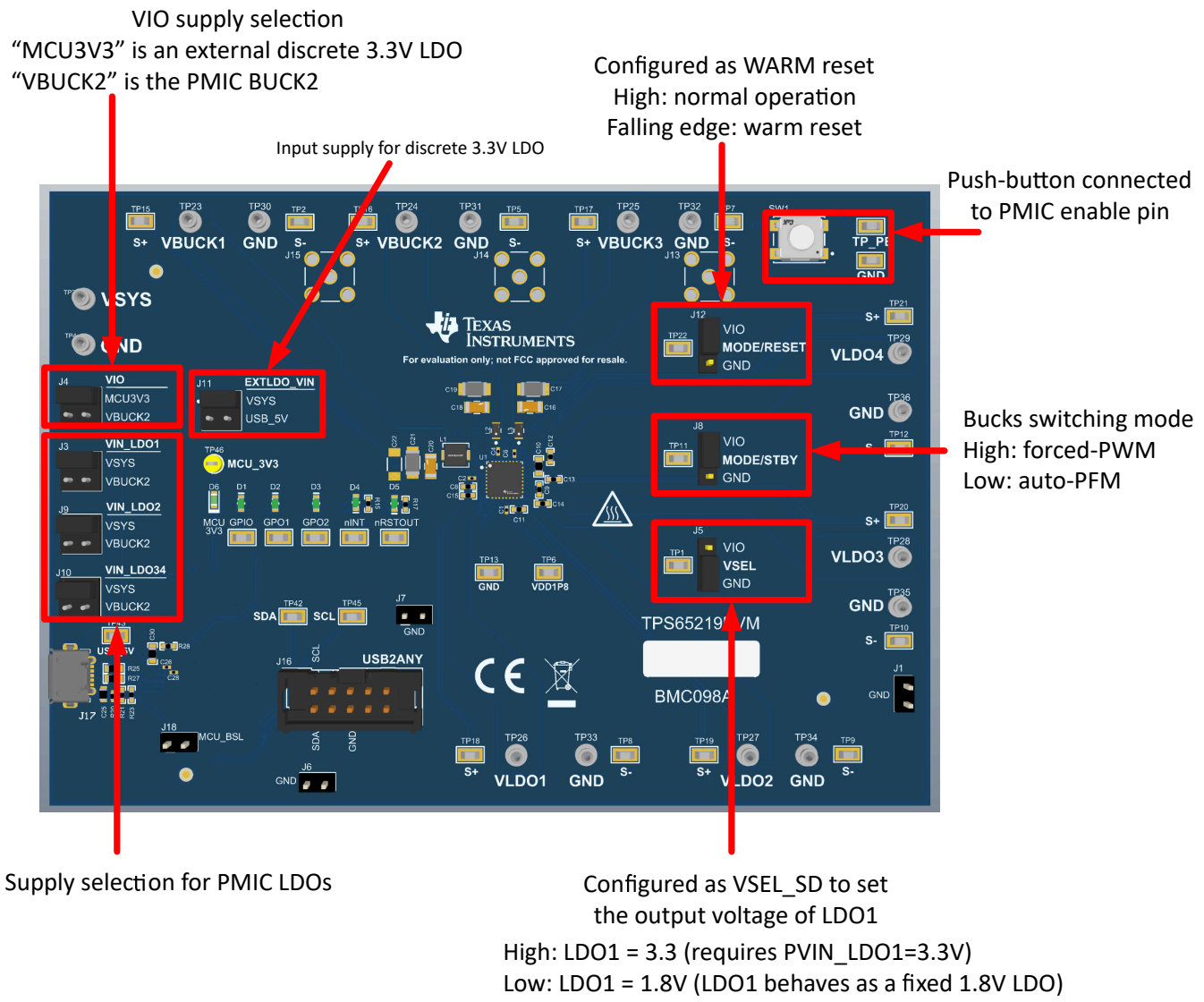


Figure 5-5. TPS65219EVM Default Configuration - Jumpers

Table 5-2. TPS65219EVM Default Jumper Configuration

	Header		Jumper Default Position
Supply voltage setup	J3	VIN_LDO1	Supply selection for LDO1 Default: setup to supply LDO1 with BUCK2
	J9	VIN_LDO2	Supply selection for LDO2 Default: setup to supply LDO2 with VSYS
	J10	VIN_LDO34	Supply selection for LDO3 and LDO4 Default: setup to supply LDO3/4 with VSYS
	J11	EXTLDO_VIN	Supply selection for the external discrete LDO. Default: setup to supply the discrete 3.3V LDO with VSYS
	J4	VIO	VIO supply selection Default: setup to use external 3.3V discrete LDO as the pull-up supply for the I2C pins and digital input pins)

Table 5-2. TPS65219EVM Default Jumper Configuration (continued)

	Header		Jumper Default Position
Multi-Function pin setup	J5	VSEL	High = sets 3.3V output voltage on LDO1 if the LDO is supplied by a 3.3V source. Low = sets 1.8V output voltage on LDO1 (default EVM config)
	J8	MODE/STBY	Bucks switching mode High = forced-PWM (default EVM config) Low = auto-PFM
	J12	MODE_RESET	High = normal operation (default EVM config) Low = performs a warm reset (reset target voltage and Bypass mode configs to the default NVM values)

5.3 Test Points

The TPS65219EVM EVM contains multiple test points for various measurements. Trace assignments to the test points are shown in the table below.

Table 5-3. TPS65219 EVM Test Points

Test Point	Associated Trace
TP1	VSEL_SD/VSEL_DDR
TP2	GND
TP3	VSYS
TP4-5	GND
TP6	VDD1P8
TP7-10	GND
TP11	MODE/STBY
TP12	GND
TP13	GND
TP14	PB / EN
TP15	Buck 1 Output SENSE
TP16	Buck 2 Output SENSE
TP17	Buck 3 Output SENSE
TP18	LDO 1 Output SENSE
TP19	LDO 2 Output SENSE
TP20	LDO 3 Output SENSE
TP21	LDO 4 Output SENSE
TP22	MODE/RST
TP23	Buck 1 Output
TP24	Buck 2 Output
TP25	Buck 3 Output
TP26	LDO 1 Output
TP27	LDO 2 Output
TP28	LDO 3 Output
TP29	LDO 4 Output
TP30-36	GND
TP37	GPIO

Table 5-3. TPS65219 EVM Test Points (continued)

Test Point	Associated Trace
TP38	GPO1
TP39	GPO2
TP40	nINT
TP41	nRSTOUT
TP42	SDA
TP43	USB_5V
TP44	GND
TP45	SCL
TP46	MCU3V3

6 Graphical User Interface (GUI)

This section covers the usage and capabilities of the TPS65219 / TPS65220 Graphical User Interface (GUI) tool from Texas Instruments.

6.1 Getting Started

Getting started involves the following steps:

1. Find the GUI within the Gallery
2. Download the required software
   a. GUI composer Runtime for running the GUI from a web browser
   b. An offline copy of the GUI
3. Launch the GUI

6.1.1 Finding the GUI

The PMIC GUI is based upon GUI Composer which is compatible with either Chrome® (version 46+) or Firefox® (version 38+). The Chrome web browser is recommended and used throughout this document for demonstration. The PMIC GUI is also compatible with Microsoft Edge® (as of version 111.0.1661.41). The GUI is found through the TI Development tools at TI DevTools page. Navigating to the Gallery from the Tools tab, highlighted in blue in Figure 6-1, is one way to enter the Gallery.

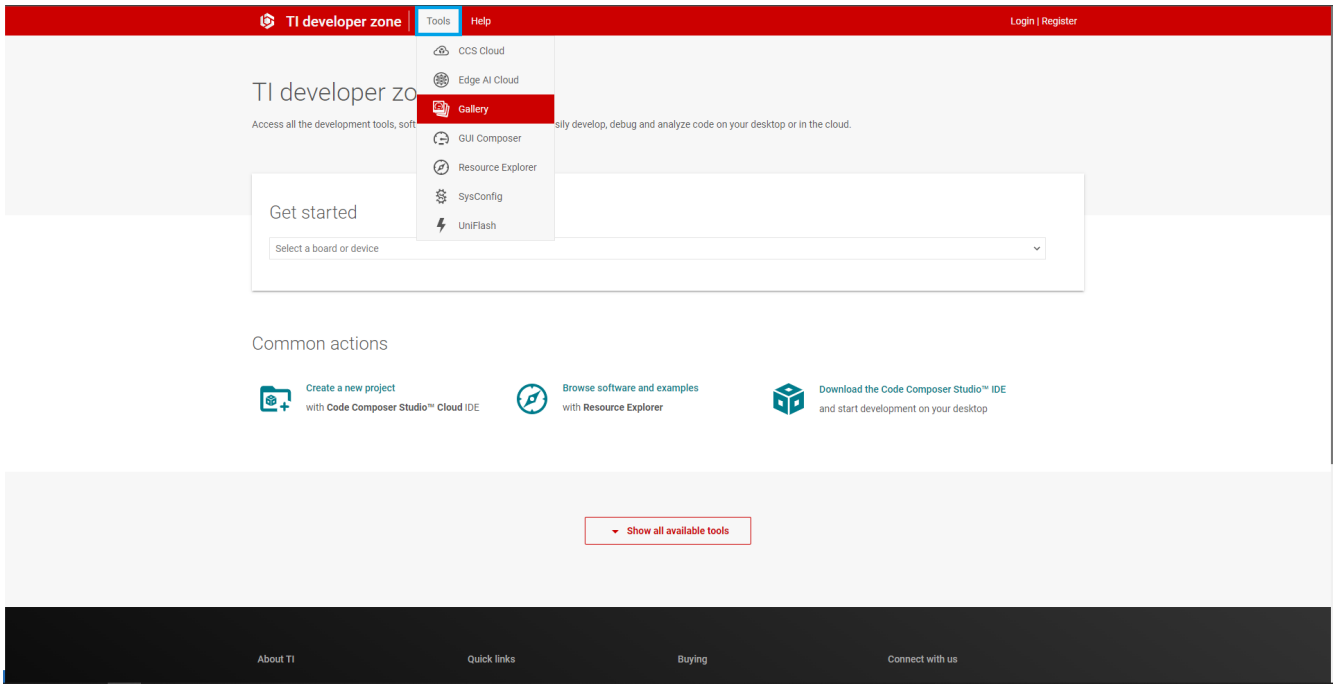


Figure 6-1. GUI Composer Gallery

In the gallery, locate the TPS65219_GUI panel shown in Figure 6-2 by using the search bar and entering TPS65219_GUI.

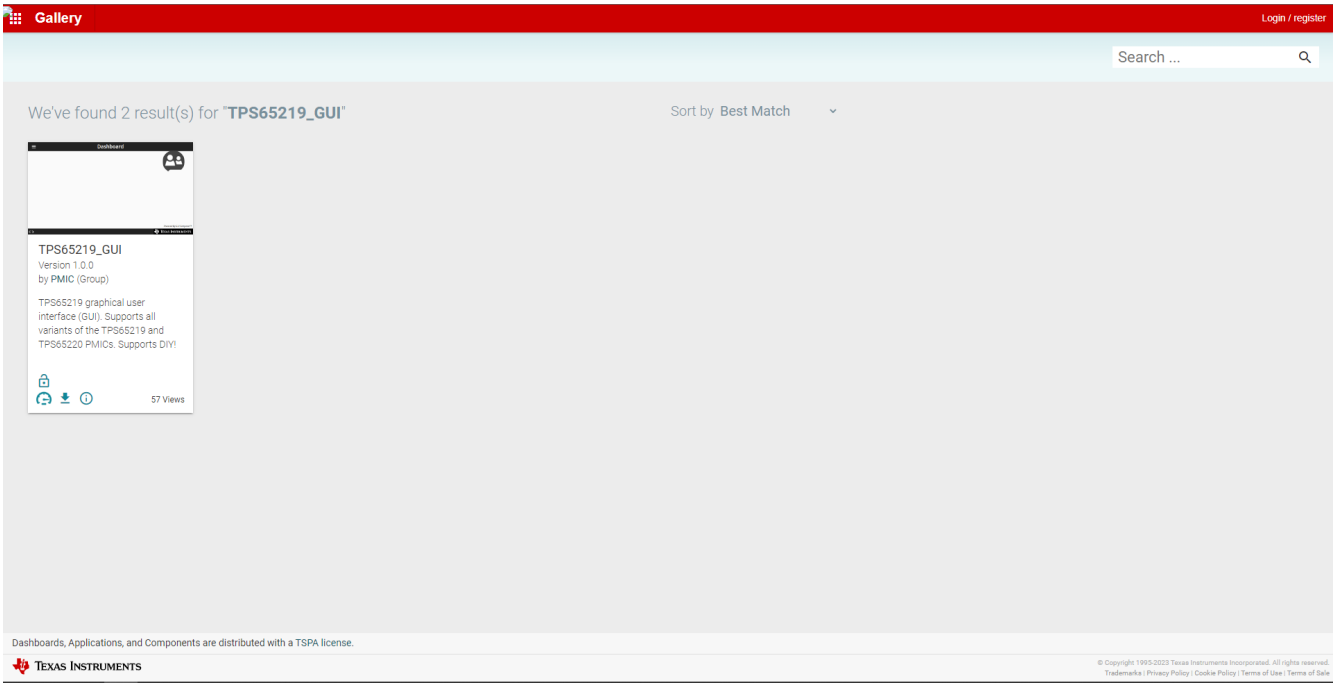


Figure 6-2. Locating the PMIC GUI in the Gallery

6.1.2 Downloading the Required Software

Both the standalone GUI and the GUI Composer Runtime are available from the PMIC panel. Again, the GUI Composer Runtime enables the GUI to be run through a web browser but requires an internet connection to be able to run the GUI. By contrast, the standalone GUI is much larger but does not require an internet connection.

The download options are found in the pop-up window, as shown in Figure 6-3, when the cursor is placed on the download icon. The upper three options offer a standalone download for the appropriate operating system, while the lower three are for the GUI Composer Runtime.

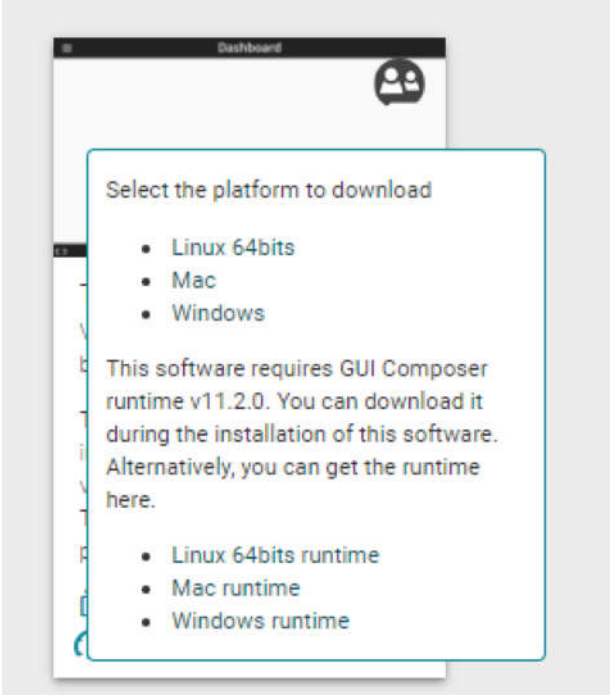


Figure 6-3. GUI Software Download Options

6.1.3 Launching the GUI

After the appropriate software has been downloaded, the GUI can be launched locally from the PC application or from the TI Cloud using the Gallery. To use the TI Cloud version of the GUI, simply click anywhere in the panel, shown in Figure 6-4, that is not associated with the download or information icons.

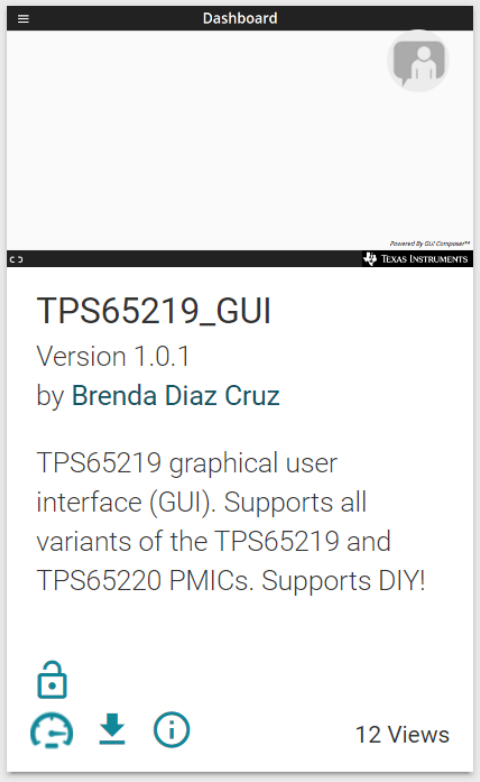


Figure 6-4. GUI Panel Within the Gallery

Figure 6-5 shows an example of the PC application.

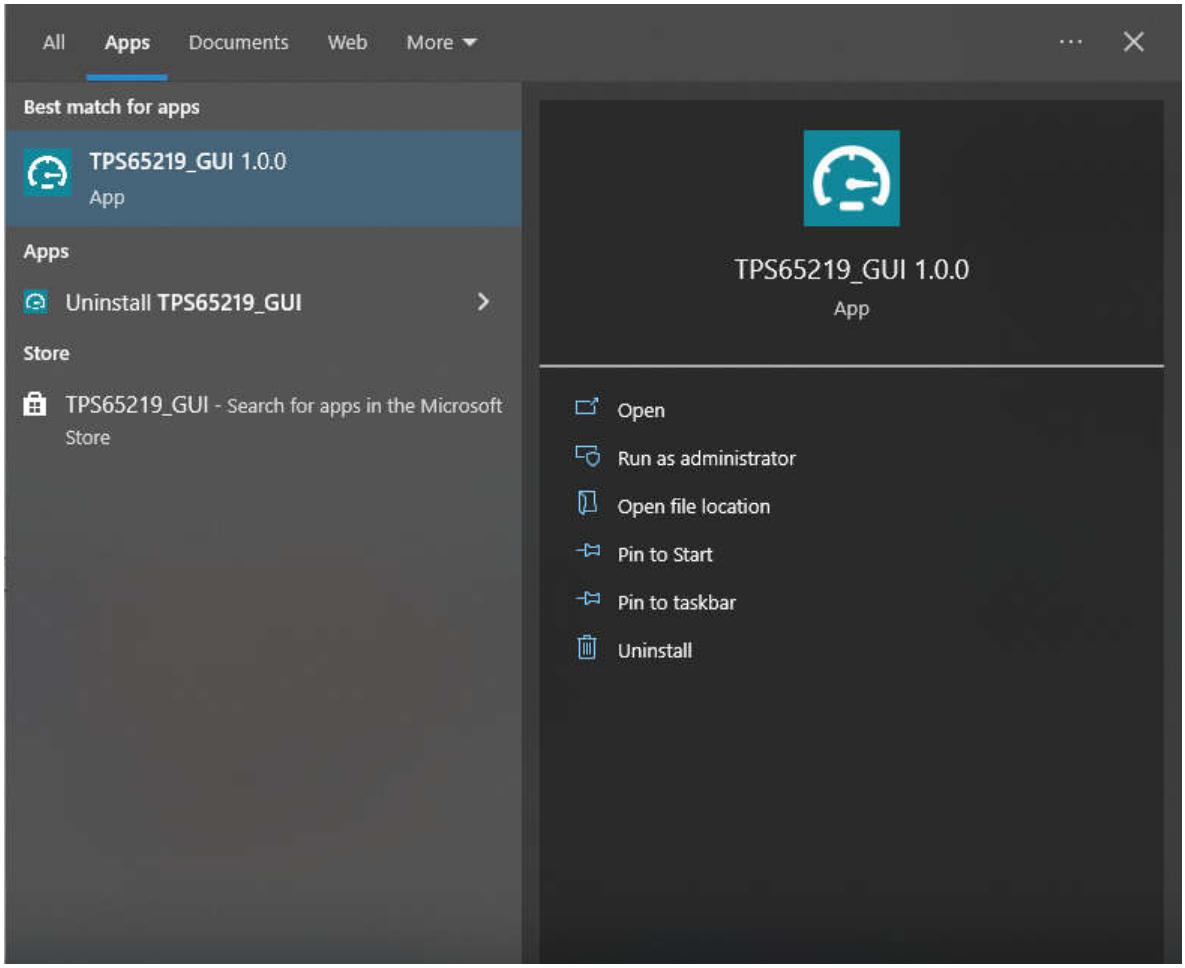


Figure 6-5. PMIC GUI Desktop Application

6.1.4 Connecting to the EVM

The README text box helps users connect the EVM board to the computer. If users want to see the README again, then users can access the README from the *Help* tab in the top left of the GUI dashboard. Here, users can also find an *About* option for information about the GUI version and additional documentation.

After users have dismissed the README message box, the GUI displays the Home page, shown in Figure 6-6. Here, users can see an overview of the TPS65219 power structure. The branching sections show what the alternate versions of the TPS65xxx family have to offer for a design.

At the bottom of the Home page, users can navigate to the other GUI pages, which are described in the subsequent sections. These pages can also be found on the left side of the GUI interface.

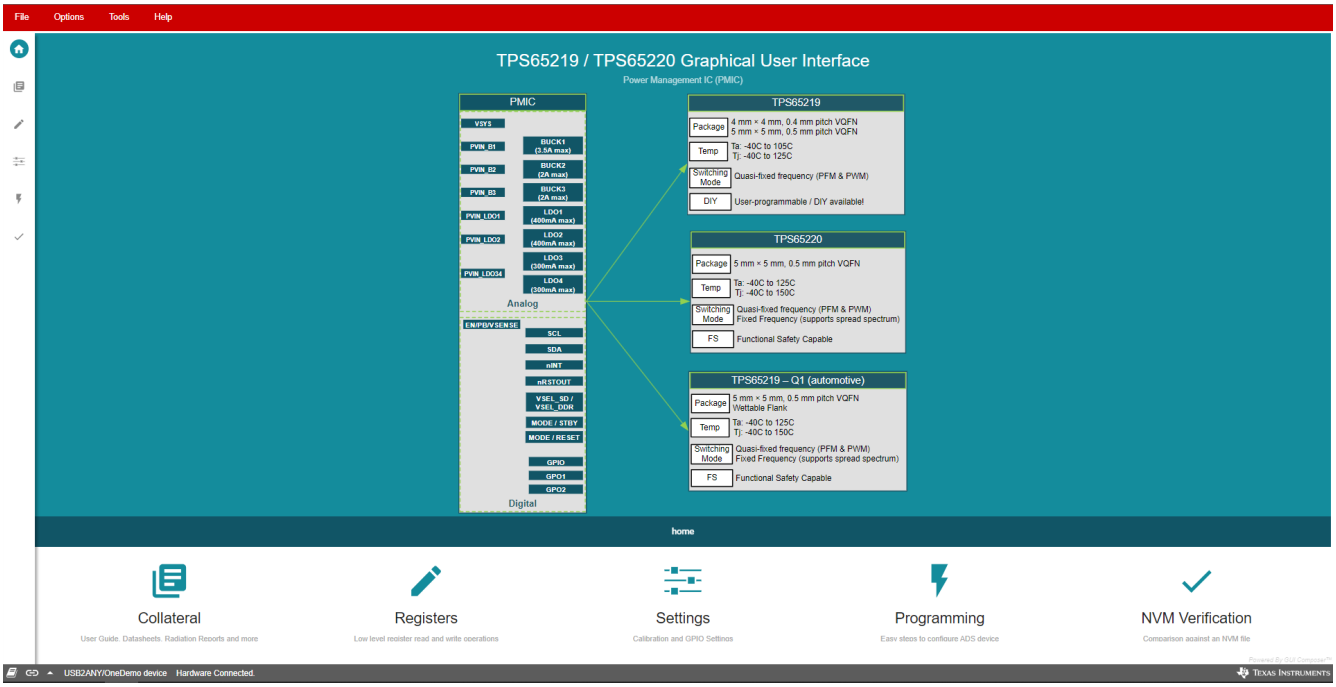


Figure 6-6. GUI Home Page

6.2 Collateral Page

The Collateral page, shown in Figure 6-7, contains relevant documentation for using the TPS65219 or TPS65220 PMICs. Here you can find a link to the EVM User's Guide, Data sheets, Application notes for processor power designs, and a tool for efficiency and thermal estimation.

At the bottom of the page, there is a link to our E2E forums for technical questions about the GUI or PMIC.

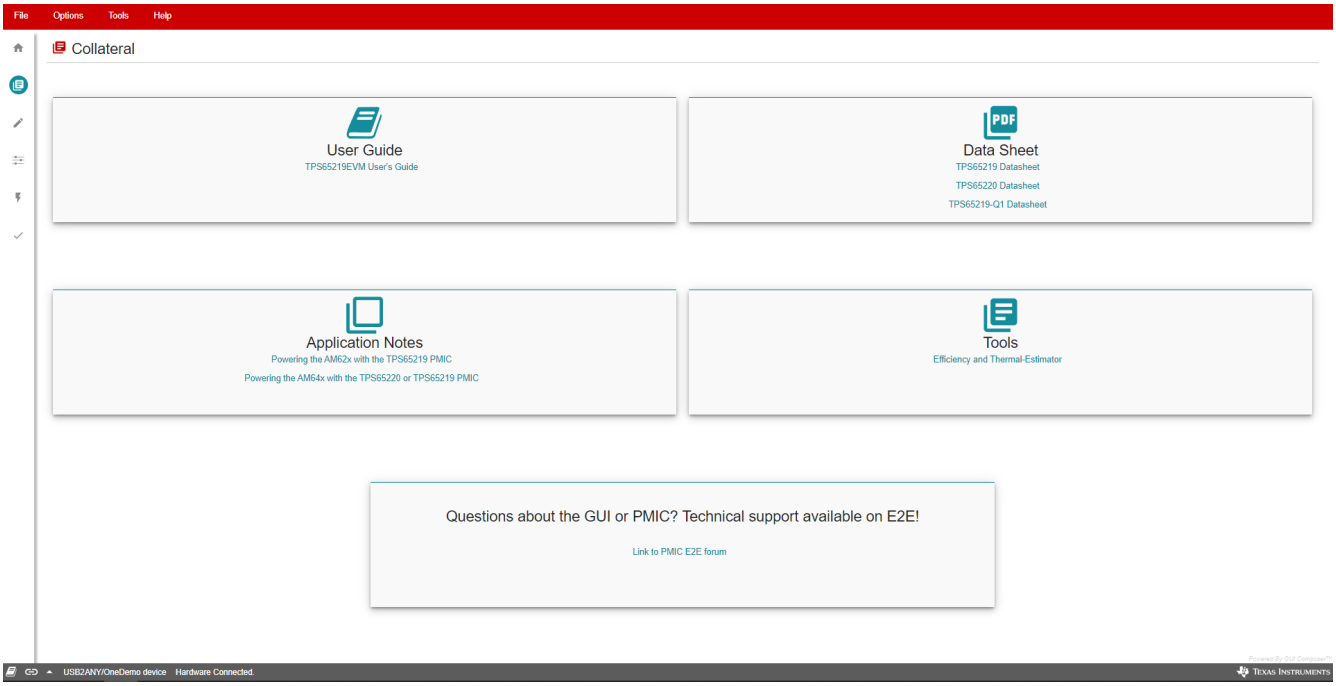


Figure 6-7. Collateral Page

6.3 Register Map Page

The Register Map page lists the different registers available for configuration and is intended for direct reads and writes to the PMIC registers, as shown in Figure 6-8. Reading and writing registers can be done individually or all at once. An Auto Read feature can be enabled by using the drop-down menu next to the *READ ALL REGISTERS* button to select an automatic read timing. Use the search bar at the top of the page to search registers by name or address.

The first three columns under the search bar show the name of each register, followed by the hexadecimal address and data value. The *Bits* column contains the bit values for each register and can be hidden by unchecking the *Show Bits* box at the top of the page, under the *READ ALL REGISTERS* button. Double-clicking a bit in this section changes the bit value.

The Field View section on the right side of the page shows register bits grouped by the respective control blocks. Users can click on any bit field box to see the corresponding bits highlighted in yellow in the *Bits* column. Each field has a name shown by the blue text at the top of each box. These names can be found using the search bar by checking the *Search Bitfields* box (next to *Show Bits*).

In the *Immediate Write* mode (drop-down option located at the top right of the page), write buttons are grayed out since individual registers are written immediately with each change in the Field View, change in bits, or change in hexadecimal value. In *Deferred Write* mode, the writing of a single register or all registers is deferred until the *WRITE REGISTER* or *WRITE ALL REGISTERS* button is selected.

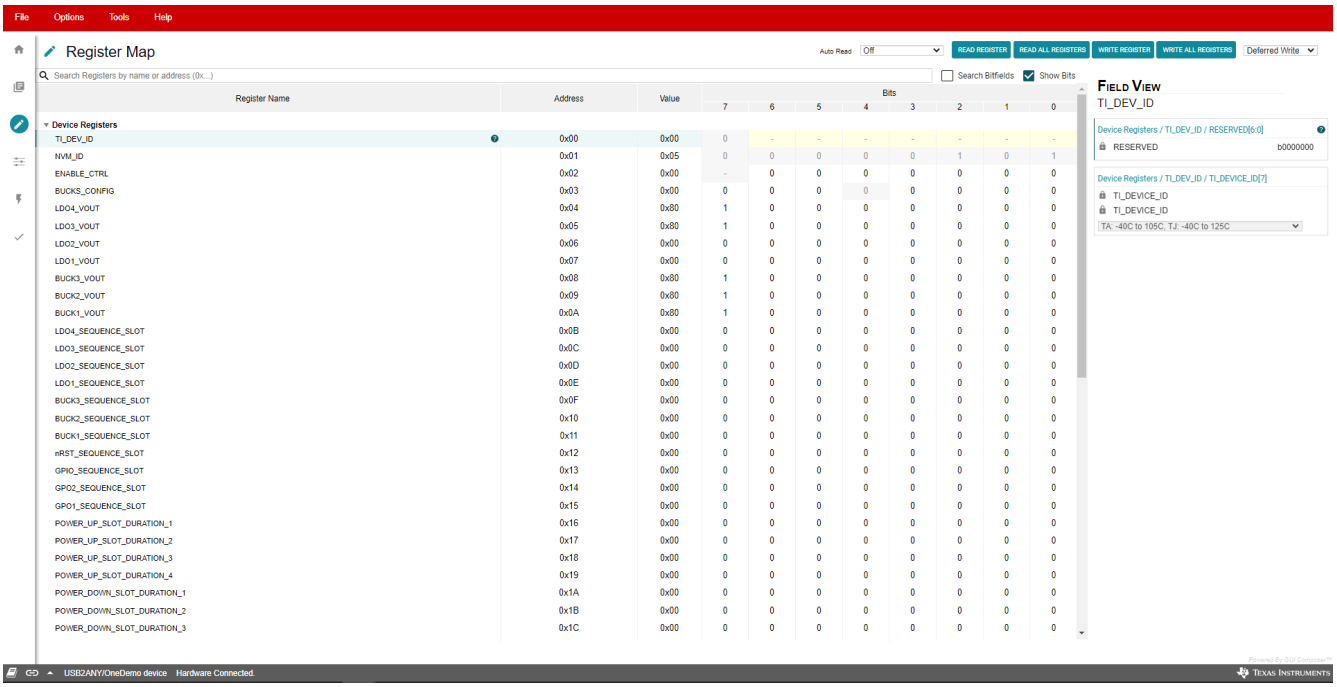


Figure 6-8. Register Map Page

Note

Although visible from the Register Map, not all registers can be edited from this page. Attempting a write to a read-only register does not generate an error. Since each write is comes with an associated read, the Register Map display is updated to reflect that the bits were not changed by the write attempt.

6.4 NVM Configuration Page

The NVM Configuration page (shown in Figure 6-9) is the main feature of the GUI and highlights the configurability of the PMIC. On this page, register fields are grouped according to the use case and are labeled to indicate which part of the PMIC is controlled by each block. The NVM configuration page also provides the interface to save a custom configuration or load an existing configuration into the NVM of the target device. A full register read can be done using the *READ ALL REGISTERS* button in the top left of the page.

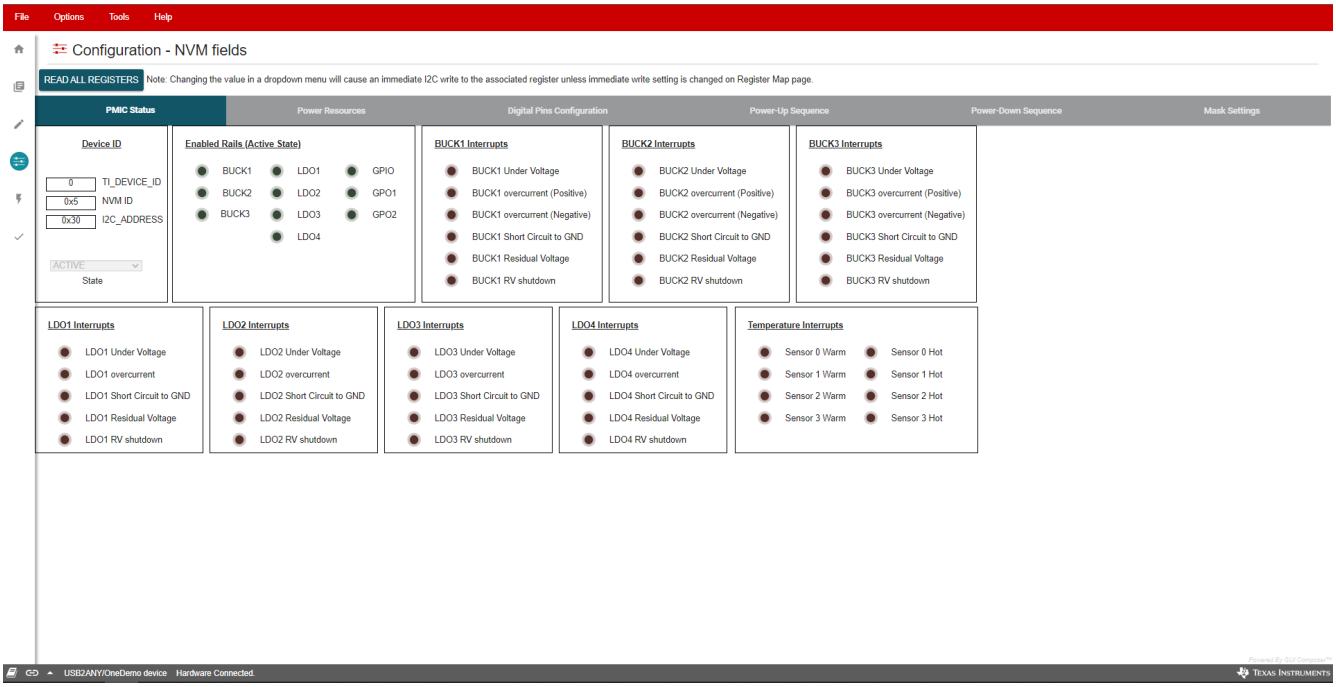


Figure 6-9. NVM Configuration Page

6.4.1 NVM Fields

Register settings can be changed on the NVM Configuration Page and follow the register write setting specified on the Register Map page (Immediate or Deferred).

The *PMIC Status* tab holds a collection of read-only status registers that show the Device ID values as well as all the power rail enables and interrupts, which are displayed as digital LEDs. This section provides fast visual feedback on the PMIC and the operating conditions.

The *Power Resources* tab holds register settings for each power rail of the PMIC. Here, users can also find a reference table for LDO1 and LDO2 configuration settings (for more information on the Load Switch and BYPASS modes, refer to the device data sheet which is included on the Collateral page).

The *Sequence* tab is used to control power rail sequence and timing registers for both power-up and power-down.

The *Digital Pins Configuration* tab is used to control settings for digital I/O pins (for details on multi-function pins, see the PMIC data sheet).

The *Mask Settings* tab allows users to control fault reporting for PMIC protection features, which includes masking for undervoltage, temperature, and interrupt signals.

6.4.2 Create and Load a Custom Configuration

The NVM Configuration page does not require hardware to develop an NVM configuration. Connection with an actual device is needed only when attempting to upload to a target device.

Once the registers are set to your desired configuration, use the *Register File Format* option, under the *File* tab at the top of the screen, to select a format for your configuration file (shown in Figure 6-10). A register configuration can be saved in either a CSV (Comma Separated Values) or a JSON (Javascript Object) format. Next, use the *Save Registers As…* option to save your configuration in your selected format. Once the file is created you can save any changes you make to the register configuration using the *Save Registers* option. This option saves to the currently loaded configuration.

To load an existing configuration into the NVM, use the *Load Registers* option and browse to the configuration file location.

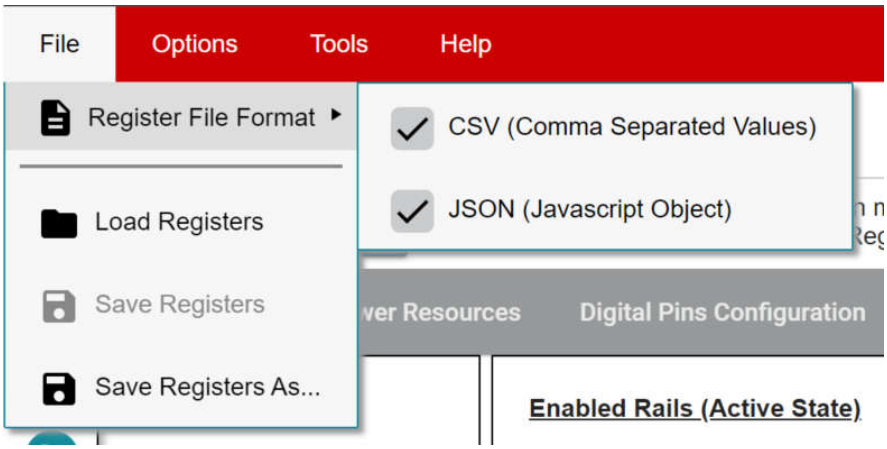


Figure 6-10. Save/Load Register Options

6.5 Sequence Configuration

The TPS65219 GUI features sequence configuration tabs for modifying and plotting the power-up and power-down sequences. The *power-up sequence* and *power-down sequence* tabs plot the voltage level of each signal as a function of time based on the corresponding settings.

Plotting Features

The features of the sequence configuration tabs is demonstrated in Figure 6-11.

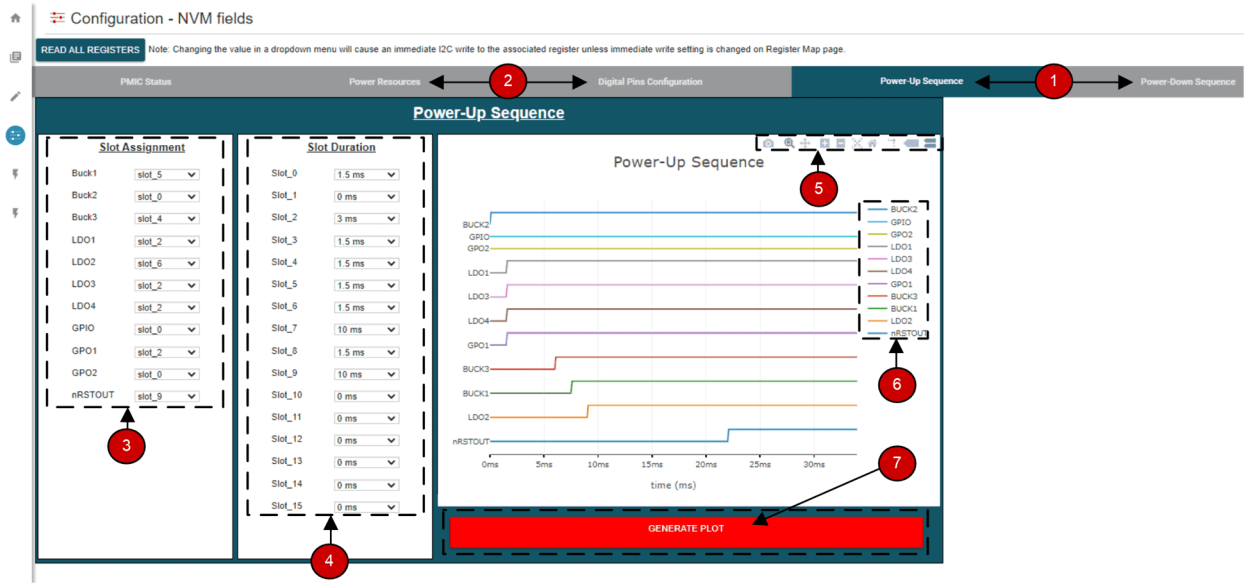


Figure 6-11. Sequence Plotting Tool

Note

Graph rise and fall time durations are not accurate. The actual rise and fall times dependent on load capacitance and other variables.

1. *Power-up sequence* and *power-down sequence* plotting tabs.
2. Rails disabled in active state always remain low when plotted. Configure these settings in the "*Power Resources* or *Digital Pins Configuration* tab.
3. Slot Assignment: The TPS65219 has 16 possible slot assignments (Slot 0 to Slot 15) which can be assigned to each rail for flexible power sequences.
4. Slot Duration: The TPS65219 has four possible slot durations (0ms, 1.5ms, 3ms, 10ms) which can be assigned to each slot for flexible power sequences.
5. Plot menu bar appears upon hovering over graph. This feature is explained in Menu bar Options
6. Click on a signal in the legend to change the visibility.
7. Plot the design by pressing the *Generate Plot* button. Signal order is sorted based on which signals rise or fall first

Menu bar Options

The plot menu bar has several settings including:

- Camera: Download Plot as PNG
- Zoom: Left click and drag the mouse on the graph to zoom into the selected area. Enabled by default.
- Pan: Left click and drag the mouse to navigate the plot.
- Zoom In
- Zoom Out
- Auto-Scale Graph
- Reset Axis
- Toggle Like Spikes
- Show Closest Data on Hover
- Compare Data on Hover. Enabled by default.

6.6 NVM Programming Page

The NVM Programming page allows re-programming the device NVM memory to change the default register settings. This page includes four main functions that correspond to the buttons shown in Figure 6-12. The first two steps *I2C OFF REQUEST* and *ENABLE I2C COMMUNICATION* are only needed when re-programming the PMIC from the Initialize state (PMIC rails OFF).

- The **I2C OFF REQUEST** button triggers an OFF request though I2C and sends the PMIC to INITIALIZE state.
- The **ENABLE I2C COMMUNICATION** button enables I2C communication in INITIALIZE state.
  - Once I2C communication is enabled, you can go to the NVM configuration page to select the desired register settings or use the *File* tab options to load a pre-configured JSON or CSV file.
- The **NVM PROGRAMMING** button programs the selected register settings into the NVM.
- The **VALIDATE NVM PROGRAMMING** button reads the NVM content and compares with the selected register settings. The result (PASS or FAIL) is stored in register 0x34, field 7 *NVM_VERIFY_RESULT*.

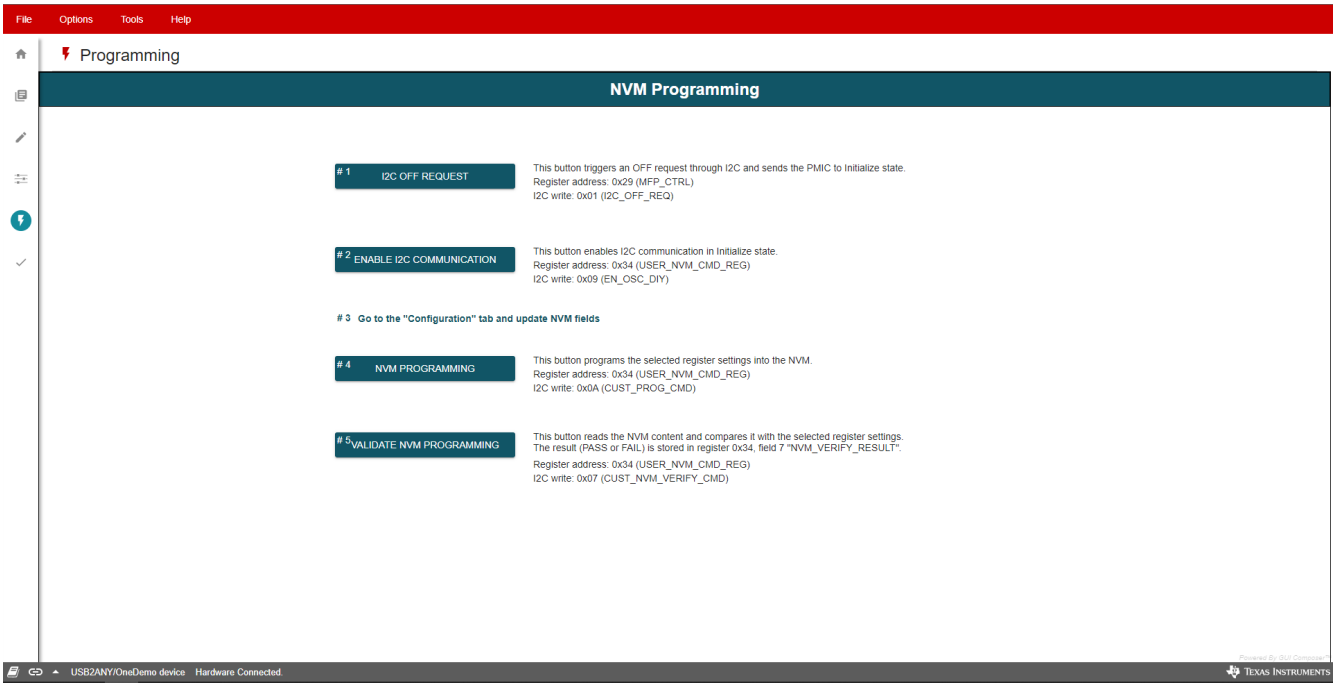


Figure 6-12. NVM Programming Page

6.7 Additional Features

In the Options tab at the top of the GUI interface, users can select *Serial Port…* to display information about the EVM connection to the computer.

The *Tools* tab includes the *Log pane* option. Select this option to open a window that lists recent messages and warnings from the GUI application. These reports are marked with the date and time that each one was received. In the top right of the log window, users can filter out the different information types, save the list of events, and clear or close the log window.

7 Schematics, PCB Layouts, and Bill of Materials

7.1 TPS65219EVM Schematic

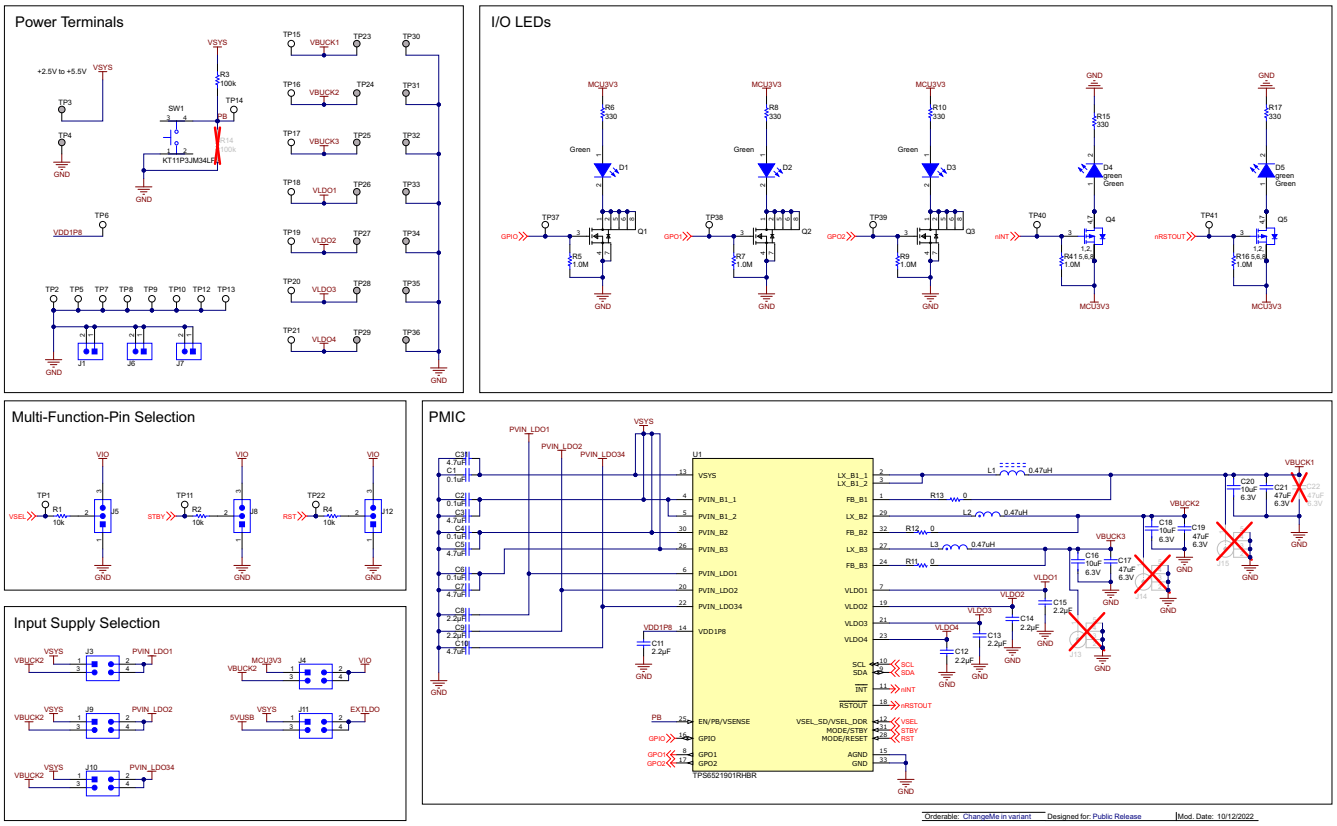


Figure 7-1. TPS65219EVM, Schematic Page 1

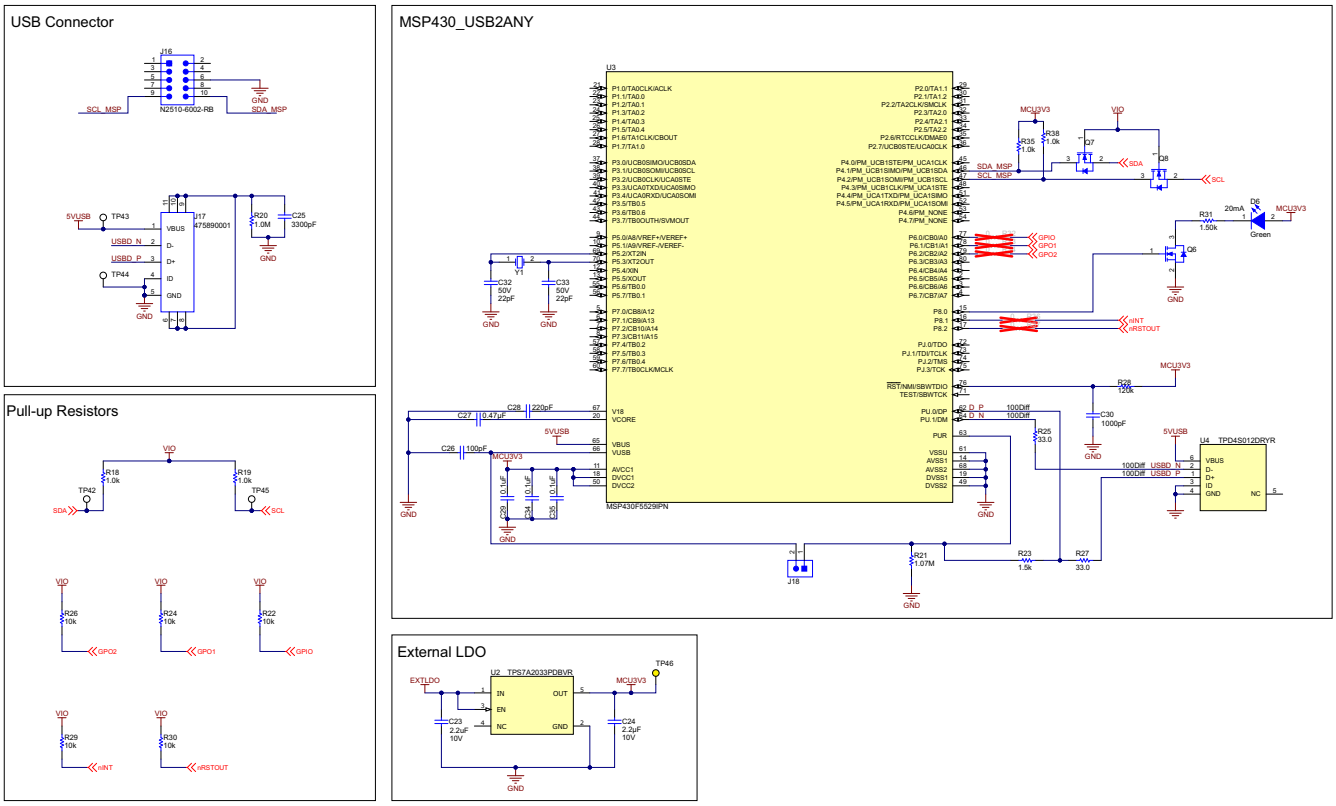


Figure 7-2. TPS65219EVM, Schematic Page 2

7.2 TPS65219EVM PCB Layers

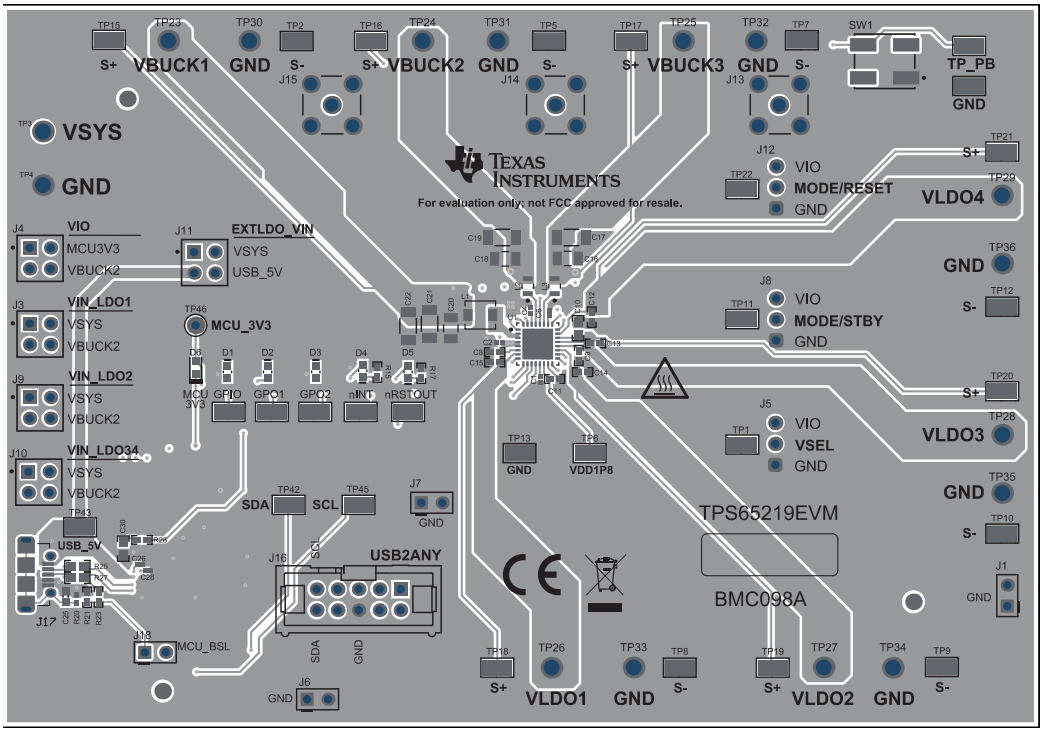


Figure 7-3. TPS65219EVM Top Layer

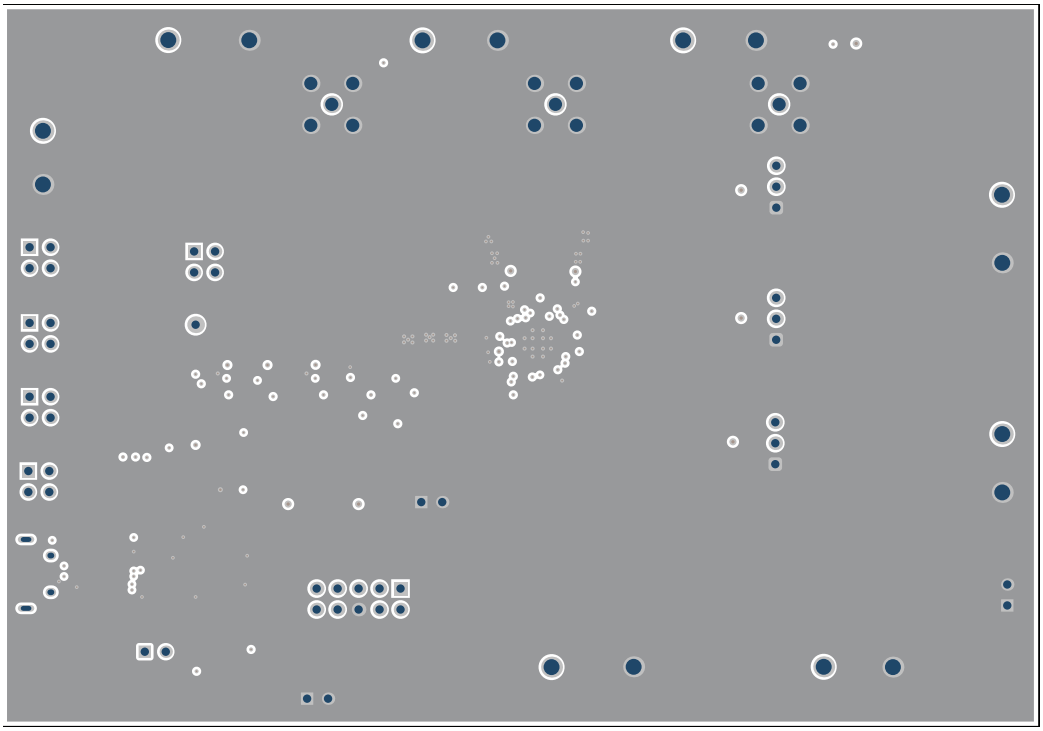


Figure 7-4. TPS65219EVM - Signal Layer1

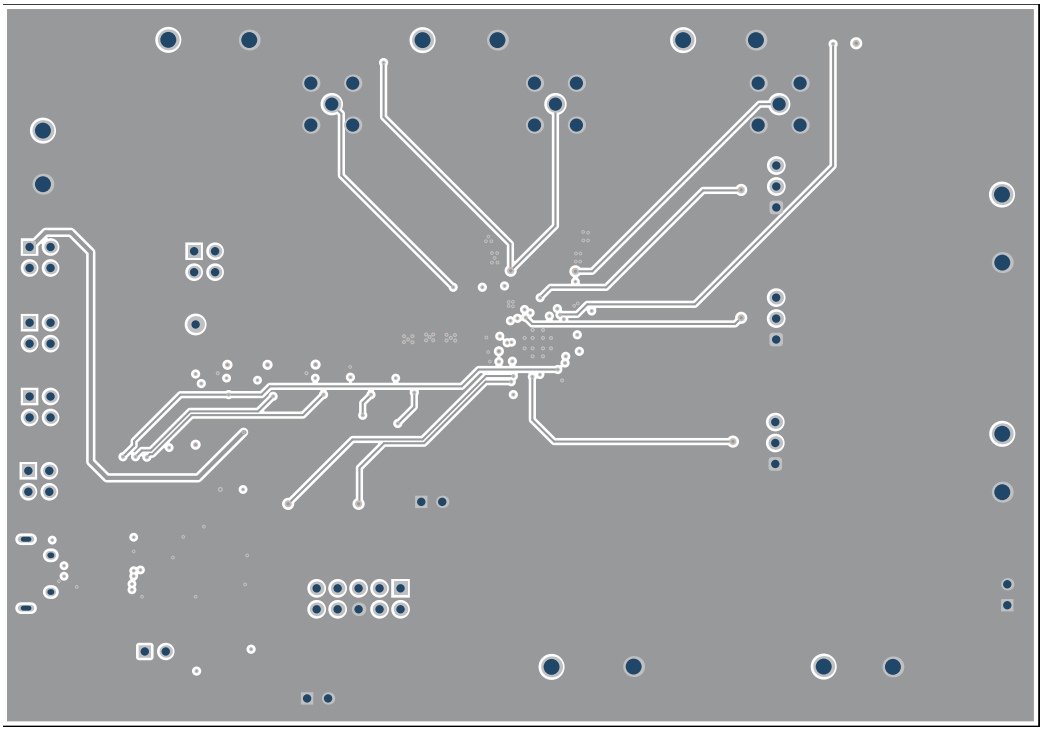


Figure 7-5. TPS65219EVM - Signal Layer2

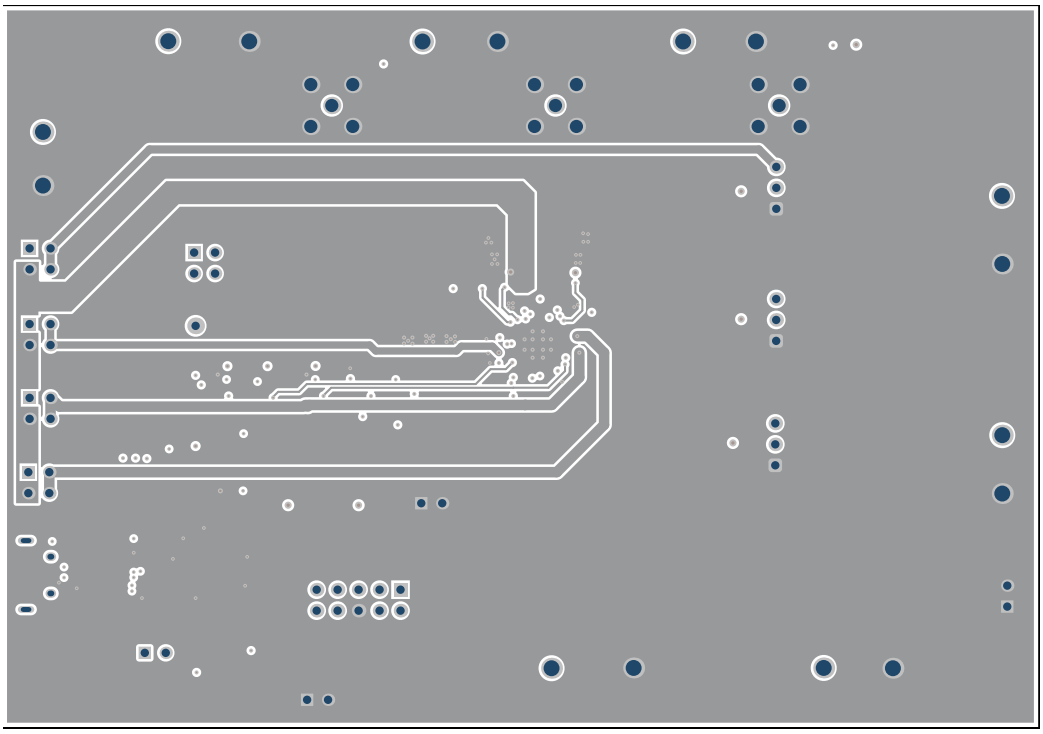


Figure 7-6. TPS65219EVM - Signal Layer3

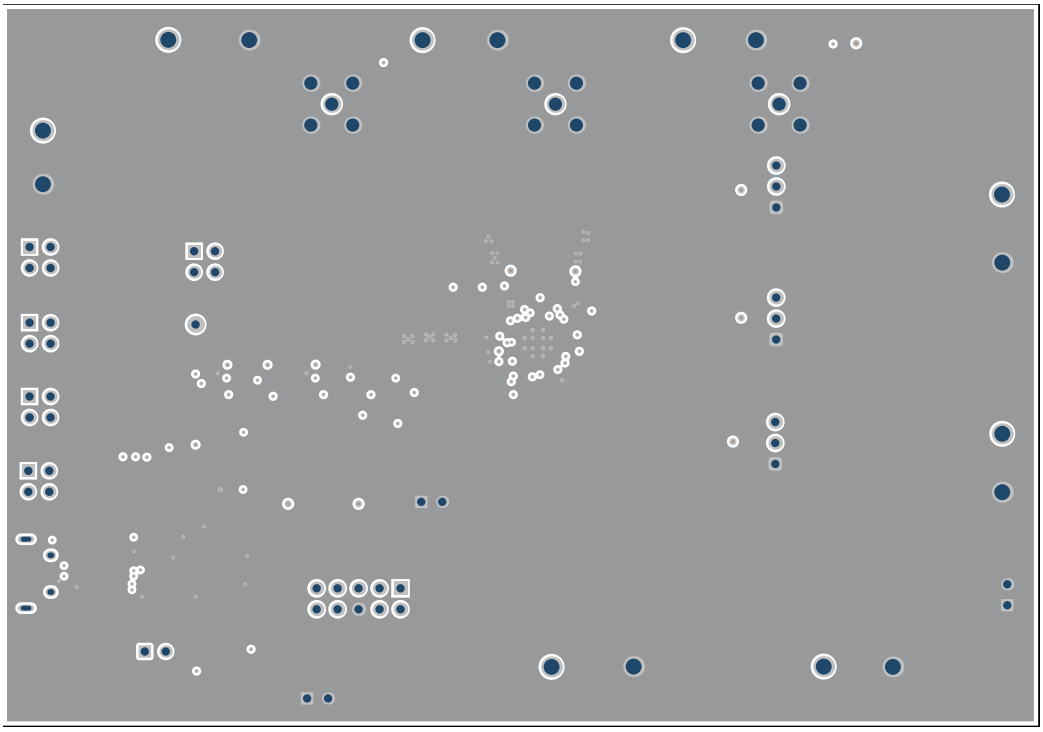


Figure 7-7. TPS65219EVM - Signal layer4

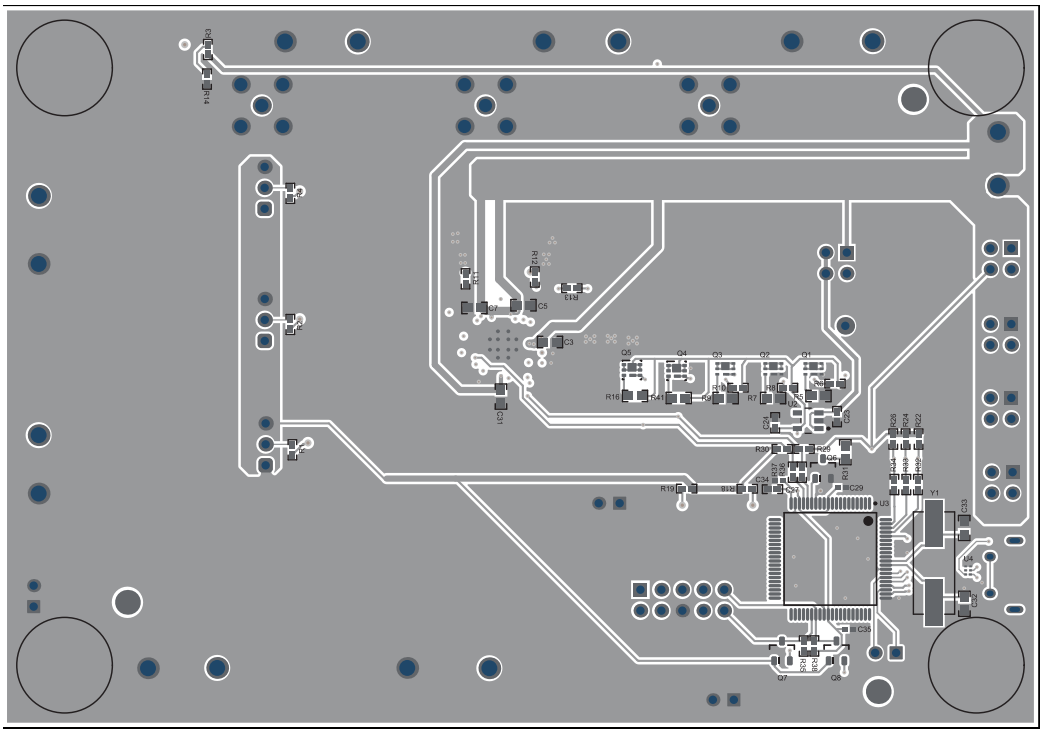


Figure 7-8. TPS65219EVM - Bottom Layer

7.3 TPS65219EVM Bill of Materials

Table 7-1. Bill of Materials

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
C1, C2, C7, C10	4	10uF	CAP, CERM, 10uF, 10V, +/- 20%, X5R, 0402	CL05A106MP5NUNC	Samsung Electro-Mechanics
C3, C4	2	22uF	CAP, CERM, 22uF, 6.3V, +/- 20%, X5R, 0603	GRM188R60J226MEA0D	MuRata
C5, C11	2	1uF	CAP, CERM, 1uF, 35V, +/- 20%, X5R, 0402	GRM155R6YA105ME11D	MuRata
C6	1	150uF	CAP, TA, 150uF, 6.3V, +/- 20%, 0.025 ohm, SMD	T520B157M006ATE025	Kemet
C8, C9	2	0.1uF	CAP, CERM, 0.1uF, 10V, +/- 20%, X5R, 0402	885012105010	Wurth Elektronik
C12, C13, C14, C17	4	4.7uF	CAP, CERM, 4.7uF, 10V, +/- 10%, X7S, 0603	C1608X7S1A475K080AC	TDK
C15, C16, C18, C19, C27, C28, C29, C30	8	2.2uF	CAP, CERM, 2.2uF, 10V, +/- 10%, X7S, 0402	C1005X7S1A225K050BC	TDK
C20, C22, C23	3	10µF	Cap Ceramic 10uF 6.3V X7R ±10% SMD 1206 +125°C Embossed T/R	CL31B106KQHNFNE	Samsung
C21, C25, C26	3	47uF	CAP, CERM, 47uF, 6.3V, +/- 20%, X7S, 1206	C3216X7S0J476M160AC	TDK
C31	1	3300pF	CAP, CERM, 3300pF, 50V, +/- 10%, X7R, 0603	C0603C332K5RACTU	Kemet
C32	1	100pF	CAP, CERM, 100pF, 16V, +/- 10%, X7R, 0201	GRM033R71C101KA01D	MuRata
C33	1	0.47uF	CAP, CERM, 0.47µF, 16V,+/- 10%, X7S, 0402	CGA2B1X7S1C474K050BE	TDK
C34	1	220pF	CAP, CERM, 220pF, 16V, +/- 10%, X7R, 0201	GRM033R71C221KA01D	MuRata
C35, C38, C39	3	0.1uF	CAP, CERM, 0.1uF, 16V, +/- 10%, X7R, 0402	GCM155R71C104KA55D	MuRata
C36	1	1000pF	CAP, CERM, 1000pF, 50V, +/- 10%, X7R, 0603	C0603C102K5RACTU	Kemet
C37, C40	2	22pF	CAP, CERM, 22pF, 50V, +/- 5%, C0G/NP0, 0603	06035A220JAT2A	AVX
D1, D2, D3, D5	4	Green	LED, Green, SMD	LG L29K-G2J1-24-Z	OSRAM
D4	1		Red 631nm LED Indication - Discrete 2.2V 0603 (1608 Metric)	HSMZ-C190	Broadcom
D6	1	Red	Red 631nm LED Indication - Discrete 2.2V 0603 (1608 Metric)	HSMZ-C190	Broadcom
D7	1	Green	LED, Green, SMD	150060VS75000	Wurth Elektronik
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	SJ-5303 (CLEAR)	3M
H5	1		IC to place in Socket XU1	TPS6521905RHBR	Texas Instruments
J1	1		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	Sullins Connector Solutions
J2, J3, J4, J5, J6	5		Header, 100mil, 2x2, Tin, TH	PEC02DAAN	Sullins Connector Solutions
J7	1		Header, 100mil, 3x2, Gold, TH	TSW-103-07-G-D	Samtec
J8, J9, J10	3		Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec
J11	1		Connector, Receptacle, Micro-USB Type AB, R/A, Bottom Mount SMT	475890001	Molex
J12	1		Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH	N2510-6002-RB	3M

Table 7-1. Bill of Materials (continued)

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
J13, J14, J15	3		Header, 100mil, 2x1, Tin, TH	PEC02SAAN	Sullins Connector Solutions
L1	1	240nH	Inductor, Shielded, Metal Composite, 240nH, 5A, 0.019 ohm, SMD	DFE201612E-R24M=P2	MuRata
L2, L4	2	0.47uH	Thin Film Power Inductor 0.47uH 20% 4.5A 29mOhm 0805	TFM201208BLE-R47MTCF	TDK
L3	1	0.47uH	470 nH Shielded Wirewound Inductor 7A 23mOhm Max 2-SMD	SRP3020TA-R47M	Bourns
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
Q1, Q2, Q3	3		30V N-Channel NexFET? Power MOSFET	CSD17318Q2	Texas Instruments
Q4, Q5	2	-20V	MOSFET, P-CH, -20 V, -20 A, DQK0006C (WSON-6)	CSD25310Q2	Texas Instruments
Q6, Q7, Q8	3	50V	MOSFET, N-CH, 50V, 0.22A, SOT-23	BSS138	Fairchild Semiconductor
R1, R4, R7, R9, R13	5	1.0Meg	RES, 1.0M, 5%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW06031M00JNEA	Vishay-Dale
R2, R5, R8, R11, R14	5	330	RES, 330, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402330RJNED	Vishay-Dale
R3, R6, R40	3	100k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	ERJ-2GEJ104X	Panasonic
R10, R26	2	1.5k	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04021K50JNED	Vishay-Dale
R12	1	205k	RES, 205 k, 1%, 0.1 W, 0603	RC0603FR-07205KL	Yageo
R15	1	680	RES, 680, 5%, 0.1 W, 0603	RC0603JR-07680RL	Yageo
R16, R17, R18, R25, R27, R29, R32, R33	8	10k	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040210K0JNED	Vishay-Dale
R20, R21, R38, R39	4	1.0k	RES, 1.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04021K00JNED	Vishay-Dale
R23	1	1.0Meg	RES, 1.0M, 5%, 0.063W, AEC-Q200 Grade 0, 0402	CRCW04021M00JNED	Vishay-Dale
R24	1	1.07Meg	RES, 1.07M, 1%, 0.063W, AEC-Q200 Grade 0, 0402	CRCW04021M07FKED	Vishay-Dale
R28, R30	2	33	RES, 33.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060333R0FKEA	Vishay-Dale
R31	1	120k	RES, 120 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402120KJNED	Vishay-Dale
R34	1	1.50k	RES, 1.50 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K50FKEA	Vishay-Dale
S1	1		Switch, Slide, SPDT, 0.2A, J Lead, SMD	CL-SB-12A-01T	Copal Electronics
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J12	11	1x2	Shunt, 100mil, Flash Gold, Black	SPC02SYAN	Sullins Connector Solutions
SW1	1		Switch Tactile N.O. SPST Round Button J-Bend 32VAC 32VDC 1VA 100000Cycles 3N SMD Tube/T/R	KT11P3JM34LFS	C&K Components
TP1, TP2, TP9, TP11, TP13, TP15, TP17, TP19, TP22, TP29, TP30, TP31, TP32, TP33, TP41, TP42	16		PCB Pin, Swage Mount, TH	2505-2-00-44-00-00-07-0	Mill-Max

Table 7-1. Bill of Materials (continued)

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
TP3, TP4, TP5, TP6, TP7, TP8, TP10, TP12, TP14, TP16, TP18, TP20, TP23, TP27, TP28, TP34, TP35, TP36, TP37, TP38, TP39, TP40, TP43, TP44, TP45, TP46, TP47, TP50	28		Test Point, Miniature, SMT	5015	Keystone
TP21	1		Test Point, Multipurpose, Yellow, TH	5014	Keystone
U1	1		2.4V to 5.5V Input, 6A Step-Down Converter in 1.5mm x 2.5mm QFN Package	TPS62867RQY	Texas Instruments
U2, U3	2		5.5V, 2A, 38m? Load Switch With Quick Output Discharge, YFP0004AAAA (DSBGA-4)	TPS22915CYFPR	Texas Instruments
U4	1		25MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	MSP430F5529IPN	Texas Instruments
U5	1		4-Channel USB ESD Solution with Power Clamp, DRY0006A (USON-6)	TPD4S012DRYR	Texas Instruments
XU1	1		Socket, QFN-32, 0.5mm pitch, TH	QFN-32_40_BT-0.5-02-00	Enplas Tech Solutions
Y1	1		Crystal, 24.000MHz, 20pF, SMD	ECS-240-20-5PX-TR	ECS Inc.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2022) to Revision A (September 2024)	Page
• Updated to reflect the new EVM revision throughout the document	1

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

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