Application Note

12 VIN to 1 VOUT Single Phase Buck Converter Using TPS7H5001-SP Controller

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ABSTRACT

The TPS7H5001-SP EVM uses the TPS7H5001-SP and LMG1210 to create a synchronous buck converter to bring the 12-V intermediate rail into a 1-V rail at high current for core voltage rails of space grade FPGAs.

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Trademarks

1 Introduction

The TPS7H5001-SP EVM uses the TPS7H5001-SP and LMG1210 to create a synchronous buck converter to bring the 12-V intermediate rail into a 1-V rail at 20-A for core voltage rails of space grade FPGAs. The limiter of the output current in the design is the bottom side GaN FET heat. The output current of this design can be increased by adding a second GaN FET in parallel on the bottom side in order to achieve higher than 20-A of output current. Due to the roughly 150-mA peak current capability of the TPS7H5001's primary switching outputs, the LMG1210 gate driver is used to amplify the current to provide the FET's of the synchronous buck with sufficient drive. These outputs are not dependent on the TPS7H5001-SP itself, and can be increased or decreased depending on the design.

2 System Design Theory

Throughout the design process of the converter equations were used to determine the values to start with. Note that sometimes the value in this section do not exactly match what is shown in the schematic. Most of the time, this is due to rounding caused by values available in lab.

2.1 Switching Frequency

Choosing a switching frequency has a tradeoff between efficiency and bandwidth. Higher switching frequencies have larger bandwidth, but a lower efficiency than lower switching frequencies. First, the maximum switching frequency for the requirements had to be calculated. For the calculation, the minimum on time for the device was determined by adding 75 ns for controller on time and 100 ns of LEB.

$$f_{sw\_max} = \frac{1}{T_{sw\_max}} = \frac{Duty\ Cycle}{t_{min\_on\_time}} = \frac{0.0833}{175\ ns} = 476\ kHz \quad (1)$$

To make sure the max switching frequency was not approached, the switching frequency was set to 400 kHz. Using equations provided by the data sheet for the TPS7H5001-SP, the RT resistor was chosen to be 260 k. The equation for the switching frequency used is Equation 2.

$$RT = \frac{112{,}000}{f_{sw}\,(kHz)} - 19.7 = \frac{112{,}000}{399\ kHz} - 19.7 = 261\ k\Omega \quad (2)$$

2.2 Leading Edge Blanking

Leading edge blank time is utilized to remove any transient noise from the current sensing loop after the primary switching outputs, OUTA or OUTB, go high. The leading-edge blank time was selected to be 100 ns. Equation 3 shows the calculation to program the LEB resistor for a chosen LEB time:

$$R_{LEB} = 1.212\ x\ LEB - 9.484 = 1.212\ x\ 100\ ns - 9.484 = 112\ k\Omega \quad (3)$$

2.3 Dead Time

The TPS7H5001-SP allows for the user to program two independent dead times. This allows for the dead times to be optimized by the user to prevent shoot-through between the primary and synchronous switches while attaining the best possible converter efficiency. The equation for determining the values of and for a desired dead time is shown in Equation 4.

$$R_{PS} = R_{SP} = 1.207\ x\ DT - 8.858 = 1.207\ x\ 25\ ns - 8.858 = 21.3\ k\Omega \quad (4)$$

2.4 Enable and UVLO

The TPS7H5001-SP EVM uses two resistors to program the controller to enable the device when VIN surpasses a user determined threshold. The two resistors are configured as a divider, with one between VIN and EN and the other between EN and AVSS. Using Equation 5, the user can calculate the value for a chosen value of . Once the resistor values are determined, Equation 6 can be used to determine the minimum startup voltage.

$$R_{UVLO\_TOP} = R_{UVLO\_Bottom}\left(\frac{V_{Start\_Max}}{V_{EN\_Rising\_Max}} - 1\right) = \left(\frac{10\ V}{0.65\ V} - 1\right) = 71.9\ k\Omega \quad (5)$$

$$V_{START,\,MIN} = V_{EN\_FALLING\_MIN}\left(\frac{R_{UVLO\_TOP}}{R_{UVLO\_BOT}} + 1\right) = \left(\frac{75\ k\Omega}{5\ k\Omega} + 1\right) = 16\ V \quad (6)$$

2.5 Output Voltage Programing

The output voltage of the power converter is set by using a resister divider from of the converter to the VSENSE pin. For a selected value of , the value of can be found using Equation 7.

$$Rbottom = \frac{V_{ref}}{Vout - V_{ref}} x\ Rtop = \frac{0.613\ V}{1\ V\ -\ 0.613\ V} x\ 10\ k\Omega = 15.8\ k\Omega \quad (7)$$

2.6 Soft Start

Using a capacitor between the soft start (SS) pin and AVSS, the soft start of the device is programmed. Equation 8 shows the calculation of the SS capacitor:

$$Css = \frac{t_{ss}\ x\ I_{ss}}{V_{ref}} = \frac{12\ ms\ x\ 2.7\ \mu A}{0.613\ V} = 52.9\ nF \quad (8)$$

2.7 Sensing Circuit

The sensing circuit of the buck converter was set-up with a similar time period to the inductance and parasitic resistance of the output inductor. This process allows for a triangle wave similar to the output current to be generated from a resistor and capacitor in parallel with the output inductor.

2.8 FAULT Mode

FAULT mode was disabled by connecting the pin to AVSS.

2.9 HICCUP Mode

For the design, the value of the hiccup capacitor used is 100 nF. Based on this value, the delay and hiccup times of the converter after an overcurrent are detected can be calculated using Equation 9 and Equation 10, respectively.

$$t_{delay} = \frac{C_{HICC}\ x\ 0.6\ V}{80\ \mu A} = \frac{100\ nF\ x\ 0.6\ V}{80\ \mu A} = 75\ \mu s \quad (9)$$

$$t_{HICC} = \frac{C_{HICC}\ x\ (1\ V - 0.3\ V)}{1\ \mu A} = \frac{100\ nF\ x\ (1\ V - 0.3\ V)}{1\ uA} = 70\ ms \quad (10)$$

2.10 Slope Compensation

To avoid errors associated with subharmonic oscillation as well as give noise immunity, slope compensation is used. The signal of the current ramp from the current sense was small enough that a large amount of slope

compensation was needed to give the needed noise immunity to the circuit. These factors lead to 75 k Ohms being used for the RSC resistor.

2.11 Output Capacitance

The output capacitance value is picked such that there is enough capacitance for the required voltage ripple and output current load step. **Equation 17** shows the calculation to find the amount of capacitance required to meet the maximum allowable voltage deviation at the output in response to a worst-case load transient. **Equation 19** determines the amount of output capacitance that is needed to meet the output voltage ripple requirements of the design.

$$C_{OUT} > \frac{\Delta I_{STEP}}{2\pi \, x \, \Delta V_{OUT} \, x \, f_C} = \frac{\Delta \, 6.67 \, A}{2\pi \, x \, 20 \, mV \, x \, 10 \, kHz} = 5.31 \, mF \quad (11)$$

$$C_{OUT} > \frac{I_{OUT} \, x \, D_{MAX}}{V_{RIPPLE} \, x \, f_{sw}} = \frac{20 \, x \, 0.0833}{5 \, mV \, x \, 400 \, kHz} = 1.67 \, mF \quad (12)$$

2.12 Compensation

Before the compensator component values can be found, the power stage transconductance was calculated as shown in Equation 13.

$$gm_{ps} = \frac{R_{CS} \, x \, C_{CS} \, x \, f_{SW}}{L_{OUT}} = \frac{1 \, k\Omega \, x \, 100 \, nF}{560 \, nH} = 179 \quad (13)$$

The following equations were used to achieve the desired crossover frequency, and values used as a starting value. These values were optimized during lab testing and movement of the poles and zeros further out in frequency were determined to work better for the converter as a whole.

$$R_{COMP} = \frac{2\pi \, x \, f_C \, x \, V_{OUT} \, x \, C_{OUT}}{gm_{ea} \, x \, V_{REF} \, x \, gm_{ps}} = \frac{2\pi \, x \, 10 \, kHz \, x \, 1 \, V \, x \, 5 \, mF}{1800 \, \mu S \, x \, 0.613 \, V \, x \, 179 \, S} = 1.590 \, k\Omega \quad (14)$$

$$C_{COMP} = \frac{V_{OUT} \, x \, C_{OUT}}{I_{OUT} \, x \, R_{COMP}} = \frac{1 \, V \, x \, 5 \, mF}{20 \, x \, 1.59 \, k\Omega} = 157 \, nF \quad (15)$$

$$f_{esr} = \frac{1}{2\pi \, x \, C_{OUT} \, x \, ESR} = \frac{1}{2\pi \, x \, 5 \, mF \, x \, 0.4 \, m\Omega} = 79.6 \, kHz \quad (16)$$

$$C_{HF} = \frac{1}{2\pi \, x \, R_{comp} \, x \, f_{esr}} = \frac{1}{2\pi \, x \, 1.59 \, k\Omega \, x \, 79.6 \, kHz} = 1.26 \, nF \quad (17)$$

3 Test Results

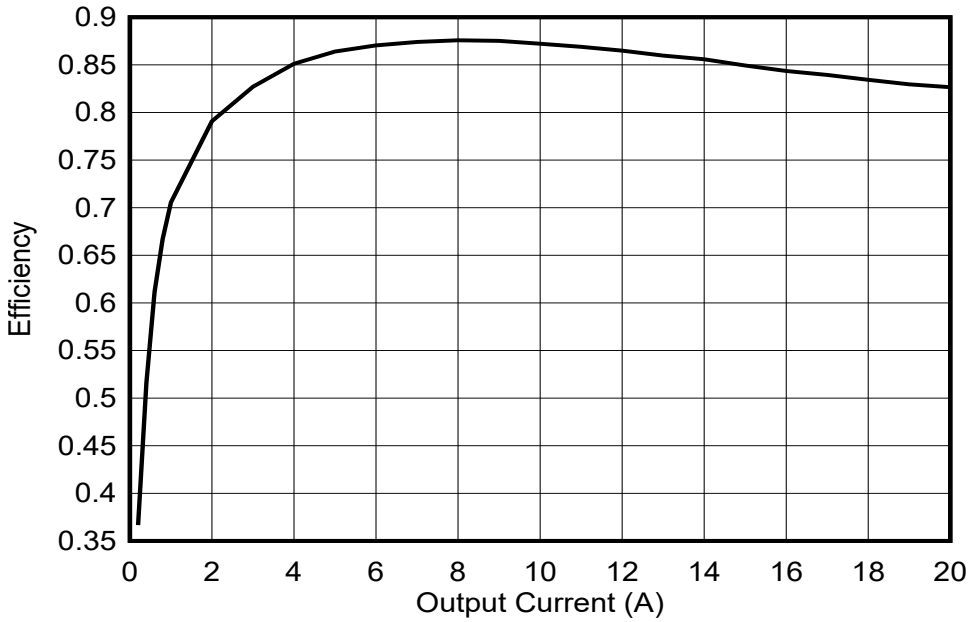


Figure 3-1. Efficiency vs. Current

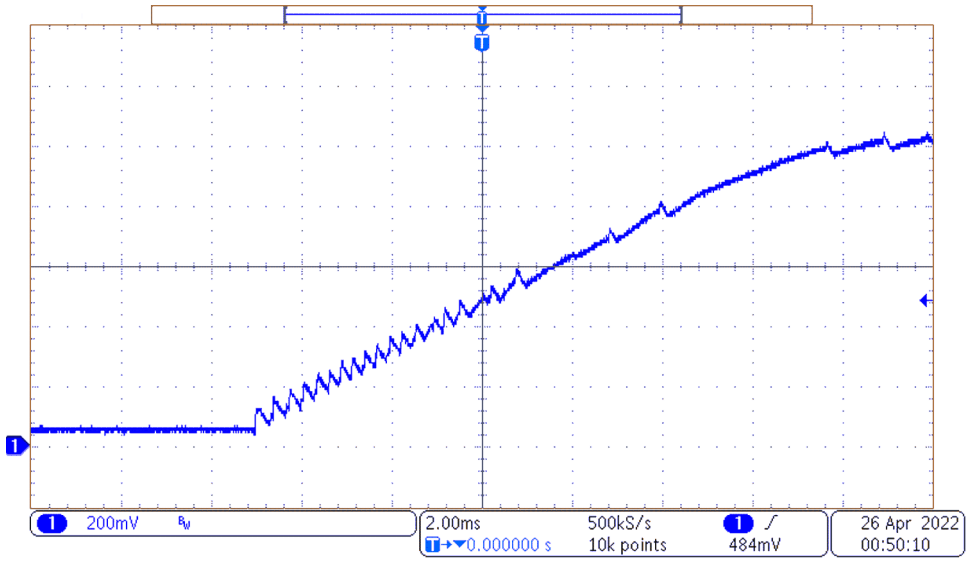


Figure 3-2. Start-up Unloaded

Figure 3-2 shows start-up of the converter when unloaded. The first 4 ms of start-up are choppy due to the minimum on-time of the converter. When the minimum on-time of the converter is smaller than the duty cycle used during parts of start-up choppiness can occur.

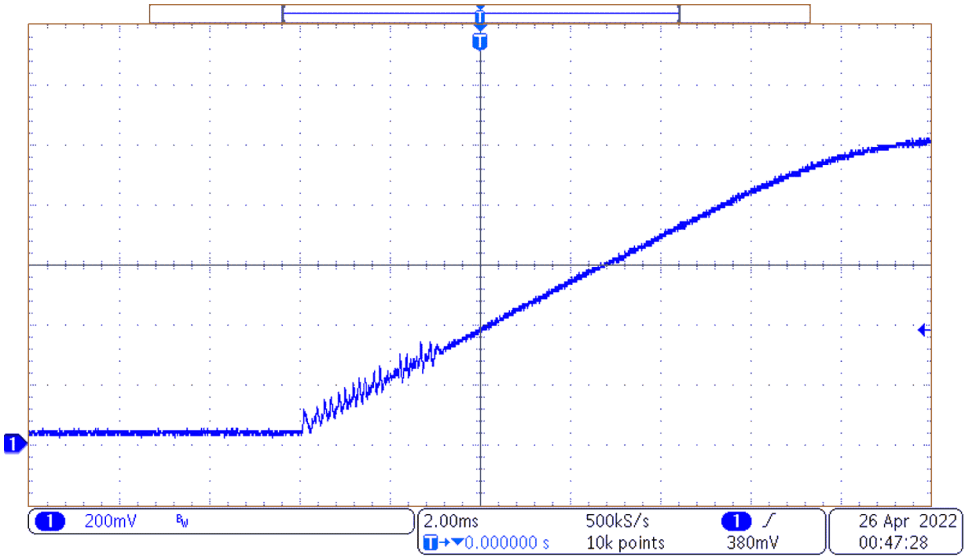


Figure 3-3. Start-up Loaded

Figure 3-3 shows start-up of the converter when loaded with 20 A for the output current. The first 4 ms of start-up are choppy due to the minimum on-time of the converter. When the minimum on-time of the converter is smaller than the duty cycle used during parts of start-up choppiness will occur.

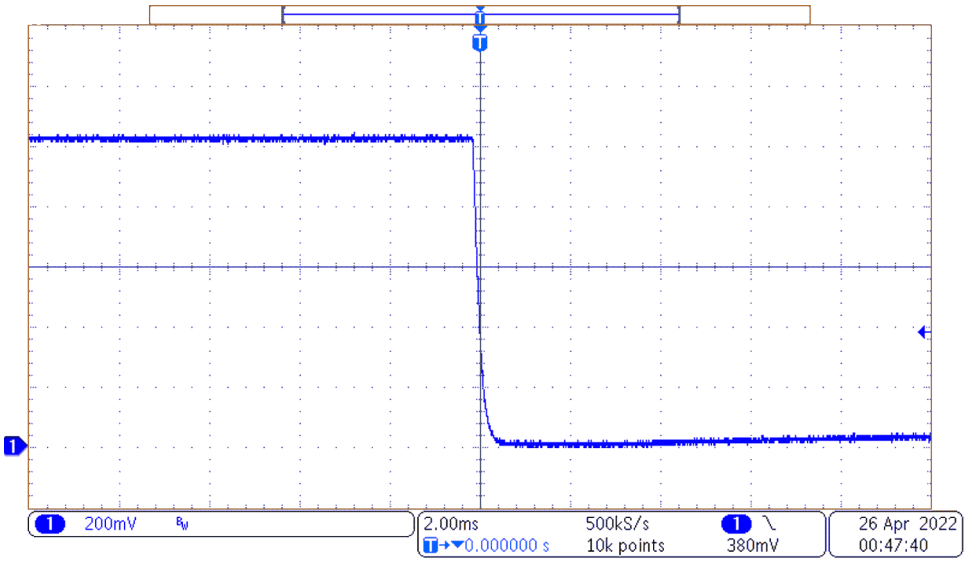


Figure 3-4. Shutdown

Figure 3-4 shows shutdown of the converter when loaded with 20 A on the output current.

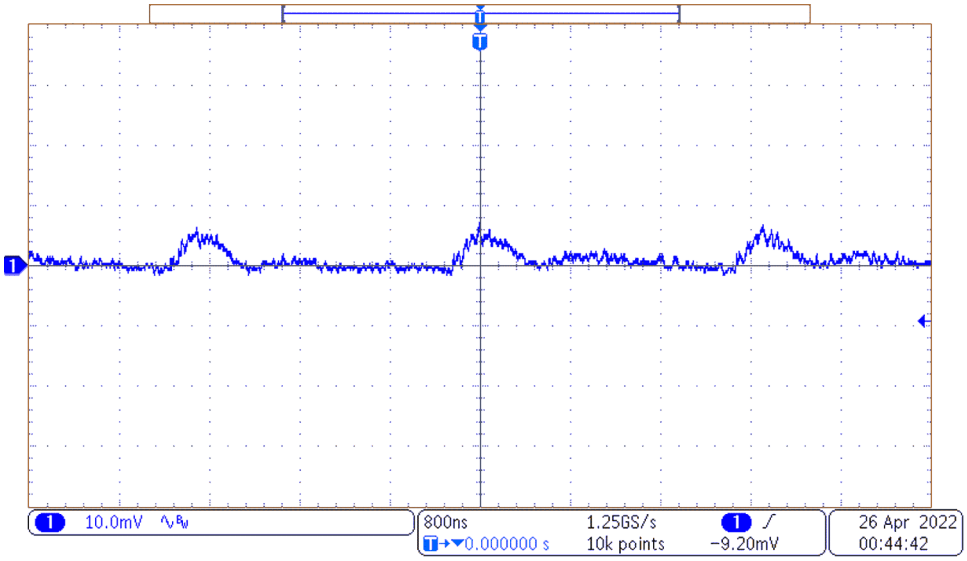


Figure 3-5. Output Voltage Ripple

Figure 3-5 shows the output voltage ripple with an output current of 20 A.

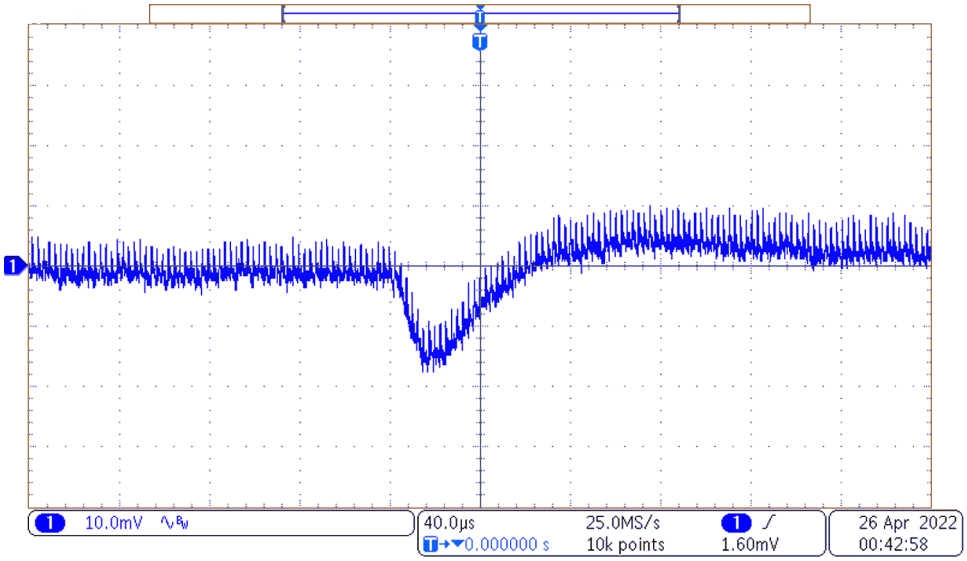


Figure 3-6. Positive Load Step

Figure 3-6 shows the output voltage dip of the converter to a 6.67 positive output current transient.

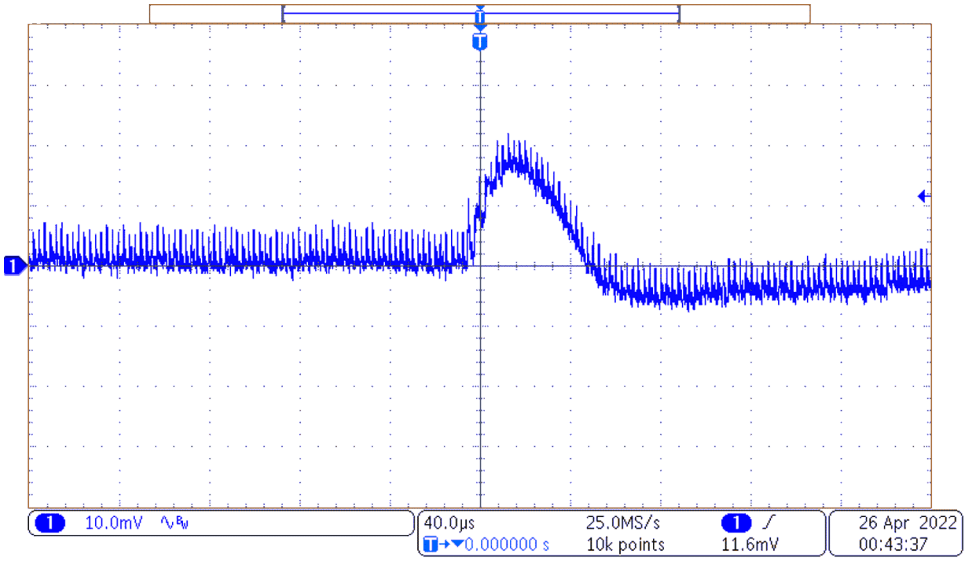


Figure 3-7. Negative Voltage Transient

Figure 3-7 shows the output voltage dip of the converter to a 6.67 positive output current transient.

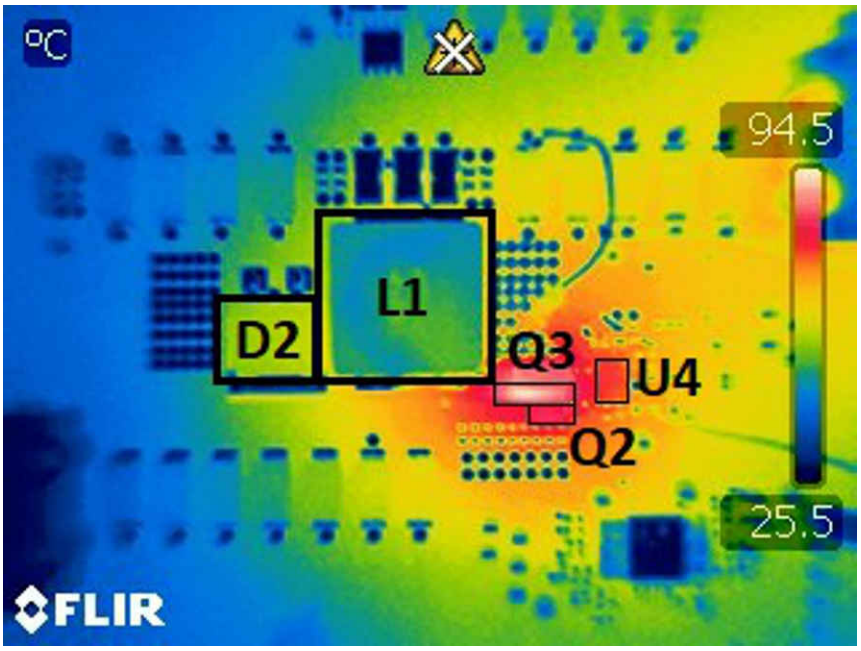


Figure 3-8. Thermal Image of Board with 20 A Output Current

Figure 3-8 shows the thermal image of the board with 20 A output current. The main hot spot of the picture is the bottom side GaN FET. This is the main limiter of the output current. It is suggested to achieve a larger output current that a second GaN FET be put in parallel on the bottom side.

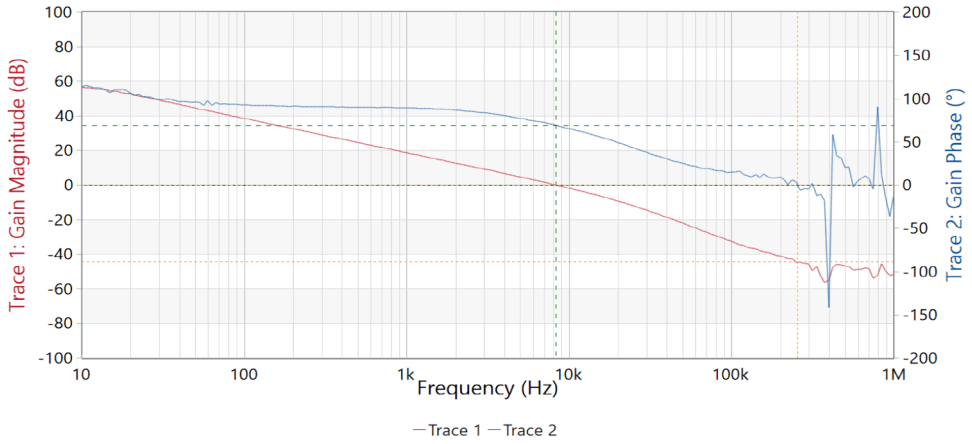


Figure 3-9. Frequency Response

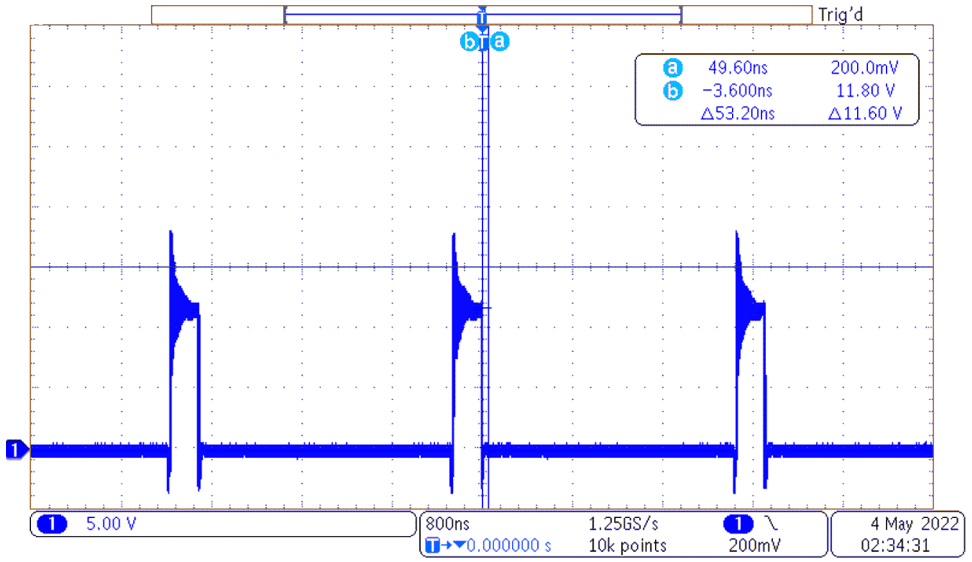


Figure 3-10. Switch Node Voltage with Full Output Current

Figure 3-10 shows the maximum voltage on the switch node of the converter with an output current of 20 A.

4 Bill of Materials

Table 4-1. Buck Converter Design BOM

Designator	Quantity	Value	Description	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
!PCB1	1		Printed Circuit Board	XXX###	Any		
C1, C10, C29, C31	4	1uF	CAP, CERM, 1 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E1X7R1C105K080AC	TDK		
C2	1	10uF	CAP, CERM, 10 uF, 50 V, +/- 10%, X7R, 1210	GRM32ER71H106KA12L	MuRata		
C3, C23, C24, C25, C26, C27, C28, C55, C56, C57	10	0.1uF	CAP, CERM, 0.1 µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	C0603C104K5RACAUTO	Kemet		
C4	1	0.47uF	CAP, CERM, 0.47 µF, 25 V,+/- 10%, X7R, 0603	C1608X7R1E474K080AE	TDK		
C5	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	C0603C104J3RAC	Kemet		
C6	1		3300pF ±5% 100V Ceramic Capacitor X7R 0603 (1608 Metric)	06031C332J4Z2A	AVX Corporation		
C7	1	330pF	CAP, CERM, 330 pF, 100 V, +/- 10%, X7R, 0603	GRM188R72A331KA01D	MuRata		
C8	1	0.056uF	CAP, CERM, 0.056 uF, 16 V, +/- 5%, X7R, 0603	C0603C563J4RACTU	Kemet		
C9	1		CAP, 1uF, 25V, ±10%, X7R, 0603	CL10B105KA8NNNC	Samsung		
C11, C14, C52	3	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	CEU4J2X7R1H104K125AE	TDK		
C16, C17, C18, C19, C20, C21, C22	7	220uF	CAP, TA, 220 µF, 16 V, +/- 10%, 0.025 ohm, SMD	TPME227K016R0025	AVX		
C30, C47, C48, C49, C50	5	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 0805	GRM21BZ71E106KE15L	MuRata		
C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46	15	330uF	CAP, Tantalum Polymer, 330 uF, 10 V, +/- 20%, 0.006 ohm, 7343-43 SMD	T530X337M010ATE006	Kemet		
C51	1	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0805	C0805C105K4RACTU	Kemet		
C53	1	2.2uF	CAP, CERM, 2.2 uF, 50 V, +/- 10%, X7R, 0805	UMK212BB7225KG-T	Taiyo Yuden		
C54	1	4.7uF	CAP, CERM, 4.7 uF, 25 V, +/- 10%, X7R, 0805	C2012X7R1E475K125AB	TDK		
D1	1	100V	Diode, Schottky, 100 V, 0.25 A, SOD-123F	BAT46WH,115	Nexperia		
D2	1		Schottky Barrier Diode 30V 40A 3-Pin TO-263S Emboss T/R	RB238NS-30TL	ROHM		

Table 4-1. Buck Converter Design BOM (continued)

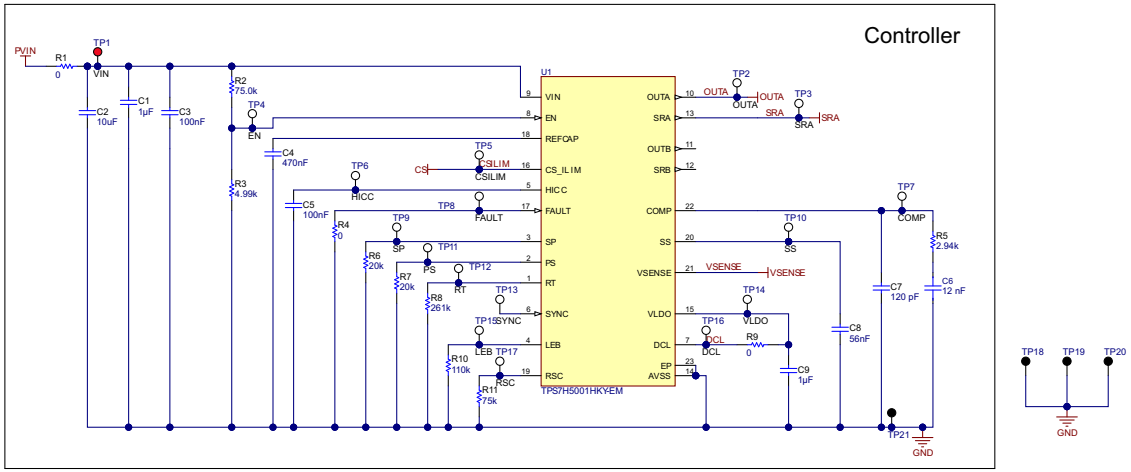
Designator	Quantity	Value	Description	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B&F Fastener Supply		
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone		
J1, J3	2		Compact Probe Tip Circuit Board Test Points, TH, 25 per	131-5031-00	Tektronix		
J2, J4	2		Fixed Terminal Blocks MKDSP 10 HV/ 2-10	1929517	Phoenix Contact		
L1	1	560nH	Inductor, Shielded, Powdered Iron, 560 nH, 61 A, 0.00091 ohm, SMD	IHLP6767GZERR56M11	Vishay-Dale		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady		
Q1	1	30V	MOSFET, N-CH, 30 V, 100 A, DQH0008A (VSON-CLIP-8)	CSD17559Q5	Texas Instruments		None
Q2	1		N-Channel Enhancement Mode Power Transistor ID 60A 100 V - - Surface Mount Die	EPC2218	EPC		
Q3	1	30V	MOSFET, N-CH, 30 V, 60 A, 6.05x2.3mm	EPC2023ENGR	EPC		None
R1, R4, R9, R25, R26, R27, R28, R35	8	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	RMCF0603ZT0R00	Stackpole Electronics Inc		
R2	1	75.0k	RES, 75.0 k, 1%, 0.1 W, 0603	RC0603FR-0775KL	Yageo		
R3	1	4.99k	RES, 4.99 k, 1%, 0.1 W, 0603	RC0603FR-074K99L	Yageo		
R5	1	35.7k	RES, 35.7 k, 1%, 0.1 W, 0603	RC0603FR-0735K7L	Yageo		
R6, R7	2	30.0k	RES, 30.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3EKF3002V	Panasonic		
R8	1	261k	RES, 261 k, 0.1%, 0.1 W, 0603	RT0603BRD07261KL	Yageo America		
R10	1	110k	RES, 110 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603110KFKEA	Vishay-Dale		
R11	1	887k	RES, 887 k, 1%, 0.1 W, 0603	RC0603FR-07887KL	Yageo		
R12, R29, R30, R31	4	0.001	RES, 0.001, 1%, 2 W, 2010	WSLP20101L000FEA	Vishay-Dale		
R13	1	1	RES, 1.00, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031R00FKEA	Vishay-Dale		
R16, R32	2	49.9	RES, 49.9, 1%, 0.1 W, 0603	M55342K12B49D9T	TT Electronics/IRC		
R18	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	M55342K12B10E0T	TT Electronics/IRC		

Table 4-1. Buck Converter Design BOM (continued)

Designator	Quantity	Value	Description	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R22, R23	2	0.02	RES, 0.02, 1%, 1 W, AEC-Q200 Grade 0, 2512	LRMAM2512-R02FT4	TT Electronics/IRC		
R33	1	10.0k	RES, 10.0 k, 0.1%, 0.1 W, 0603	RG1608P-103-B-T5	Susumu Co Ltd		
R34	1	15.8k	RES, 15.8 k, 1%, 0.1 W, 0603	RC0603FR-0715K8L	Yageo		
R36	1	1.96	RES, 1.96, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031R96FKEA	Vishay-Dale		
TP1, TP29, TP30, TP33	4		Test Point, Miniature, Red, TH	5000	Keystone		
TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP25, TP31, TP34, TP35	20		Test Point, Miniature, White, TH	5002	Keystone		
TP18, TP19, TP20, TP21, TP28	5		Test Point, Miniature, Black, TH	5001	Keystone		
U1	1		Radiation-Hardness-Assured Si and GaN Dual Output Controller	TPS7H5001HKY-EM	Texas Instruments		
U4	1		200-V, 1.5-A, 3-A Half-Bridge GaN Driver With Adjustable Dead Time, RVR0019A (WQFN-19)	LMG1210RVRR	Texas Instruments	LMG1210RVRT	Texas Instruments
FID1, FID2, FID3	0		Fiduciary mark. There is nothing to buy or mount.	N/A	N/A		

5 Schematics

Figure 5-1 through Figure 5-12 show the EVM schematics.



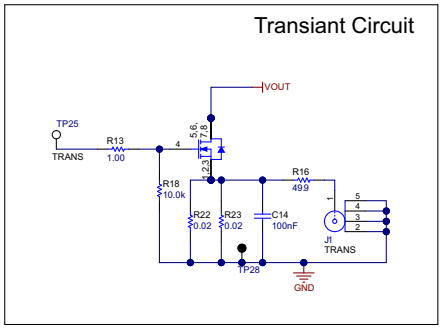


Figure 5-1. Buck Converter Schematic (Page 1)

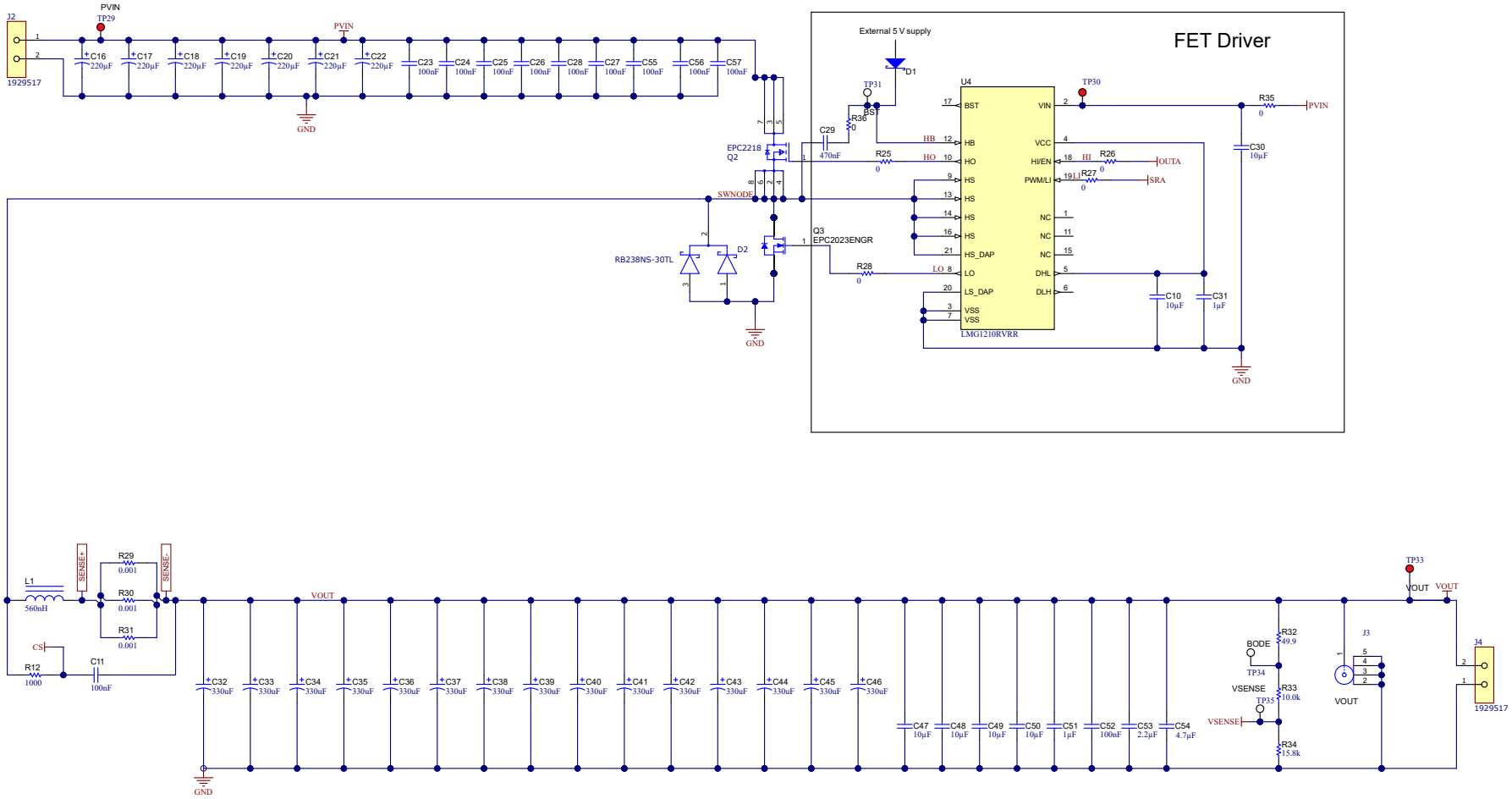


Figure 5-2. Buck Converter Schematic (Page 2)

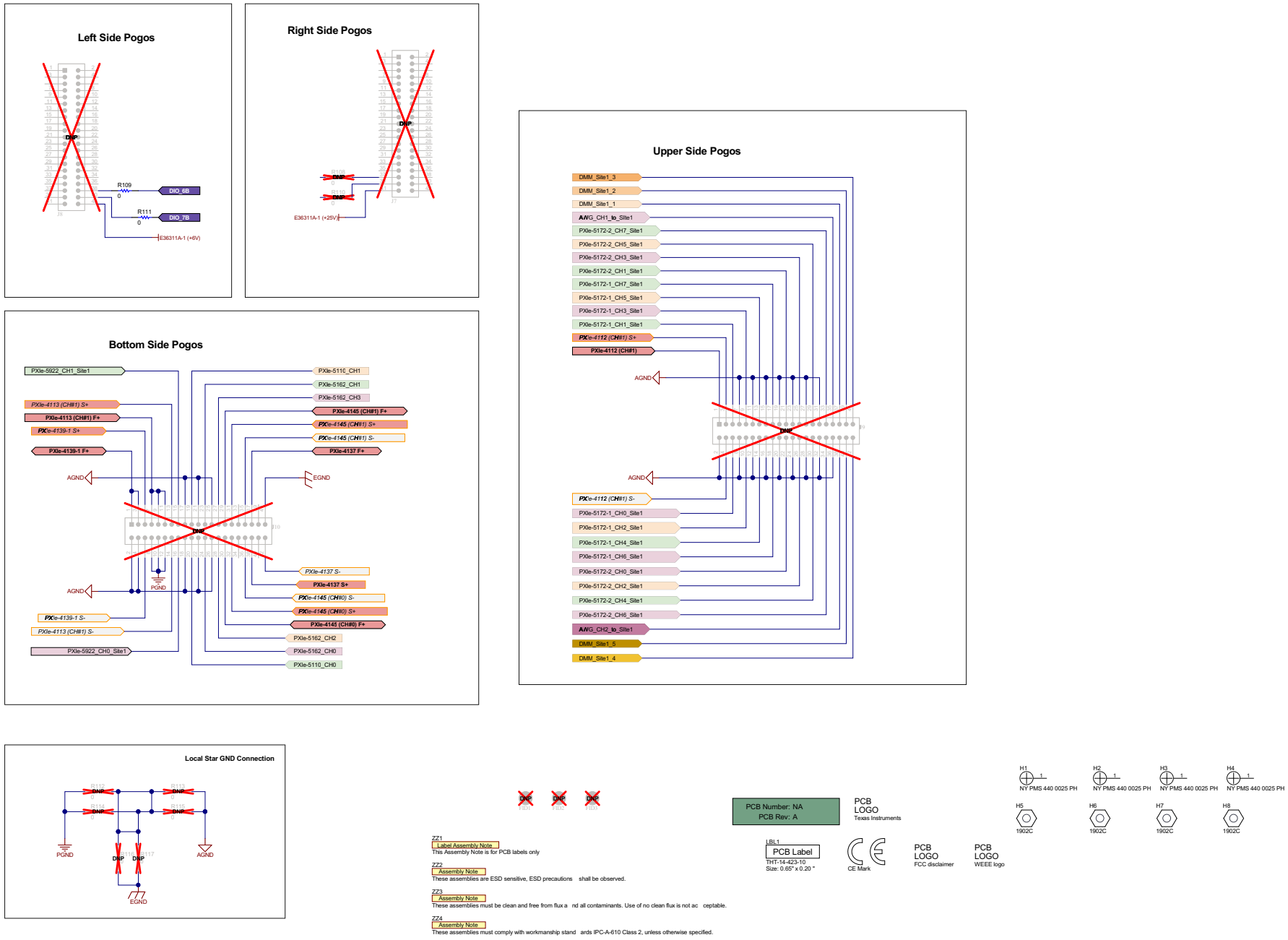


Figure 5-3. TPS7H5001EVM-CVAL Schematic (Page 3)

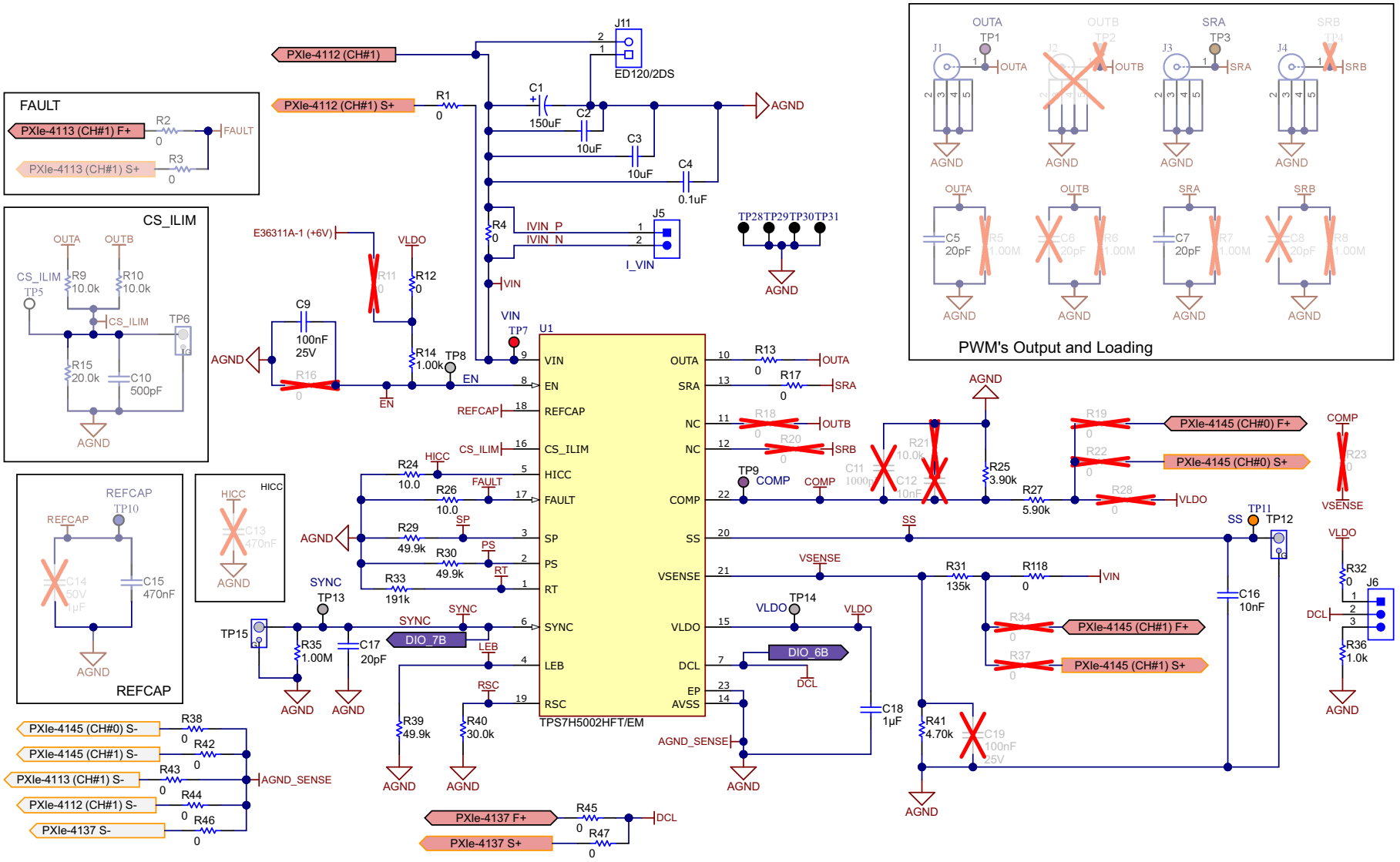


Figure 5-4. TPS7H5002EVM-CVAL Schematic (Page 1)

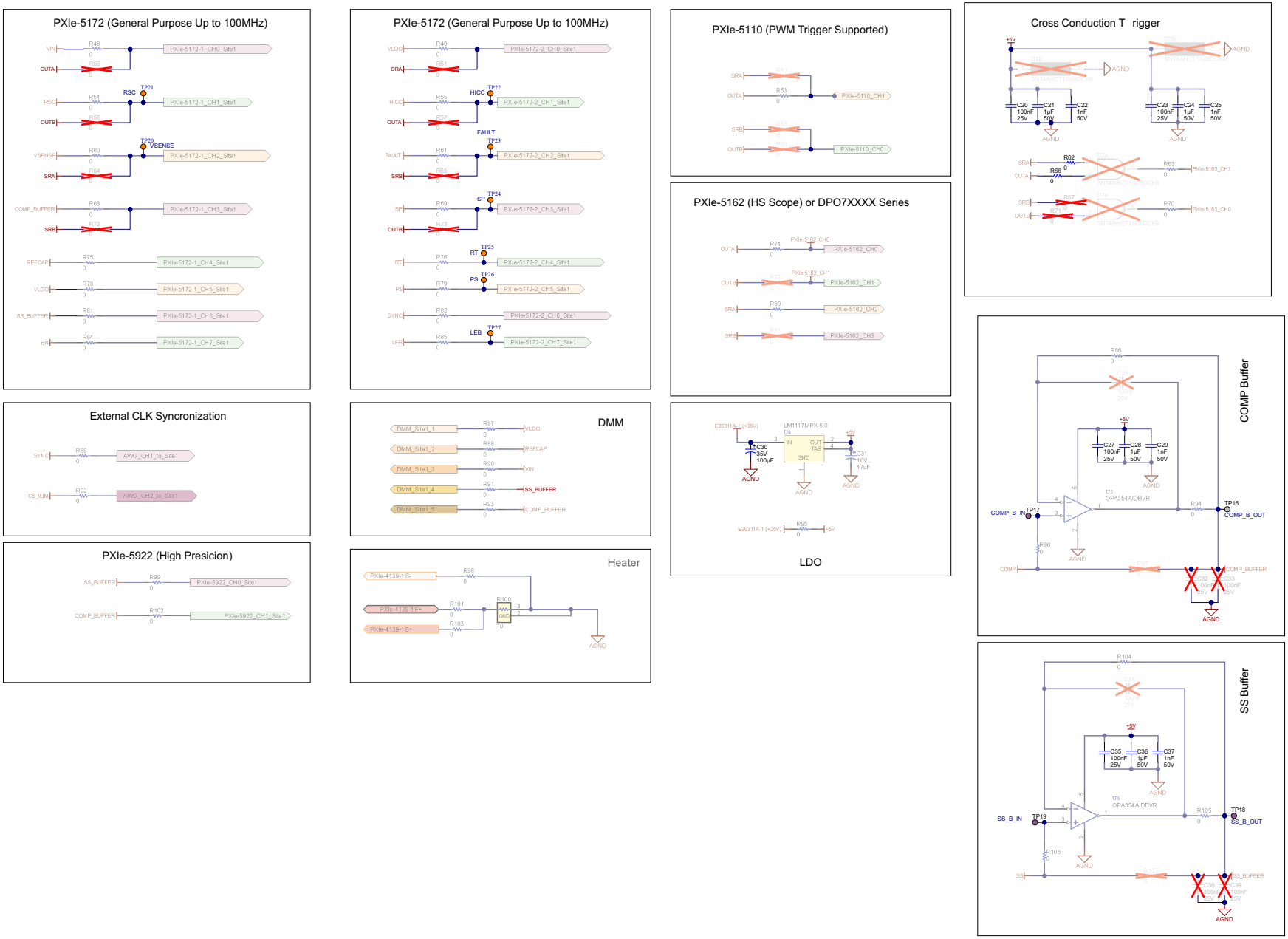


Figure 5-5. TPS7H5002EVM-CVAL Schematic (Page 2)

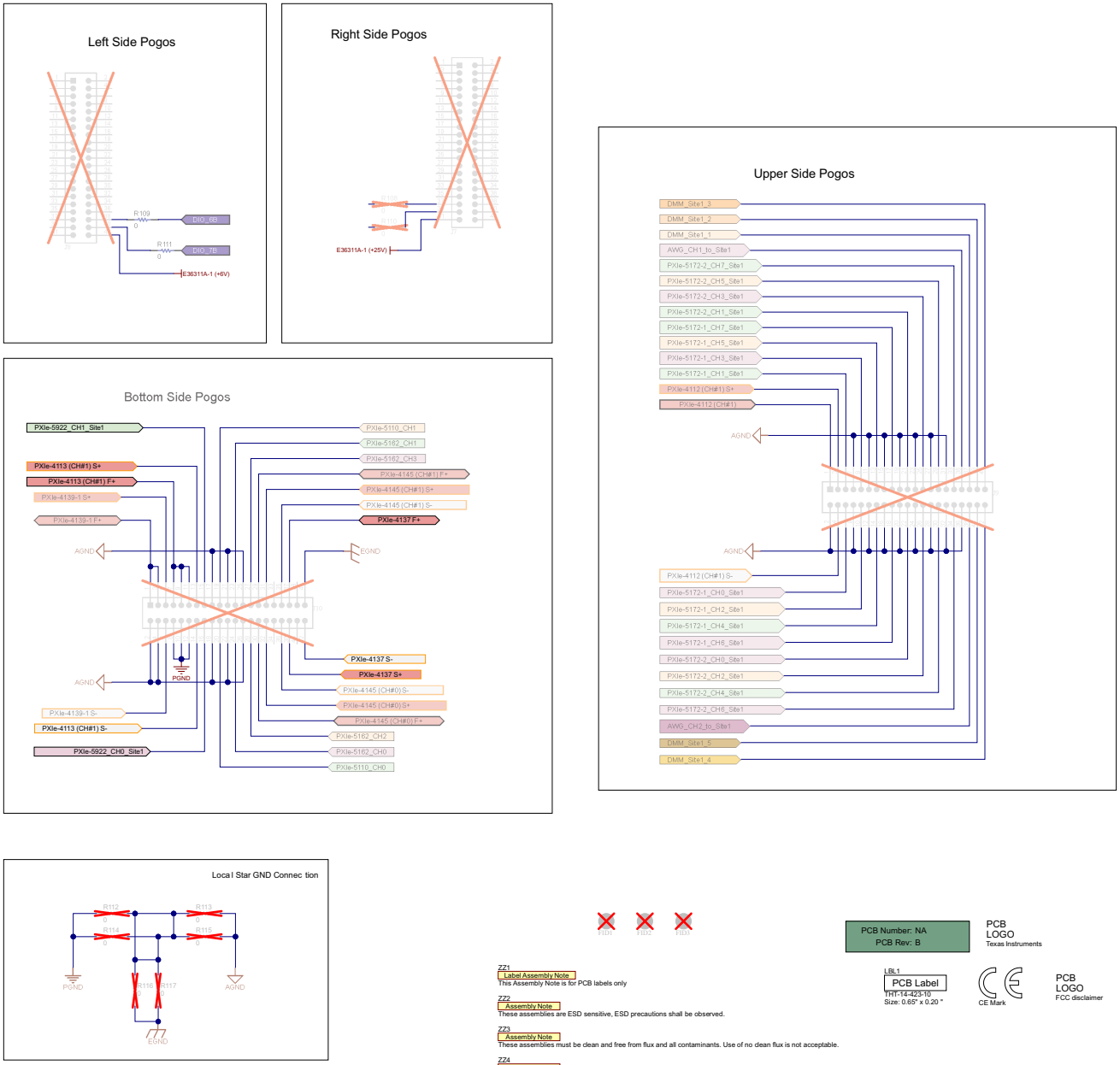


Figure 5-6. TPS7H5002EVM-CVAL Schematic (Page 3)

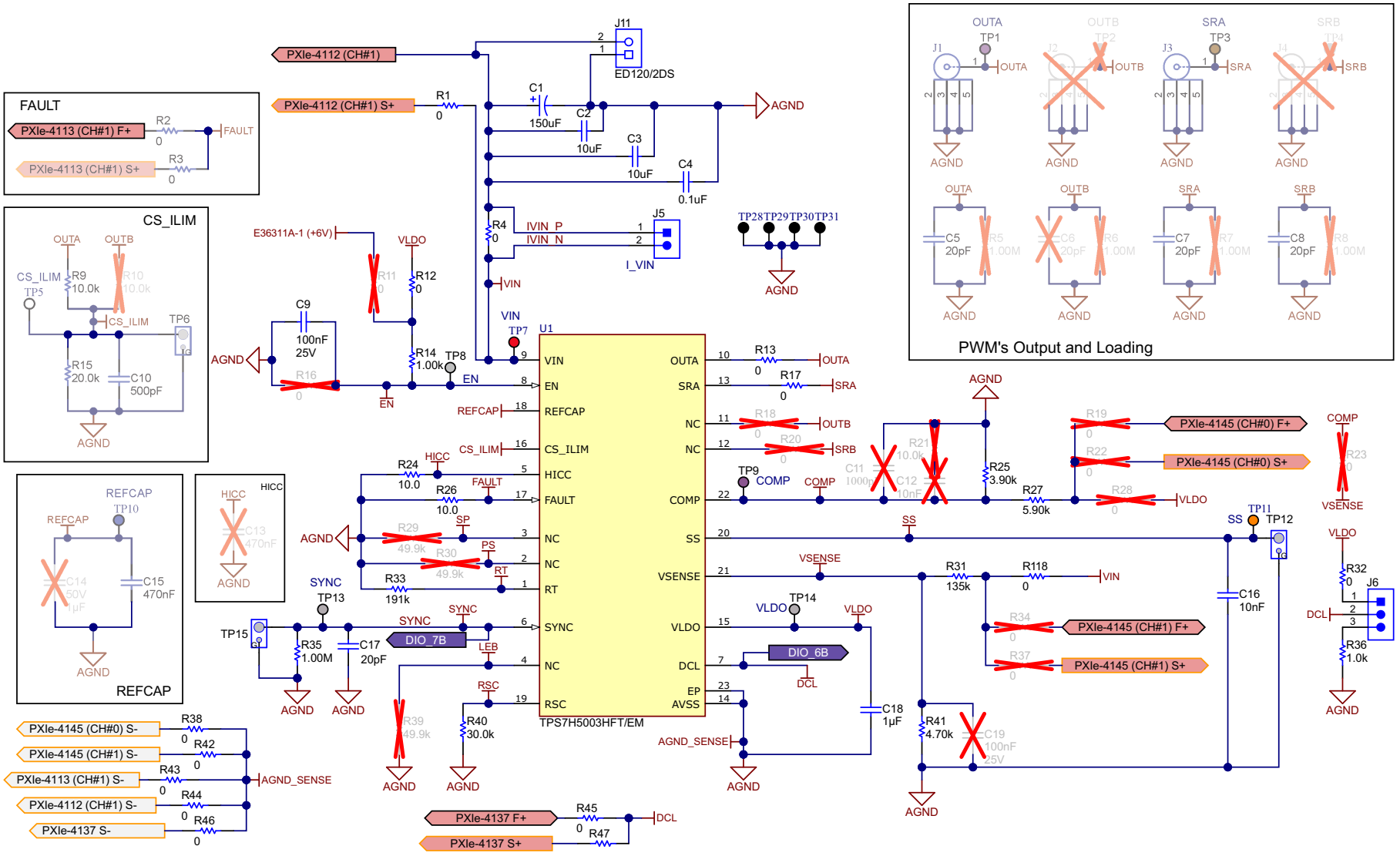


Figure 5-7. TPS7H5003EVM-CVAL Schematic (Page 1)

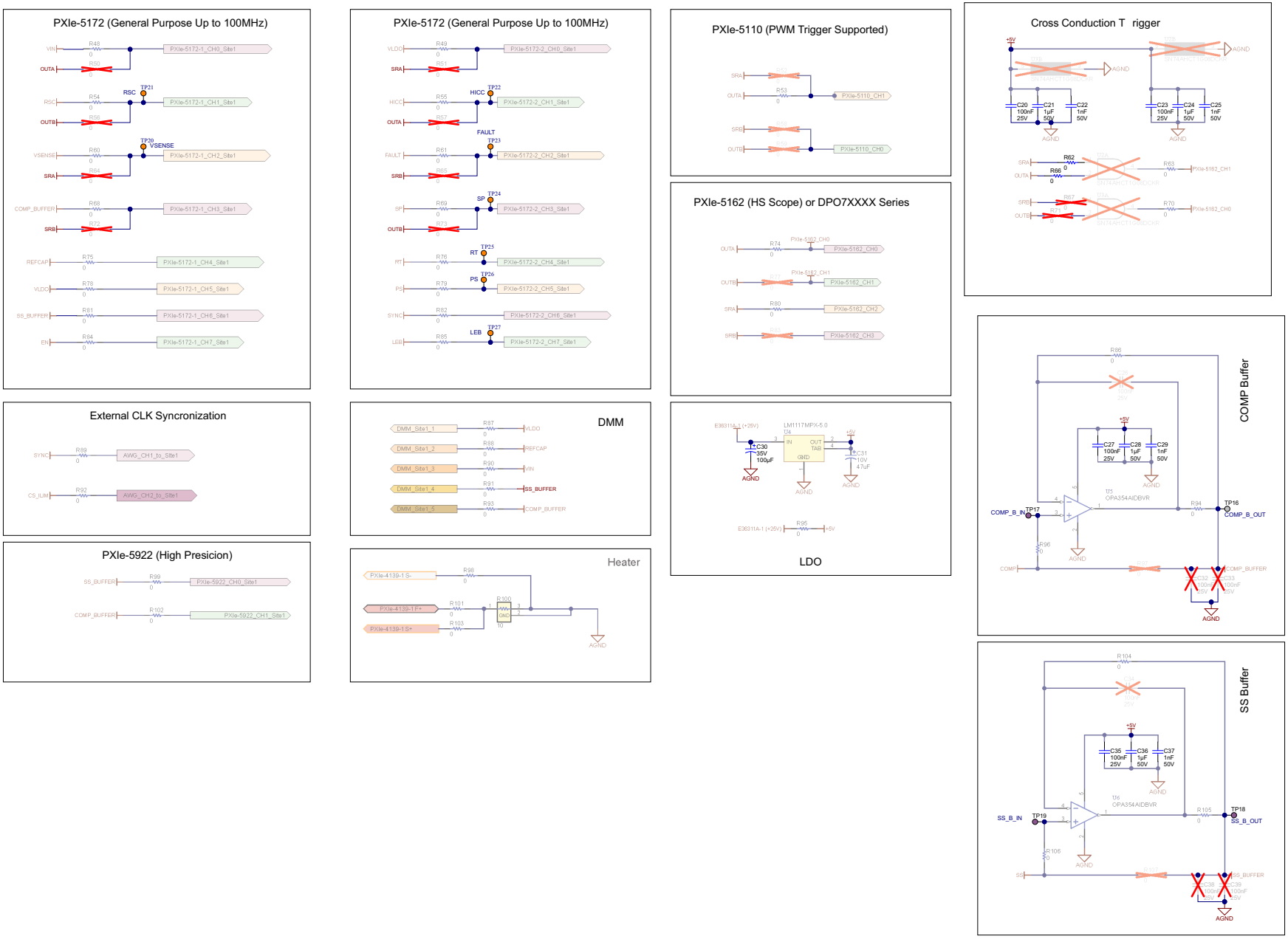


Figure 5-8. TPS7H5003EVM-CVAL Schematic (Page 2)

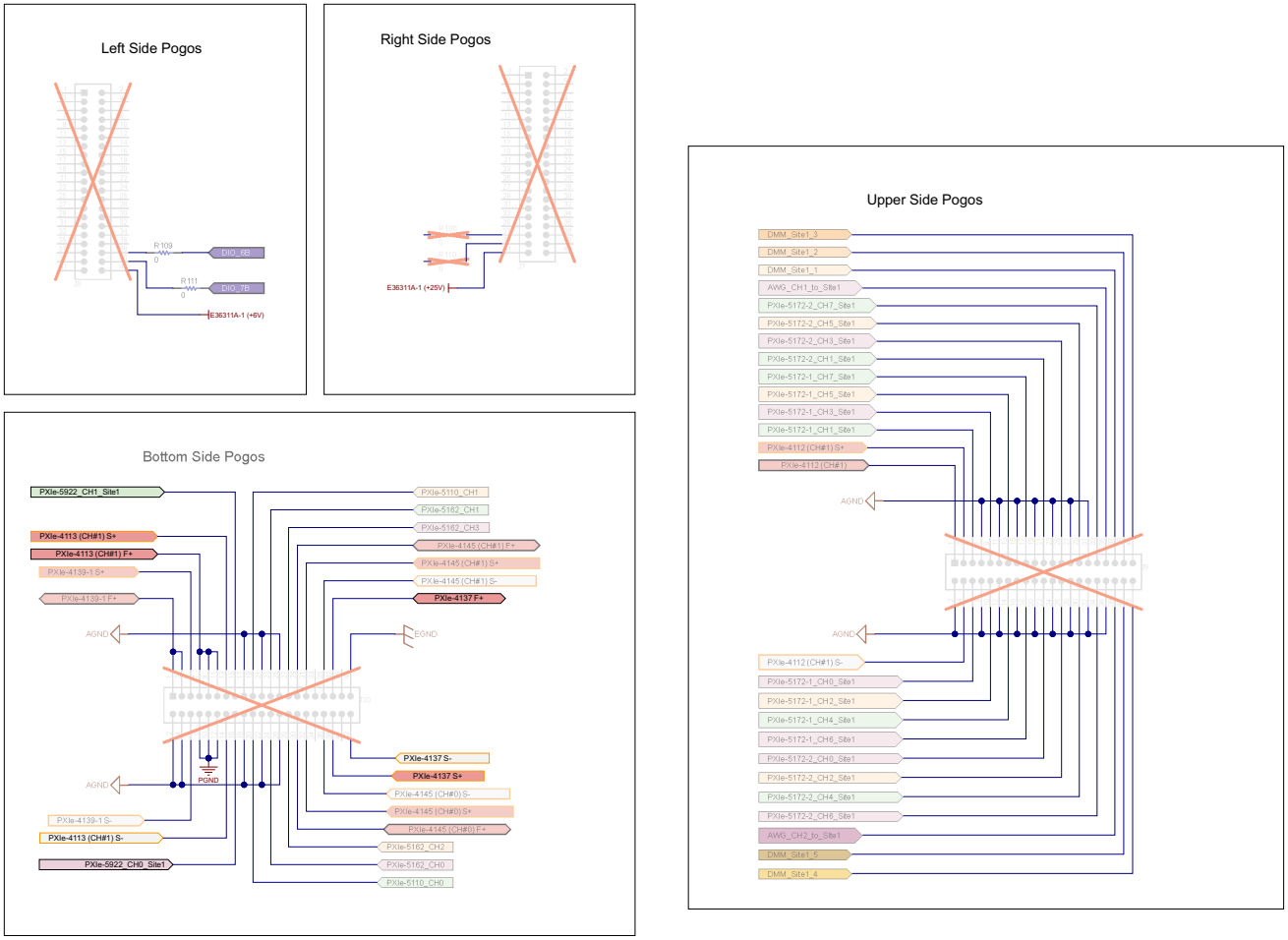


Figure 5-9. TPS7H5003EVM-CVAL Schematic (Page 3)

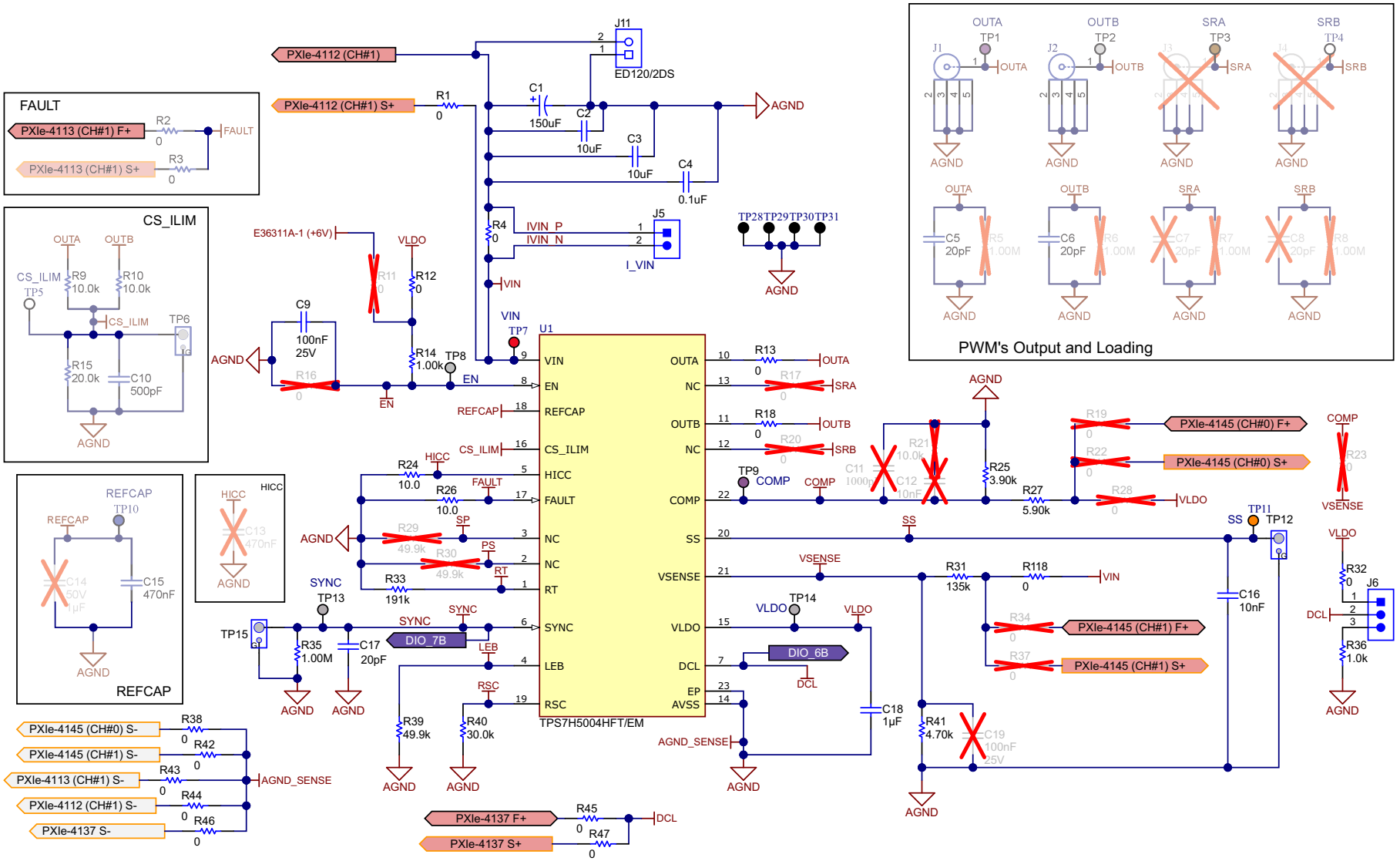


Figure 5-10. TPS7H5004EVM-CVAL Schematic (Page 1)

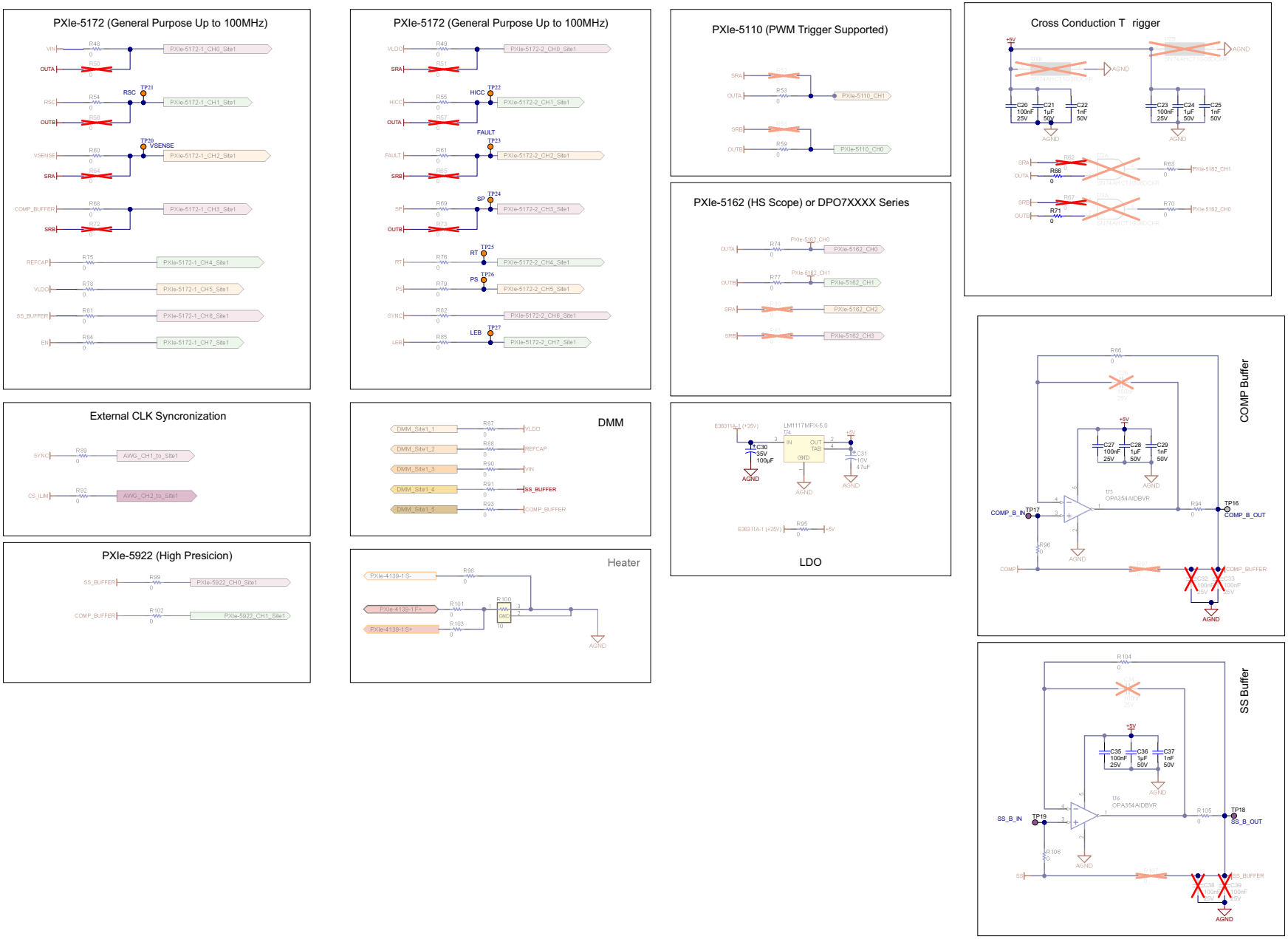


Figure 5-11. TPS7H5004EVM-CVAL Schematic (Page 2)

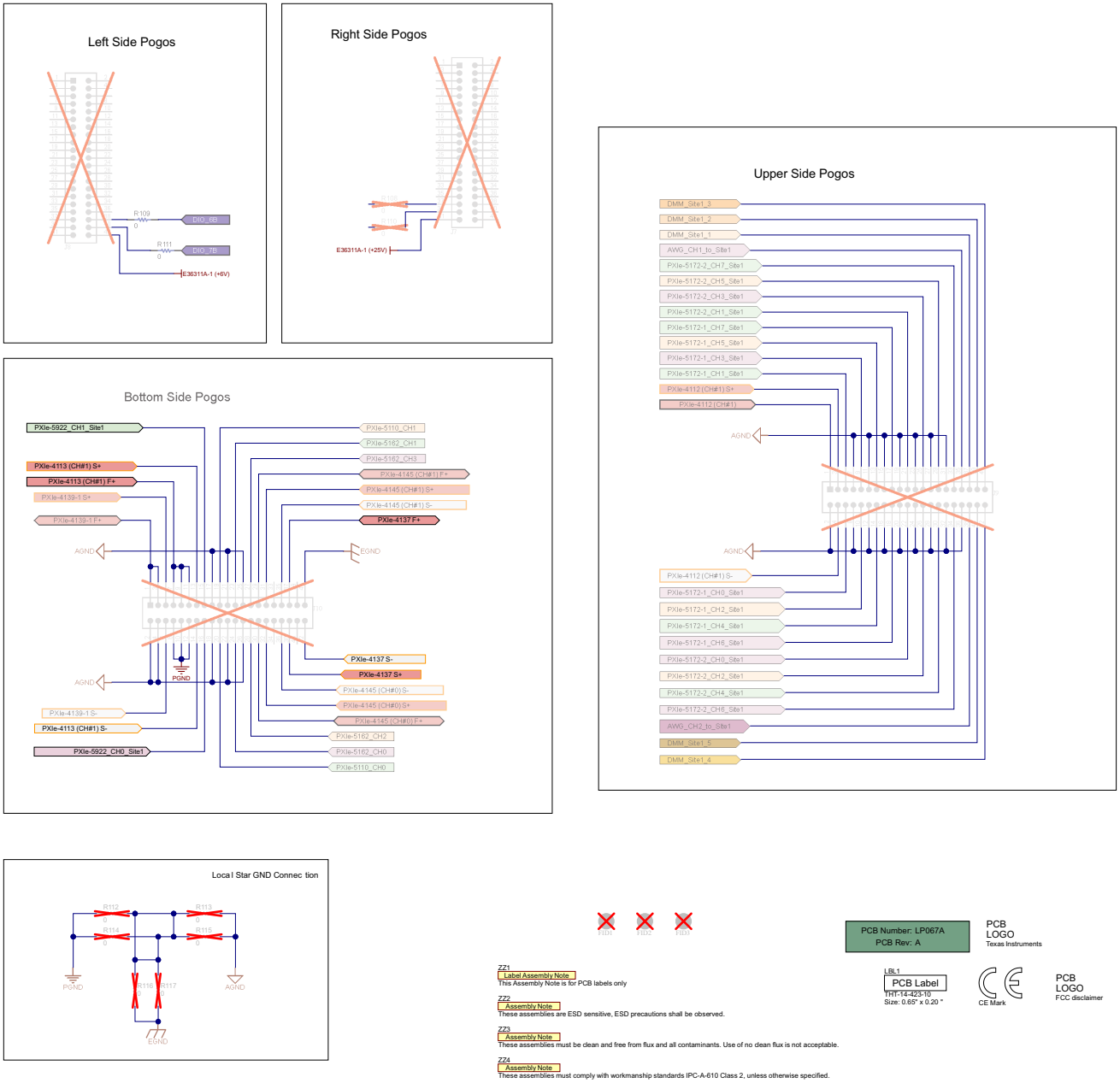


Figure 5-12. TPS7H5004EVM-CVAL Schematic (Page 3)

6 PCB Layouts

Figure 6-1 through Figure 6-13 show the EVM PCB layout images.

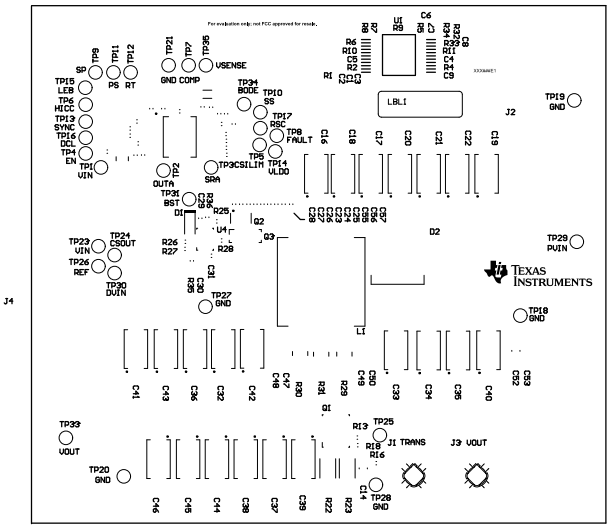


Figure 6-1. Top Overlay

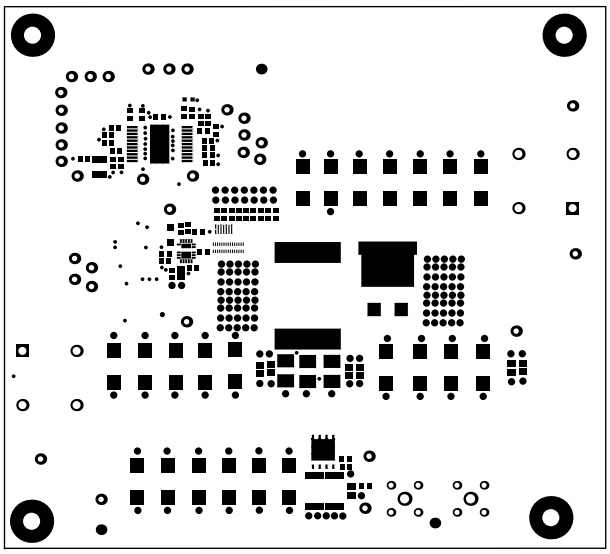


Figure 6-2. Top Solder

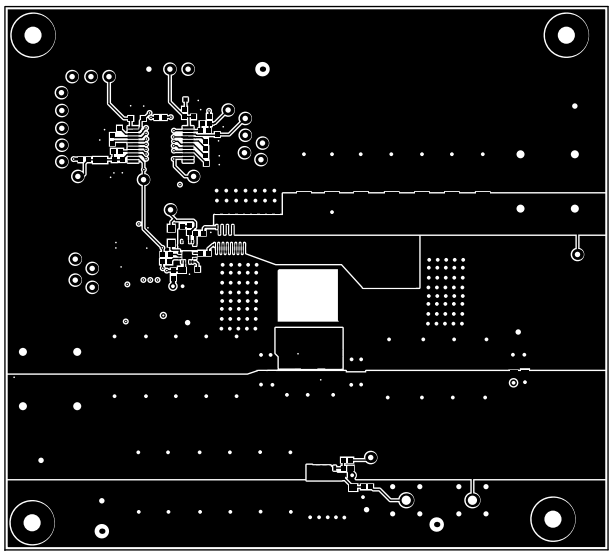


Figure 6-3. Top Layer

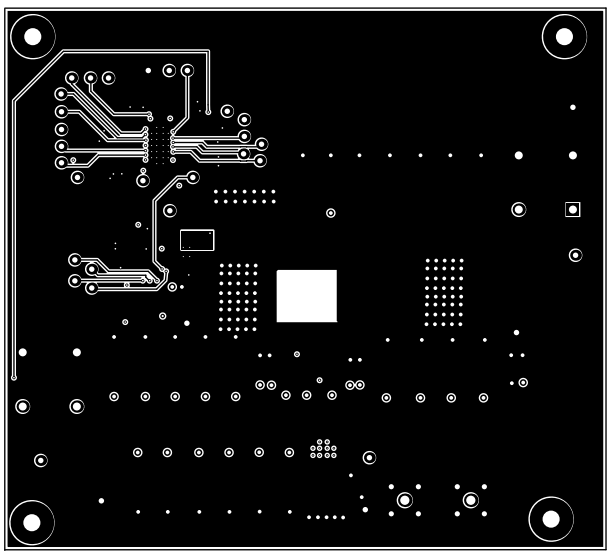


Figure 6-4. Signal Layer 1

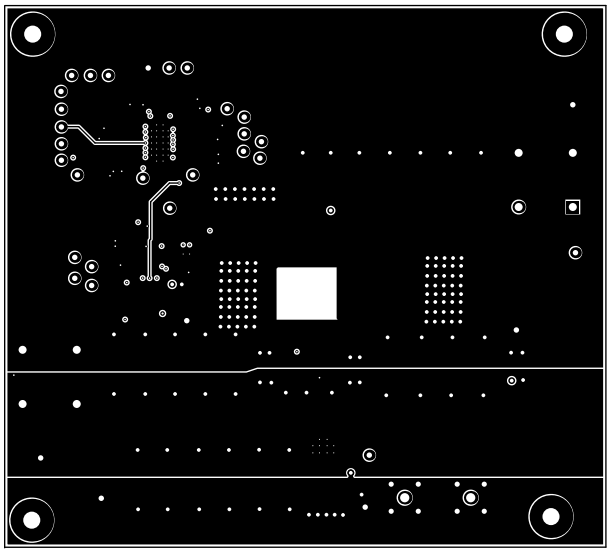


Figure 6-5. Signal Layer 2

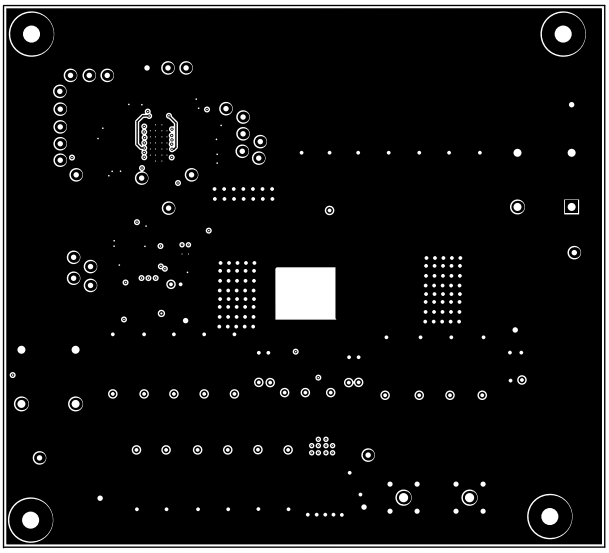


Figure 6-6. Signal Layer 3

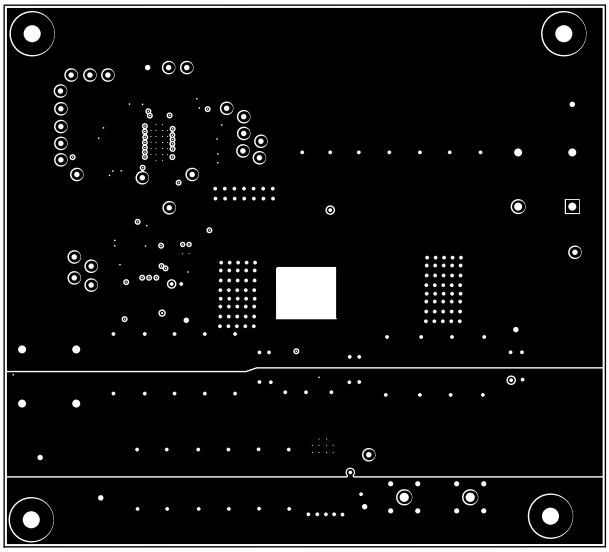


Figure 6-7. Signal Layer 4

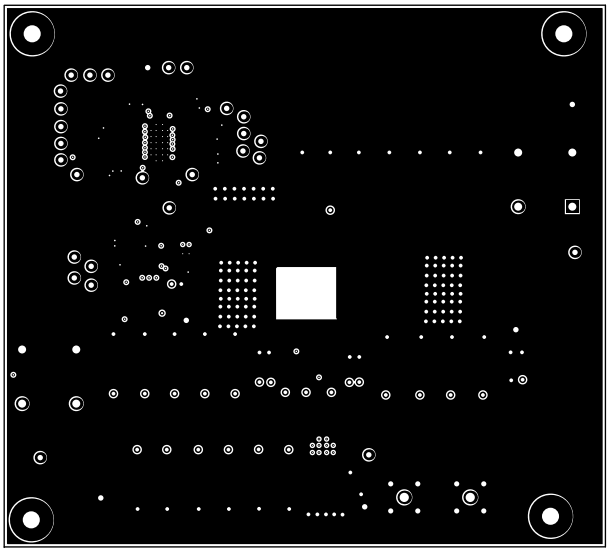


Figure 6-8. Signal Layer 5

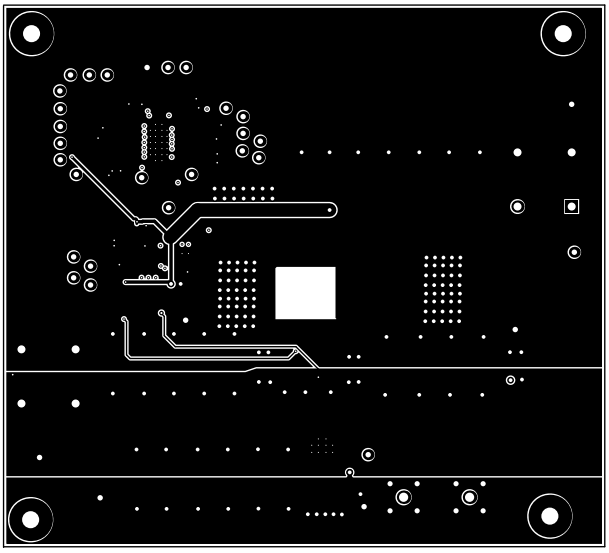


Figure 6-9. Signal Layer 6

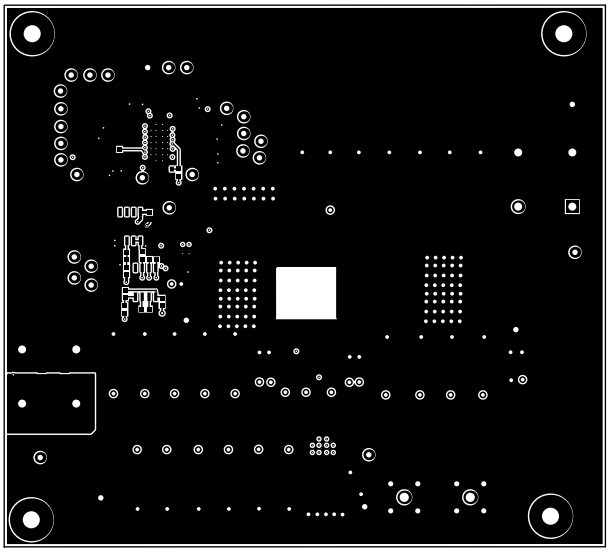


Figure 6-10. Bottom Solder

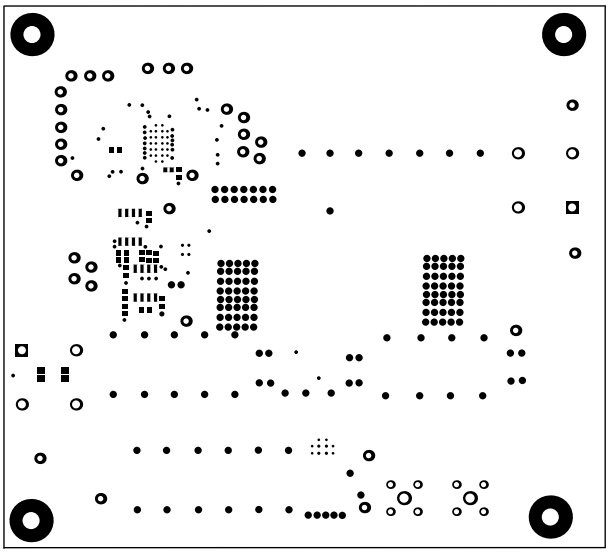


Figure 6-11. Bottom Solder Mask

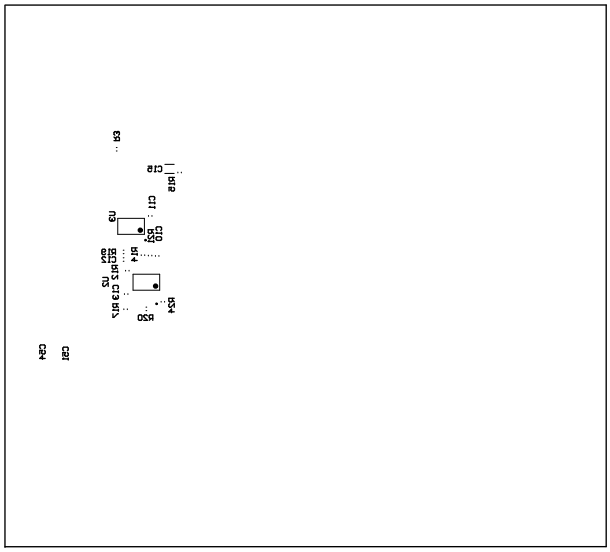


Figure 6-12. Bottom Overlay

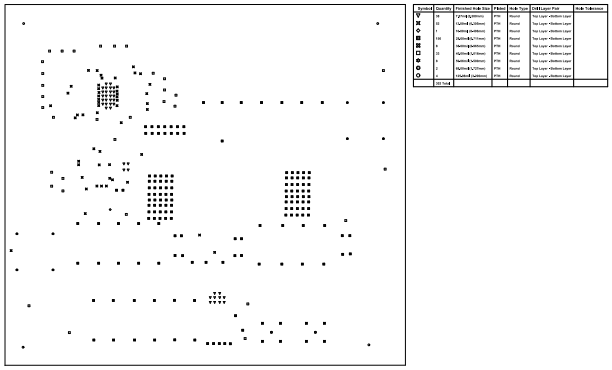


Figure 6-13. Drill Drawing

7 References

- Texas Instruments, *TPS7H500x-SP Radiation-Hardness-Assured 2-MHz Current Mode PWM Controllers*, data sheet.
- Texas Instruments, *LMG1210 200-V, 1.5-A, 3-A Half-Bridge MOSFET and GaN FET Driver With Adjustable Dead Time for Applications up to 50 MHz*, data sheet.

8 Revision History

Changes from Revision A (February 2023) to Revision B (May 2023)	Page
• Changed *coverter* to *converter*	1

Changes from Revision * (February 2023) to Revision A (February 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the document title from *TPS7H5001-SP Buck Converter* to *12 VIN to 1 VOUT Single Phase Buck Converter Using TPS7H5001-SP Controller*	1
• Added additional information to the *Abstract* topic	1
• Added additional information to the *Introduction* topic	2

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