The IBIS model: A conduit into signal-integrity analysis, Part 1

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Texas Instruments (TI) is developing a new arsenal of digital input/output buffer information specification (IBIS) simulation models to meet a variety of customer needs. This style of model (Figure 1) might be used in a simulation environment to help solve board-level overshoot, undershoot, or crosstalk problems, to name a few. On a more fundamental level, IBIS models provide useful product information, such as the pin capacitance and parasitics or the rise/fall times of the digital output buffers.

This article, Part 1 of a three-part series, shows the fundamental elements of IBIS models and how they are generated in the SPICE environment. Part 2 will investigate IBIS-model validation. Part 3 will show how IBIS users investigate signal-integrity issues and problems during the development phase of a printed circuit board (PCB).

As Figure 1 shows, the IBIS model contains the package parasitics and the silicon input capacitance (C_comp) for all pins. The IBIS model also includes tables of data that represent the product's DC operation within the product's operating range and beyond the power supplies (power-clamp, ground-clamp, pullup, and pulldown boxes). In addition, the output-model structure in Figure 1 provides tables that represent the AC or transient response (rising ramp and falling ramp) within the operating range of the product.

An IBIS model includes AC and DC tables that reflect the operation of the product. This type of model has pin- and package-parasitics elements that complete the interface to the PCB. The simulation model produces the performance of the digital buffer's interaction with the PCB but omits interactions with nodes inside the chip. The IBIS model simulates the system-level PCB behavior, specifically modeling the connection from the outside world to the product's digital input/output (I/O) buffers.

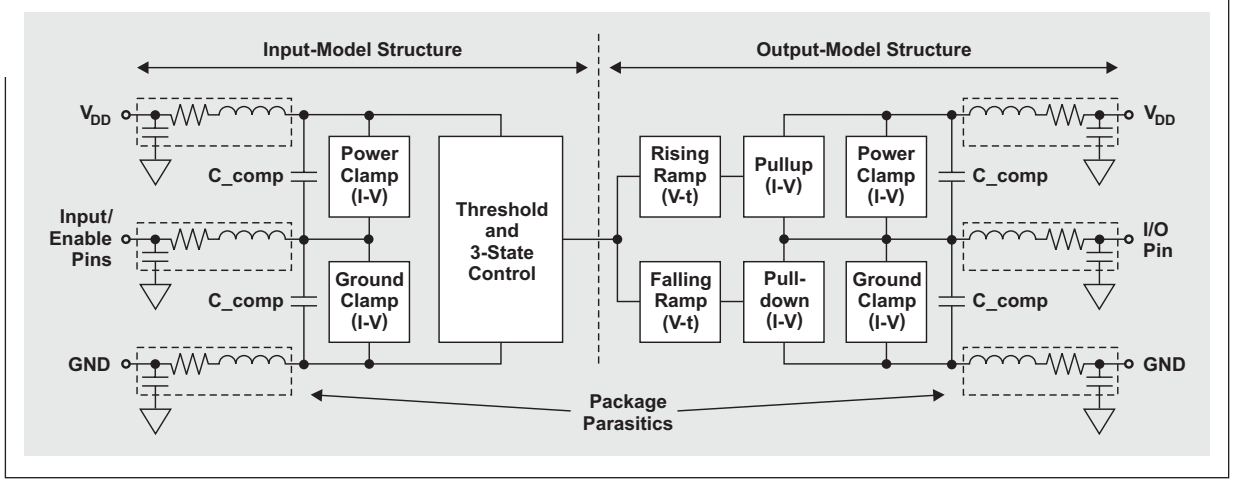
Foundations of the IBIS model

An IBIS model contains information relating to the digital buffers of an IC chip. The core of the IBIS model contains the product buffer's DC information in the form of current-voltage (I-V) tables, and its AC information in the form of voltage-time (V-t) tables. If these tables are generated with the product's SPICE deck, it is possible to include nominal, strong, and weak corners with variations in process, supply voltage, and temperature. Table 1 shows an example of six corners for the DAC8812, which is a dual serial-input, 16-bit multiplying digital-to-analog converter. Three of these corners (1, 2, and 3) are centered around a nominal digital power-supply voltage (V_{DD}) of 3.3 V. The other

Table 1. Process, voltage, and temperature corners for DAC8812 IBIS model

CORNER NUMBER	PROCESS	VOLTAGE (V)	TEMPERATURE (°C)
1	Weak	3.0	85
2	Nominal	3.3	25
3	Strong	3.6	–40
4	Weak	4.5	85
5	Nominal	5.0	25
6	Strong	5.5	–40

Figure 1. Block diagram of IBIS model with digital I/O buffers



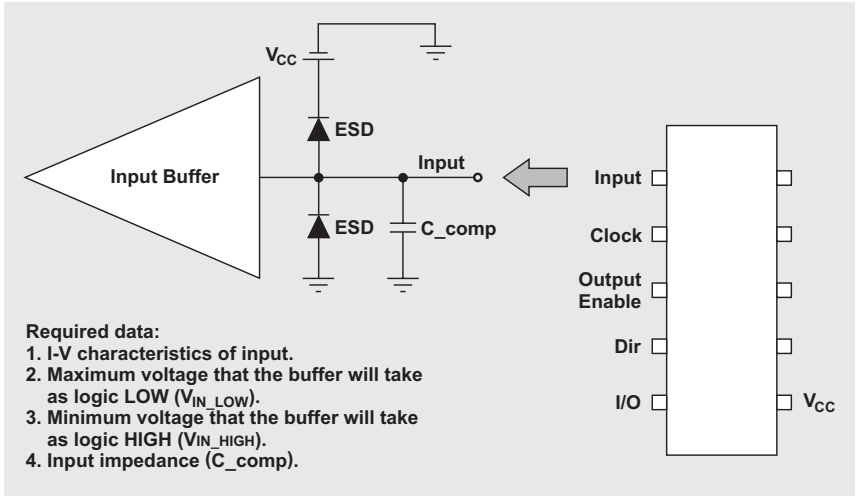
three corners (4, 5, and 6) are centered around a nominal V_{DD} of 5.0 V.

An IBIS model created at the bench is limited to the tests from one to a few devices. The bench-tested IBIS models usually do not show silicon-process variations.

IBIS models can contain data for any of several different buffer types: input, output, I/O, tri-state, terminator, output_open_source, output_open_sink, I/O_open_source, I/O_open_sink, input_ECL, output_ECL, and I/O_ECL.

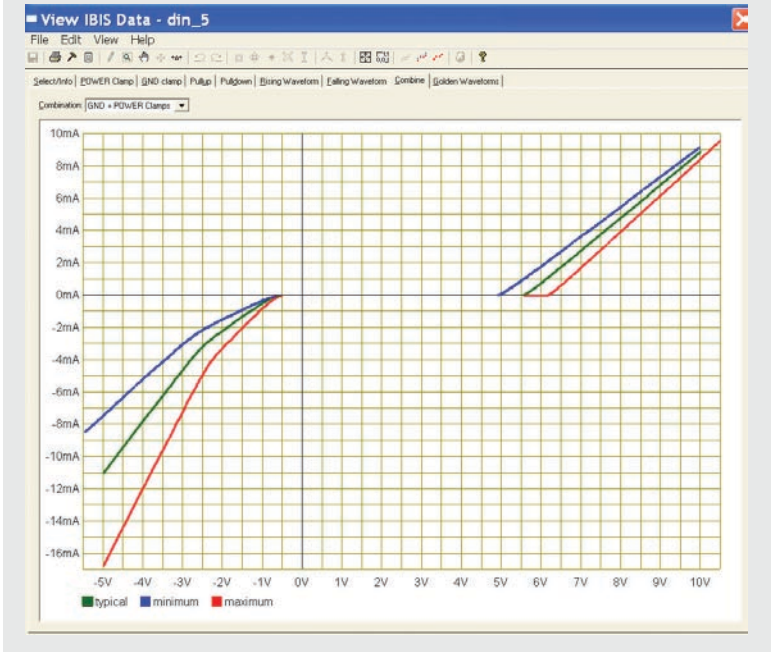
The voltage at an input or output buffer's pin in the DC tables extends beyond the supply voltage (V_{DD}) from $-V_{DD}$ to $2 \times V_{DD}$. This exercises the product buffer's ESD structures beyond the supply voltage. In this manner, IBIS models are capable of showing the overshoot and undershoot responses of poorly terminated PCB signals. IBIS models contain I-V data for input and output buffers.

Figure 2. Example of input buffer's basic functionality for an IBIS model



The example of an input buffer in Figure 2 shows the input buffer, the ESD cells, and the buffer's capacitance (C_comp). An IBIS model for an input buffer provides I-V tables of data that extend beyond ground and the supply voltage (V_{DD}). Note that the IBIS model does not require circuitry beyond the immediate interface. IBIS models do not reflect the product's interior logic and interactions. Figure 3 shows a composite graphical example of an input buffer's power-clamp and ground-clamp I-V tables from an IBIS model.

Figure 3. Graphical representation of IBIS model's I-V tables



V-t tables represent the AC behavior of an output buffer like the one in Figure 4. With V-t tables, the output buffer's pin remains inside the product's power-supply rails. IBIS models are capable of simulating the buffer within its operating range, exhibiting accurate simulations of rise and fall times.

Figure 4 shows the pullup and pulldown circuitry as well as the input capacitance of a two-state output buffer. With the output buffer, an IBIS model will typically have I-V tables as well as V-t tables. Once again, the IBIS model does not require circuitry beyond the immediate interface because the model does not reflect the product's interior logic and interactions. Figure 5 shows a graphical example of the rising-time waveform from an IBIS model's V-t table.

Figure 4. Example of two-state output buffer's basic functionality for an IBIS model

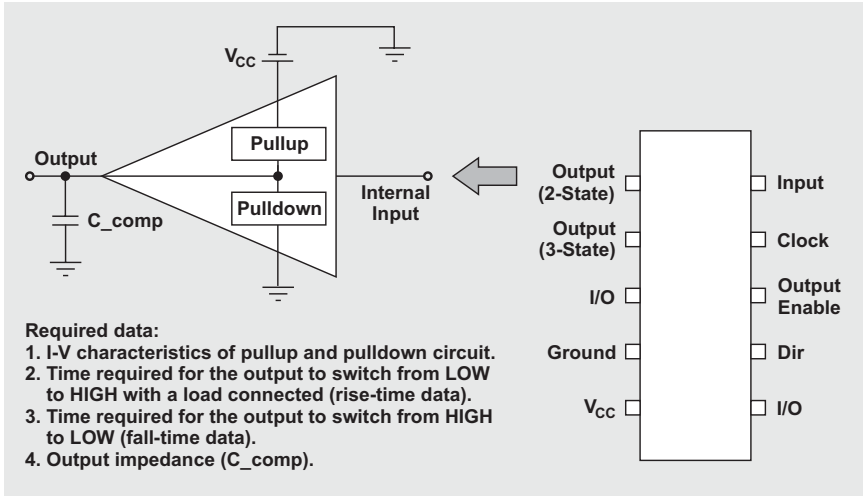
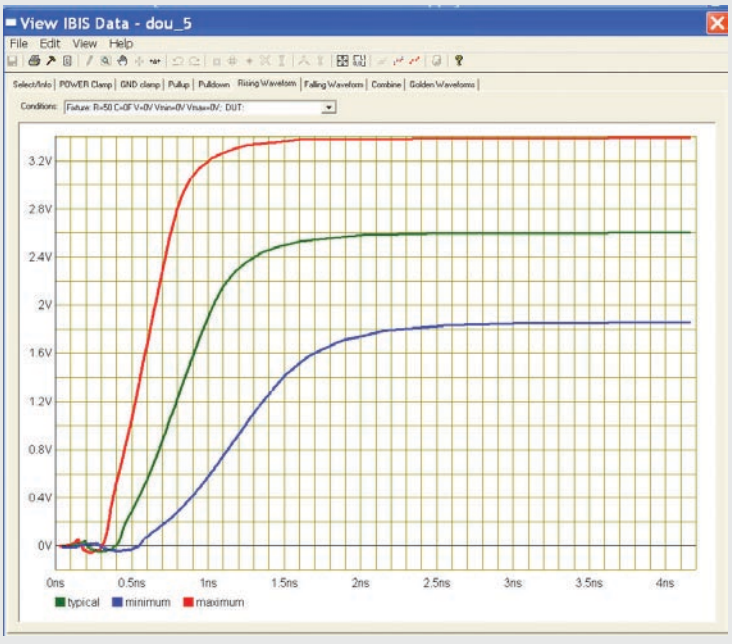


Figure 5. Graphical representation of rising time from IBIS model's V-t table



Format of IBIS model

The format of the IBIS model starts with a header, which is generated by hand and includes a description of the relevant IC or ICs. Following the IC description is general information about the model, including origination date, model source, and user notes. Figure 6 shows an example header of an IBIS model for TI's TMP512 and TMP513, which are temperature and supply-system monitors with an SMBus interface. The "Notes" section is the most important portion of the IBIS model header, where details of the model creation are found along with the basic format of the digital buffers.

The model header is followed by detailed information about the package(s) for the product(s), including values for pin resistance, inductance, and capacitance. To find the total capacitance for a specific pin, the capacitance values in this section are combined with the capacitance (C_comp) values called out next in the buffer tables. The core of the IBIS model follows with I-V and V-t tables buffer by buffer.

Extracting single-ended SPICE buffer data

The last section of this article will explain how to obtain the I-V and switching information (V-t) from a buffer's transistor-level model. An automated simulation template, an extraction tool (such as S2IBIS3), or manual simulations can be used. This discussion will include only totem-pole CMOS structures.

Extracting I-V data from SPICE simulations

To extract the I-V data for an IBIS model from a SPICE input buffer, the buffer pad is connected to an independent voltage source (V_{SOURCE}). Once the buffer's input is set to its desired state (LOW, HIGH, or OFF), V_{SOURCE} is exercised with a DC-analysis function over the sweep range of $-V_{SWEEP}$ to $2 \times V_{SWEEP}$, where the V_{SWEEP} limit is set by the product's supply voltage (V_{DD}). For instance, if the buffer is powered by a 5-V supply, the range of V_{SWEEP} will be –5 V to 10 V. While performing this sweep, the simulator records the current that goes into the buffer.

If the buffer is configured in a high-impedance state (OFF), the data collected produces the ground-clamp and power-clamp tables. The data in the ground-clamp table is referenced to ground, and the data in the power-clamp table is referenced to V_{DD}.

Extracting the I-V data for an output buffer's IBIS model results in a pulldown table and a pullup table. Data for the pulldown table is collected while the buffer is in an output LOW state. Data for the pullup table is collected while the buffer is in an output HIGH state. Data in the pulldown table is referenced to ground, and data in the pullup table is referenced to V_{DD}.

Figure 6. IBIS model header for TMP512 and TMP513

```
|*************************************************************************************
|Texas Instruments Incorporated
|Temperature and Supply System Monitors  SMBus interface
|
| Marketing part#      Digital Voltage   Analog Voltage   Package   # Pins
|                        Range             Range           Type
|TMP512AIDG4           2.1V to 3.6V      3.0V to 26V     SO-14       14
|TMP512AIDRG4          2.1V to 3.6V      3.0V to 26V     SO-14       14
|
|TMP513AIDG4           2.1V to 3.6V      3.0V to 26V     SO-16       16
|TMP513AIDRG4          2.1V to 3.6V      3.0V to 26V     SO-16       16
|TMP513AIRSATG4        2.1V to 3.6V      3.0V to 26V     QFN-16      16
|TMP513AIRSARG4        2.1V to 3.6V      3.0V to 26V     QFN-16      16
|*************************************************************************************
[IBIS Ver]      4.0
[File name]     tmp512_3.ibs
[File Rev]      1.0
[Date]          04/14/2010
[Source]        Texas Instruments Incorporated.
                Analog-eLab , HPA
                12500 TI Blvd
                Dallas, TX -75243
                For Support e-mail: elab_ibis@list.ti.com

[Notes]         Revision History:
                1.0: 04/14/2010
              - Initial version of the model
              - Initial Model generated from simulations in TISPICED
              - Model not matched to measurements
              - Non-monotnic warnings - combined  pulldown and pullup data
                The GPIO non-monotonic current delta is less than 1 mA in a
                full-scale range of ~95 mA. Given these conditions, these
                warnings are deemed insignificant.
                1.1: 04/18/2010 corrected spelling errors
|
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```

Extracting V-t data from SPICE simulations

When a CMOS buffer is modeled, the required simulations that relate to the ramp rate and V-t tables are straightforward. For each simulation corner (typical, minimum, and maximum), there are four V-t data sets. Data for two of the waveforms is gathered by switching the buffer output from LOW to HIGH with the load referenced to a low voltage. Data for the other two waveforms is collected with a load referenced to V_{DD}. For the latter two curves, the buffer's output switches from HIGH to LOW. From these simulations, the ramp rate or dV/dt ratio is extracted as the device is switching HIGH against a low-voltage reference and switching LOW against a high-voltage reference.

Required and recommended IBIS-model curves

There is a variety of buffer types that the IBIS standard describes with I-V and V-t tables. Tables 2 and 3 from Reference 1 list the required and recommended buffer data for each type of buffer.

Conclusion

An IBIS model assists PCB designers during their evaluations of signal-integrity issues and problems. The model's silicon-based DC and AC data facilitates the evaluation of over-power-supply behavior as well as rise- and fall-time behavior. In Part 2, the validity of the IBIS model will be evaluated by verifying that it meets IBIS standards and by comparing it to SPICE simulations.

References

1. The IBIS Open Forum. (2005, Sept. 15). *IBIS Modeling Cookbook for IBIS Version 4.0* [Online]. Available: www.eda.org/ibis/cookbook/cookbook-v4.pdf
2. Roy Leventhal and Lynne Green, *Semiconductor Modeling for Simulating Signal, Power, and Electromagnetic Integrity.* New York: Springer Science+Business Media, LLC, 2006.

Related Web sites

dataconverter.ti.com
www.ti.com/sc/device/DAC8812
www.ti.com/sc/device/TMP512
www.ti.com/sc/device/ TMP513

Table 2. Required and recommended I-V data versus IBIS buffer types

Model_type	[Pullup]	[Pulldown]	[POWER Clamp]	[GND Clamp]	Notes
Input	n/a	n/a	Recommended	Recommended	
I/O	Required	Required	Recommended	Recommended	
I/O_open_sink I/O_open_drain	n/a	Required	Recommended	Recommended	1
I/O_open_source	Required	n/a	Recommended	Recommended	1
Open_sink Open_drain	n/a	Required	Recommended	Recommended	4
Open_source	Required	n/a	Recommended	Recommended	4
Output	Required	Required	Recommended	Recommended	4
3-state	Required	Required	Recommended	Recommended	2
Series_switch	n/a	n/a	n/a	n/a	3
Series	n/a	n/a	n/a	n/a	3
Terminator	n/a	n/a	Recommended	Recommended	3
Input_ECL	n/a	n/a	Recommended	Recommended	
I/O_ECL	Required	Required	Recommended	Recommended	2
Output_ECL	Required	Required	Recommended	Recommended	4
3-state_ECL	Required	Required	Recommended	Recommended	2

1. Keywords listing "n/a" may be included if the currents are set to 0 for all voltage points
2. Functionally similar to I/O, but without input threshold information (Vinh, Vinl, etc.)
3. Special syntax required; use of clamp data on pins that also feature buffers using these Model_types is allowed
4. Clamp data may technically be excluded; however, this data aids analysis of reflections arriving at the driving buffer

Table 3. Required and recommended V-t data versus IBIS buffer types

	[Rising Waveform]		[Falling Waveform]		
Model_type	Load to Vcc	Load to GND	Load to Vcc	Load to GND	Notes
Input	n/a	n/a	n/a	n/a	
I/O	Recommended	Recommended	Recommended	Recommended	
I/O_open_drain	Recommended	n/a	Recommended	n/a	1
I/O_open_source	n/a	Recommended	n/a	Recommended	1
I/O_open_sink I/O_open_drain	Recommended	n/a	Recommended	n/a	1
Open_source	n/a	Recommended	n/a	Recommended	
Open_sink Open_drain	Recommended	n/a	Recommended	n/a	
3-state	Recommended	Recommended	Recommended	Recommended	
Series_switch	n/a	n/a	n/a	n/a	2
Series	n/a	n/a	n/a	n/a	2
Output	Recommended	Recommended	Recommended	Recommended	
Terminator	n/a	n/a	n/a	n/a	
Input_ECL	n/a	n/a	n/a	n/a	
I/O_ECL	Recommended (to Vcc – 2)		Recommended (to Vcc – 2)		3
Output_ECL	Recommended (to Vcc – 2)		Recommended (to Vcc – 2)		3
3-state_ECL	Recommended (to Vcc – 2)		Recommended (to Vcc – 2)		3

1. The presence of internal terminations may require adding waveforms in place of "n/a"
2. Special syntax required
3. For ECL, the fixture is Vcc-2; multiple waveforms to various voltages using the same load impedance may be useful in some contexts

Tables 2 and 3 from Reference 1 reproduced with permission of the IBIS Open Forum and TechAmerica.

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