How delta-sigma ADCs work, Part 2

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A strong addition to the process-control design environment is the delta-sigma (ΔΣ) analog-to-digital converter (ADC). This device's claim to fame is its high 24-bit resolution, which provides 2^{24} or about 16 million output codes. Granted, not all of the lower bits are noise-free, but it is not unusual for a ΔΣ ADC to have 20 noise-free bits, or about 1 million noise-free output codes. This is at least four times better than the performance of 16-bit converters.

Figure 1 shows a block diagram of a ΔΣ ADC. As explained in Part 1 of this article series (see Reference 1), the modulator of a ΔΣ converter shapes the data in such a way as to allow high resolution by reducing low-frequency noise. Part 1 also pointed out that the undesirable characteristics of the modulator output are high-frequency noise and a high-speed, 1-bit output rate. Once the signal resides in the digital domain, a low-pass digital-filter function can be used to attenuate the high-frequency noise, and a decimator-filter function can be used to slow down the output-data rate. This article, Part 2, will consider each function independently, although real-world designs intertwine them in the same silicon.

The digital-filter function

The digital-filter function implements a low-pass filter by first sampling the modulator stream of the 1-bit code. Figure 2 shows a first-order, low-pass averaging filter. An averaging filter is the most common filter technique used in ΔΣ converters. As can be seen, the digital filter in Figure 2 is a weighted averaging filter. Almost all ΔΣ ADCs incorporate a class of averaging filters called sinc filters, named for their frequency response. Many ΔΣ devices, especially audio devices, use other filters in conjunction with sinc filters as part of a process called two-stage decimation. Low-speed industrial ΔΣ ADCs usually use only the sinc filter.

Figure 1. Block diagram of ΔΣ ADC

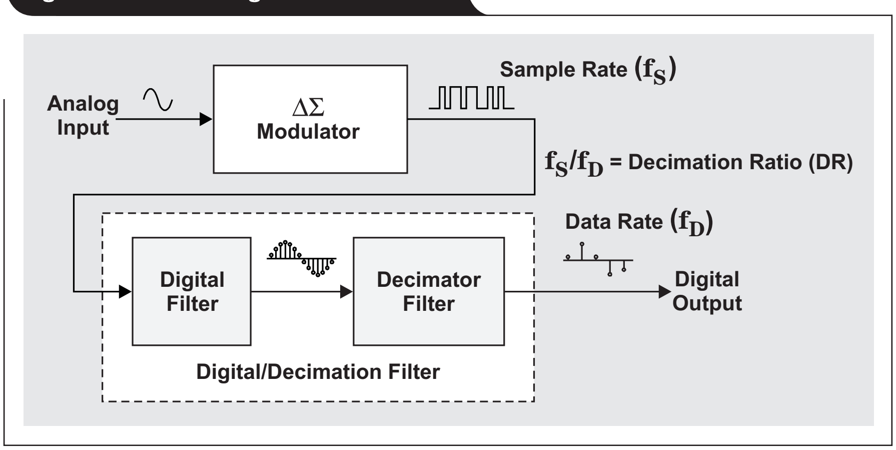
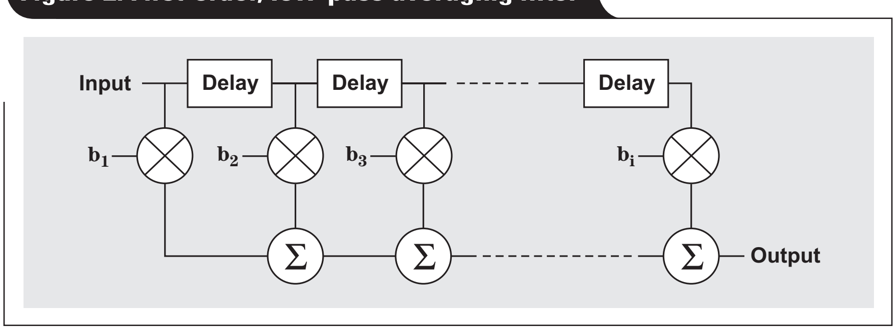


Figure 2. First-order, low-pass averaging filter

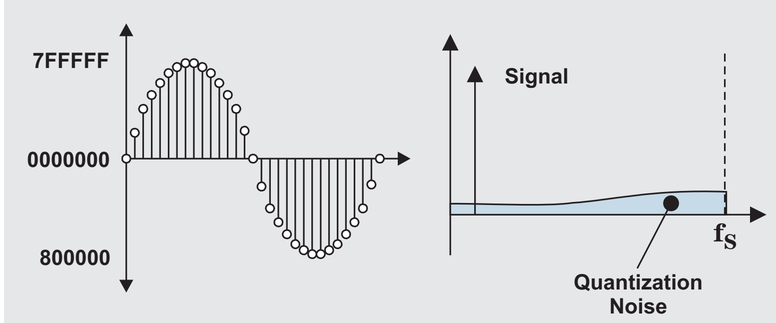


The output rate of a digital filter is the same as the sampling rate. Figure 3 shows a digital filter's outputs. In the time domain (Figure 3a), the digital filter is responsible for the high resolution of the ΔΣ converter. Notice that the 24-bit code train resembles the original signal. However, in the frequency domain (Figure 3b), the digital filter applies only a low-pass filter to the signal. In so doing, it attenuates the modulator's quantization noise; but it also reduces the frequency bandwidth, as any good low-pass filter will. With the quantization noise reduced, the signal re-emerges in the time domain.

The signal is now a high-resolution, digital version of the input signal, but it is still too fast to be useful. The designer could have the converter deliver every one of the samples, but it would be pointless to do so because:

- This converter would require a very fast controller or processor.
- While it might appear that there is an abundance of high-quality samples at the high sampling rate of the modulator, most of them don't provide any useful information, since a low-pass filter has been applied. In other words, the extra samples are interpolations or intermediate results.

Figure 3. Outputs of a digital filter



(a) Time domain (b) Frequency domain

The decimator-filter function

The second function of the digital/decimation filter is the decimator. The word "decimate" was originally used by the Roman army to mean the killing of every tenth man of a group that was guilty of mutiny. In the case of the digital/decimation filter, the "decimation" of the digital filter's samples is much more dramatic. In the decimation circuit, the digital signal's output rate is reduced by throwing away or "killing" portions of the output data. The way to do this is to discard some of the samples.

This may seem a bit distressing. Previously, there was a beautiful sine wave that was well-defined with a large number of samples. Throwing away a large number of those samples leaves a skeleton of the original signal; but, remember, most of those samples are not "real." They can be thought of as the filter's work-in-process samples. In fact, according to the Nyquist theorem, the new "skeletal" version of the signal has exactly the same informational content as the previous waveform, but now it is at a manageable data rate. Decimating some of the samples has not caused any information to be lost.

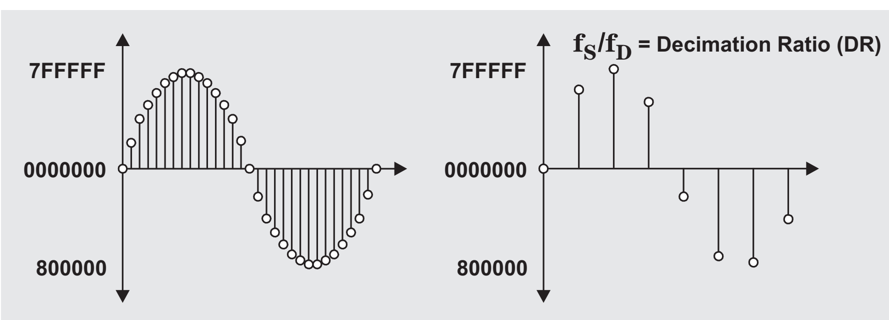
Figure 4 conceptually shows the decimation process. The digital filter's time-domain output in Figure 3a has been brought forward to Figure 4a. Figure 4b shows the decimator-filter function's output signal.

This completes the description of the digital-filter and decimator-filter functions in a ΔΣ converter.

Pulling the ΔΣ ADC together

Part 1 of this series showed the inner workings of the modulator in the time and frequency domains. It also showed how the modulator shaped noise into higher

Figure 4. Digital/decimation filter's output from decimation process

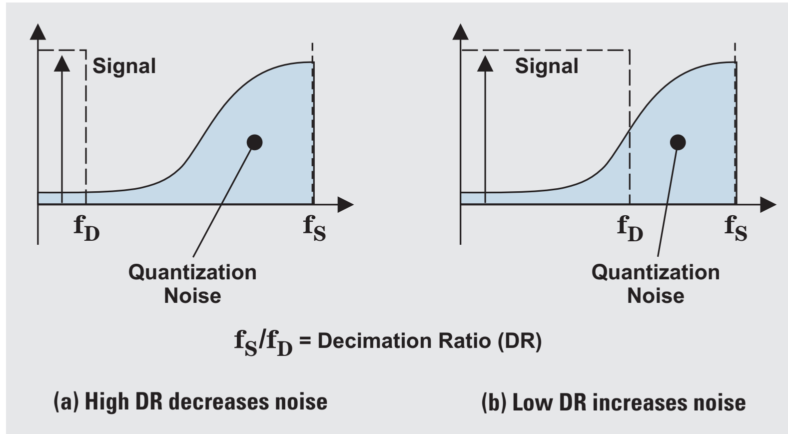


(a) Input sampling rate (f_S) (b) Output-data rate (f_D)

frequencies because of an oversampling system with negative feedback. As previously stated in the present article, the digital/decimation filter reduces high-frequency noise and passes the input signal to the output of the converter at a reduced data rate. The combination of these two components provides a high-resolution ADC.

The meaningful variables in this system are the modulator's sampling rate (f_S) and the digital/decimation filter's output-data rate (f_D). The ratio between these two variables is defined as the decimation ratio (DR). The decimation ratio is equal to the number of modulator samples per data output. Decimation ratio values range anywhere from 4 in the Texas Instruments (TI) ADS1605 ADC to a maximum of 32,768 for TI's ADS1256 ADC.

Figure 5. Increased DR provides a lower-noise, slower output signal



Consider the output spectrum of the ΔΣ modulator in Figure 5. The modulator samples at a frequency of f_S and, in doing so, shapes the quantization noise into higher frequencies. Many ΔΣ converters permit the designer to program the data rate directly by adjusting the decimation ratio. Suppose the data rate is chosen to be some fraction of f_S, as shown in Figure 5a. The frequencies from 0 to f_D, which constitute the output, are in the signal band. Note the noise level in the signal band.

In Figure 5a, the effective number of bits (ENOB) is very high. Since the output-data rate (f_D) is determined by the decimator-filter function, it depends on the decimation ratio (DR), where $\mathbf{DR = f_S/f_D}$. Figure 5b shows that the value for f_D, which has moved to the right, is now higher. Unfortunately, there is also more noise. Most of the noise is in the higher frequencies, decreasing the signal-to-noise ratio and the ENOB.

There is a way to increase the sampling speed (f_S) while keeping the ENOB the same, and that is to increase the master-clock rate. This will also increase f_D but will not decrease the decimation ratio. Unfortunately, increasing the master-clock rate will also increase power consumption. Additionally, most converters have a practical limit for f_S beyond which they will not function properly.

Conclusion

A ΔΣ ADC fundamentally includes a modulator and a digital/decimation filter. The modulator converts the analog signal directly into the digital domain by using a 1-bit ADC and oversampling. The modulator topology implements a noise-shaping function that drives the lower-frequency quantization noise into higher frequencies. The low-pass digital/decimation filter throws away the high-frequency noise that was shaped by the modulator stage and reduces the data-output rate of the device to a usable frequency.

There is a strong relationship between the output-data rate and the converter's resolution. If the sample rate is kept constant, lower data rates provide high effective resolution, or ENOB, at the output of the converter.

ΔΣ ADCs have other functions besides the basics in these two articles, acting as current sources, voltage sources, input buffers, etc. However, examining any ΔΣ ADC will always reveal a modulator and a digital/decimation filter. In choosing a ΔΣ ADC, it is best to start with the fundamentals and then see what else the device has to offer.

References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. Bonnie Baker, "How delta-sigma ADCs work, Part 1," *Analog Applications Journal* (3Q 2011)	SLYT423
2. "16-bit, 5MSPS analog-to-digital converter," ADS1605/6 Datasheet	SBAS274
3. "Very low noise, 24-bit analog-to-digital converter," ADS1255/6 Datasheet	SBAS288

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