Measuring op amp settling time by using sample-and-hold technique

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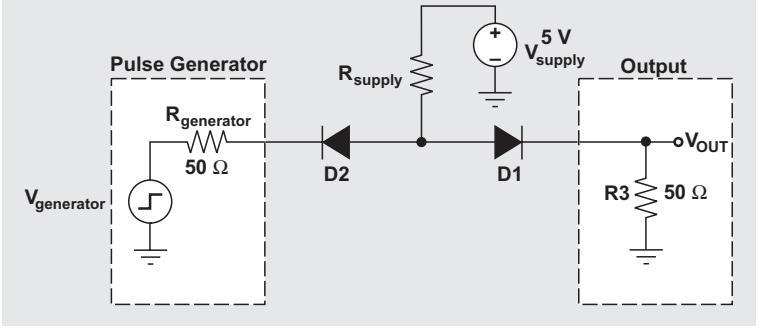
Introduction

Modern high-speed operational amplifiers (op amps) are designed with settling time in the range of nanoseconds. This time is so brief that measuring it within a reasonable error band presents a challenging task not only on automatic test equipment (ATE) but also on the bench. In today's op amp datasheets, settling time is usually given as a simulated value due to the cost and challenges associated with implementing additional hardware to test it on the bench. Traditional high-speed oscilloscopes have only a 10-bit analog-to-digital converter, which limits any measurement resolution to a maximum of 0.1%.

Figure 1. Flat-bottom pulse generator (FBPG)



This article describes a new methodology that has proven to be effective in making these measurements. Detailed is a relatively inexpensive and simple way to measure settling time that bases accuracy and precision on the relative speed of the waveform generator and the sample-and-hold circuit.

Step input for the device under test

In this article, settling time refers to the time that elapses from the application of an ideal step input to the time at which the device under test (DUT) enters and remains within a specified error band that is symmetrical about the final value. An ideal step input is easily generated in simulation, but there are no instruments that can produce an ideal step waveform in any lab setting. Even under ideal conditions, the output of overdamped and critically damped instruments would take a few RC time constants to monotonically settle to within tenths of a percent of the final value.

For underdamped systems, a step waveform can overshoot the final value, and ringing may occur. In practice, even critically damped systems have underdamped behaviors. Generally, the faster the fall time of the step waveform, the more overshoot and ringing one observes. This non-ideality is then propagated into the measured output waveform of the DUT. Fortunately, with the aid of computer-logged records of input and output data, the output can be normalized by lining up the two and subtracting the input from the output (with the DUT in a non-inverting unity-gain configuration).

Flat-bottom pulse generator

When the falling edge of a waveform generator is used as the input to the DUT, a flat-bottom pulse generator (FBPG) can be used to clean up the low-voltage level of the generated signal. The FBPG clamps the falling voltage to ground at the cost of a bigger overshoot. This gives test engineers some control over trade-offs in the test setup. Similarly, a flat-top pulse generator can be used to clean up the high-voltage level.

Figure 1 illustrates two back-to-back high-speed Zener diodes, each with a separate, adjustable power supply. As a rule of thumb, the setup should be started as follows: The R_{supply} should be adjusted to obtain 5 V at the D1/D2 connection, and the $V_{generator}$ output voltage should be adjusted to swing between a 2-V high and a –5-V low. This should bias the output at 2 V_{PP} and the low-voltage level at 0 V. When $V_{generator}$ is high, D2 is turned off and D1 is turned on. During this time, the output voltage becomes a function of D1's forward voltage (V_{supply}) and of the amount of current that flows through R_{supply} and D1. When the input is low, D1 is turned off and D2 is turned on. During this time, the output voltage swings to ground, and its slew rate is proportional to the amount of current that flows into the matching resistor, R3. The transient response is a function of the diode's capacitance, reverse recovery time, and forward recovery voltage.

Because of the diodes' nonlinearity, it does not make sense to derive rigorous equations to determine the DC levels and transient response of the FBPG. Instead, the equations can be simulated in software such as TINA-TI™ from Texas Instruments. Assuming that the pulse generator is very fast, the fall time and overshoot of the output waveform become functions of the diodes' speed and recovery time, as well as of the parasitic capacitance and inductance of the printed circuit board (PCB) on which the FBPG is built. In other words, the designer should pick the fastest, most robust diode and follow guidelines for

good PCB layout when using FBPG for generating high-speed waveforms.

Sample-and-hold methodology for measuring settling time

For the example presented here, the TI OPA615 (see Figure 2) was chosen to implement the sample-and-hold (S/H) functions of settling-time measurement because of its wideband operational transconductance amplifier (OTA), which is optimized for low input-bias current, and its fast and precise sampling OTA (SOTA), which also serves as a comparator and buffer. The analog input (V_{IN}) is sampled by the SOTA onto the capacitor (C_{HOLD}) when the Hold-Control pin is high. The voltage on C_{HOLD} is held and reflected at the output (V_{OUT}) when the Hold-Control pin swings low. During sampling, the voltage on C_{HOLD} is adjusted to the real-time voltage level on the input. If there is a large voltage difference between the input and C_{HOLD} and there are only a few nanoseconds of sampling time, then fast slewing is required. During holding, the voltage on C_{HOLD} invariably charges/discharges due to its leakage current and any biasing current needed for the OTA. The current-feedback loop ensures that the SOTA slews fast enough to capture the correct voltage level at V_{IN}.

Figure 3 shows an example of a S/H output of a 100-kHz sine-wave input. A waveform generator can be used to produce the input step function for the DUT and to synchronize a S/H signal to that step function. A S/H circuit can be used to capture points on the DUT's output waveform. Any arbitrary waveform generator should work if it has a marker output that synchronizes with the output, thus creating a very convenient Hold-Control signal. The example test used a Tektronix AWG610, which has a sampling time of 2.6 Gbps and a minimum marker step of 100 ps, making it fast enough for most measurements of high-speed op amp settling time.

Figure 4 shows how to capture points on a curve by using a S/H circuit with the marker as the Hold-Control signal. The designer can capture sequential points on the curve by moving the marker position. After all the points

Figure 2. Sample-and-hold (S/H) circuit

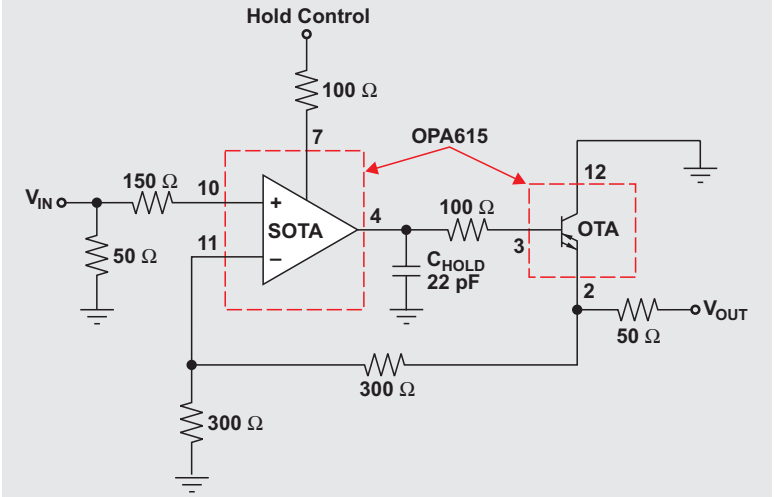


Figure 3. Example 1-MHz S/H output of a 100-kHz sine wave

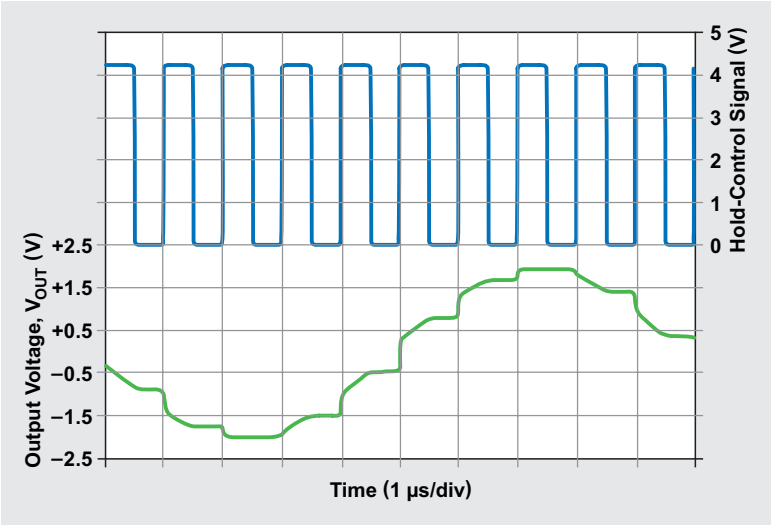
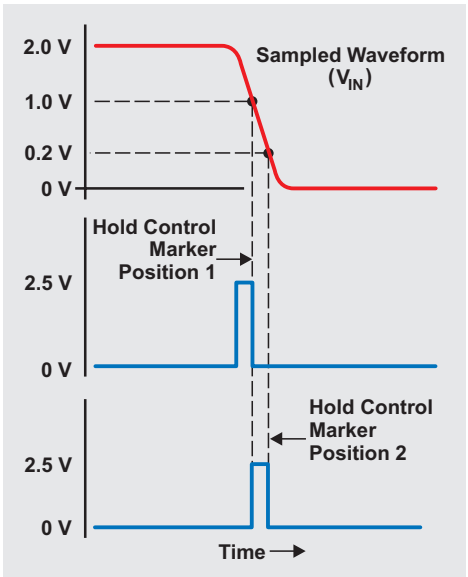


Figure 4. Example of AWG610 output and marker synchronization



have been recorded, the S/H curve can be plotted and analyzed. Programming the waveform generator with software like MATLAB® or LabVIEW™ makes changing the marker and recording the results very simple. With the marker set in position 1, the S/H circuit tracks the V_{IN} voltage level when the marker is high and holds that value when the marker is low. At position 1, the output is held at 1 V. At position 2, the output is held at 0.2 V.

Figure 5 shows the test setup for measuring settling time where the AWG610 and OPA615 were used for the S/H functions. All signal lines were matched at 50 Ω. The output of the waveform generator was used as the test signal with two S/H circuits: One measured the input of the DUT (OPA656), and the other measured the DUT output. Digital multimeters (DMMs) were used to record the held values.

As an example of this method, take measuring a settling time of up to 100 ns. Assume that the waveform generator is programmed to continually output a square wave with a duty cycle of 50% and a period of 200 ns. The marker is initially set at the beginning of the falling edge of the waveform generator's output. The generator runs continually (executes many cycles of sampling and holding), and the S/H circuit integrates its output voltage to a steady DC value. This value is then recorded by the DMM, and the test engineer moves the marker to the next position, repeating this cycle until data for 100 ns has been recorded.

Figure 6 shows the plotted waveforms that resulted when the test setup in Figure 5 was used. To obtain a settling-time error waveform, the DC error was offset, and the output was normalized to the input. The result is shown in Figure 7.

Limitations and challenges

There are some limitations to the setup described here that should be kept in mind. When in doubt, the designer should always use the following equation:

$$I = C_{HOLD} \times dv/dt$$

For this equation, the size of the initial C_{HOLD} should be chosen based on three factors:

1. During the holding time, the OTA biasing current will flow in or out of the capacitor, thus affecting the accuracy of the voltage held.
2. Since a voltage droop will occur on the capacitor due to the biasing current, a delta voltage should be chosen based on the percentage of error within which the measurement should stay.
3. Delta time is the duration for which the sampled voltage is held and should be no longer than the planned settling time to be measured.

For example, C_{HOLD} should be no less than 50 pF under the following conditions: The biasing current of the OTA is 0.5 µA; an error of less than 0.1% of a 1-V_{PP} signal is to be achieved; and the duration to be measured is 100 ns.

Figure 5. Test setup for measuring settling time

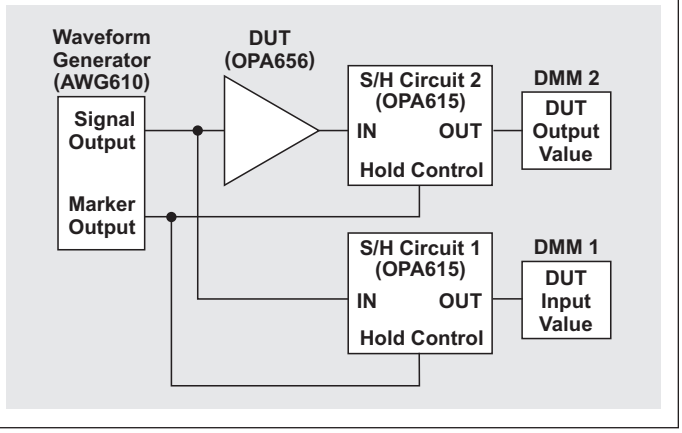


Figure 6. Step waveforms of op amp's input and output

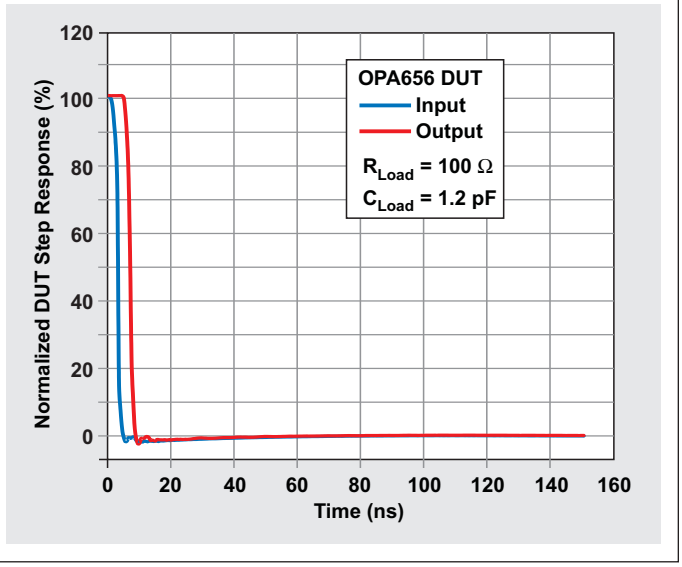


Figure 7. Op amp's normalized settling error

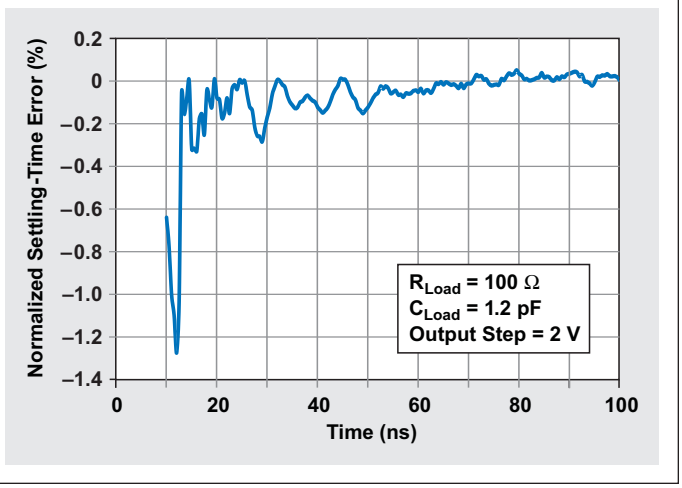
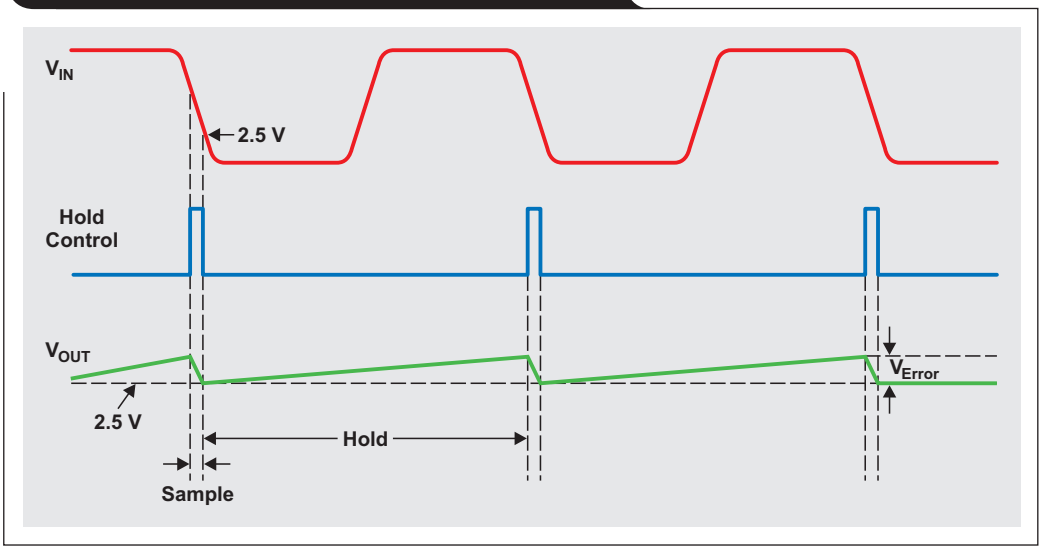


Figure 8. Charge leakage on sampling capacitor



Other considerations

The duration of the sampling time could greatly affect the result of the measurement. During holding, the voltage on the sampling capacitor invariably strays from the supposed DC value because the OTA demands a biasing current. This voltage is then readjusted back to the expected DC value during sampling. The DMM that is reading the output of the S/H circuit is thus essentially taking an average value of this triangle waveform. This phenomenon is shown in Figure 8. To reduce this error, the holding time should be minimized and the capacitor size maximized. It should be kept in mind that the bigger the sampling capacitor is, the more S/H cycles (integration time) will be needed for the charges to integrate to a steady DC value.

Of course, increasing the sampling time does not mitigate the leakage problem. A minimum sampling time should be used that still guarantees the SOTA's holding-time delay and ensures enough time for the sampling capacitor's charge/discharge while it is tracking the S/H circuit's input. Figure 9 shows the recorded values of the op amp's settling time when different sampling times were used with the same holding and integration times. The results were measured against the same waveform taken from a 6-GHz, 10-bit oscilloscope, which showed a maximum overshoot of –60 mV. The measurement using a 20-ns sampling time matched that from the oscilloscope, but at the cost of applying a significant filter over the result. Conversely, the measurement using 6 ns applied a smaller filter but produced a bigger overshoot, which is an artifact of the measurement.

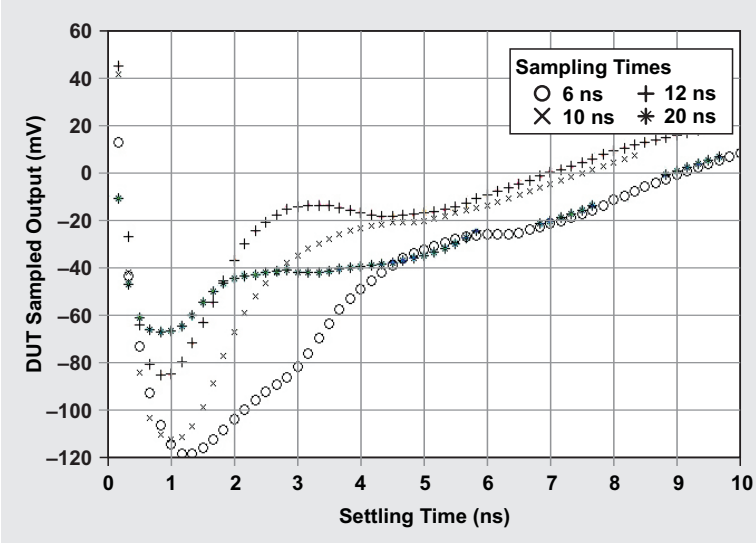
Conclusion

Numerous techniques exist for measuring settling time. This article has introduced a simple yet accurate technique that uses a relatively fast waveform generator and a S/H circuit. Knowing the limitations of this method, the user should be able to adjust any measurement parameters necessary to obtain the best results for a given settling-time range and expected accuracy.

Related Web sites

amplifier.ti.com
www.ti.com/product/OPA615
www.ti.com/product/OPA656
www.ti.com/tinati-ca

Figure 9. Settling time measured with different sampling times



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