

# SPICE models for Precision DACs

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## The challenge – complete system verification

Predicting the performance of a design before it is implemented is a challenge faced by every design engineer. IC designers have myriads of tools and models at their disposal to simulate their designs even before fabrication. However, when considering the full system design, there are very few components for which accurate models exist.

This means that a full system-level verification has to be done manually by the designer via budgeting, spot checks, modeling, visual inspection and modifications based on previous experience. Unfortunately, this leaves a potential for errors and bugs in the design. In some cases, several board revisions are required to achieve the intended functionality and performance.

## The building blocks – Precision DAC models

The latest TINA-TI™ software models for precision DACs, such as the DAC8411 family from Texas Instruments, enable full system-level verification. The DAC8411 family consists of 8- to 16-bit single-channel, voltage-output digital-to-analog converters (DACs). The SPICE models for this family are available in two variants. The first is a parallel n-bit wide interface with output buffer, compatible with all TINA versions (Figure 1).

The second is a serial peripheral interface (SPI) with output buffer, compatible with professional TINA-TI software (Figure 2).

Both variants can be useful in simulating the analog signal chain from the DAC output buffer. The SPI model with the output buffer completely models the full DAC functionality. It can be used to simulate the digital signal chain from the DAC's input.

The output buffer model for the DAC includes common DC parameters such as end-point errors with respective temperature coefficients, quiescent current, as well as AC parameters such as capacitive load stability, slew rate, settling time, and power-on glitch, among others. For example, simulation results for DAC8411 gain (Gerr) and offset (Offs) error are shown in Figure 3. Note that the gain error is a percentage of the full-scale range, and the offset error is in microvolts ( $\mu\text{V}$ ).

Figure 1. DAC parallel interface model

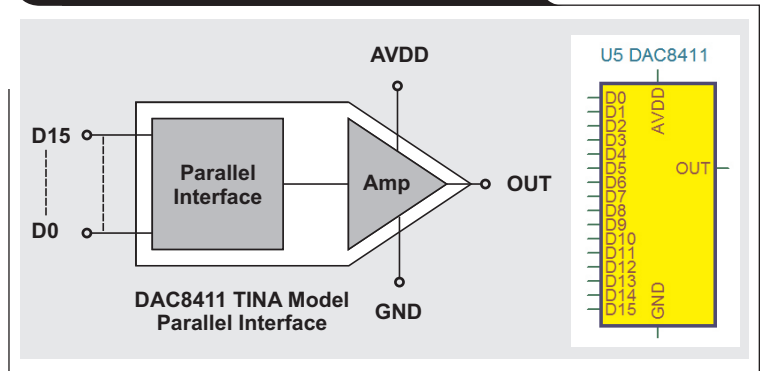


Figure 2. DAC serial interface model

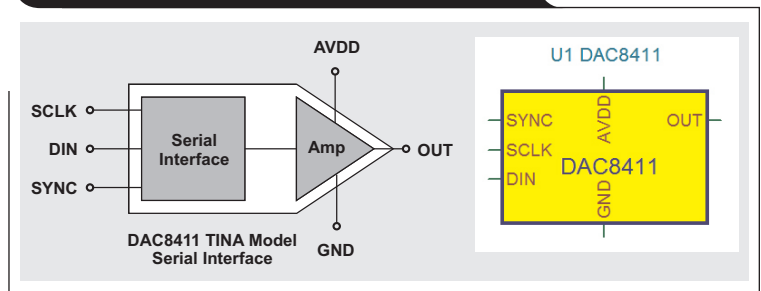


Figure 3. Gain and offset error DC simulations

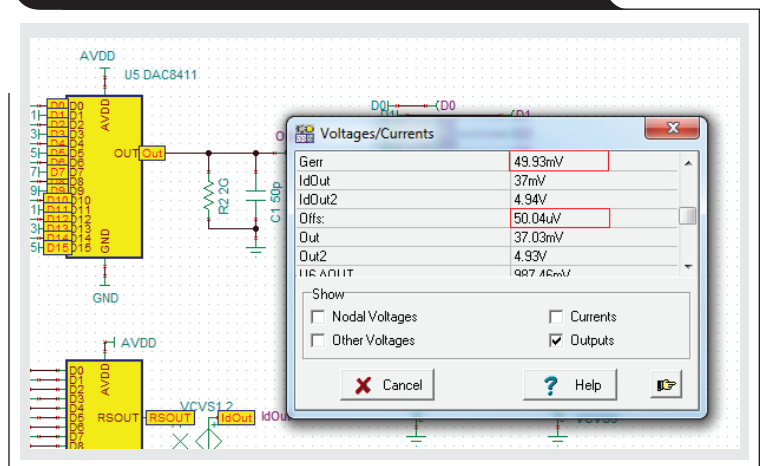


Figure 4 shows a transient simulation that was performed on the DAC with a code step from quarter to three-quarter scale. The plot shows close correlation of the simulated plot to the datasheet plot for this analysis.

The models also allow the designer to enter specific values for some parameters such as the DAC gain and offset errors. This is particularly useful in running what-if simulations for estimating system performance.

### Bringing it together – complete system models

#### Case Study: 0- to 20-mA DAC

One of the most common DAC applications is to create a 0- to 20-mA signal in an industrial automation system, also known as a three-wire system. There are multiple ways to implement this system that range from a fully discrete implementation using a DAC, operations amplifiers, and passive components, to fully-integrated implementations using devices such as the DAC8760.

For this exercise, let's design a basic 0- to 20-mA system using a fully discrete implementation with TINA models for the DAC8411 and OPA192 (Figure 5).

#### Theory of operation

This implementation uses models for the DAC8411, two OPA192 operational amplifiers (OP1 and OP2), two MOS transistors (T1 and T2), and four resistors (R1, R2, R4, and RLOAD). This system generates an output load current into RLOAD that is proportional to a 16-bit input digital code. For this design, OP1 and OP2 are required to handle rail-to-rail inputs.

In order to understand this basic system, we will assume that OP1 and OP2 are ideal. However, subsequent sections use the OPA192 TINA models to simulate the complete system. The DAC8411 model converts the 16-bit DAC code into a proportional analog output voltage (VDAC) in the 0- to 5-V range. This voltage is then applied to the positive input of the operational amplifier (OP2). The negative input of OP2 is also driven to the DAC output voltage (VDAC), thus forcing a current through resistor R4 (VDAC/R4). The operational amplifier (OP2) ensures this current by controlling the gate voltage of MOSFET (T2).

This current is drawn from the supply (V2) via resistor R1. This completes the first stage of this design in which a code proportional current is generated.

The operational amplifier (OP1) maintains equal voltage drops across R1 and R2. Since the value of R2 in this design is a 100 times less than R1, for an equal voltage drop, the current flowing through R2 must be a 100 times greater than the current flowing through R1. This current can be expressed by the formula  $(VDAC/R4) \times (R1/R2)$ .

The operational amplifier (OP1) ensures this current by controlling

Figure 4. Transient simulation showing half-scale settling time

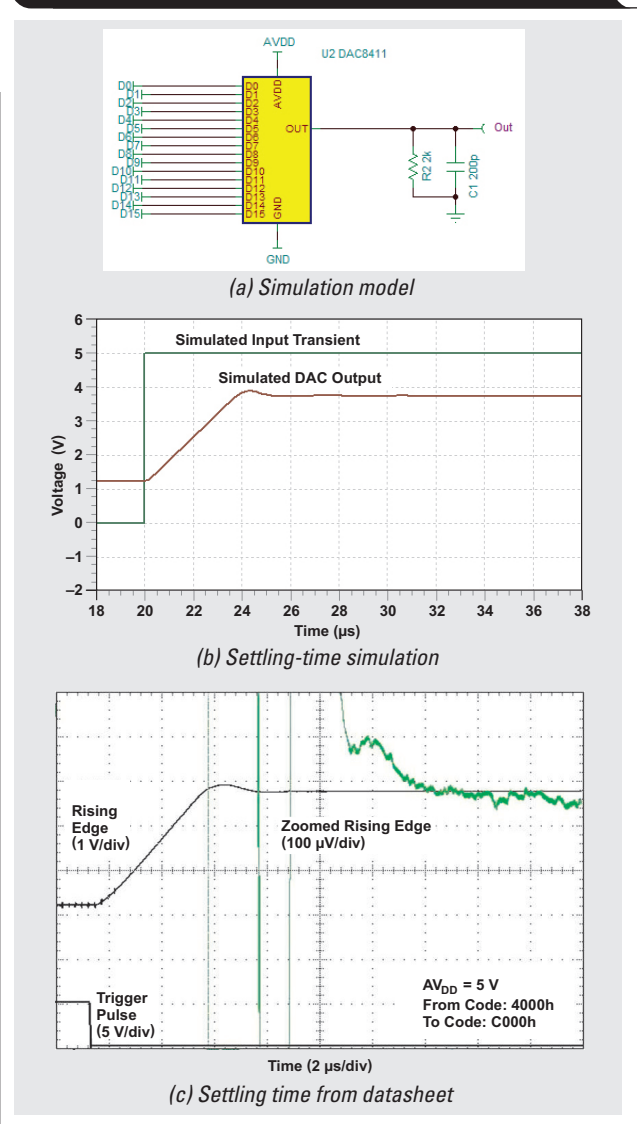
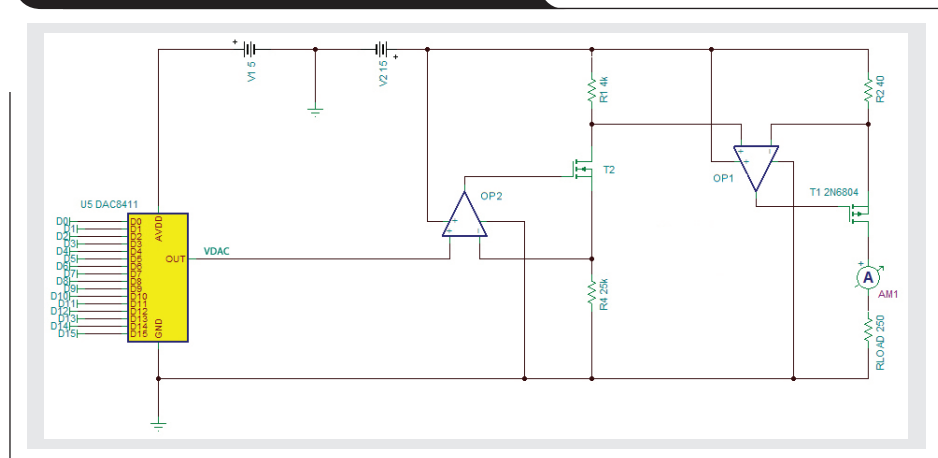
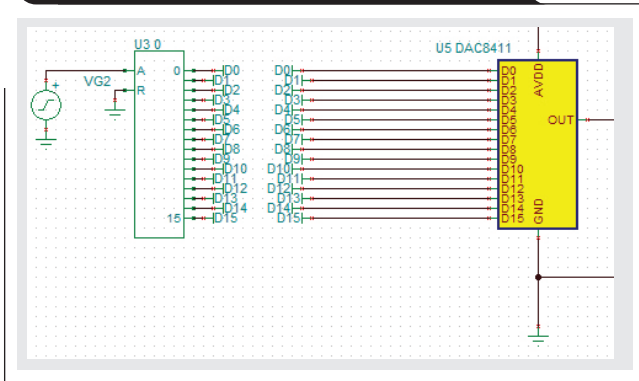


Figure 5. DAC 0- to 20-mA system model



**Figure 6. Input interface test bench for 0- to 20-mA DAC system**



the gate of MOSFET T1. The drain of the T1 is connected to the 250-Ω load resistor (RLOAD) via an ammeter (AM1).

**Simulation setup and results**

The test-bench configuration shown in Figure 6 uses an ideal 16-bit analog-to-digital converter (ADC) to convert a 0- to 1-V analog signal (VG2) into the 16-bit code for the system. A DC sweep of VG2 generates full 16-bit code for the system. The resulting output current is shown in Figure 7.

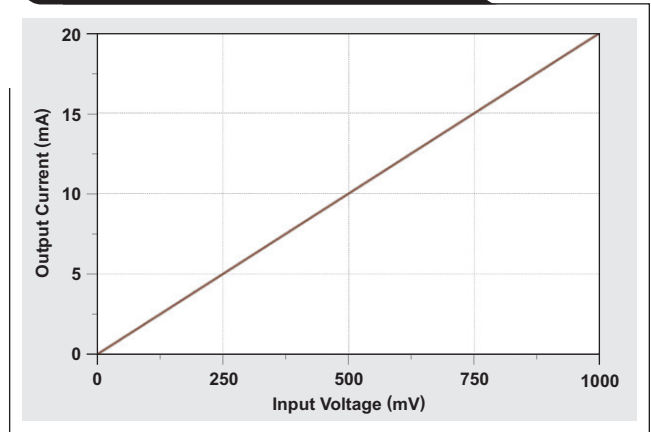
Figure 8 shows a transient analysis for the same circuit. The DAC code is toggled from zero scale to full scale and the resulting output current is plotted.

**Real system non-idealities**

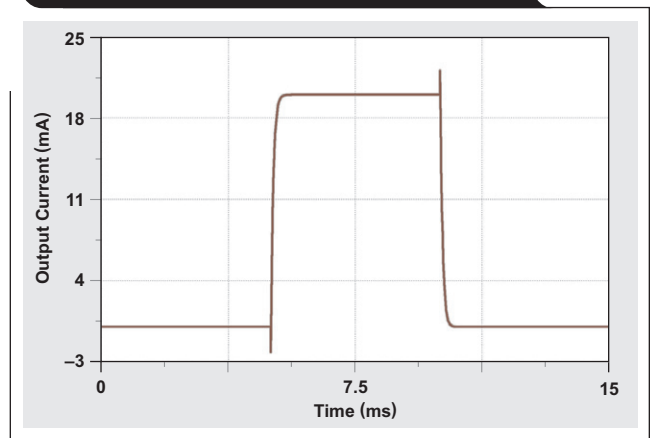
Previously, the 0- to 20-mA system was simulated with DAC8411 and OPA192 parameters modeled as typical. As with any integrated chip, the parameters listed in the datasheet have a typical value, and for some, a max/min value. The intent of placing these boundaries is to guarantee a level of performance on these parameters over a specified temperature range, supply voltages, and process variations. Thus, it is useful to have the system simulated for these variations in the specifications.

The latest TINA-TI software models for the DAC allow designers to modify some critical parameters and run what-if simulations. To illustrate this feature, an example simulation was chosen in which the DAC offset voltage is varied from a typical to the maximum value. This spec is captured in the models by the OFFS parameter shown in Figure 9.

**Figure 7. DAC system simulation of output current DC sweep**



**Figure 8. DAC system simulation of output current transient**



**Figure 9. DAC model, user-adjustable DAC offset voltage**

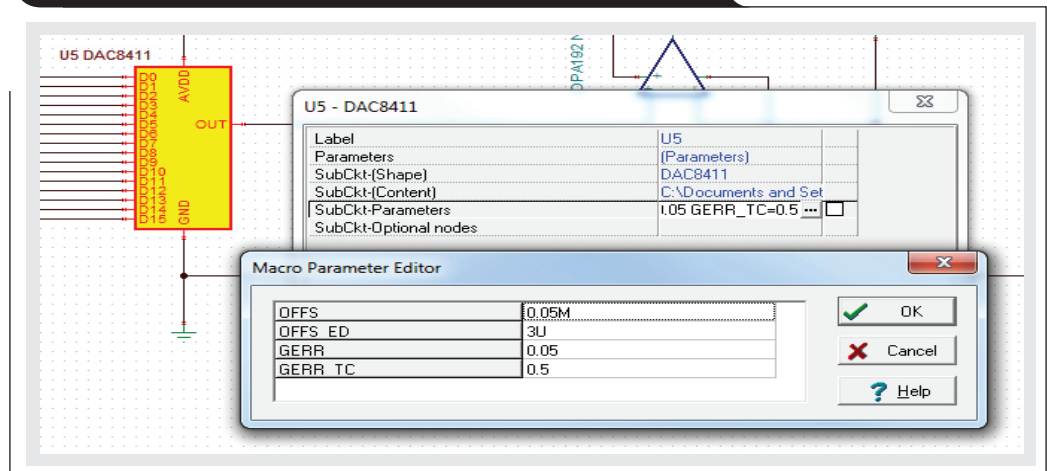


Figure 10 shows the system's DC performance (system output current of model in Figure 5) for two values of DAC offset voltage.

Note that the green curve is the simulation result with the worst-case offset voltage (3 mV), and the red curve is with offset voltage set to typical value of 0.05 mV. For simplicity, the displayed output current in Figure 10 is zoomed in to show the offset in the output. This particular simulation is useful to predict the response of the system for the worst-case DAC offset voltage.

## Conclusion

The DAC models described allow full system verification. However, the level of accuracy and system parameters that can be verified depend on the accuracy of the models as well as the capability of the simulation tool. Using the system shown in Figure 5 as an example, the level of verification depends on the DAC models, operational amplifiers, MOSFETs, and discrete components along with the capability of the TINA simulator. The simulator capability can be improved by using the professional version of the simulation software. This leaves the accuracy of the component models to be the limiting factor for comprehensiveness of the system verification.

## References

1. SPICE-Based Analog Simulation Program by Texas Instruments. Available: [www.ti.com/tool/tina-ti](http://www.ti.com/tool/tina-ti)
2. DAC8411 models. Available: [www.ti.com/product/DAC8411/toolssoftware](http://www.ti.com/product/DAC8411/toolssoftware)
3. OPA192 models. Available: [www.ti.com/product/OPA192/toolssoftware](http://www.ti.com/product/OPA192/toolssoftware)

## Related Web sites

[www.ti.com/4q14-DAC8411](http://www.ti.com/4q14-DAC8411)

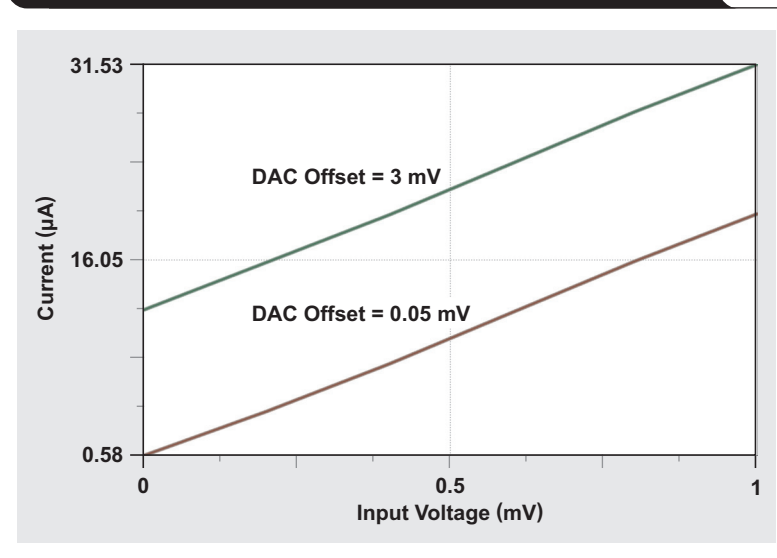
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**Figure 10. DAC system simulation for output-current DC sweep with user-adjusted offset error**



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