How to select input capacitors for a buck converter

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Introduction

Electromagnetic interference (EMI) can create serious issues for manufacturers in an industrial environment. A buck converter generates a pulsating ripple current with high di/dt at the input. Without input capacitors, ripple current is supplied by the upper power source. Printed circuit board (PCB) resistance and inductance causes high-voltage ripple that disrupts electronic devices. The circulating ripple current results in increased conducted and radiated EMI. Input capacitors provide a short bypass path for ripple current and stabilize bus voltage during a transient event.

In recent years, the advancements in power-MOSFET technology have dramatically increased switching frequency and gate driving speeds of switch-mode power supplies. Therefore, reducing the input-voltage ripple of a buck converter has become more challenging. This article uses a buck converter as an example to demonstrate how to select capacitors to achieve optimal performance.

Figure 1 shows the basic circuit of a buck converter. The converter input current (i_{IN_D}) consists of an alternating ripple current (Δi_{IN_D}) and DC current (I_{IN_DC}).

Design parameters:

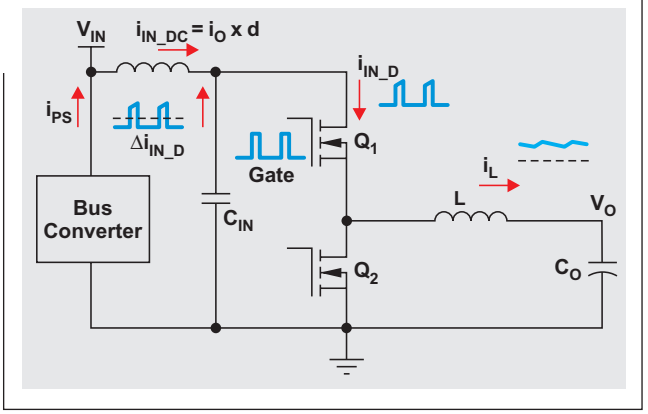
- Output voltage, V_O = 1.2 V
- Maximum load current, I_O = 6 A
- Estimated efficiency at maximum load, η = 87%
- Switching frequency, f_{SW} = 600 kHz
- DC input bus voltage = 12 V with 5% tolerance
- Worst-case maximum input voltage, V_{IN_max} = 16 V
- Bus converter control bandwidth = 6 kHz
- Transient load step, I_{Step} = 3 A
- Worst-case board temperature = 75°C

Design requirements:

- Allowed input peak-to-peak ripple voltage, $\Delta V_{IN\_PP} \leq 0.24$ V
- Allowed input transient undershoot or overshoot, $\Delta V_{IN\_Tran} \leq 0.36$ V

The capacitor voltage rating should meet reliability and safety requirements. For this example, all input capacitors are rated at 25 V or above. The following discussion focuses on meeting electrical and thermal requirements, optimizing performance, and lowering size and cost.

Figure 1. The basic circuit of a buck converter



1. Select key ceramic capacitors to bypass input ripple current

Among the different types of capacitors, the multilayer ceramic capacitor (MLCC) is particularly good regarding allowable ripple current. A starting point is to select the key ceramic capacitors to meet the requirements for ripple voltage and current.

Table 1 shows five different ceramic capacitors that were chosen for this article. Due to DC bias capacitance degrading, the effective capacitance is not the same as the rated capacitance.

Table 1. Key electrical specifications of five ceramic capacitors

Designators	Size Code	Rated Capacitance (µF) at 0 VDC	Tolerance (%)	Temperature Code
A	SM1210	10	±10	X5R
B	SM1206	10	±10	X5R
C	SM0805	4.7	±10	X5R
D	SM0603	1	±10	X5R
E	SM0402	1	±10	X5R

Figure 2 shows the AC current flowing through the input capacitors and the resulting voltage ripple across the ceramic capacitors, assuming the majority of the ripple current flows through these ceramic capacitors. Since the equivalent series resistance (ESR) of ceramic capacitors is very low, ripple resulting from ESR can be ignored.

Equation 1 is used to estimate the required effective capacitance that will meet the ripple requirement. The worst case for this example occurs at maximum duty cycle, which is less than 50%.

$$C_{IN} \geq \frac{D \times (1-D) \times I_O}{\Delta V_{IN\_PP} \times f_{sw}} \quad (1)$$

Duty cycle, D, can be calculated with Equation 2. For this example, D ranges from 8.6% to 12.1% with maximum load.

$$D = \frac{V_O}{V_{IN} \times \eta} \quad (2)$$

The input capacitance should be greater than 4.43 µF as calculated with Equation 1. Taking 10% tolerance into consideration, the total effective capacitance should be greater than 4.92 µF with 12-V DC bias. Figure 3 shows the effective capacitance over DC bias of different capacitors in the inventory.

Besides the ripple-voltage requirement, the ceramic capacitors should meet the thermal stress requirement as well. A starting point is to estimate the maximum root-mean-square (RMS) of Δi_{IN_D}. Figure 4 shows the ratio of input ripple current RMS over load current (I_{IN_RMS}/I_{Load}) as a function of the duty cycle.

For this example, the maximum input ripple current RMS occurs at full load and with duty cycle of 12.1%, according to Figure 4. Now calculate $I_{IN\_RMS\_max}$ using Equation 3. $I_{IN\_RMS\_max}$ = 1.97 A_{RMS}.

$$I_{IN\_RMS\_max} = I_O \times \sqrt{D \times (1-D) + \frac{1}{12} \times \left(\frac{V_O}{L \times f_{SW} \times I_O} \right)^2 \times (1-D)^2 \times D} \quad (3)$$

Figure 2. Input ripple current and ripple voltage waveforms

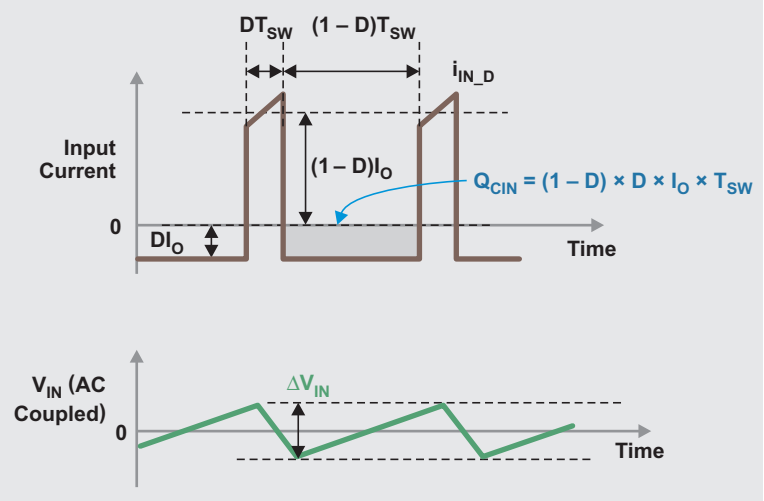


Figure 3. Capacitance using ceramic capacitors versus DC bias

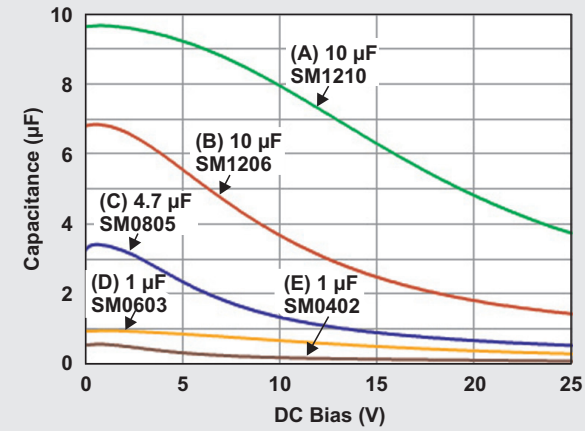


Figure 4. Input RMS/Load current ratio versus duty cycle

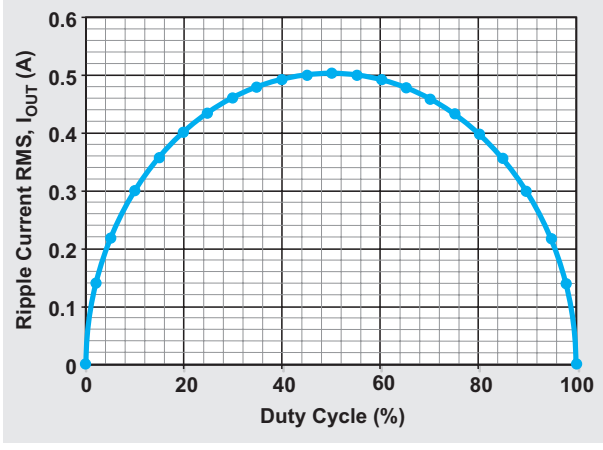


Figure 5. Temperature characteristics of different capacitors

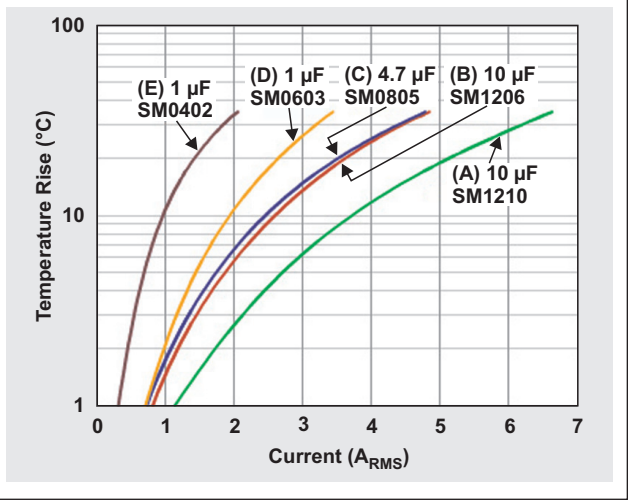
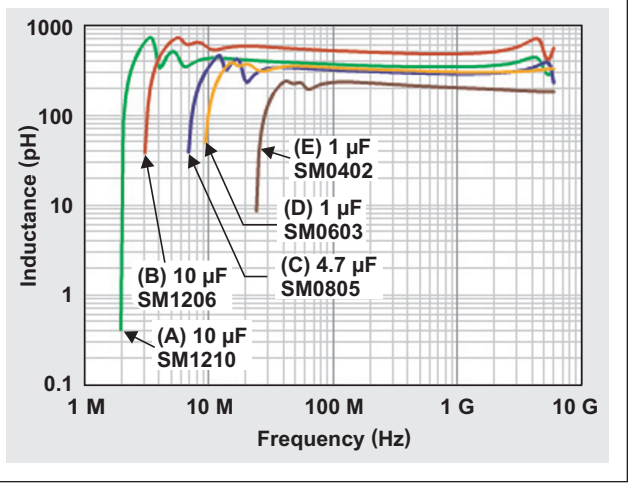


Figure 6. Equivalent series inductance of multilayer ceramic chip capacitors



Since the board temperature is 75°C and the X5R MLCC is rated for 85°C, capacitor temperature rise should be lower than 10°C. Figure 5 shows the temperature rise characteristics of different ceramic capacitors.

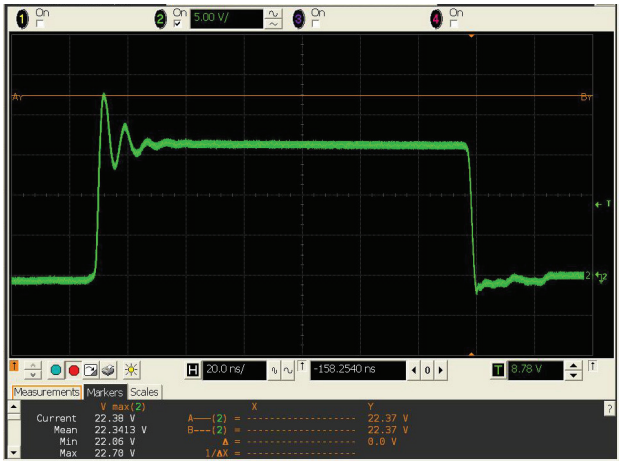
According to Figures 3 and 5, the ripple and thermal stress requirements can be met by combining two (B) capacitors or one (A) capacitor. Both selections have a similar cost and solution size. At this point, a third factor, the equivalent series inductance (ESL) should be included. Figure 6 shows the ESL of all five capacitors.

With two (B) capacitors in parallel, the combined ESL is about 0.3 nH, while one (A) capacitor has an ESL of 0.5 nH. Two (B) capacitors were selected for a total effective capacitance of 6 µF, and an allowable ripple current of 5.2 A_{RMS} with a 10°C temperature rise.

2. Add small ceramic capacitor(s) with low ESL to alleviate input spikes and phase-node ringing

With MOSFET technology advancement, transition time is dramatically reduced which improves efficiency. This leads to a high di/dt slope of the input current and high-voltage spike at the input and phase node. The ESL of the ceramic capacitors plays a significant role. Thus, it is desirable to further lower the input capacitor ESL. This can be achieved by adding a small capacitor with low ESL. Despite the fact that ESL varies with material and structure, a common rule of thumb is that a capacitor with a smaller case has a lower ESL (Figure 6).

Figure 7. Switch-node waveform without additional small input ceramic capacitor



For phase-node ringing, it is common practice to use a boot resistor to slow down the gate speed and a snubber circuit for alleviation. However, both methods incur additional power loss and sacrifice efficiency. Phase-node ringing can be reduced without the penalty of lower efficiency.

Figure 7 shows the phase-node waveform of the TPS53318 with two (B) capacitors as the only input capacitors. V_{IN} is 16 V and the load is 6 A. The phase-node voltage spike is 22.7 V.

Under the same test conditions, one (D) capacitor was added to the input. As shown in Figure 8, the spike voltage was reduced from 22.7 V to 20.5 V. This is a significant improvement without sacrificing efficiency.

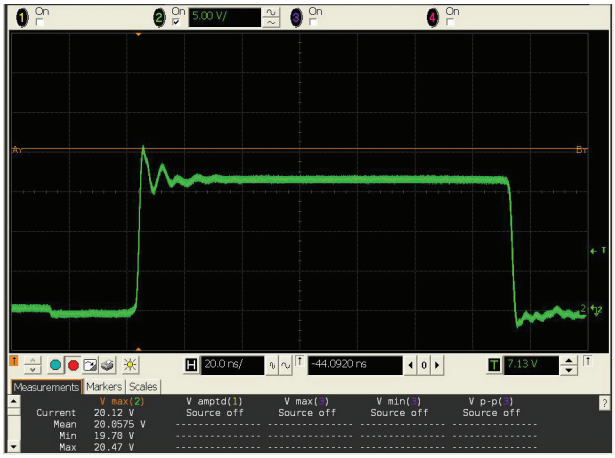
While an additional small ceramic capacitor can alleviate phase-node ringing, it can take up precious PCB space and in some cases increase cost. It is a trade-off of cost, size and performance. However, in this example, the added (D) capacitor did not increase the solution size.

3. Select bulk capacitors

While the MLCC is excellent regarding allowable ripple current, it is notorious regarding effective capacitance that is necessary to meet transient response requirements. Bulk capacitors with high capacitance are more cost-effective than using all ceramic capacitors. Aluminum electrolytic and polymer are popular capacitors for this purpose. There are two key factors for selecting bulk input capacitors: 1) overshoot and undershoot requirement of transient response; and 2) allowable ripple current requirement.

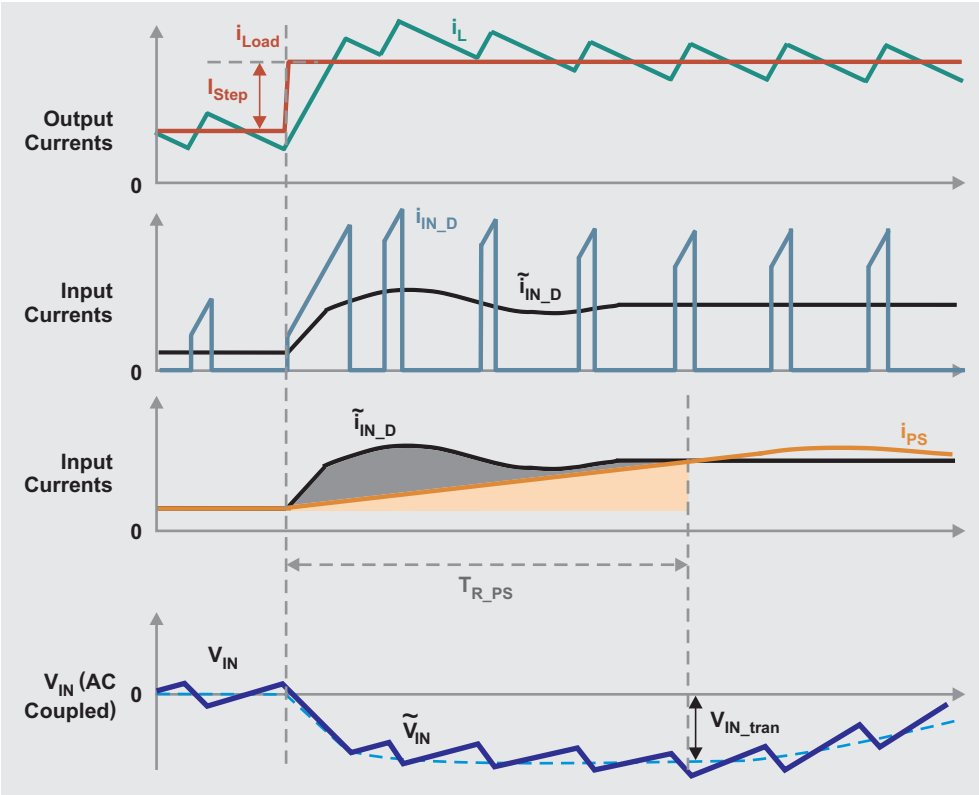
The ESR of the bulk capacitor (ESR_B) and the capacitance (C_B) need to meet the transient response requirement. Figure 9 shows the idealized load-transient current (i_{Load}), inductor current (i_L), input-transient current (i_{IN_D}) and bus-converter current (i_{PS}). The average input current ($\tilde{i}_{IN\_D}$) can be approximated by the product of i_L and the duty cycle, D.

Figure 8. Switch-node waveform with additional small input ceramic capacitor



There could be two V_{IN} spikes during the transient: the first spike is related to the ESR_B; and the second spike is caused by the difference between the buck-converter input current ($\tilde{i}_{IN\_D}$) and the bus-converter output current (i_{PS}). Both spikes should be lower than the V_{IN} undershoot or overshoot requirement (V_{IN_tran}).

Figure 9. An idealized transient current plot



The ESR_B should be lower than that calculated with Equation 4.

$$ESR_B \le \frac{V_{IN\_Tran}}{I_{Step} \times D_{max}} \quad (4)$$

With D_{max} = 12.1%, I_{Step} = 3 A, and ΔV_{IN_tran} = 0.36 V, ESR_B should be less than 0.99 Ω.

The second spike is related to the response of the bus converter. The converter output-current rise time during a transient event, T_{R_PS}, can be approximated by Equation 5.

$$T_{R\_PS} \cong \frac{1}{f_{BW\_PS} \times 4} \quad (5)$$

T_{R_PS} is about 41.67 µs with a control bandwidth of 6 kHz.

The capacitance of the bulk capacitor (C_B) should be greater than that calculated with Equation 6.

$$C_B \ge \frac{\frac{1}{2} \times I_{Step} \times D_{max} \times T_{R\_PS}}{V_{IN\_Tran}} - C_{CE\_Total} \times (1 - Tol.) \quad (6)$$

Where C_{CE_Total} is the total capacitance of the ceramic capacitors, and the tolerance of the capacitors is 10%. Also, C_B should be greater than 15.07 µF. Given a 20% tolerance, the rated capacitance of the bulk capacitor should be greater than 18.84 µF.

Another factor for selecting a bulk capacitor is the allowable ripple current. It is a common practice that most low-cost electrolytic capacitors have an impedance that is much higher than the ceramic capacitors used for ripple-current bypassing. Thus, it can be assumed that the ripple voltage is not affected by the bulk capacitor. Figure 10 shows the idealized ripple current through the bulk capacitor.

The bulk capacitor ripple current (Δi_{CB}) can be approximated by the input ripple voltage divided by the ESR_B. Since the current-ripple waveform is triangular, the RMS of the ripple current (I_{CB_RMS}) can be estimated with Equation 7.

$$I_{CB\_RMS} = \frac{1}{2 \times \sqrt{3}} \times \frac{\Delta V_{IN\_PP}}{ESR_B} \quad (7)$$

The input ripple voltage can be calculated with Equation 8.

$$\Delta V_{IN\_PP} \approx \frac{D \times (1 - D) \times I_O}{C_{CE\_Total} \times f_{SW} \times (1 - Tol.)} \quad (8)$$

When selecting the bulk capacitor, I_{CB_RMS} should be less than the allowable ripple current, $I_{CB\_RMS\_Allowed}$.

$$I_{CB\_RMS\_Allowed} \ge I_{CB\_RMS} \quad (9)$$

Thus, the allowable ripple current and bulk-capacitor ESR should meet the constraint specified with Equation 9 as shown by Equation 10.

$$I_{CB\_RMS\_Allowed} \times ESR_B \ge \frac{1}{2 \times \sqrt{3}} \times \Delta V_{IN\_PP\_max} \quad (10)$$

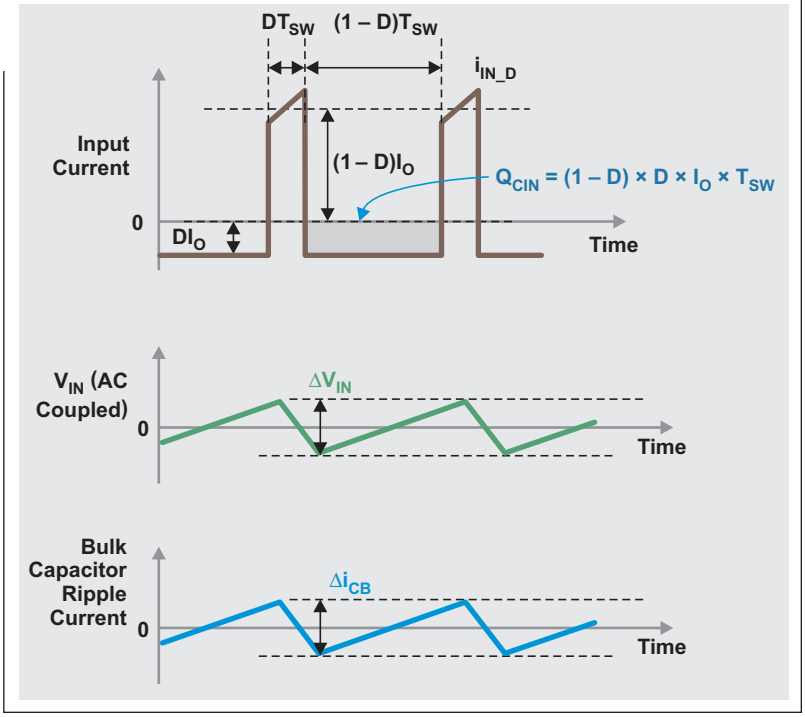
With D_{max} = 12.1%, C_{CE_Total} = 6.6 µF and tolerance = 10%, the maximum input ripple voltage ($\Delta V_{IN\_PP\_max}$) is about 179 mV. Thus, the product of the allowable ripple current and the ESR should be greater than 51.7 mV by Equation 9. Table 2 shows the parameters of five different electrolytic capacitors.

Table 2. Electrical performance of bulk capacitors

Designators	Rated Capacitance (µF)	Ripple Current (100 kHz) (105°C) (mA) (RMS)	Impedance (100 kHz) (+20°C) (Ω)	Tolerance (%)
F	10	90	1.35	±20
G	22	160	0.7	±20
H	33	160	0.7	±20
I	33	240	0.36	±20
J	47	240	0.36	±20

To meet both the transient and ripple current requirements, capacitor G was selected from Table 2 for the input bulk capacitor. For applications where one electrolytic capacitor is not sufficient, multiple electrolytic capacitors can be put in parallel to meet transient requirements.

Figure 10. Idealized input ripple currents and input ripple voltage



However, the criterion for the product of the allowable ripple current and the ESR_B remains the same. If no electrolytic capacitor meets the ripple-current requirement, extra ceramic capacitors are necessary. The extra ceramic capacitance can be estimated by solving Equations 8 and 9.

The proper PCB layout is also critical for the performance of the switch-mode converter. Robert Taylor demonstrated the recommended input capacitors placement in his Power Tips post.[1] Please refer to his blog post for input capacitor PCB layout recommendations.

Conclusion

The combination of ceramic and electrolytic capacitors renders a cost-effective solution for bypassing high-di/dt input ripple current and meeting load-transient response requirements. Following the tips and processes described could help you to select the proper input capacitors for a reliable, highly-efficient and compact DC/DC converter.

References

1. Robert Taylor, “Don’t let your power supply layout ruin your day!” Power House blog, TI E2E™ Community, January 23, 2015.
2. Chester Simpson, “Engineers Note: Capacitors are key to voltage regulator design,” (SNOA842), Texas Instruments, 2011.

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