Automotive EMC-compliant reverse-battery protection with ideal-diode controllers

By Dilip Jain, *System Lead, Power Switches, Bangalore*
Abhijeet Godbole, *System Engineer, Power Switches, Bangalore*

Introduction

Given the emergence of new trends in automotive electronics such as autonomous driving and car infotainment systems, system designers are facing new challenges when designing automotive front-end power systems. Discrete reverse-battery protection solutions like Schottky diodes and P-channel field-effect transistors (FETs) are no longer a viable solution for the 100- to 1,000-W power levels required in electronic control unit (ECU) designs due to their poor efficiency, need for thermal management and the space they consume on a printed circuit board. The need to adhere to strict automotive electromagnetic compatibility (EMC) testing limits adds another layer of complexity when designing these front-end power systems.

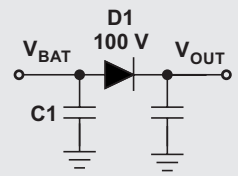
This article highlights how a dual gate-drive architecture driving back-to-back power N-channel FETs helps simplify the design of a reverse-battery protection system and enables designers to adhere to EMC compliant testing limits set by various standards or original equipment manufacturers (OEMs).

Reverse-battery protection

Reverse-battery protection activates when battery terminals are incorrectly connected during jump start, vehicle maintenance or service because a connection error can damage the components in ECUs if they are not rated to handle reverse polarity. Reverse-battery protection is an important feature for semiconductor components that operate directly from a vehicle battery.

There are various solutions available to realize reverse polarity protection. A common solution is series diode in the positive path, and another is a P-channel metal-oxide semiconductor field-effect transistor (MOSFET)-based architecture. However, ideal-diode controllers driving N-channel FET-based reverse-battery protection circuits are gaining wider acceptance because of system-level benefits in terms of efficiency, size and cost, along with the ability to comply with EMC-compliant testing limits. Figure 1 compares these three solutions and lists their performance benefits.

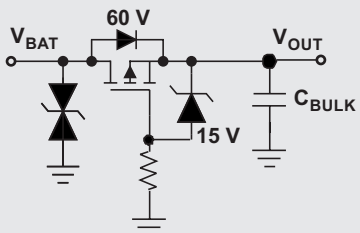
Figure 1. Common schemes for reverse-battery protection



Pros:
- Simple to use
- Suitable for lower current levels (1 to 3 A)

Cons:
- Poor efficiency at higher current levels
- Poorer cold-crank performance due to forward drop (0.5 to 1 V)

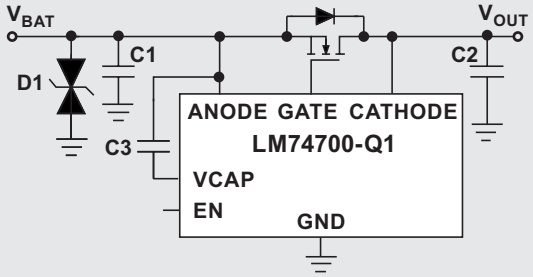
(a) Series diode



Pros:
- Simple to use

Cons:
- Larger size and higher cost for lower $R_{DS(on)}$
- Poorer thermal performance compared to N-FET based solution
- No reverse current blocking

(b) P-FET



Pros:
- Simple to use
- Size, cost and efficiency benefits at higher current levels
- Provides reverse current blocking
- Easier to meet system-level EMC performance

Cons:
- Optimum system solution for load current more than 3 A

(c) Ideal-diode controller + N-FET

Automotive EMC testing

An automotive battery connects to multiple loads, including ECUs, relays and motors. Several system-level events, such as turning inductive loads on or off, can create voltage transients on the battery supply lines. Capacitive and inductive coupling via lines other than the battery supply lines can also create electrical transients.

International Organization for Standardization (ISO) 7637-2, ISO 16750-2, Japanese Automotive Standards Organization A-1 and Society of Automotive Engineers J1113-11 all specify automotive electrical line transient's behavior and impact. Apart from these automotive industry standards, many automotive OEMs have their own standards. One such standard is LV 124, which was drawn up by representatives from Audi AG, BMW AG, Daimler AG, Porsche AG and Volkswagen AG. Figure 2 illustrates some of the tests specified in LV 124.

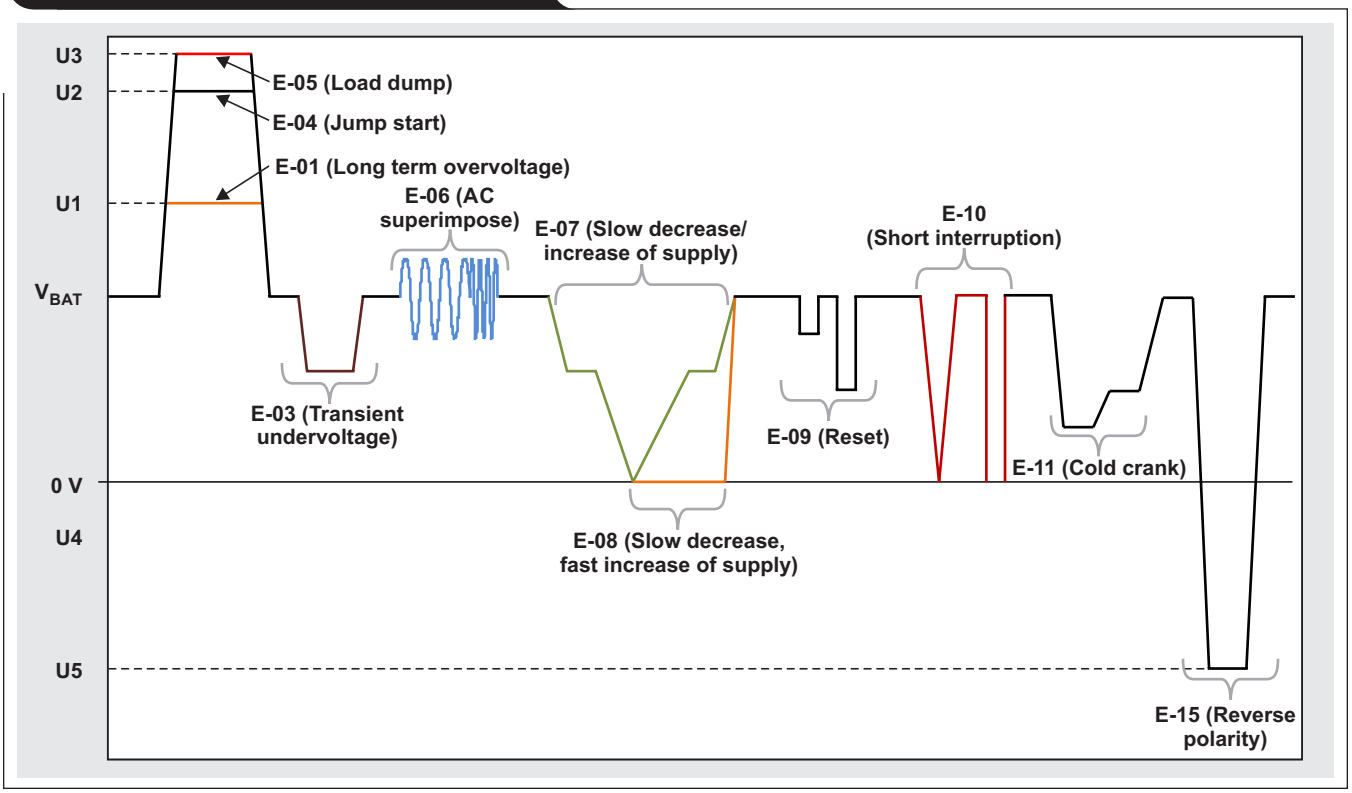
All reverse-battery protection devices must meet system-level tests. Some tests, such as LV 124 E-06 (superimposed alternating voltage) and E-10 (short interruption) are very hard to meet with diode and P-channel FET-based reverse-battery protection solutions. The LV 124 E-06 test applies a superimposed alternating voltage while the engine is running. This test requires an AC peak-to-peak ripple as high as 6 V on a 13.5-V_{DC} battery voltage, swept from 15 Hz to 30 kHz. The LV 124 E-10 test applies short interruptions at the input, typically for a duration ranging from 10 µs to few milliseconds to check whether electronic modules are immune to short interruptions in the battery supply. Such interruptions can occur due to events such as contact and line errors or bouncing relays. To achieve functional pass status A, electronic modules must function properly with up to 100-µs interruptions in input power.

To achieve active rectification of a 6-V, 30-kHz peak-to-peak AC input voltage during the E-06 test, and to meet class A performance during the E-10 test, having the gate turn off and on quickly is a very important feature. This article addresses specific challenges when implementing a single gate-drive, ideal-diode controller that can comply with LV 124 E-06 and E-10 test requirements.

Reverse-battery protection with back-to-back FETs

Apart from driving a single N-channel FET to realize reverse-battery protection, many systems need driving of back-to-back connected N-channel FETs. Back-to-back connected FETs offer flexibility to designers by offering in-rush current limiting, overvoltage protection control and load disconnection. In order to avoid large current peaks while starting up, in-rush current control is required with huge millifarad capacitive loads. The overvoltage protection feature enables the use of output electrolytic capacitors with a lower voltage rating, which in turn helps reduce the overall solution size for space-constrained applications such as advanced driver-assistance system camera modules. The load disconnect feature enables a reduction of quiescent current when the system is in sleep mode. Dual battery systems for power multiplexer designs also require a back-to-back FET-based reverse-battery protection solution.

Figure 2. LV 124 system-level EMC tests



Ideal-diode controller with single gate-drive driving back-to-back FETs

Figure 3 shows an ideal-diode controller with single gate-drive architecture driving back-to-back FETs. This topology is known as a common source topology.

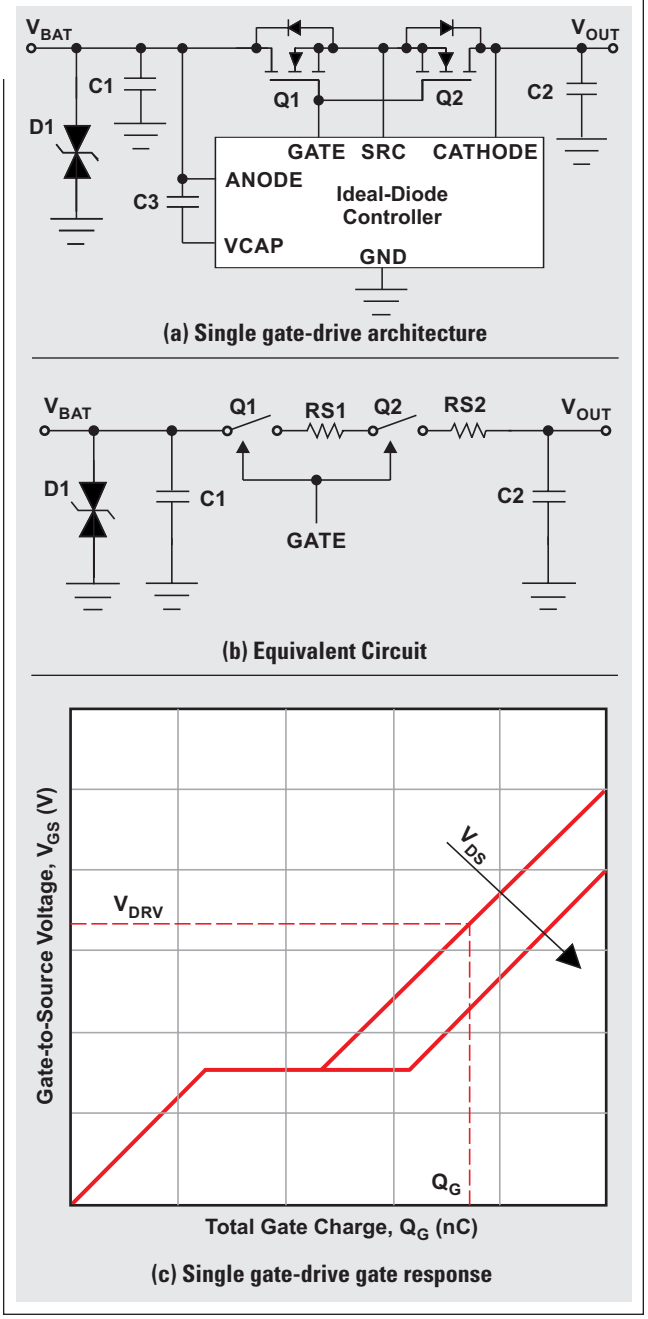
When applying a superimposed alternating voltage to the system, the output bulk capacitor (C2) charges to the peak input voltage. Whenever the input voltage falls below the output voltage, the ideal-diode controller detects a reverse current and turns off FETs Q1 and Q2. When the input voltage rises higher than the output voltage, the ideal-diode controller needs to turn on both FETs quickly, a process that requires charging the gate capacitance greater than the threshold voltage (V_T) of both FETs. The minimum charge pump drive strength required to realize active rectification is given by Equation 1.

$$I_{CP} = (Q_{G1} + Q_{G2}) \times f_{SW} \quad (1)$$

where Q_{G1} and Q_{G2} are the total gate charge for FETs Q1 and Q2, respectively, and f_{SW} is the AC superimpose frequency of the E-06 test.

Equation 1 shows that the total gate charge needed to turn on the FETs is a combination of the individual gate charges of FETs Q1 and Q2. This gate charge varies with the drain-to-source voltage across the FET at the turn-on time. Because a single gate-drive architecture drives two FETs at the same time, this architecture requires a charge pump with a higher gate-drive strength. As mentioned previously, this is one of the specific challenges associated with implementing a single gate-driver architecture. A charge pump with insufficient drive for both FETs can result in skipped cycles during active rectification, as well as higher power losses across the FETs caused by increased switching losses and higher input peak currents during the E-06 test. The single gate-drive architecture also results in a higher output-voltage droop during E-10 testing, resulting in inferior system performance.

Figure 3. An ideal-diode controller with single gate-drive for back-to-back connected FETs



Ideal-diode controller with dual gate-drive driving back-to-back FETs

Figure 4 shows the Texas Instruments LM74800-Q1 ideal-diode controller with an integrated dual gate drive. The DGATE output drives the first FET (Q1) to replace a Schottky diode for reverse input protection and output voltage holdup, while the HGATE output drives the second FET (Q2) to realize power-path on and off control, in-rush current limiting and overvoltage protection. A strong charge pump with a 20-mA, peak GATE current driver and short turn-on and turn-off delay times ensure a fast transient response, which helps stay under LV 124 EMC testing limits.

The LM74800-Q1 rectifies the superimposed alternating voltage (the E-06 test) by controlling DGATE, turning Q1 off quickly to cut off reverse current, and turning Q1 on quickly during forward conduction. Q2 remains on, as it is controlled by the HGATE driver stage. Having Q1 operate as an active rectifier while keeping Q2 on effectively reduces the output-voltage droop to a maximum of the body-diode drop only, and also results in improved power-supply rejection ratio (PSRR) performance when compared to a single gate-drive architecture.

Charge pump loading is reduced by half compared to a single gate-drive architecture. The minimum charge pump drive current required to realize active rectification is given by Equation 2.

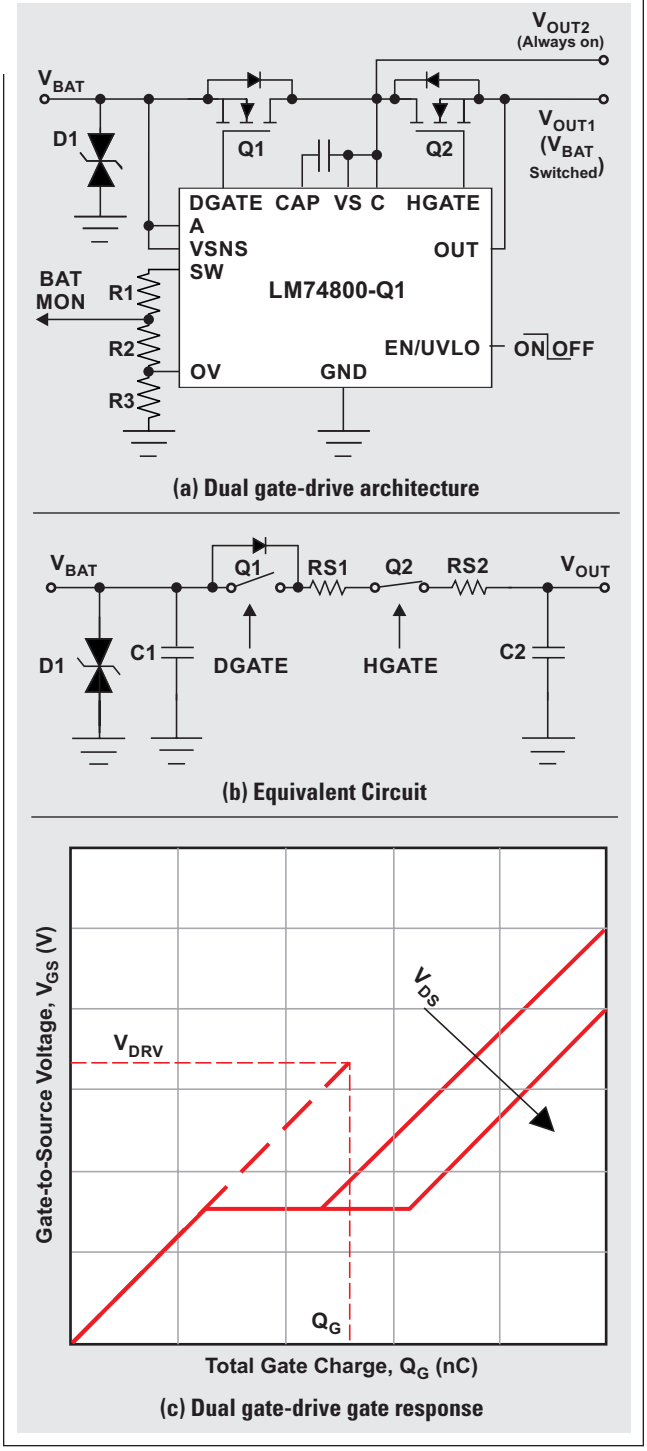
$$I_{CP} = Q_{G1} \times f_{SW} \quad (2)$$

where Q_{G1} is the total gate charge of Q1 and f_{SW} is the AC superimpose frequency of the E-06 test.

Because only Q1 turns on and off during E-06 and E-10 tests, the peak current required to charge the gate is lower than it is for a single gate-drive architecture. Due to Q1 switching, the Miller region is very minimal due to the drain-to-source voltage transition from the body diode drop to $I \times R_{DS(on)}$. The total charge (Q_G) follows a dotted line, as shown in Figure 4.

Active rectification with fast turn-off and turn-on of Q1 results in an AC-rectified current profile and lower root-mean-square currents. Active rectification improves PSRR performance, thereby reducing filtering requirements, which is valuable in end products such as audio amplifiers. Active rectification also reduces the power dissipation in Q1 and the output electrolytic capacitors by more than half compared to a single gate-drive-based controller, thereby reducing the heating effect and increasing the lifetime of the end product, such an ADAS sensor fusion.

Figure 4. LM74800-Q1 ideal-diode controller driving back-to-back FETs



Performance comparison of single and dual gate-drive architectures

It is clear that the single gate-drive architecture needs a higher total gate charge for a given gate-drive voltage level to fully turn on back-to-back connected FETs. This total gate-charge value depends on many variables, such as the drain-to-source voltage, the Miller effect of the FETs, the total output capacitance and the load current when the FET turns on. Assuming identical operating conditions for both architectures and ignoring the Miller effect, the total gate charge required for single gate-drive architecture is about two times that required for dual gate-drive architecture.

Table 1 shows performance comparison of single and dual gate-drive architectures with respect to the minimum charge-pump and current drive strength required to achieve an active rectification. The main cause of permanently superimposed alternating voltages in the electrical system is the energy transformer (e. g. alternator or a DC-DC converter) that powers the electrical system.

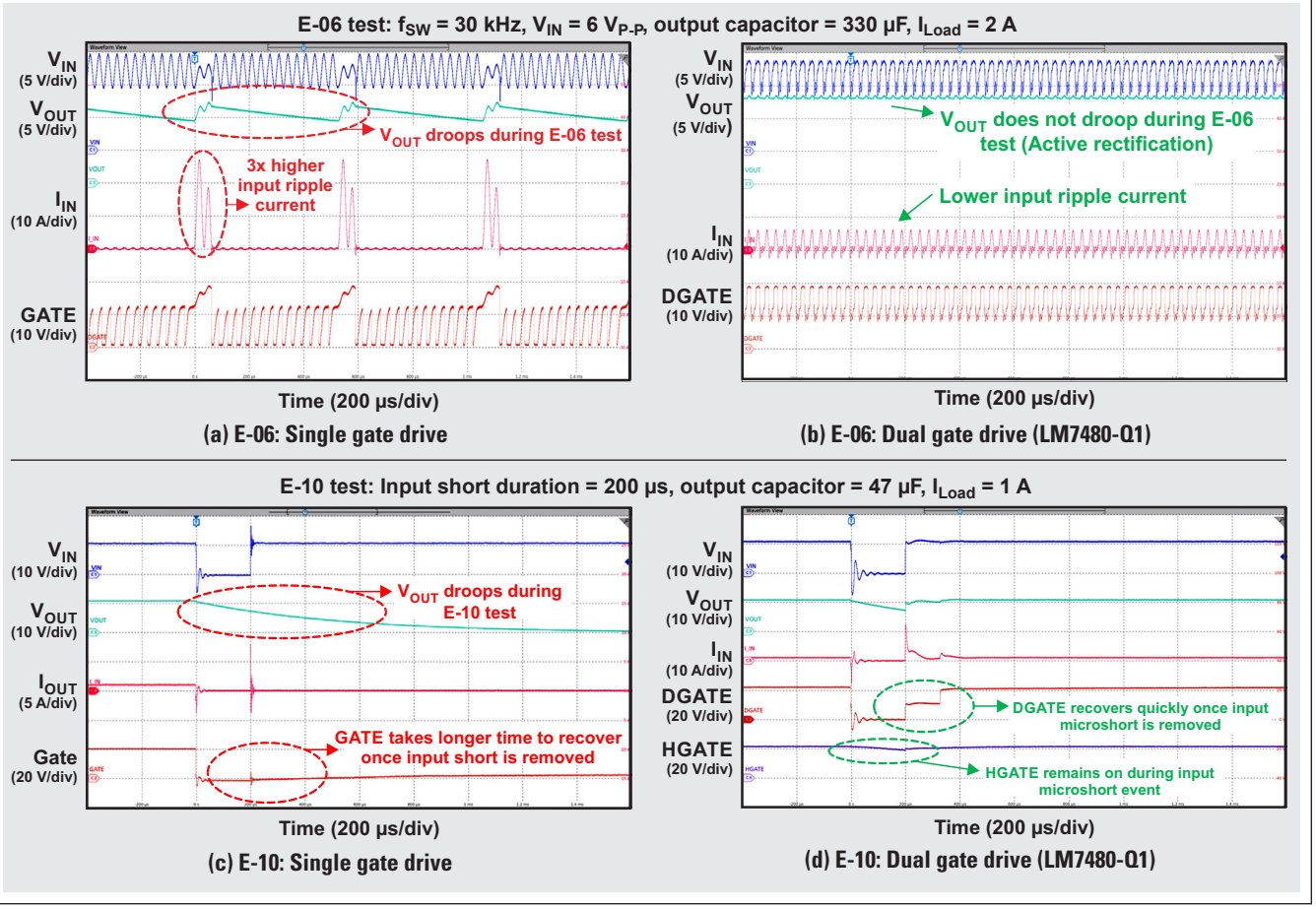
AC superimposed frequency of up to 30 kHz usually comes from an alternator and 200 kHz from a DC-DC converter. The comparison in Table 1 considers commonly used N-FETs with a total gate charge of 13 nC at a gate-drive voltage of 6 V and an AC superimposed frequency of 30 kHz and 200 kHz.

Figure 5 shows performance comparison of single and dual gate-drive architectures when subjected to LV 124 E-06 and E-10 test. Test conditions under which performance is captured for each architecture is also highlighted in Figure 5.

Table 1. Comparison of single vs. dual gate-drive architectures

Parameter	Topology	
	Single Gate-Drive Architecture	Dual Gate-Drive Architecture
Minimum charge pump drive strength (I_{CP_MIN}) at f_{SW} = 30 kHz	$(Q_{G1} + Q_{G2}) \times f_{SW}$ = (13 nC + 13 nC) × 30 kHz = 780 µA	$Q_{G1} \times f_{SW}$ = 13 nC × 30 kHz = 390 µA
Minimum charge pump drive strength (I_{CP_MIN}) at f_{SW} = 200 kHz	$(Q_{G1} + Q_{G2}) \times f_{SW}$ = (13 nC + 13 nC) × 200 kHz = 5200 µA	$Q_{G1} \times f_{SW}$ = 13 nC × 200 kHz = 2600 µA

Figure 5. Comparing single and dual gate-drive architectures in the context of LV 124 E-06 and E-10 tests



Conclusion

Ideal-diode controllers are gaining popularity for systems with front-end reverse-battery protection because of the benefits they offer with respect to size and thermal performance over conventional power diode and P-FET-based solutions. Reverse-battery protection devices are subjected to stringent automotive EMC transients, and their ability to handle EMC transients directly affects overall system reliability. A dual gate-drive architecture, with separate gate control of back-to-back connected FETs enables robust and superior system-level performance during EMC compliance tests. Such architecture also offers flexibility with various features such as in-rush current control, overvoltage protection and load disconnect.

Reference

1. Dilip Jain, "Six System Architectures with Robust Reverse-battery Protection Using an Ideal-diode Controller," Texas Instruments Application Report (SLVAES2), April 2020.

Related Web sites

Product information:
LM7480-Q1
LM7481-Q1

TI Worldwide Technical Support

TI Support

Thank you for your business. Find the answer to your support need or get in touch with our support center at

www.ti.com/support

China: http://www.ti.com.cn/guidedsupport/cn/docs/supporthome.tsp

Japan: http://www.tij.co.jp/guidedsupport/jp/docs/supporthome.tsp

Technical support forums

Search through millions of technical questions and answers at TI's E2E™ Community (engineer-to-engineer) at

e2e.ti.com

China: http://www.deyisupport.com/

Japan: http://e2e.ti.com/group/jp/

TI Training

From technology fundamentals to advanced implementation, we offer on-demand and live training to help bring your next-generation designs to life. Get started now at

training.ti.com

China: http://www.ti.com.cn/general/cn/docs/gencontent.tsp?contentId=71968

Japan: https://training.ti.com/jp

A011617

SLYT802

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265