Application Report
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CDCE6214-Q1 Crystal-Based Oscillator Design

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ABSTRACT

The low-power clock generator CDCE6214-Q1 incorporates a crystal-driver circuit that can drive an external crystal resonator (XTAL). Design procedures related to crystal input are explained in this article. Both the CDCE6214-Q1 and CDCI6214 devices share the same crystal driver circuit. This application report assumes an audience that has a basic understanding of crystal resonators and crystal oscillators.

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1 Introduction

The CDCE6214-Q1 device has selectable clock input paths to accommodate various reference clock options. One of the possible configurations supports an external crystal connection to form a crystal oscillator. Figure 1 shows a simplified circuit for crystal input. A crystal in series with R_S is connected to pin 1 and pin 2 of the CDCE6214-Q1 device, where R_S is a series resistor used to reduce drive level. C_{L1} and C_{L2} are two single-ended load capacitors used to control initial frequency accuracy of the crystal. One concept to help in the design of crystal oscillators is "negative resistance", or –R. Negative resistance is generated by the active circuit inside the chip and can effectively "cancel out" the positive resistance in order for the crystal to start and maintain oscillation.

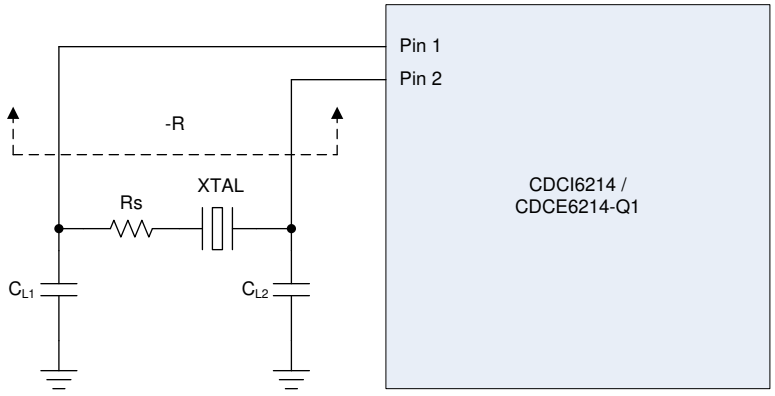

Figure 1. XTAL Input Schematic

The goals of crystal circuit design are:

1. Ensure that the crystal and external network meet the conditions of oscillation. This requires the –R to be large enough to provide sufficient power for the crystal to oscillate.
2. Do not overdrive the crystal. This requires the crystal power consumption to be kept to a level such that crystal is not overdriven. The consequences of overdriving a crystal are reduced lifetime, accelerated aging, and unwanted harmonics or spurs. R_S is used to reduce power dissipation when the drive level is too high. Crystal vendors typically specify the maximum drive level that should not be violated.
3. Minimize crystal frequency error. Crystal vendors typically require load capacitance (C_L) of a certain value to achieve frequency accuracy. If C_L is too low, the actual frequency will be higher than the target frequency, and vice versa.

Based on the previous discussion, to design a circuit for crystal input, a designer needs to decide the value of R_S as well as C_{L1} and C_{L2}. Further, the CDCE6214-Q1 and CDCI6214 devices provide controllable driver bias current and programmable internal load capacitance, which makes the design much easier once the user understands how it works. This is explained in detail in later sections.

2 Crystal Circuit Design Description

2.1 Negative Resistance and Oscillation Criteria

For a successful crystal circuit design, the first step is to make the crystal oscillate. This subsection explains the oscillation criteria of a crystal and how to design with sufficient margin. To start, a review of the concepts of ESR (Equivalent Series Resistance) and negative resistance is provided.

Figure 2 shows a crystal resonator can be modeled as an RLC circuit. An RLC circuit cannot start or maintain oscillation without an external supply because motional resistance (R_m) is lossy and dissipates power. Therefore, an active network is needed for a crystal to oscillate.

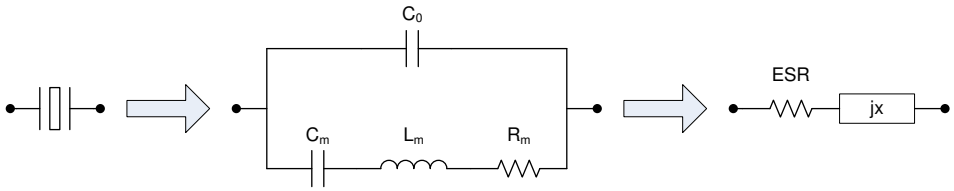

Figure 2. XTAL Equivalent Circuit

As mentioned in the introduction, a crystal driver provides an equivalent "negative resistance" (–R) to effectively eliminate the real part (ESR + R_S). Although *during* oscillation the total impedance is purely imaginary -- meaning that magnitude of –R is equal to ESR + R_S, for the XTAL to *start* oscillation, the magnitude of –R needs to be larger than that. Equation 1 shows a general rule for an oscillator to start oscillating:

$$\text{abs}(-R) = (3 \sim 5) \times (ESR + R_S) \quad (1)$$

Equation 1 means that the absolute value or magnitude of –R should be 3 to 5 times larger than the real part of crystal impedance + R_S. Three times of series loss is the minimum requirement for negative resistance. A factor of 5 is usually recommended for a good margin.

ESR can be estimated using Equation 2, where C_0 is shunt capacitance shown in Figure 2. If R_m or C_0 values are unavailable, simply use the max ESR specified in the crystal data sheet for a rough estimation.

$$ESR = R_m \left(1 + \frac{C_0}{C_L}\right)^2 \quad (2)$$

–R can be calculated using Equation 3, where ω is angular resonant frequency in rad/s. g_m values for CDCE6214-Q1 or CDCI6214 are provided in Table 1.

$$-R = -\frac{g_m}{(2\omega C_L)^2} \quad (3)$$

Notice how –R is related to resonant frequency and load capacitance. The higher the frequency and the larger the C_L, the smaller the magnitude of –R, meaning that there is typically less margin of negative resistance at high frequency and with large load capacitance and vice versa.

Table 1. g_m Table

R24 [5:2] of CDCE6214-Q1 or R26 [5:2] of CDCI6214	Bias Current (µA)	g_m (ms)(1)
0x0	0	NA
0x1	14	0.02
0x2	29	0.38
0x3	44	0.71
0x4	59	1.01
0x5	148	1.3
0x6	295	2.83
0x7	443	4.92
0x8	591	6.66
0x9	884	8.18
0xA	1177	10.7
0xB	1468	12.78
0xC	1758	14.53

(1) These g_m values are extracted based on 1.8-V mode (all VDD pins and VDDO pins are set to 1.8 V). The 3.3-V mode has slightly more margin, meaning that the g_m values at 3.3 V are slightly higher. So instead of choosing a factor of 5, use a factor of 3 or 4 instead.

Table 2 shows calculation results for –R using common resonant frequencies (25 MHz, 40 MHz and 50 MHz) and load capacitances (18 pF, 12 pF and 8 pF). For a successful design, ESR + R_S should be 3 to 5 times smaller than the values in Table 2.

Remember that the crystal driver starts to saturate when 1177 µA or higher bias current is chosen. Equation 3 should only be applied to bias current below 1177 µA. Avoid using 1468 µA and 1758 µA unless necessary, because with these bias current values, the magnitude of actual –R is lower than what is predicted using the equation. This is better demonstrated with bench measurement results in later sections.

Table 2. Calculated Negative Resistance

Bias Current (µA)	C_L = 18 pF			C_L = 12 pF			C_L = 8 pF		
	25 MHz	40 MHz	50 MHz	25 MHz	40 MHz	50 MHz	25 MHz	40 MHz	50 MHz
295[(1)]	89	35	22	199	78	50	448	175	112
443	154	60	39	347	135	87	780	305	195
591	208	81	52	469	183	117	1055	412	264
884	256	100	64	576	225	144	1296	506	324
1177	335	131	84	754	294	188	1696	662	424
1468	400	156	100	900	352	225	2025	791	506
1758	455	178	114	1023	400	256	2303	899	576

(1) Bias current below 295 µA is not recommended because phase noise performance with 148 µA or lower is inferior. In general, phase noise performance achieves optimum at and above 295 µA. It gets slightly better with an increase of bias current.

2.2 R_S, Bias Current, and Drive Level

According to Table 1 and Table 2, higher bias current provides larger g_m, and hence more negative resistance and more margin for maximum ESR. Then why not choose the maximum bias current? Because higher bias current also means higher drive level, and as mentioned earlier, if the drive level is too high, it will lead to reduced lifetime, accelerated aging, and unwanted harmonics and spurs. This section discusses how to control the drive level so that it is within the maximum drivel level specified in the crystal data sheet (typical 100 µW or 200 µW). First, review the concept of drive level and the effect of R_S.

Drive level (DL) is the amount of power dissipated in a crystal as calculated in Equation 4:

$$DL = I_{RMS}^2 ESR \quad (4)$$

where

- I_{RMS} is the RMS current flowing through the crystal

I_{RMS} can be measured using a current probe with crystal deadbugged or flywired. Calculate ESR using Equation 2. Max ESR in the data sheet is not acceptable for drive level calculation because it may lead to a much larger value than the actual one. A series resistor R_S can decrease the drive level because I_{RMS} is reduced while ESR is unchanged. However, equations cannot predict the relationship between R_S and I_{RMS} accurately. Most often, designers do trial and error before R_S can be finalized.

Fortunately, the crystal driver of the CDCE6214-Q1 device was designed in a way such that no R_S is needed. The programmable bias current makes sure that drive level can be controlled within an acceptable range. An example measurement was performed using a family of crystals with similar C_0 and R_m across frequency. Drive level vs bias current for 25-MHz and 50-MHz crystals are shown in Table 3 and Table 4.

Table 3. Drive Level vs Bias Current With 25-MHz Crystal

Bias Current (µA)	R_m (Ω)	C_0 (pF)	C_L (pF)	ESR (Ω)	3.3 V		1.8 V	
					I_{RMS} (mA)	Drive Level (µW)	I_{RMS} (mA)	Drive Level (µW)
295	12.6	1.3	8.0	17.0	1.9 (1)	59.2	1.8	52.6
443	12.6	1.3	8.0	17.0	2.3	91.2	1.9	64.7
591	12.6	1.3	8.0	17.0	2.7	122.2	2.2	84.6
884	12.6	1.3	8.0	17.0	2.9	144.6	2.7	126.1
1177	12.6	1.3	8.0	17.0	2.9	146.7	2.8	136.2
1468	12.6	1.3	8.0	17.0	2.8	136.2	2.8	136.2
1758	12.6	1.3	8.0	17.0	2.7	128.1	2.8	136.2

(1) Numbers in each column are rounded to one decimal place separately. Drive level is calculated based on original numbers.

Table 4. Drive Level vs Bias Current With 50-MHz Crystal

Bias Current (µA)	R_m (Ω)	C_0 (pF)	C_L (pF)	ESR (Ω)	3.3 V		1.8 V	
					I_{RMS} (mA)	Drive Level (µW)	I_{RMS} (mA)	Drive Level (µW)
295	13.4	1.3	8.0	18.1	1.1	20.8	0.4	3.3
443	13.4	1.3	8.0	18.1	1.4	37.3	1.1	22.5
591	13.4	1.3	8.0	18.1	1.9	67.3	1.3	29.9
884	13.4	1.3	8.0	18.1	2.4	108.1	1.5	39.6
1177	13.4	1.3	8.0	18.1	2.7	134.1	1.6	49.3
1468	13.4	1.3	8.0	18.1	2.8	147.1	1.8	60.1
1758	13.4	1.3	8.0	18.1	2.9	156.1	2.0	70.4

Since no external resistance is required, drive level should typically fall below 100 µW automatically, once a proper bias current is selected based on negative resistance calculation. Even if drive level is somehow higher than the crystal limit, it can be easily reduced by adjusting the programmable bias current, due to the flexibility of the CDCE6214-Q1 clock generator.

2.3 Load Capacitance

Crystal vendors require a specific load capacitance value for the resonator to oscillate with minimal frequency error. C_L is defined as equivalent capacitance seen by the crystal. As Figure 3 shows, C_L consists of three parts: external load capacitance (C_{L1} and C_{L2}), internal load capacitance (C_{int_L1} and C_{int_L2}), and stray capacitance (C_{stray}) that encompasses all kinds of pin and PCB parasitics.

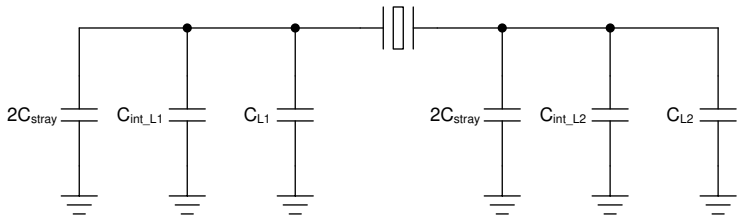

Figure 3. Load Capacitance Diagram

The equivalent capacitance seen by XTAL is the parallel equivalent of these three parts. Each part is the series equivalent of two single-ended capacitors. C_L can be calculated using:

$$C_L = \frac{C_{L1}C_{L2}}{C_{L1}+C_{L2}} + \frac{C_{int\_L1}C_{int\_L2}}{C_{int\_L1}+C_{int\_L2}} + C_{stray} \quad (5)$$

C_{int_L1} is equal to C_{int_L2}, and normally, C_{L1} and C_{L2} are also equal. Therefore, Equation 5 can be simplified to:

$$C_L = \frac{C_{L1}}{2} + \frac{C_{int\_L1}}{2} + C_{stray} \quad (6)$$

Programmable C_{int_L1} and C_{int_L2} are controlled by register IP_XO_CLOAD. Generally, it is recommended to first estimate the stray capacitance, calculate the sum of extra load capacitance needed, then target external load capacitance lower than the calculated value in case the stray capacitance is higher than estimated. If the load capacitance turns out to be lower than expected, then program the internal load capacitance to fine tune the value.

For example, if the required load capacitance is 12 pF and PCB stray capacitance is estimated to be 3 pF, then 9 pF of extra capacitance is needed. Set C_{L1} and C_{L2} to 8 pF and there is still 5-pF margin. Fine tune the internal load capacitance using register IP_XO_CLOAD to attain accurate frequency.

3 Bench Measurement Examples

In this section, Equation 1 and Equation 3 are verified with bench measurement results. To do so, measure the maximum series resistance with which the crystal can start oscillating, then add to that the ESR of the crystal. The result is the maximum acceptable ESR with zero margin.

Table 5. Measured Maximum ESR to Start Oscillation

Bias Current (µA)	Measured Maximum ESR (Ω)								
	C_L = 18 pF			C_L = 12 pF			C_L = 8 pF		
	25 MHz	40 MHz	50 MHz	25 MHz	40 MHz	50 MHz	25 MHz	40 MHz	50 MHz
295	45	NA(1)	NA(1)	85	45	23	215	75	40
443	65	27	17	135	55	35	335	120	65
591	85	30	19	165	85	43	415	145	90
884	105	33	21	255	100	53	515	185	100
1177	135	37	23	315	115	55	615	220	105
1468	135	41	25	315	120	56	615	225	115
1758	135	43	27	315	120	57	615	225	120

(1) Crystal does not oscillate.

Comparing Table 5 with Table 2, it is evident that the numbers predicted in Table 2 are quite accurate, and a margin factor of 4 or 5 is recommended considering process, voltage, and temperature variation.

Notice how maximum negative resistance stops increasing or increases slowly beyond 1177 µA because of crystal driver saturation.

4 Design Procedures Summary

1. Set R_S = 0. Based on information provided in Section 2.1, determine the required negative resistance value and find out the bias current that meets the general oscillation rules.
2. According to Section 2.3, set internal and external load capacitance.
3. After the board is built, send it to the crystal vendor to generate a test report. ESR, drive level as well as stray capacitance should be included in that report. Make sure that –R is approximately 3 to 5 times of the *measured* ESR and that the drive level is less than what is specified in the crystal data sheet. Adjust the bias current if necessary. Measure the output frequency on a frequency counter. Fine tune the frequency by adjusting the internal load capacitance. Increment frequency by reducing the load capacitance and decrement the frequency by increasing the load capacitance.

5 Conclusion

With external series resistance eliminated, CDCE6214-Q1 based crystal oscillator design is made predictable and requires less iterations. Fine adjustment can be quickly made due to the programmability of drive level and load capacitance.

6 References

1. Texas Instruments, *CDCE6214-Q1 Ultra-low power clock generator with 1 PLL, 4 differential outputs, 2 inputs, and internal EEPROM Product Folder*
2. Texas Instruments, *CDCE6214-Q1 Ultra-Low Power Clock Generator With One PLL, Four Differential Outputs, Two Inputs, and Internal EEPROM Data Sheet*
3. Texas Instruments, *CDCE6214-Q1 CDCE6214-Q1 Register Map User's Guide*
4. Texas Instruments, *CDCE6214-Q1 EVM User's Guide*

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