

LMK03318EVM

User's Guide



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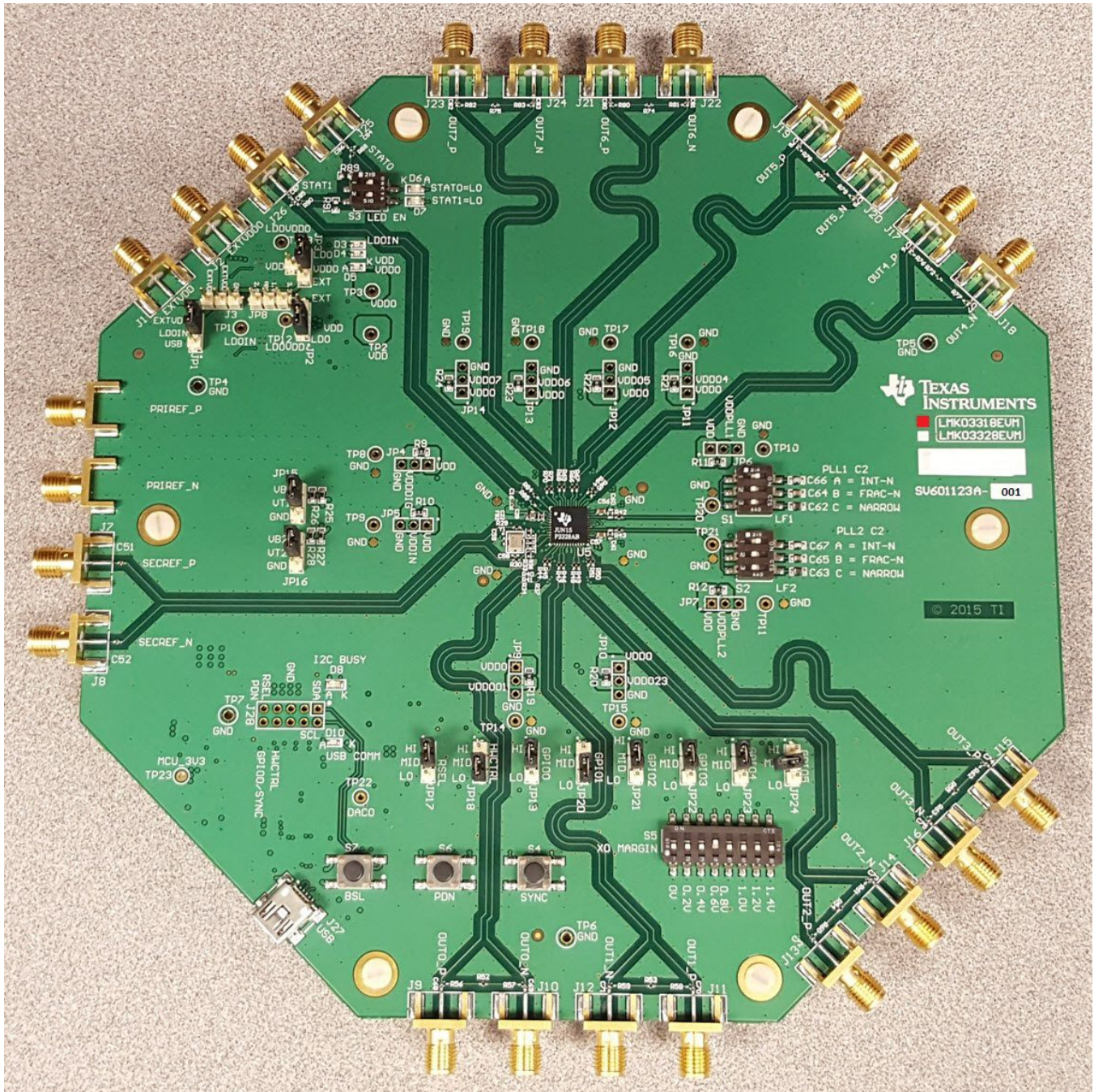


Figure 1. LMK03318EVM Photo

Table 1. Ordering Information

EVM ID	DEVICE ID	DEVICE PACKAGE
LMK03318EVM	LMK03318RHS	QFN-48

1 Overview

The LMK03318EVM evaluation module provides a complete clocking platform to evaluate the clock performance, pin-/software-configuration modes and features of the Texas Instruments LMK03318 Ultra-Low-Jitter Clock Generator with 1 PLL, 8 outputs, 2 inputs, and integrated EEPROM.

The LMK03318EVM can be used as a flexible, multi-output clock source for compliance testing, performance evaluation, and initial system prototyping. The onboard edge-launch SMA ports provide access to the LMK03318 clock inputs and outputs for interfacing to test equipment and reference boards using commercially available coaxial cables, adapters, or baluns (not included). This connectivity enables integrated system level testing between TI's LMK03318 and third-party FPGA/ASIC/SoC reference boards. A software graphical user interface (GUI) platform can be installed on a Host PC to access the LMK03318 device registers and EEPROM via the on-board USB-to-I2C interface. The GUI platform can also be used to export / import Register and EEPROM data files to facilitate factory or in-system programming of custom device configurations.

2 Features

- High performance, flexible clock generator with 6 independent output dividers for clocking multiple interface standards/protocols
- Outputs up to 8 pairs of Differential or 1.8-V LVCMOS clocks, or any combination of both
 - 100 Ω differential and 50 Ω single-ended output drivers
- Two selectable reference inputs
 - Differential / single-ended clock or crystal input (50 MHz crystal on-board)
 - Automatic or pin-controlled input selection mux to PLL
 - Either reference can be directly buffered on up to 4 output pairs (bypass PLL and output dividers)
- Flexible pin modes offer multiple start-up register configuration (jumper selectable)
 - Soft Pin Modes: 6 pre-programmed settings in EEPROM (100+ programming cycles)
 - Hard Pin Modes: 64 predefined settings in ROM
 - Register Default Mode
- Clock frequency margining
 - Up to ± 50 ppm adjustment of output frequencies via on-board pullable crystal
- Jumper-selectable power options using direct or on-board regulator supplies:
 - VDD = 3.3 V
 - VDDO = 1.8, 2.5, or 3.3 V
- GUI platform for full access to device registers and EEPROM
- On-board USB-to-I2C programming interface
- LEDs indicators: Loss of Reference and Lock Detection, and USB / I2C activity

3 Modes of Operation

The LMK03318 can be configured to start-up in one of three modes upon power-on/reset (POR). The mode of operation and associated control pins determine which on-chip memory type and memory page settings are used to initialize the active registers for configuring the Input, PLL, Output, Device Control, and Status blocks for full operation:

1. **Soft Pin Modes** (EVM Default) – Loads all registers with one of the 6 page settings stored in EEPROM. In the EVM-default EEPROM image, all 6 EEPROM pages have pre-programmed register settings to demonstrate the various clock configurations in Soft Pin Mode using the default EVM hardware. The EEPROM settings can be easily re-programmed by the user through the GUI platform.
2. **Hard Pin Modes** – Loads all registers from one of the 64 page settings stored in ROM. All 64 ROM pages are “hard-coded” with predefined register settings by TI.

NOTE: Refer to the ROM page configurations for Hard Pin Mode in the LMK03318 datasheet. Some ROM page settings may not operate with the default EVM configuration, and modification of the EVM may be necessary to operate the intended mode. EVM modification areas may include the crystal (Y1), PRIREF / SECREF input interfaces, OUT / STATUS output interfaces, and PLL loop filter C2 capacitor selection (switch S1).

3. **Register Default Mode** – Loads all registers from the register default setting. The Register Default Mode is hard-coded with predefined settings.

NOTE: Refer to the Register Default Mode in the LMK03318 datasheet. The Register Default Mode will NOT operate using the on-board 50 MHz crystal (Y1) as the device expects a 25 MHz reference input. To operate in Register Default Mode using a crystal input, Y1 must be changed to a 25-MHz, 9-pF crystal (example P/N: TXC 7M25072001).

Once the LMK03318 is start-up in any of these modes, the I2C interface is enabled to provide (optional) access to all device registers for full control of the LMK03318 settings. For convenience, a USB-to-I2C interface is integrated on-board and can be controlled by the GUI platform.

4 Configuring the EVM

The LMK03318 is a highly-configurable clock generator with multiple power domains and input & output clock domains. To support a wide range of evaluation use cases, the EVM was designed for maximum flexibility so it has more functionality and peripheral circuitry than needed to implement the clock solution in a typical customer system application.

This section describes the jumpers and connectors on the EVM, as well as how to connect, set-up, and use the LMK03318EVM. When operating the LMK03318EVM, the power supply, clock inputs, and clock outputs can be connected to the SMA ports shown in [Figure 2](#). These SMA ports are labeled in the top silkscreen layer.

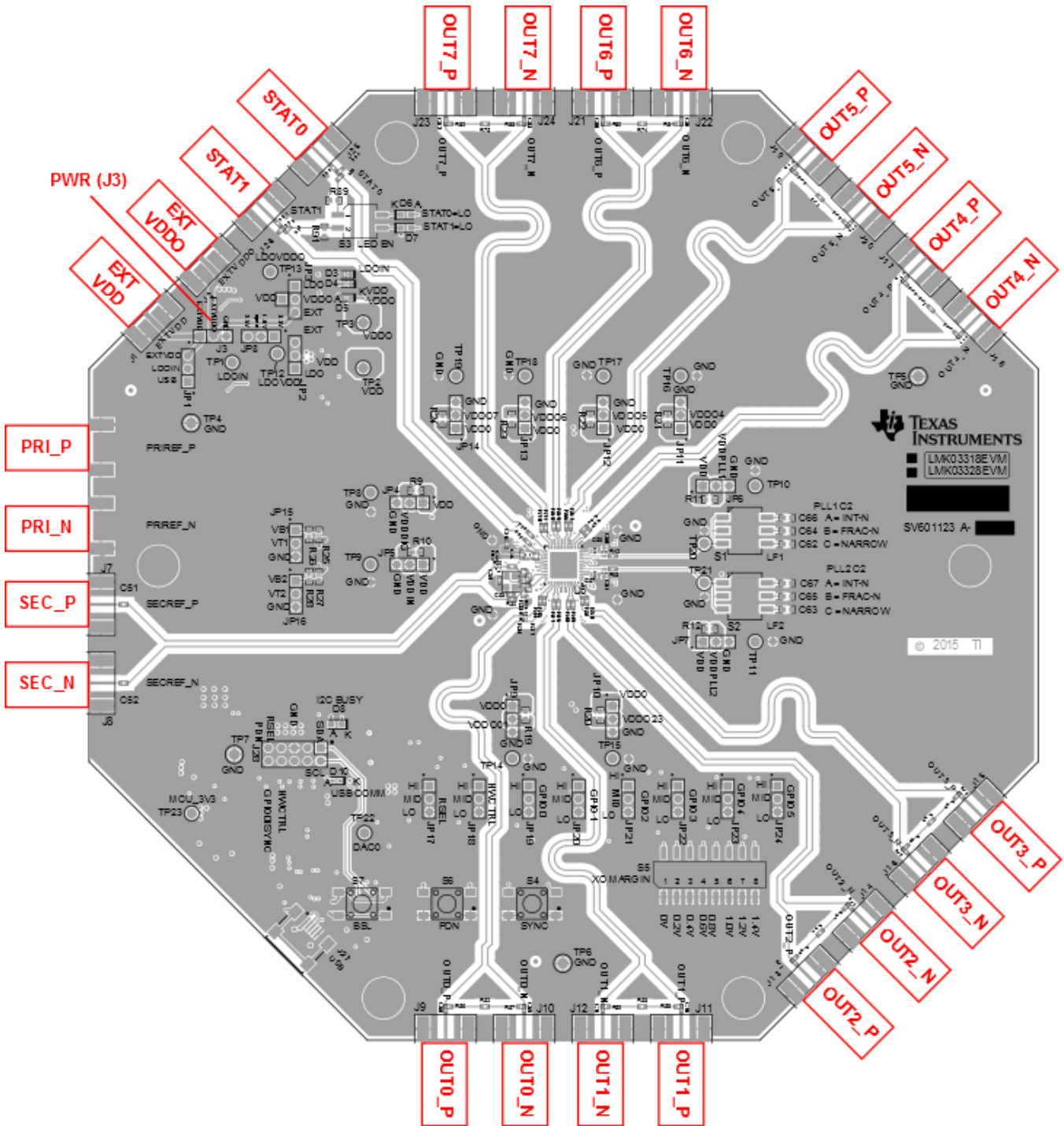


Figure 2. Power, Input, and Output Connections

4.1 Configuring the Power Supply

The LMK03318 has four VDD (analog/digital core) supply pins that operate from 3.3V (+/- 5%) and six VDDO (output) supply pins that operate from 1.8V to 3.3V (+/- 5%). The VDD and VDDO power planes on the EVM can be powered from a single supply (3.3 V) or dual supplies (3.3 V and 1.8/2.5/3.3 V). Each plane can be powered directly from an external supply or an on-board LDO regulator. Though the LMK03318 already has integrated LDO regulators for excellent power-supply-ripple-rejection (PSRR), the EVM's on-board regulators (U3 & U4) allows the user to power the EVM using a higher supply voltage (like 5 V) and enable jumper selection of the VDDO voltage. The direct external supplies or on-board regulator supplies can be independently routed for the VDD and VDDO planes by configuring the power terminals and jumpers shown in [Figure 3](#).

J3 (PWR) is the main power terminal block for the EVM for connecting power and GND leads from an external power supply. Power SMA ports EXT VDD (J1) and EXT VDDO (J3) provide an alternative connector style to apply power using coax cables.

NOTE: Some power connections may NOT be used or required to operate the EVM.

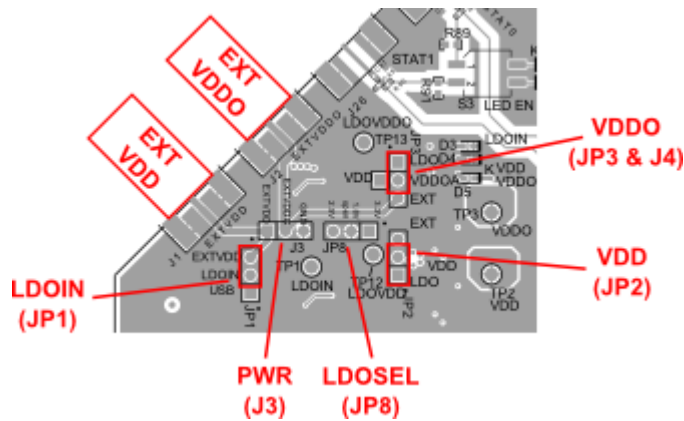


Figure 3. Power Terminals and Jumpers

Table 2 summarizes the EVM power configurations to connect and route power to the VDD and VDDO supply domains of the LMK03318. Refer to Section 7 for more details.

Table 2. Power Configurations

CONNECTION	NAME	On-board Regulators (Default)	Direct Single Supply	Direct Dual Supply
LMK03318 VDD pins	VDD[x]	3.3 V	3.3 V	3.3 V
LMK03318 VDDO pins	VDDO[x]	1.8 / 2.5 / 3.3 V	3.3 V	1.8 / 2.5 / 3.3 V
J1	EXTVDD	Alternative SMA power connection to J3 pins 1 & 3		
J2	EXTVDDO	Alternative SMA power connection to J3 pins 2 & 3		
J3	PWR	-Pin 1 (EXTVDD): Connect to 5-V supply -Pin 2: N/A -Pin 3 (GND): Connect to GND supply	-Pin 1 (EXTVDD): Connect to 3.3-V supply -Pin 2: N/A -Pin 3 (GND): Connect to GND supply	-Pin 1 (EXTVDD): Connect to 3.3-V supply -Pin 2 (EXTVDDO): Connect to 1.8 / 2.5 / 3.3 V supply -Pin 3 (GND): Connect to GND supply
JP1 ⁽¹⁾	LDOIN	Tie pins 2-3: Selects 5 V from EXTVDD to operate regulators	N/A	N/A
JP2	VDD	Tie pins 1-2: Selects VDD = 3.3 V from U3	Tie pins 2-3: Selects 3.3 V directly from EXTVDD	Tie pins 2-3: Selects 3.3 V directly from EXTVDD
JP3 & J4 ⁽²⁾	VDDO	Tie pins 1-2: Selects VDDO = 1.8 / 2.5 / 3.3 V from U4	Tie pins 2-4: Selects 3.3 V from VDD	Tie pins 2-3: Selects 1.8 / 2.5 / 3.3 V directly from EXTVDDO
JP8	LDOSEL (U4)	-Open (JP8 Default): Selects VDDO = 1.8 V -Tie pins 1-2: Selects VDDO = 3.3 V -Tie pins 2-3: Selects VDDO = 2.5 V	N/A	N/A

⁽¹⁾ In typical configurations, the LMK03318EVM can consume more current than USB 2.0 limit of 0.5 A. Thus, it is advised to not use the USB5V rail to power the on-board LDO regulators (i.e. do not tie pins 1-2 on JP1) unless the LMK03318 configuration and peripheral circuitry are assured to never exceed 0.5 A current limit imposed by the TPS2553 USB switch (U10). The LMK03318 may not initialize or operate properly when current limited.

⁽²⁾ JP3 and J4 form a 3-way header where J4 is pin 4.

4.2 Configuring the Control Pins

The LMK03318 has multiple external control pins to configure the operating mode and initial settings on POR (see Section 3). Depending on the selected mode, some control pins will change between 2-level, 3-level, or 8-level input scheme to increase the amount of control with a limited number of pins.

The LMK03318 control pins can be configured through the jumpers and switches shown in Figure 4.

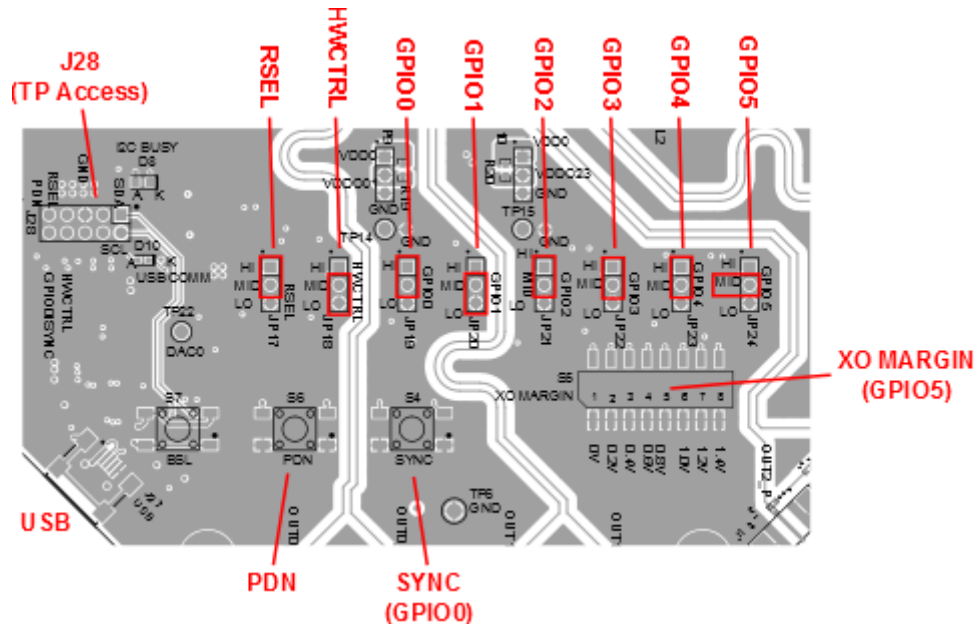


Figure 4. Control Pin Interfaces (Default Jumper Settings)

Jumpers JP17 through JP24 can be used to configure the corresponding control pin to either high or low state by strapping the center pin to “HI” position (tie pins 1-2) or “LO” position (tie pins 2-3), respectively.

Jumpers JP17, JP20, JP21, and JP22 can be used to configure the control pin with 3-level input scheme, where $V_{LO} < 0.4V$, $V_{MID} \sim 0.9V$, $V_{HI} > 1.4V$. Each of these 4 jumpers use a resistor divider network to bias the control pin to a mid-level state of 0.9 V, when the jumper is left open (“MID” position).

The LMK03318 control pins perform different functions depending on the mode of operation.

- For **Soft Pin Modes** or **Register Default Mode**, refer to Table 3 for jumper and switch descriptions.
- For **Hard Pin Modes**, refer to Table 4. Jumpers not listed in Table 4 have identical functions described in Table 3.

Table 3. Control Pin Interfaces for Soft Pin Mode or Register Default Mode (JP18 HWCTRL = LO)

COMPONENT	NAME (TYPE)	DESCRIPTION	
JP18	HWCTRL (2-level input)	Hardware / Software Control (HW_SW_CTRL) pin HWCTRL state is sampled on POR and determines the mode of operation.	
		HWCTRL STATE	OPERATING MODE
		LO (JP Default)	Soft Pin Mode or Register Default Mode GPIO[3:2] pins are also sampled on POR to determine the initial page setting loaded to registers (from EEPROM or default).
		HI	Hard Pin Mode GPIO[5:0] pins are also sampled on POR to determine the initial page setting loaded to registers (from ROM). See Table 4 : Control Pin Interfaces for Hard Pin Mode (JP18 HWCTRL = HI)
JP17	RSEL (3-level input)	Reference Select (REFSEL) pin for PLL Input Mux RSEL selects the PLL reference input when external "Pin Select" control is configured by the INSEL_PLL register bits (R50[1:0] = 01b).	
		RSEL STATE ⁽¹⁾	PLL REF INPUT
		LO	PRIREF
		MID	SECREF
		HI (JP Default)	Auto Select ⁽²⁾
⁽¹⁾ RSEL is ignored when INSEL_PLL bits ≠ 01b. ⁽²⁾ In Auto Select mode, PRIREF is prioritized over SECREF when a valid signal is detected by the on-chip reference detector logic. To use the SECREF input in Auto Select mode, the input signal to PRIREF must be made invalid (disabled or disqualified by the reference detector).			
JP19	GPIO0 (2-level input)	SYNC pin (active low) GPIO0 can be used to mute the output clocks (when asserted) and trigger output divider synchronization (when de-asserted) if synchronization is permitted by the SYNC_MUTE and PLL_SYNC_EN register bits.	
		GPIO0 STATE	SYNC OPERATION
		LO	Assert SYNC: Outputs muted, dividers in reset
		HI (JP Default)	Normal output operation
SYNC can also be asserted when switch S4 is pressed.			
JP20	GPIO1 (3-level input)	I2C Slave Address LSB Select pin GPIO1 is sampled on POR to configure the lower 2 bits of the 7-bit slave address. The upper 5 bits of the slave address are initialized from EEPROM (SLAVEADR[7:3] = 10100b). By configuring GPIO1, the composite slave address can be selected as follows:	
		GPIO1 STATE	7-BIT SLAVE ADDRESS (excludes W/R bit)
		LO (JP Default)	1010000b / 0x50
		MID	1010001b / 0x51
HI	1010011b / 0x53		

Table 3. Control Pin Interfaces for Soft Pin Mode or Register Default Mode (JP18 HWCTRL = LO) (continued)

COMPONENT	NAME (TYPE)	DESCRIPTION		
JP21 JP22	GPIO2 GPIO3 (3-level inputs)	Page Select pins for Soft Pin Mode or Register Default Mode With HWCTRL = LO, GPIO[3:2] pins are sampled on POR to select the EEPROM page or Register Default settings to initialize the registers as follows:		
		GPIO3 STATE	GPIO2 STATE	DEVICE MODE / PAGE SELECT ^{(1) (2)}
		LO	LO	Soft Pin Mode, EEPROM Page 0
		LO	MID	Soft Pin Mode, EEPROM Page 1
		LO	HI	Soft Pin Mode, EEPROM Page 2
		HI	LO	Soft Pin Mode, EEPROM Page 3
		HI	MID	Soft Pin Mode, EEPROM Page 4
		HI (JP Default)	HI (JP Default)	Soft Pin Mode, EEPROM Page 5
		MID	MID	Register Default Mode
⁽¹⁾ Refer to Table 6 for Soft Pin Mode configurations pre-programmed to the EEPROM for EVM demonstration purposes. ⁽²⁾ Register Default Mode will not operate using the on-board 50 MHz crystal (Y1) as the device expects a 25 MHz reference input. To use Register Default Mode with a crystal input, Y1 must be changed to a 25-MHz 9-pF crystal (example P/N: TXC 7M25072001).				
JP23	GPIO4 (2-level input)	XTAL Frequency Margining Enable pin GPIO4 can be used to enable XTAL frequency margining when permitted by the MARGIN_OPTION register setting (R86[3:2]) as follows:		
		GPIO4 STATE	XO MARGIN PIN CONTROL	
			MARGIN_OPTION=01b	MARGIN_OPTION=00b (Default)
		LO	XO Margining enabled. GPIO5 pin state selects XO Margining offset. ⁽¹⁾	XO Margining enabled. GPIO5 pin state selects XO Margining offset. ⁽¹⁾
HI (JP Default)		XO Margining disabled. GPIO5 pin is ignored. ⁽²⁾		
⁽¹⁾ See the description for JP24 (GPIO5) and switch S5 (XO MARGIN). ⁽²⁾ XOOFFSET_STEP4 register setting sets the nominal XTAL frequency offset when XO margining is disabled.				
JP24	GPIO5 (8-level input)	XTAL Frequency Margining Offset Select pin GPIO5 can be used to select the one of the 8 on-chip XTAL load capacitance settings on the crystal input (SECREf input) when XTAL frequency margining is enabled by the MARGIN_OPTION register and JP23 setting (GPIO4). The 8 load capacitance settings are programmable (via XOOFFSET_STEP# register bits) and initialized from the selected operating mode/page setting. The 8-level input state on GPIO5 can be configured by selecting one of the pull-down resistor values via switch S5 . By default, JP24 is left open, so switch S5 can be used to set the frequency margining offset. See the description for S5 (XO MARGIN).		
S4	SYNC	SYNC push-button switch When pressed, the GPIO0 pin is pulled low to assert SYNC and mute the outputs. When released, the GPIO pin is pulled high to trigger output synchronization and normal output operation.		

Table 3. Control Pin Interfaces for Soft Pin Mode or Register Default Mode (JP18 HWCTRL = LO) (continued)

COMPONENT	NAME (TYPE)	DESCRIPTION																																																						
S5	XO MARGIN (8-position SPST switch)	XTAL Frequency Margining Offset Resistor switch bank If the XTAL input is used as the PLL reference, the PLL and its output clocks will track the frequency offset of the XTAL. When JP24 is open and JP23 is low, switch S5 can be used to select one of the 8 pull-down resistors (R_{PD}) on GPIO5 which determines the corresponding XTAL load capacitance and frequency offset state (STEP1 to STEP8) as follows:																																																						
		<table border="1"> <thead> <tr> <th>S5 Position ON⁽¹⁾</th> <th>GPIO5 R_{PD}</th> <th>GPIO5 Voltage</th> <th>XOOFFSET_STEP# Register Control</th> <th>XOOFFSET_STEP# Setting (dec)⁽²⁾</th> <th>Nominal Frequency Offset⁽²⁾</th> </tr> </thead> <tbody> <tr> <td>Pos. 1</td> <td>0 Ω</td> <td>0.0 V</td> <td>STEP1</td> <td>227</td> <td>+50 ppm</td> </tr> <tr> <td>Pos. 2</td> <td>2.32 kΩ</td> <td>0.2 V</td> <td>STEP2</td> <td>306</td> <td>+25 ppm</td> </tr> <tr> <td>Pos. 3</td> <td>5.62 kΩ</td> <td>0.4 V</td> <td>STEP3</td> <td>345</td> <td>+15 ppm</td> </tr> <tr> <td>Pos. 4 (Default)</td> <td>10.5 kΩ</td> <td>0.6 V</td> <td>STEP4</td> <td>412</td> <td>0 ppm</td> </tr> <tr> <td>Pos. 5</td> <td>18.7 kΩ</td> <td>0.8 V</td> <td>STEP5</td> <td>494</td> <td>-15 ppm</td> </tr> <tr> <td>Pos. 6</td> <td>34.8 kΩ</td> <td>1.0 V</td> <td>STEP6</td> <td>558</td> <td>-25 ppm</td> </tr> <tr> <td>Pos. 7</td> <td>84.5 kΩ</td> <td>1.2 V</td> <td>STEP7</td> <td>676</td> <td>-40 ppm</td> </tr> <tr> <td>Pos. 8</td> <td>open</td> <td>1.4 V</td> <td>STEP8</td> <td>778</td> <td>-50 ppm</td> </tr> </tbody> </table>	S5 Position ON ⁽¹⁾	GPIO5 R_{PD}	GPIO5 Voltage	XOOFFSET_STEP# Register Control	XOOFFSET_STEP# Setting (dec) ⁽²⁾	Nominal Frequency Offset ⁽²⁾	Pos. 1	0 Ω	0.0 V	STEP1	227	+50 ppm	Pos. 2	2.32 k Ω	0.2 V	STEP2	306	+25 ppm	Pos. 3	5.62 k Ω	0.4 V	STEP3	345	+15 ppm	Pos. 4 (Default)	10.5 k Ω	0.6 V	STEP4	412	0 ppm	Pos. 5	18.7 k Ω	0.8 V	STEP5	494	-15 ppm	Pos. 6	34.8 k Ω	1.0 V	STEP6	558	-25 ppm	Pos. 7	84.5 k Ω	1.2 V	STEP7	676	-40 ppm	Pos. 8	open	1.4 V	STEP8	778	-50 ppm
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⁽¹⁾ Only one position should be ON at a time (all others are OFF). ⁽²⁾ Applies only to Soft Pin Mode using the EVM's default EEPROM settings optimized for a 9-pF crystal. For Register Default Mode, refer to the datasheet for the default XOOFFSET_STEP# register settings.																																																								
S6	PDN (2-level input)	PDN push-button switch When pressed, the device PDN pin (active low) is pulled down to power-down the device. When released, the PDN pin is pulled high to trigger the POR sequence, initialize the registers per the selected operating mode, and begin normal operation.																																																						
		<table border="1"> <thead> <tr> <th>PDN STATE</th> <th>DEVICE OPERATION</th> </tr> </thead> <tbody> <tr> <td>LO (Pushed)</td> <td>Power-down mode (I2C interface disabled)</td> </tr> <tr> <td>HI (Released)</td> <td>Normal operation</td> </tr> </tbody> </table>	PDN STATE	DEVICE OPERATION	LO (Pushed)	Power-down mode (I2C interface disabled)	HI (Released)	Normal operation																																																
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J27	USB	USB port (Mini-B type) Using the GUI platform, USB controller (U8) provides the USB-to-I2C interface to manage the LMK03318 device registers and EEPROM. LED D10 (USB COMM) should be lit green once USB communication is established with the GUI running on the Host PC. By default, the USB port powers the LDO regulator U9 to supply 3.3 V power for the MCU and its peripheral circuitry.																																																						
J28 (not populated)	U2A	Test Point Access to I2C and Device Control pins SDA and SCL lines are connected to 1.5 k Ω pull-up resistors. LED D8 (I2C BUSY) will blink yellow during I2C communication.																																																						
		Pin 1: SDA	Pin 2: SCL																																																					
		Pin 4: Not connected	Pin 3: Not connected																																																					
		Pin 5: GND	Pin 6: Not connected																																																					
		Pin 7: REFSEL	Pin 8: HW_SW_CTRL																																																					
	Pin 9: PDN	Pin 10: GPIO0																																																						

Table 4. Control Pin Interfaces for Hard Pin Mode (JP18 HWCTRL = HI)⁽¹⁾⁽²⁾

COMPONENT	NAME (TYPE)	DESCRIPTION	
JP19 JP20 JP21 JP22 JP23 JP24	GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 (2-level inputs)	Page Select pins for Hard Pin Mode GPIO[5:0] pins are sampled on POR and select the ROM page settings to initialize the registers as follows:	
		GPIO[5:0] STATES⁽³⁾	DEVICE MODE / PAGE SELECT
		000000	Hard Pin Mode, ROM Page 0
		000001	Hard Pin Mode, ROM Page 1
		000010	Hard Pin Mode, ROM Page 2
		000011	Hard Pin Mode, ROM Page 3
		000100	Hard Pin Mode, ROM Page 4
	
		111101	Hard Pin Mode, ROM Page 61
		111101	Hard Pin Mode, ROM Page 61
		111110	Hard Pin Mode, ROM Page 62
		111111	Hard Pin Mode, ROM Page 63
S4	SYNC	Not used for Hard Pin Mode.	
S5	XO MARGIN	Not used for Hard Pin Mode. Set all switch position to OFF.	

⁽¹⁾ Jumpers not listed in Table 4 are identical to functions described in Table 3.

⁽²⁾ Refer to the ROM page configurations for Hard Pin Mode in the LMK03318 datasheet. These settings may not operate with the default EVM configuration, and modification of the EVM hardware may be required to operate the intended Hard Pin Mode configuration. EVM modification areas may include the crystal (Y1), PRIREF / SECREF input interfaces, OUT / STATUS output interfaces, and PLL loop filter C2 capacitor selection (switch S1).

⁽³⁾ GPIO[5:0] values are BCD representation of the ROM Page value.

4.3 Configuring the PLL Loop Filter

The LMK03318 has configurable PLL loop bandwidth with most loop filter components integrated on-chip (C1, R2, C3, and R3). Only one loop filter capacitor, C2, needs to be connected externally to LF (pin 34) for PLL.

The LF pin is connected to the 3-position SPST switch (S1) to allow easy selection between one of the three C2 values listed in Table 5. The C2 values were chosen to work well for different PLL modes / loop bandwidths (BW).

Table 5. PLL Loop Filter C2 Selection

COMPONENT	NAME	DESCRIPTION		
S1	LF1	PLL Loop Filter C2 Capacitor Select Only one position should be ON at a time (all others are OFF).		
		S1 Position ON	C2 Value	Intended PLL Mode (Loop BW)
		Pos. A	3300 pF	Integer-N (Wide BW, >100 kHz)
		Pos. B	0.033 uF	Fractional-N (Med BW, <100 kHz)
	Pos. C	22 uF	Jitter Cleaner (Narrow BW, <1 kHz)	

4.4 Configuring the Reference Inputs

The LMK03318 has two reference input pairs, PRIREF and SECREF, which can be configured to accept single-ended clock input, differential clock input, or crystal input (SECREF only). The input SMAs labeled PRI_P and PRI_N are routed to the PRIREF inputs, and SMAs labeled SEC_P and SEC_N are routed to the SECREF inputs. Both SMA input pairs are routed using 50-ohm single-ended traces to the input pins of the chip.

The PRI_P and PRI_N input SMAs are DC-coupled on the EVM and have no on-board terminations at the PRIREF input pins (high impedance inputs). By default, a LVCMOS clock input with 1.5V to 3.3V levels can be connected to the PRI_P input for DC-coupling to the PRIREF_P input (assumes the LVCMOS driver is source-terminated). The unused complementary input (PRIREF_N) can be tied to GND. If a differential clock source is required, LMK03318 supports programmable 50 ohm input termination and common-mode biasing options (through 200 kohm internal bias resistors) for either DC- or AC-coupled inputs.

The SECREF input pins of the LMK03318 can accept a fundamental-mode crystal for the internal crystal oscillator circuit. By default, R40 and R41 are installed to enable the onboard 50-MHz crystal (Y1), which can be selected as the PLL reference input when using the Soft Pin Mode configurations listed in [Table 6](#). If a different crystal is required for the intended configuration (e.g. Register Default or Hard Pin mode configurations), remove the original crystal on Y1 and install the new part. The new part should comply with the recommended crystal characteristics specified in the LMK03318 datasheet. If using a crystal with high load capacitance spec (e.g. 18 pF), external trim capacitors may be installed on C58 and C59 to supplement the on-chip load capacitance.

The SECREF_P and SECREF_N input SMAs are AC-coupled on the EVM and have 100-ohm center-tapped differential termination near the inputs. The input common-mode voltage is biased to 1.2 V when tying pins 1-2 on JP16. If using a differential clock input to SEC_P and SEC_N, remove R40 and R41 to disconnect the crystal input path and install 0 ohms on R36 and R37. If using a LVCMOS clock input with 1.5V to 2.5V levels to SEC_P, remove R40 and R41 to disconnect the crystal path, install 0 ohms on C51 and C52, and remove R33 and R34 to provide a DC-coupled, high-impedance path to the SECREF_P input (assumes the LVCMOS driver is source-terminated). The unused complementary input (SECREF_N) can be tied to GND. If using a 3.3-V LVCMOS clock input to SECREF_P, a voltage divider network is required, like shown in [Figure 5](#), to comply with the maximum single-ended input swing of 2.6 V. The resistive divider can be installed on R29 and R33 with the shunt resistor connected to GND by tying pins 2-3 of JP16.

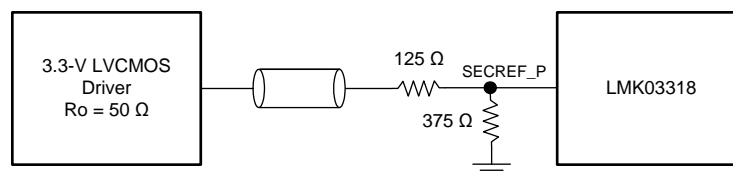


Figure 5. Interfacing a 3.3-V LVCMOS Clock Input to SECREF_P

4.5 Configuring the Clock Outputs

All eight clock output pairs of LMK03318 are routed via 50-ohm single-ended traces to SMA ports (OUT[7:0]_P/_N) through AC coupling capacitors. These outputs have series resistor (0- Ω populated) options. Each output pair supports AC-coupled Differential output levels with 400 mV (LVDS-like), 600 mV (CML-like), and 800 mV (LVPECL-like) single-ended swing, HCSL output levels (programmable 50- Ω on-chip termination), and 1.8-V LVCMOS output levels. Each channel divider output bank has its own VDDO output supply pin that operates from 1.8 V to 3.3 V. The on-chip LDOs provide regulated power to the output channel and provide excellent PSRR. The LVCMOS output is limited to an output high level of 1.8 V even with VDDO of 2.5 V or 3.3 V, since the LDOs step-down the output driver supply to 1.8 V internally.

4.6 Configuring the Status Outputs

The STATUS0 and STATUS1 outputs of LMK03318 are configured as 3.3-V LVCMOS by default and are routed via 50-ohm single-ended traces to SMA ports (STAT0 and STAT1) through AC coupling capacitors. The status pins can also be connected to yellow LEDs (D6 and D7) through switch S3 (2 positions) to enable or disable visual indication of the status output states. When the switch position is ON, the LED will be lit when the STATUS output state is logic low.

4.7 Using the USB Interface Connection

The on-board MSP430F5529 USB microcontroller (U8) provides an I2C host interface to the LMK03318 slave device. The device registers can be controlled via USB using the GUI platform running on a Host PC.

5 EVM Quick Start Guide

The following guide allows the user to quickly configure the LMK03318 to evaluate any of the pre-programmed Soft Pin Mode configurations.

1. Confirm the EVM Default power configuration is set per [Table 2](#) / [Figure 3](#) to power the LMK03318 using the on-board LDO regulators with VDD = 3.3 V and VDDO = 1.8 V.
2. Connect the 5-V lead to EXTVDD (J3, pin 1) and ground lead to GND (J3, pin 3) from a 1A-capable power supply, and enable the 5-V output.
3. Set the Control Pin jumpers to select the desired Soft Pin Mode configuration in [Table 6](#).
4. To use the on-board XTAL on SECFREF as the reference input to the PLLs, set JP17 = HI and do not connect any input clock to PRIREF SMAs.
5. Toggle the PDN push-button switch to restart the device in the selected mode.
6. Observe any active output clock on OUT[7:0] SMA ports or STAT[1:0] SMA ports.
 - (a) All clock and status outputs are AC-coupled to the SMAs.
 - (b) Use 50-ohm coax cables to connect the test equipment to the output SMA ports. If making a single-ended measurement on a differential output, terminate the unused SMA port with a 50-ohm load.
 - (c) To minimize output clock switching noise from affecting jitter-sensitive measurements, terminate any unused active output clock pair using 50-ohm SMA loads or connecting the 100-ohm differential load resistors (R52 to R55, R72 to R75); otherwise, power-down unused output clocks via register programming.
 - (d) Status LEDs, D6 & D7 (active low), can also be monitored for activity on STATUS pins when switch S3 is in the "ON" position.
7. Refer to the Soft Pin Mode Control Interfaces descriptions in [Table 3](#) for configuration of PLL reference input selection (JP17), output SYNC (switch S4), and XTAL frequency margining (JP23, JP24, and switch S5) features.

Table 6. Soft Pin Mode - EEPROM Page Configurations (Default EVM EEPROM Image)

EEPROM Page	Page 0	Page 1	Page 2	Page 3	Page 4	Page 5
HWCTRL (JP18) Jumper Setting	LO	LO	LO	LO	LO	LO
GPIO3 (JP22) Jumper Setting	LO	LO	LO	HI	HI	HI
GPIO2 (JP21) Jumper Setting	LO	MID	HI	LO	MID	HI
PRIREF Input	50 MHz LVCMOS	50 MHz LVCMOS	50 MHz LVCMOS	50 MHz LVCMOS	50 MHz LVCMOS	50 MHz LVCMOS
SECREF Input	50 MHz XTAL on-board	50 MHz XTAL on-board	50 MHz XTAL on-board	50 MHz XTAL on-board	50 MHz XTAL on-board	50 MHz XTAL on-board
PLL Input Mux	Pin Control ⁽¹⁾	Pin Control ⁽¹⁾	Pin Control ⁽¹⁾	Pin Control ⁽¹⁾	Pin Control ⁽¹⁾	Pin Control ⁽¹⁾
PLL Configuration	Fractional mode PFD = 100 MHz VCO = 5.15625 GHz	Integer mode PFD = 100 MHz VCO = 5 GHz	Integer mode PFD = 100 MHz VCO = 5 GHz	Integer mode PFD = 100 MHz VCO = 5 GHz	Integer mode PFD = 100 MHz VCO = 5.1 GHz	Integer mode PFD = 100 MHz VCO = 5.0 GHz
C2 Value (S1 Position ON)	0.033 uF (Pos. B)	3300 pF (Pos. A)	3300 pF (Pos. A)	3300 pF (Pos. A)	3300 pF (Pos. A)	3300 pF (Pos. A)
OUT0	161.1328125 MHz LVPECL	156.25 MHz LVPECL	156.25 MHz LVPECL	156.25 MHz LVPECL	100 MHz HCSL (50Ω on-chip)	156.25 MHz LVPECL
OUT1	161.1328125 MHz LVPECL	156.25 MHz LVPECL	156.25 MHz LVPECL	156.25 MHz LVPECL	100 MHz HCSL (50Ω on-chip)	156.25 MHz LVPECL
OUT2	161.1328125 MHz LVPECL	156.25 MHz LVPECL	125 MHz LVPECL	156.25 MHz LVPECL	100 MHz HCSL (50Ω on-chip)	125 MHz LVPECL
OUT3	161.1328125 MHz LVPECL	156.25 MHz LVPECL	125 MHz LVPECL	156.25 MHz LVPECL	100 MHz HCSL (50Ω on-chip)	125 MHz LVPECL
OUT4	161.1328125 MHz LVPECL	156.25 MHz LVPECL	125 MHz LVPECL	25 MHz LVPECL	100 MHz LVPECL	100 MHz LVPECL
OUT5	161.1328125 MHz LVPECL	125 MHz LVPECL	125 MHz LVPECL	25 MHz LVPECL	100 MHz LVPECL	100 MHz LVPECL
OUT6	161.1328125 MHz LVPECL	125 MHz LVPECL	125 MHz LVPECL	25 MHz LVPECL	100 MHz LVPECL	25 MHz LVPECL
OUT7	161.1328125 MHz LVPECL	125 MHz LVPECL	125 MHz LVPECL	25 MHz LVPECL	100 MHz LVCMOS(+/-) 1.8V	25 MHz LVPECL
STATUS0	PRIREF loss of signal (active low)	25 MHz LVCMOS 3.3V (active high)	25 MHz LVCMOS 3.3V (active high)	PLL loss of lock (active low)	PLL loss of lock (active low)	PLL loss of lock (active low)
STATUS1	PLL loss of lock (active low)	25 MHz LVCMOS 3.3V (active low)	25 MHz LVCMOS 3.3V (active low)	PRIREF loss of signal (active low)	PRIREF loss of signal (active low)	PRIREF loss of signal (active low)

6 EVM Layout

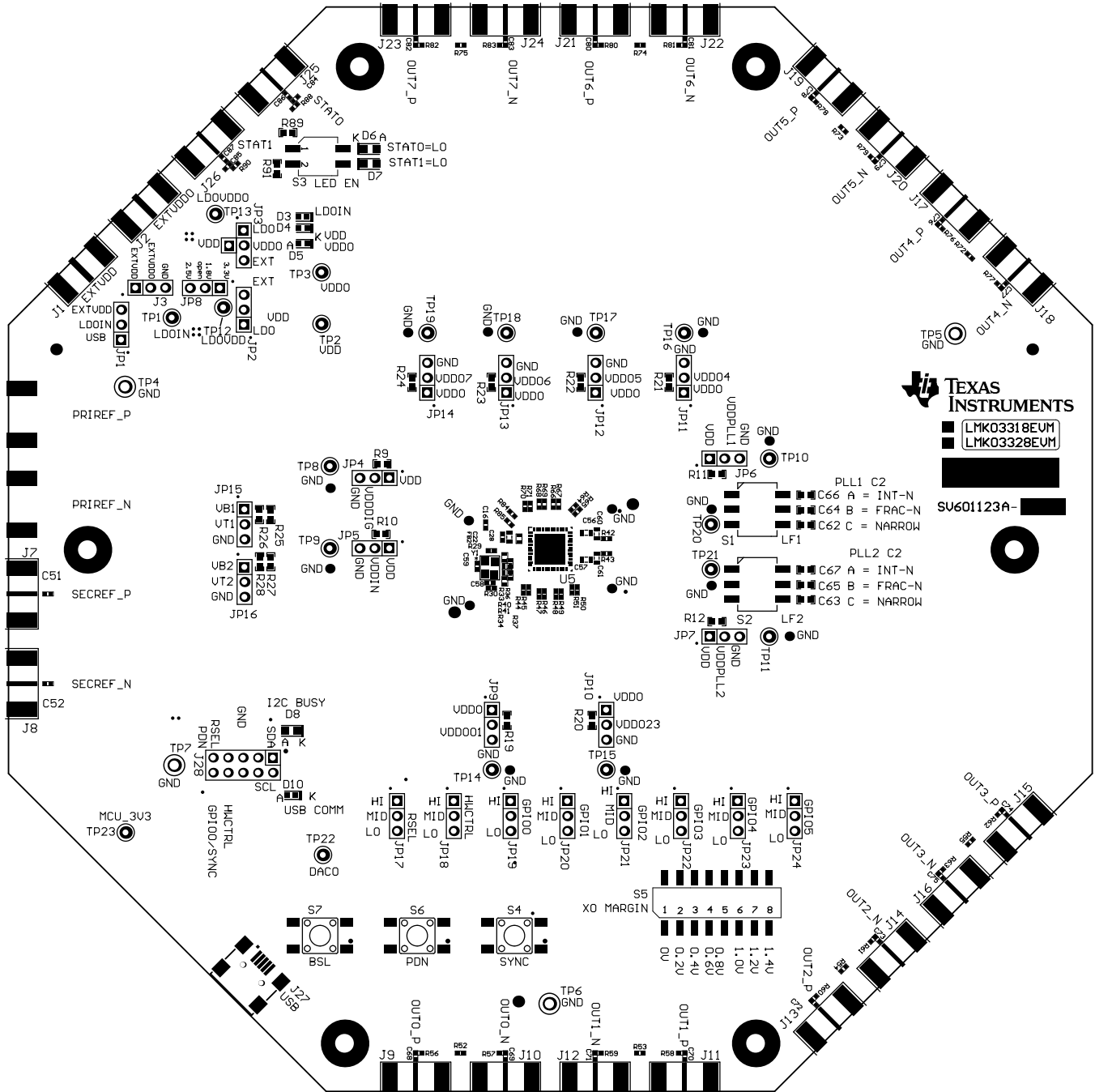


Figure 6. Top Overlay

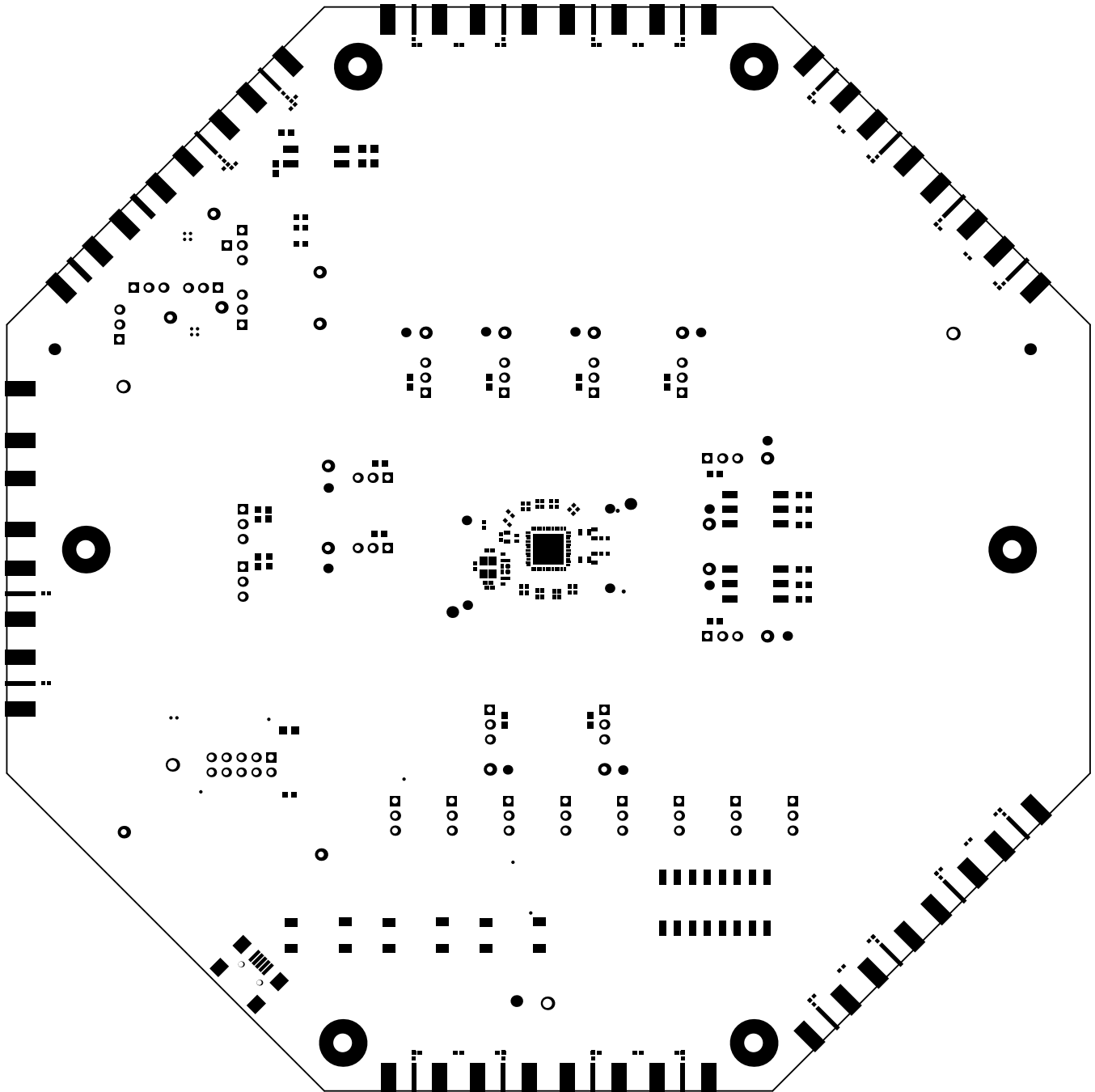


Figure 7. Top Solder Mask

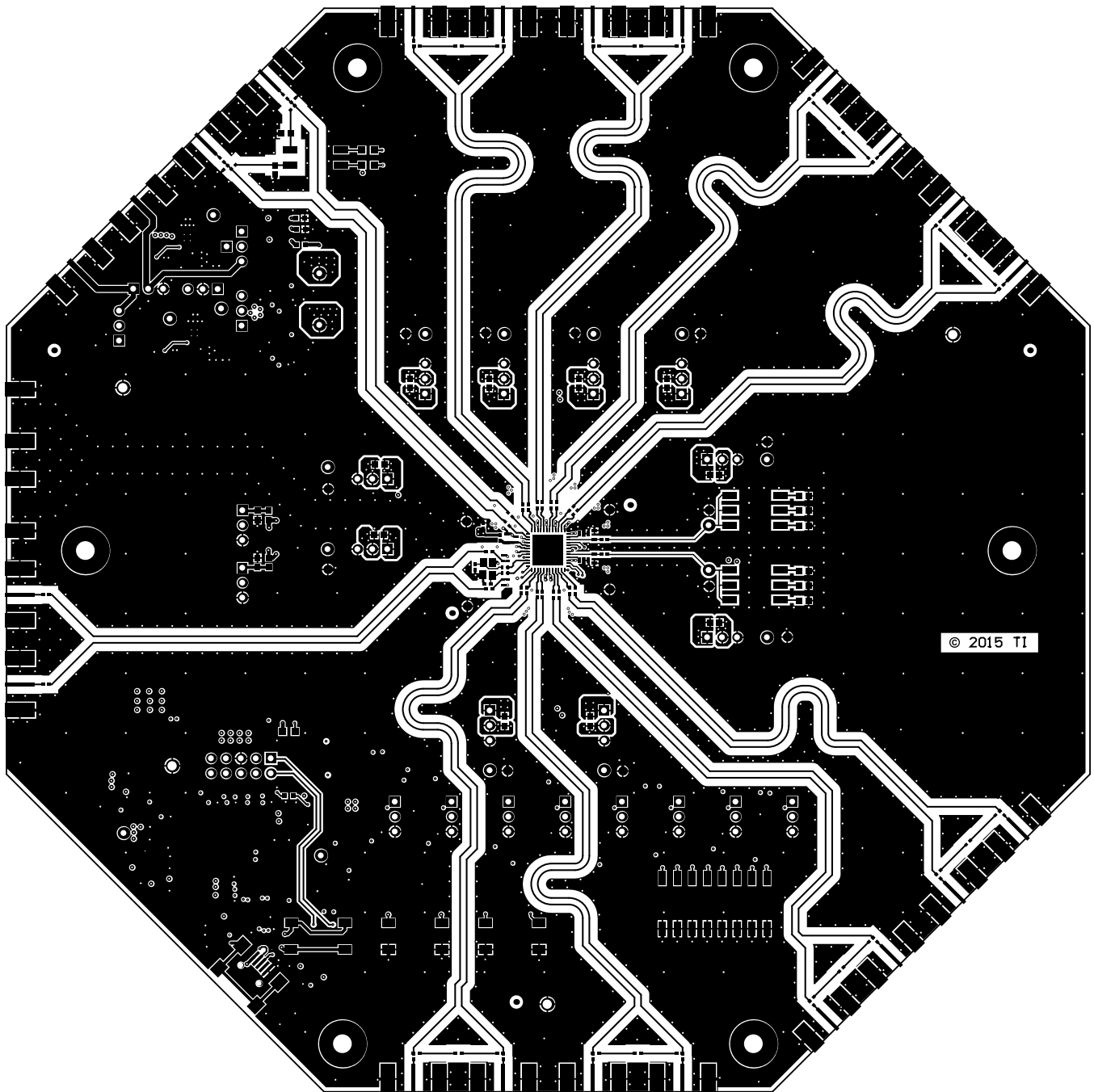


Figure 8. Layer 1 (Top Side)

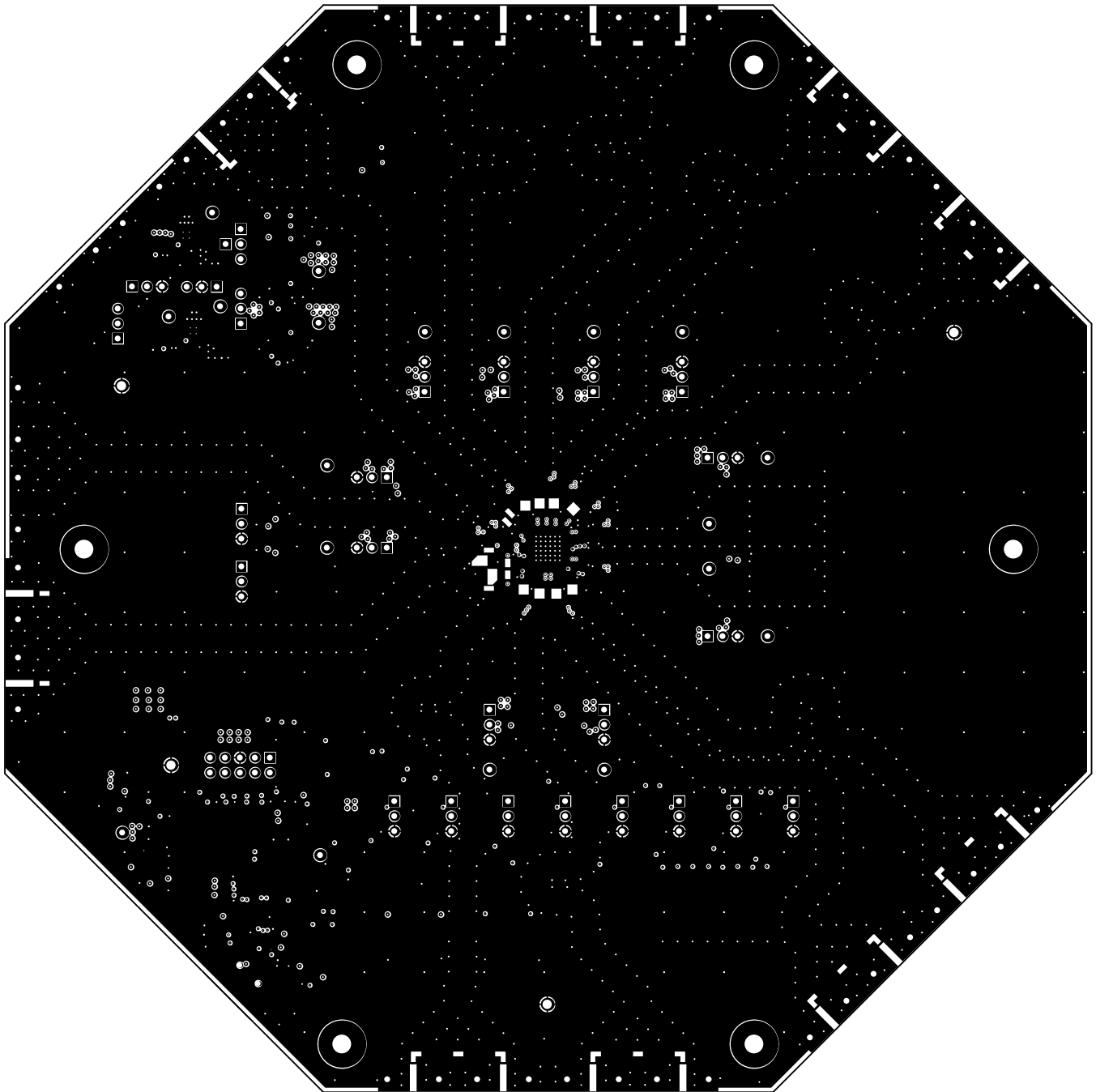


Figure 9. Layer 2

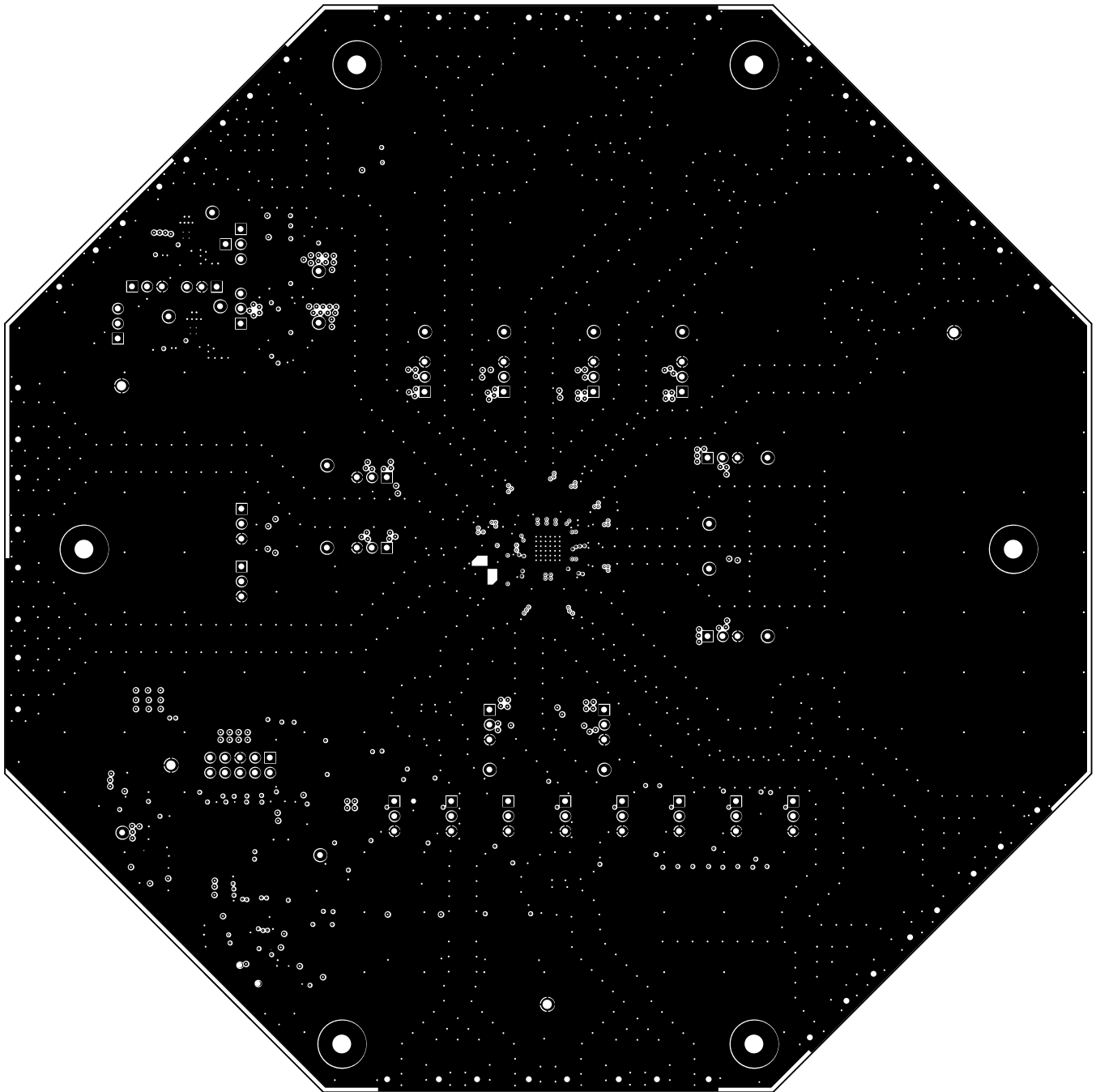


Figure 10. Layer 3

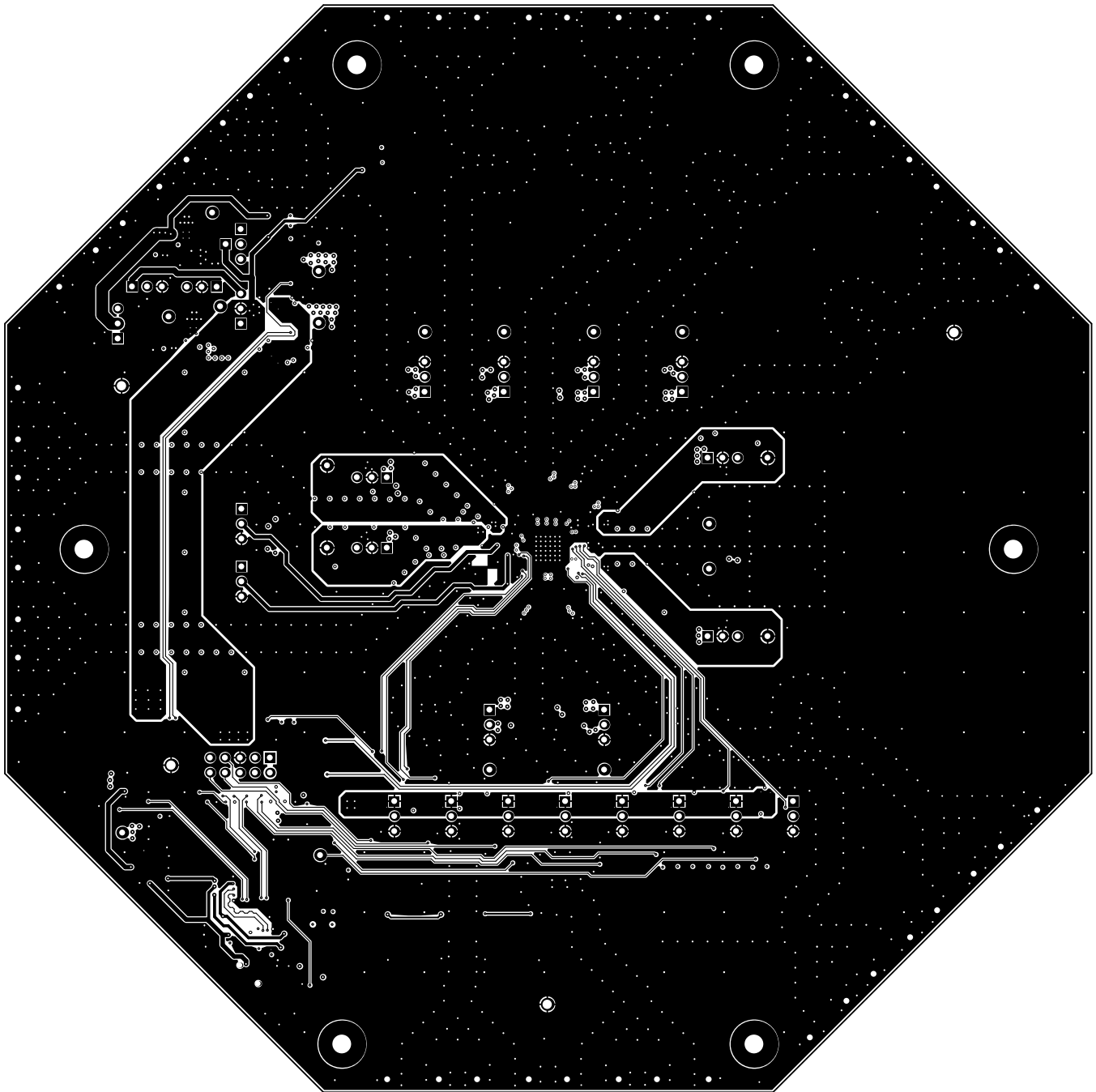


Figure 11. Layer 4

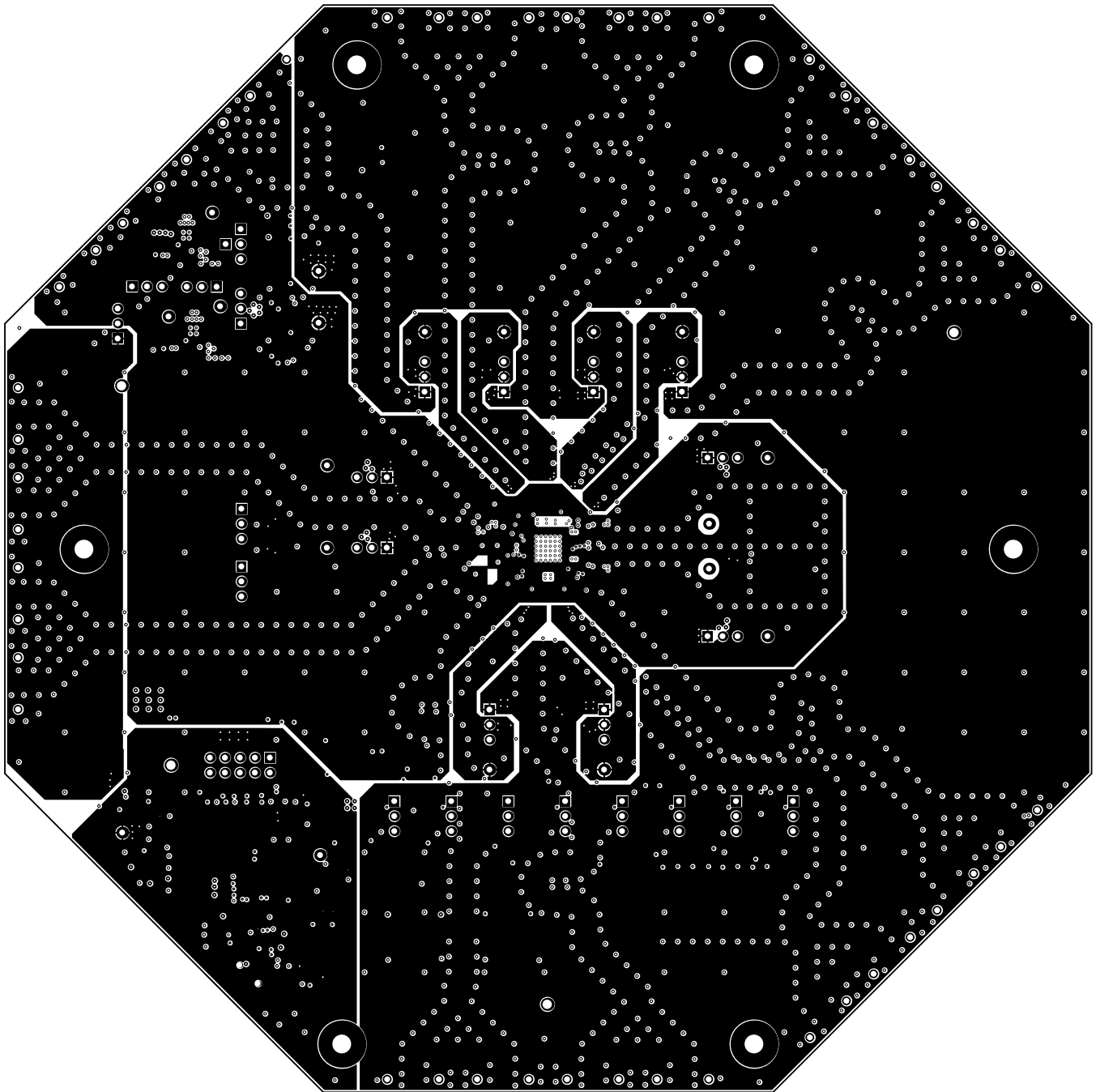


Figure 12. Layer 5

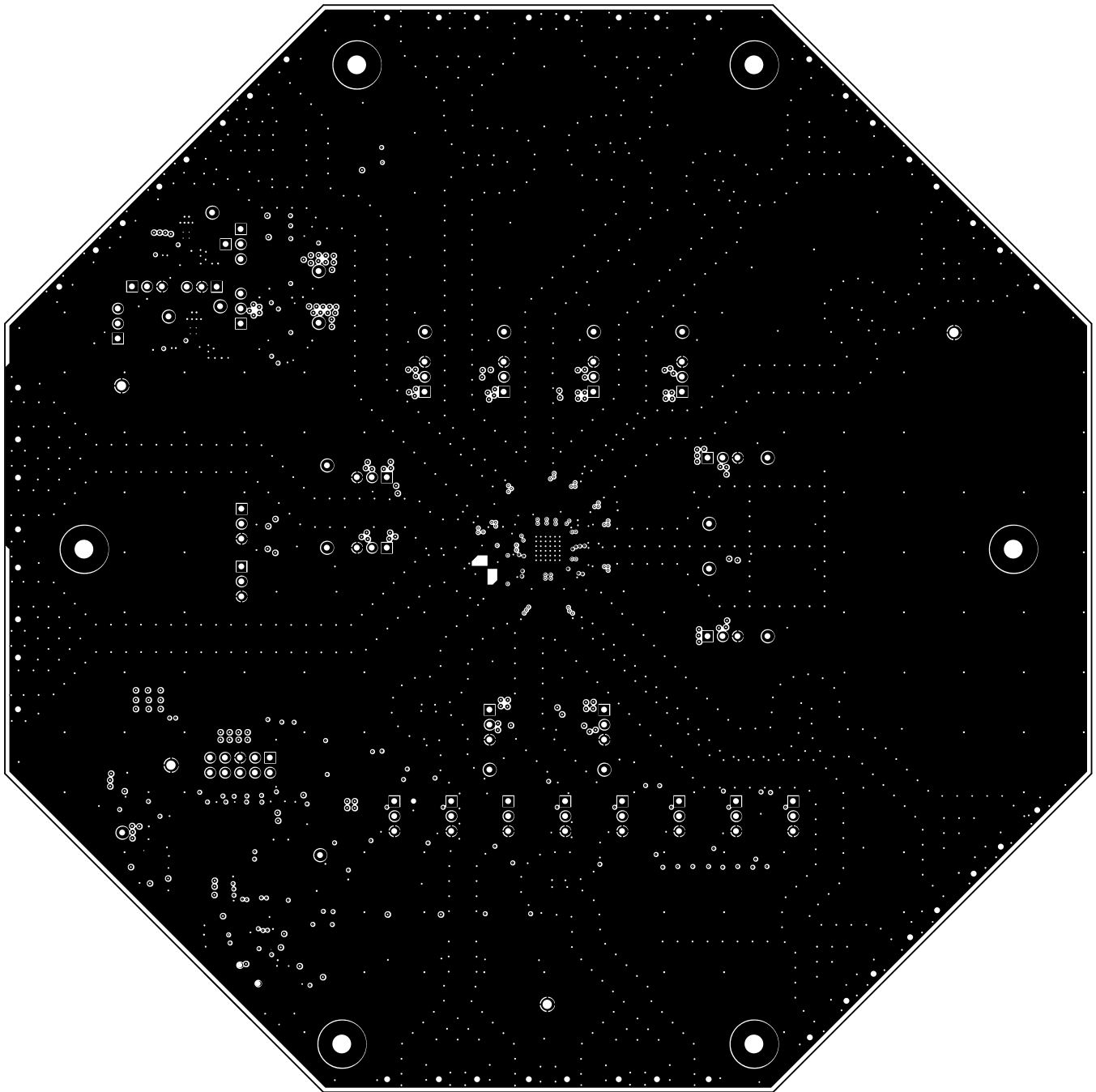


Figure 13. Layer 6

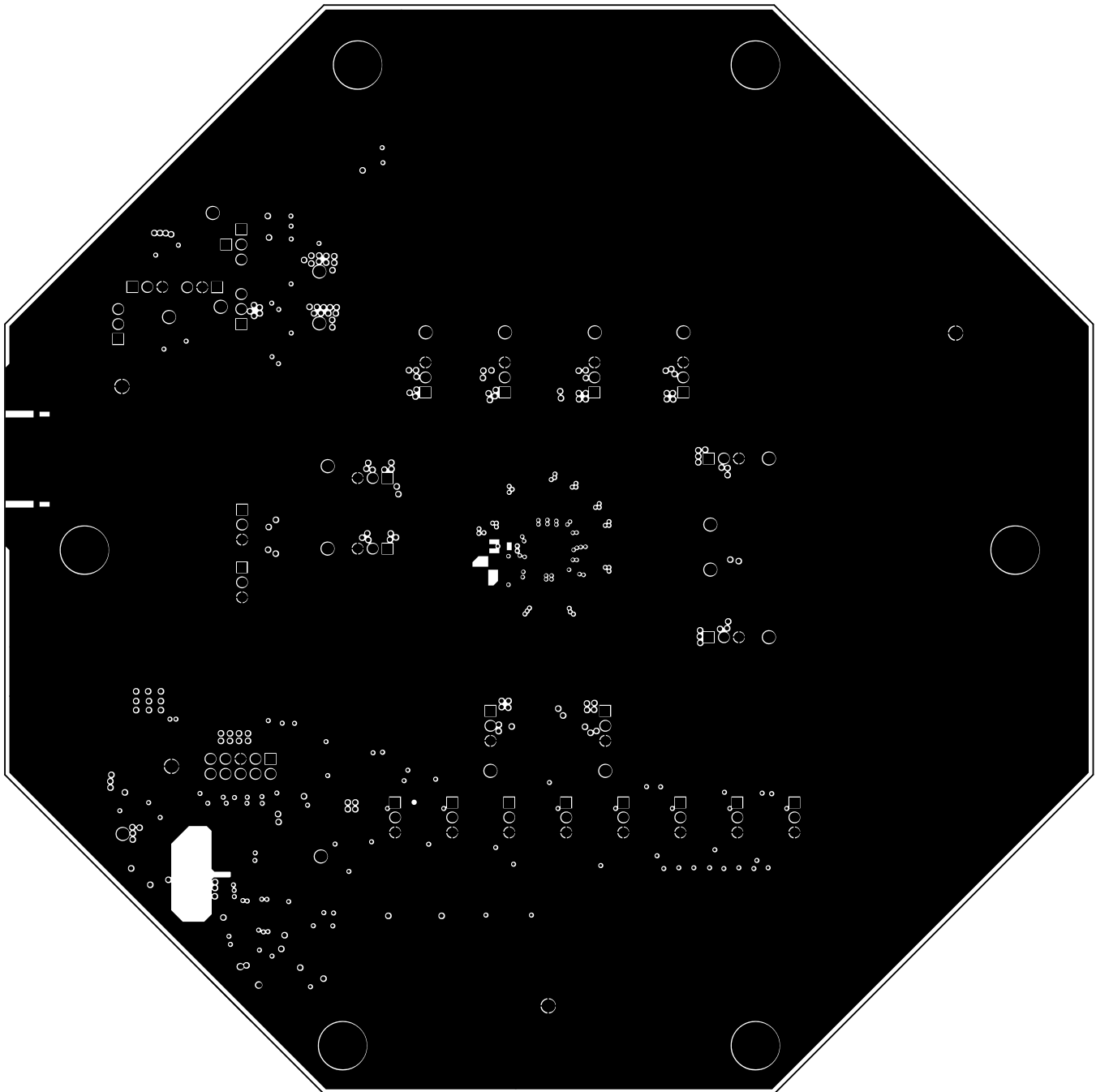


Figure 14. Layer 7

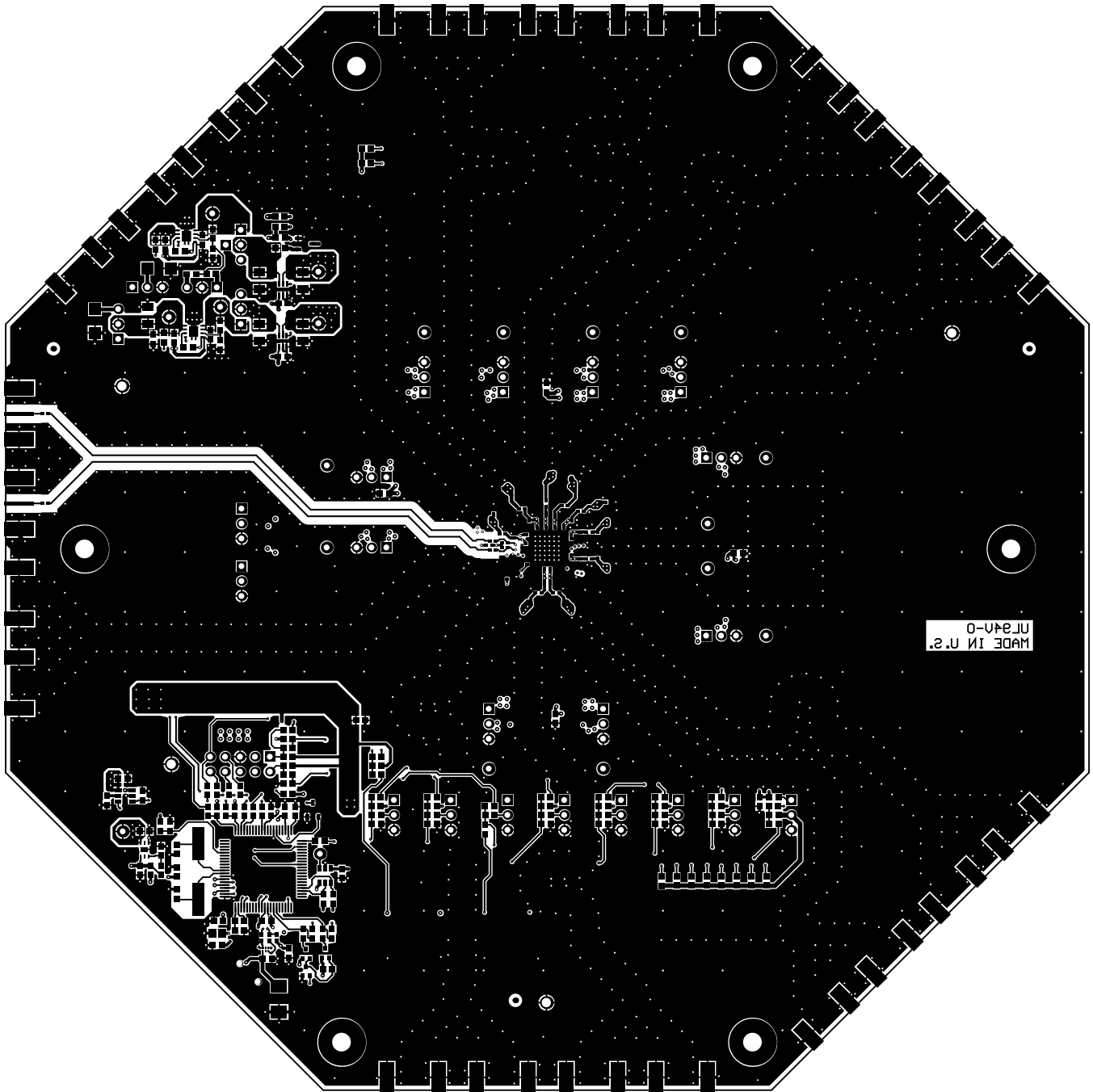


Figure 15. Layer 8 (Bottom Side, View from Top)

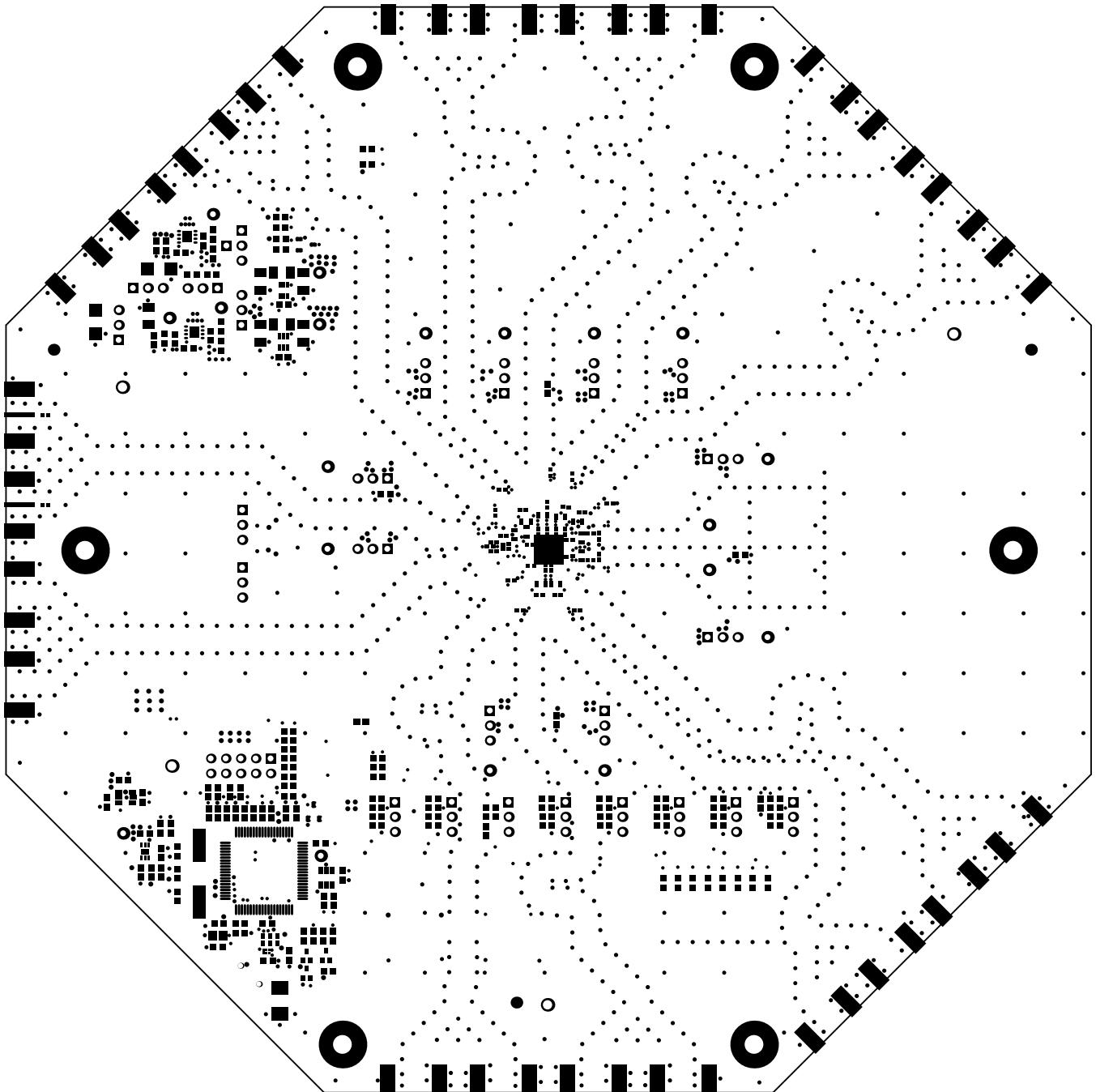


Figure 16. Bottom Solder Mask

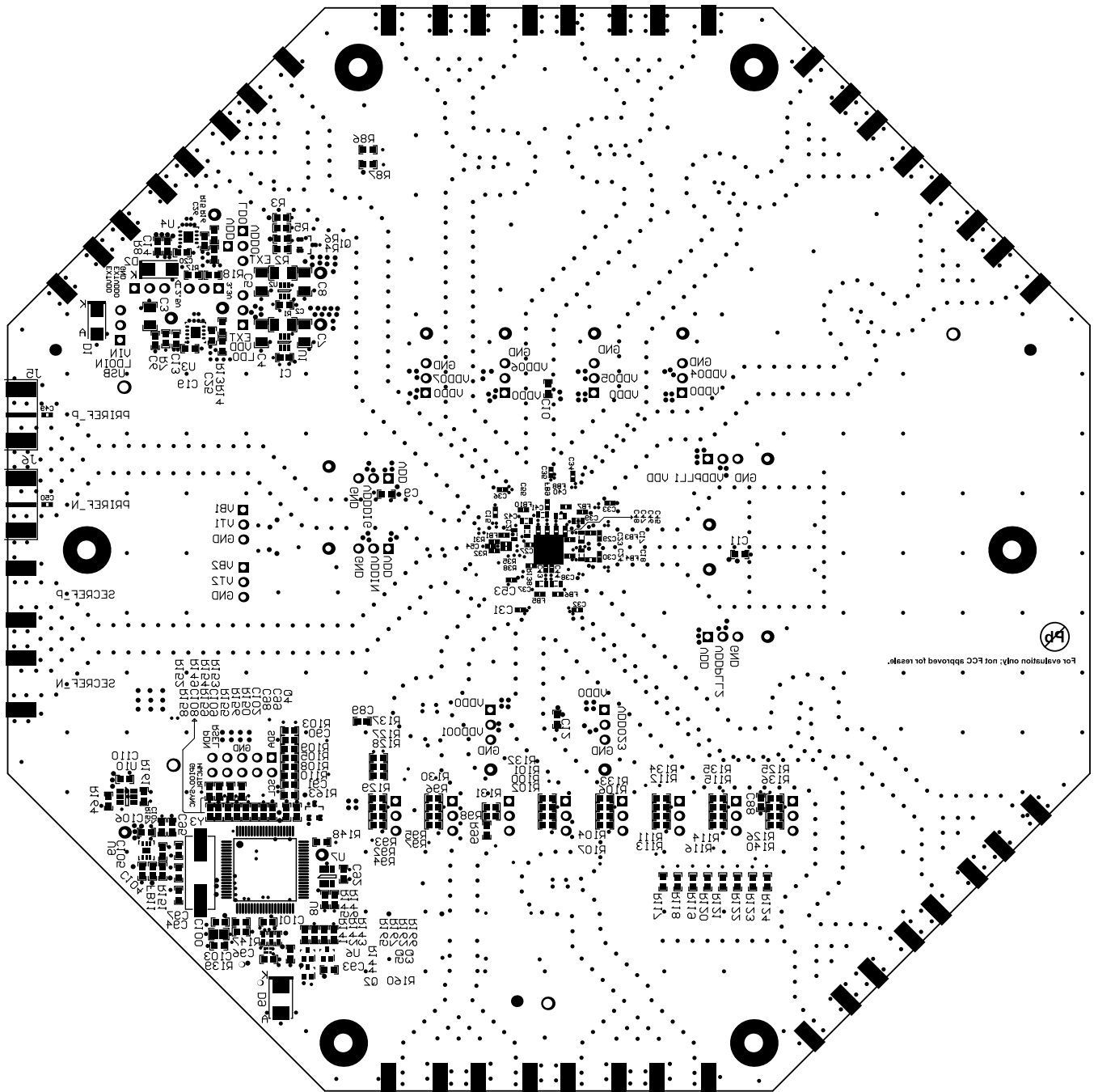


Figure 17. Bottom Overlay

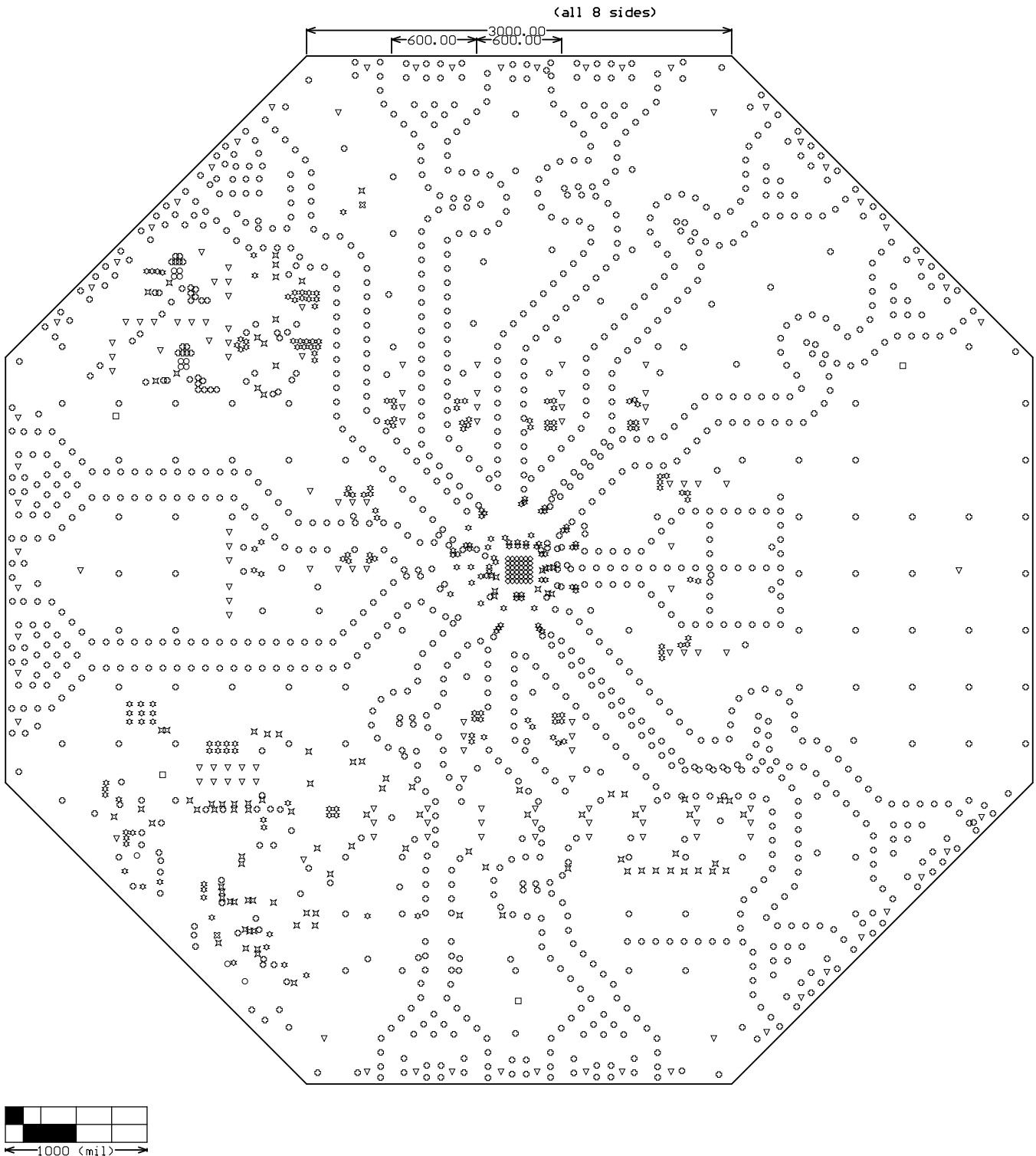


Figure 18. Drill Drawing

7 EVM Schematic

LMK033x8 EVALUATION MODULE (EVM)

PCB DIMENSIONS, STACKUP, CONTROLLED IMPEDANCE

DIMENSIONS:

- OCTOGON shape with 3" sides with equal length
- Final PCB thickness 62 mil +/- 10%

STACKUP: 8 layers

- Layer 1: Device layer with Digital routing, Signal/Power Jumpers/Switches, Crystal, RF microstrip traces from DUT to SMAs, Ground flood
==== FR4: 7 mil
- Layer 2: Ground Plane
==== FR4: 7 mil
- Layer 3: Ground Plane
==== FR4: 5 mil
- Layer 4: Digital and Power routing, Ground flood
==== FR4: 16 mil
- Layer 5: Split Power plane
==== FR4: 5 mil
- Layer 6: Ground Plane
====FR406: 7 mil
- Layer 7: Ground Plane
==== FR406: 7 mil
- Layer 8: RF microstrip traces from SMAs to DUT, Digital and Power routing, Ground flood

CONTROLLED IMPEDANCE TRACES:

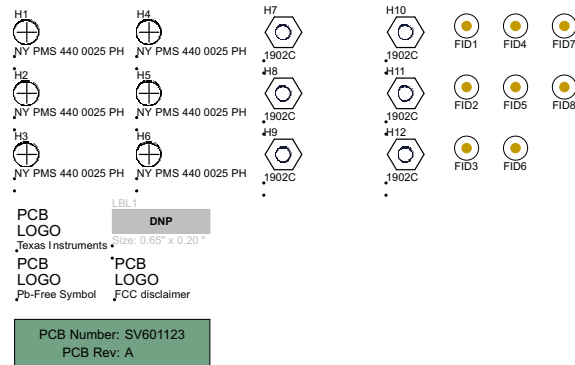
- EXTERNAL 11 mil traces to be 50 ohm Z_0 +/- 10%
- INTERNAL 6 mil traces to be 50 ohm Z_0 +/- 10%
- TOP 25 mil traces to be 50 ohm Z_0 +/- 10%, ref to Layer 3 (plane cutout on Layer 2)
- BOTTOM 25 mil traces to be 50 ohm Z_0 +/- 10%, ref to Layer 6 (plane cutout on Layer 7)

GROUND VIA STITCHING:

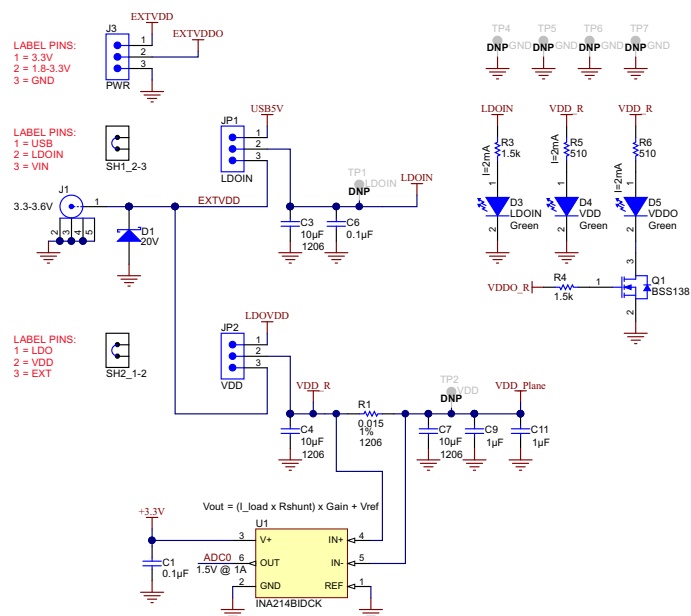
- Use ground vias with 100 mil spacing to stitch ground shielding around RF microstrip traces from DUT to SMAs.
- Use ground vias with 400 mil spacing to stitch ground planes/floods across the rest of board.

HARDWARE AND MARKINGS

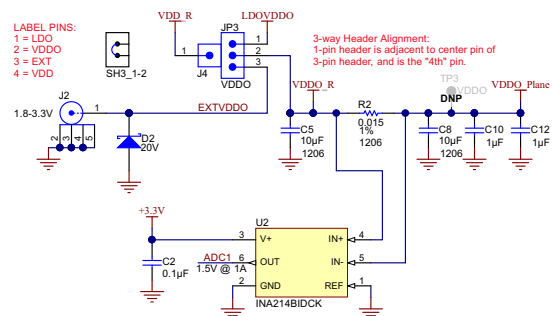
LAYOUT NOTE:
Place 6 standoffs at corners of the board .



POWER SUPPLY INPUTS



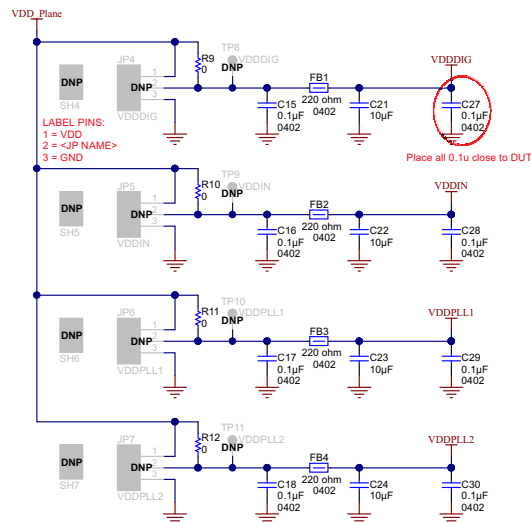
VDD CURRENT MONITOR



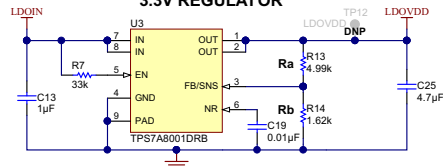
VDDO CURRENT MONITOR



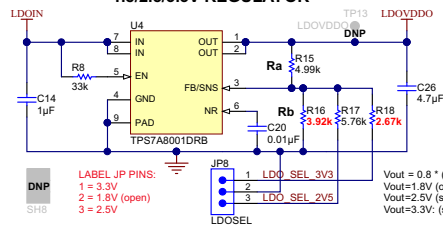
VDD CORE SUPPLY SELECTION & BYPASSING



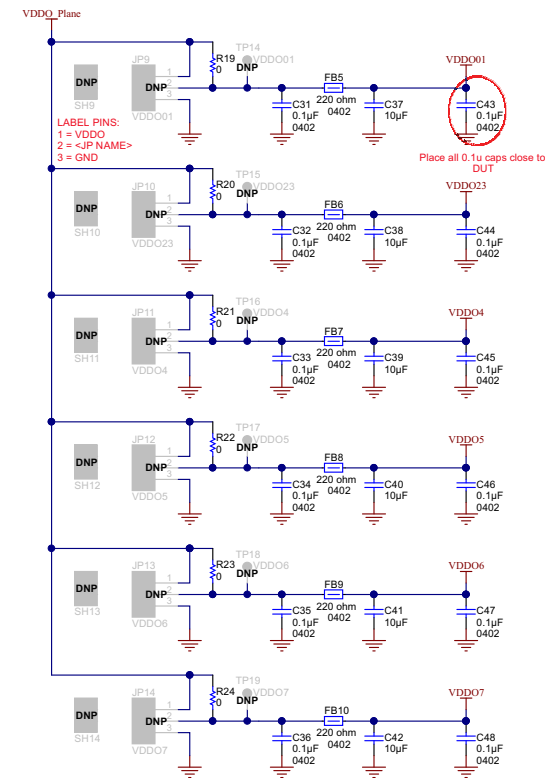
3.3V REGULATOR



1.8/2.5/3V REGULATOR



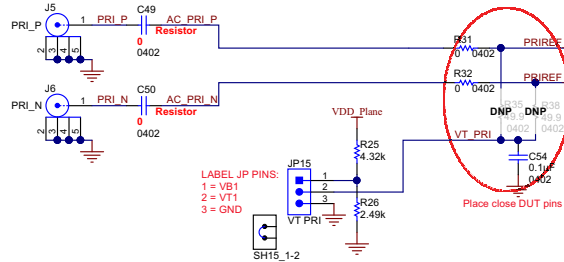
VDDO OUTPUT SUPPLY SELECTION & BYPASSING



USER NOTE:
Most applications may not require as many ferrite beads and decoupling / bypass caps. Multiple bypass caps in parallel are used to provide low power supply impedance over a wide frequency range for general evaluation. A ferrite bead and bulk cap may be shared to supply multiple output banks with the same PLL/frequency, but each VDDO pin should have its own bypass cap.

PRIMARY REF INPUT
50-ohm single-ended RF traces

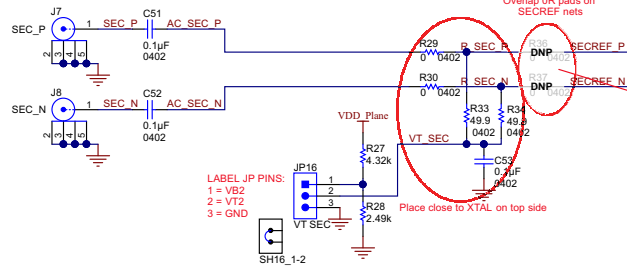
USER NOTE:
By default, PR1REF SMA ports are DC-coupled to DUT inputs with programmable on-chip termination.



LABEL JP PINS:
1 = VB1
2 = VT1
3 = GND

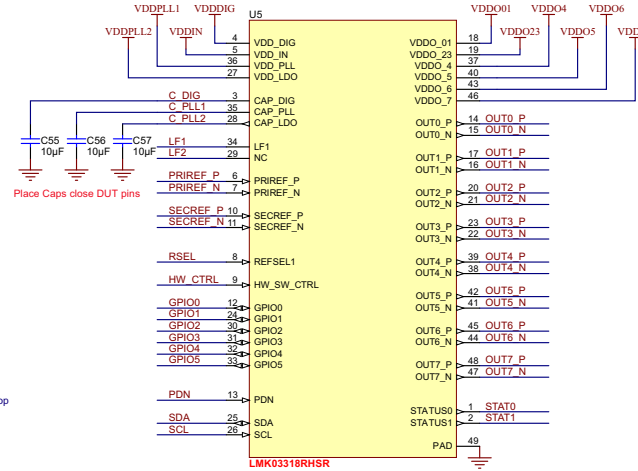
SECONDARY REF INPUT
50-ohm single-ended RF traces

USER NOTE:
By default, the onboard crystal (Y1) is connected to the SECREF inputs of the DUT. To use the SECREF SMA ports, depop R40/R41 and short R36/R37 to bypass/disable the crystal input. SECREF SMA ports are AC-coupled to external termination/biasing (on-chip termination disabled).



LABEL JP PINS:
1 = VB2
2 = VT2
3 = GND

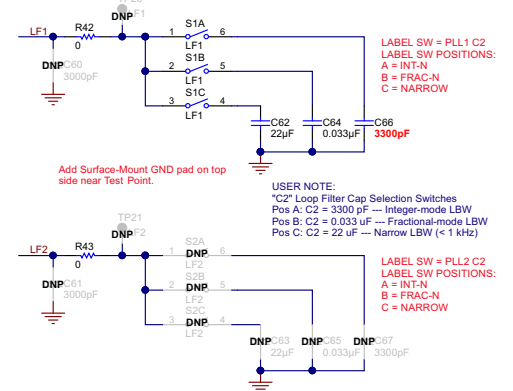
LMK033x8 DUT



Place Caps close DUT pins

DUT LAYOUT NOTES:
*** THERMAL REQUIREMENTS ***
- LMK03328 thermal vias: Use 6x6 via array with 0.3mm hole, 0.5mm via diameter, 0.8mm via pitch, 1 oz. copper plating.
- Remove soldermask on bottom thermal pad to expose copper.
- Use Ground flood on all layers (except split power plane) and DUT thermal vias using solid connection (no thermal relief) to all ground layers.

LOOP FILTER "C2" CAP SELECTION



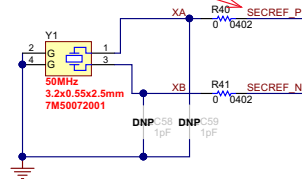
Add Surface-Mount GND pad on top side near Test Point.

USER NOTE:
"C2" Loop Filter Cap Selection Switches
Pos A: C2 = 3300 pF --- Integer-mode LBW
Pos B: C2 = 0.033 uF --- Fractional-mode LBW
Pos C: C2 = 22 uF --- Narrow LBW (< 1 kHz)

LABEL SW = PLL2 C2
LABEL SW POSITIONS:
A = INT-N
B = FRAC-N
C = NARROW

LOOP FILTER LAYOUT NOTES:
- Use sufficient clearance on these noise-sensitive nodes (traces, vias, TPs) from dynamic signals and power planes/traces.
- Connect loop filter caps to clean analog ground return path back to DUT.

CRYSTAL INPUT

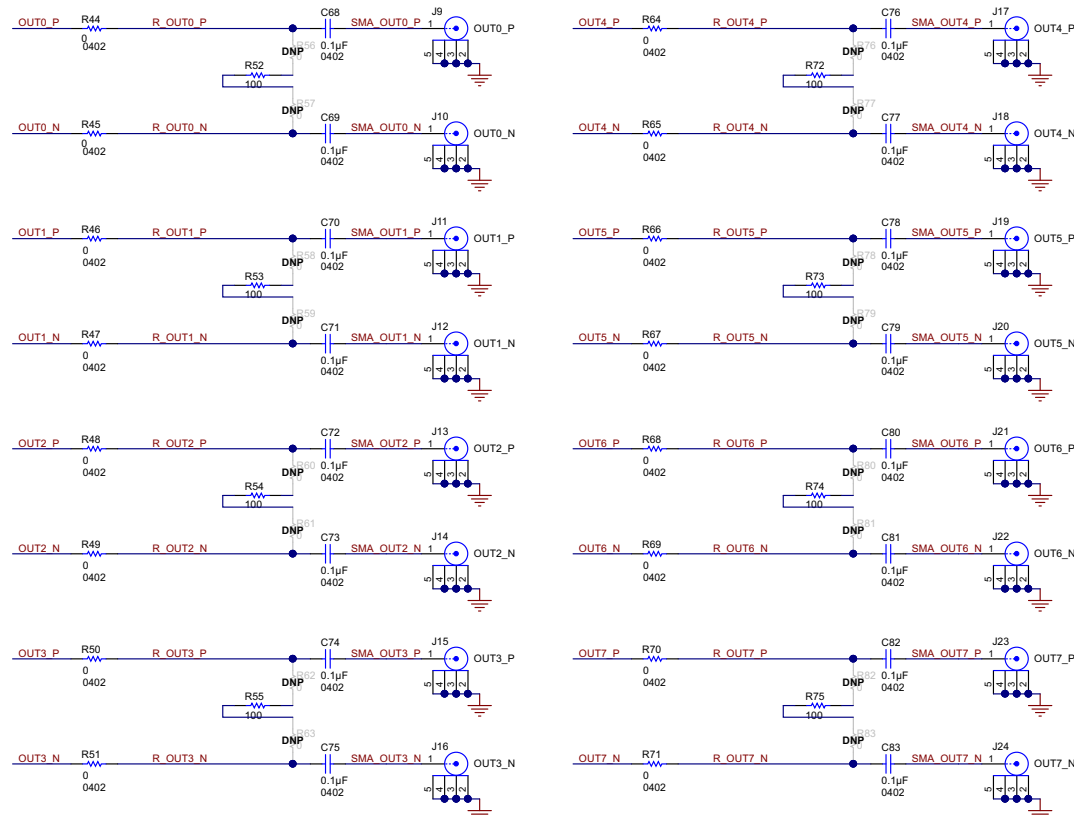


CRYSTAL LAYOUT REQUIREMENTS:
*** PLACEMENT ***
- CRITICAL: Minimize PCB trace and Pad parasitic cap <0.9pF (each leg of XTAL to DUT pin)
- Place XTAL as close as possible to DUT on Top side with short traces.
- Try to match lengths from each XTAL pin (XA/XB) to DUT pin (SECREF_P/N).
*** SHIELDING / ISOLATION ***
- XA/SECREF_P and XB/SECREF_N traces should be separated and kept away from other traces.
- Avoid routing below the XTAL pads and use plane cutouts below XTAL pads to minimize parasitic capacitance.

CLOCK INPUT (PR1REF_P/_N, SECREF_P/_N) LAYOUT REQUIREMENTS:
*** CONTROLLED IMPEDANCE ***
- Route as 50-ohm (+/-5% tol.) controlled-impedance single-ended RF traces from SMA center pin to DUT pin
- Place component pads directly on RF traces (no stubs), match 50-ohm trace width to SMA center pad, and use 50-ohm Zo via structures.
*** LENGTH / SKEW MATCHING ***
- Match input path length WITHIN pair from DUT to SMA pins (minimize intra-pair skew).
*** SHIELDING / ISOLATION ***
- Use ground shielding on routing layers with sufficient clearance to not affect controlled impedance of RF traces.
- Use ground stitching vias with 100 mil spacing around RF traces to connect together GND shielding on all layers.
- Use sufficient clearance between OUT# paths, as well as from other dynamic signal paths.
- Avoid crossing Digital signal/return paths with REF input signal/return paths; if unavoidable, cross at a 90 deg. angle

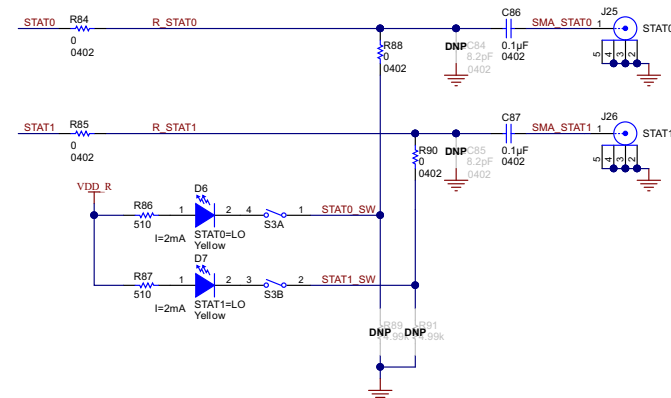
CLOCK OUTPUTS

50-ohm (+/-5%) single-ended RF traces



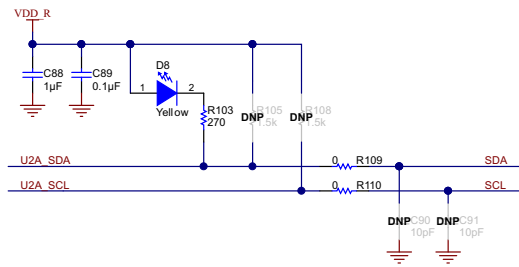
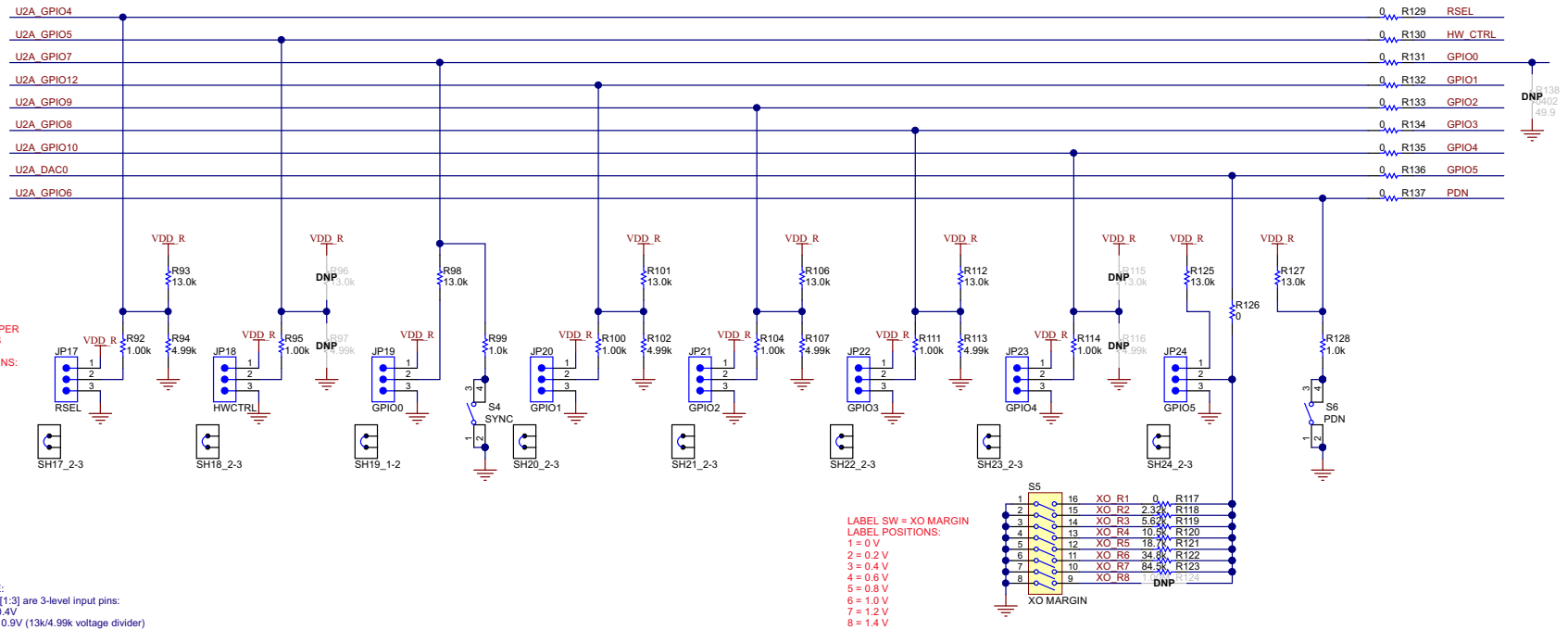
CLOCK OUTPUT (OUT#_P, OUT#_N) LAYOUT REQUIREMENTS:
 *** CONTROLLED IMPEDANCE ***
 - Route as 50-ohm (+/-5% tol.) controlled-impedance single-ended RF traces from DUT pin to SMA center pin.
 - Place component pads directly on RF traces (no stubs), match 50-ohm trace width to SMA center pad (25 mils wide), and use 50-ohm Zo via structures.
 *** LENGTH / SKEW MATCHING ***
 - Match output path lengths between all OUT#_P/N pairs from DUT to SMA pins (Minimize inter-pair or intra-pair skew).
 *** SHIELDING / ISOLATION ***
 - Use ground shielding on routing layers with sufficient clearance to not affect controlled impedance of RF traces.
 - Use ground stitching vias with 100 mil spacing around RF traces to connect GND shielding on all layers.
 - Use sufficient clearance between OUT# paths, as well as from other dynamic signal paths.
 - Avoid crossing Digital signal/return paths with clock OUT signal/return paths; if unavoidable, cross at a 90 deg. angle

STATUS OUTPUTS

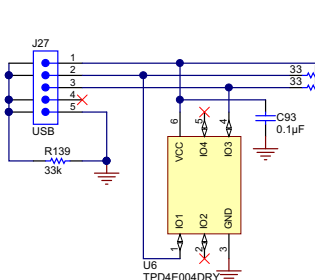


STATUS OUTPUT (STAT0, STAT1) LAYOUT REQUIREMENTS:
 *** CONTROLLED IMPEDANCE ***
 - Route as 50-ohm (+/-5% tol.) controlled-impedance single-ended RF traces from DUT pin to SMA center pin.
 - Place component pads directly on RF traces (no stubs), match 50-ohm trace width to SMA center pad (25 mils wide), and use 50-ohm Zo via structures.
 *** LENGTH / SKEW MATCHING ***
 - Match status output path lengths between STAT0 and STAT1 paths from DUT to SMA pins.
 *** SHIELDING / ISOLATION ***
 - Use ground shielding on routing layers with sufficient clearance to not affect controlled impedance of RF traces.
 - Use ground stitching vias with 100 mil spacing around RF traces to tie together GND shielding on all layers.
 - Use sufficient clearance between STAT0 and STAT1 paths, as well as from other RF paths.
 - Avoid crossing Digital signal/return paths with STATUS signal/return paths; if unavoidable, cross at a 90 deg. angle

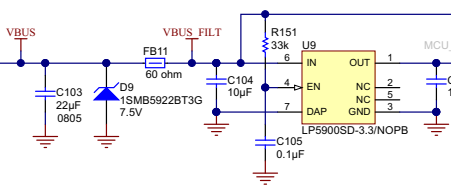
DIGITAL CONTROL PIN CONNECTIONS



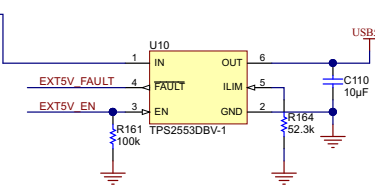
USB MINI-B CONNECTOR



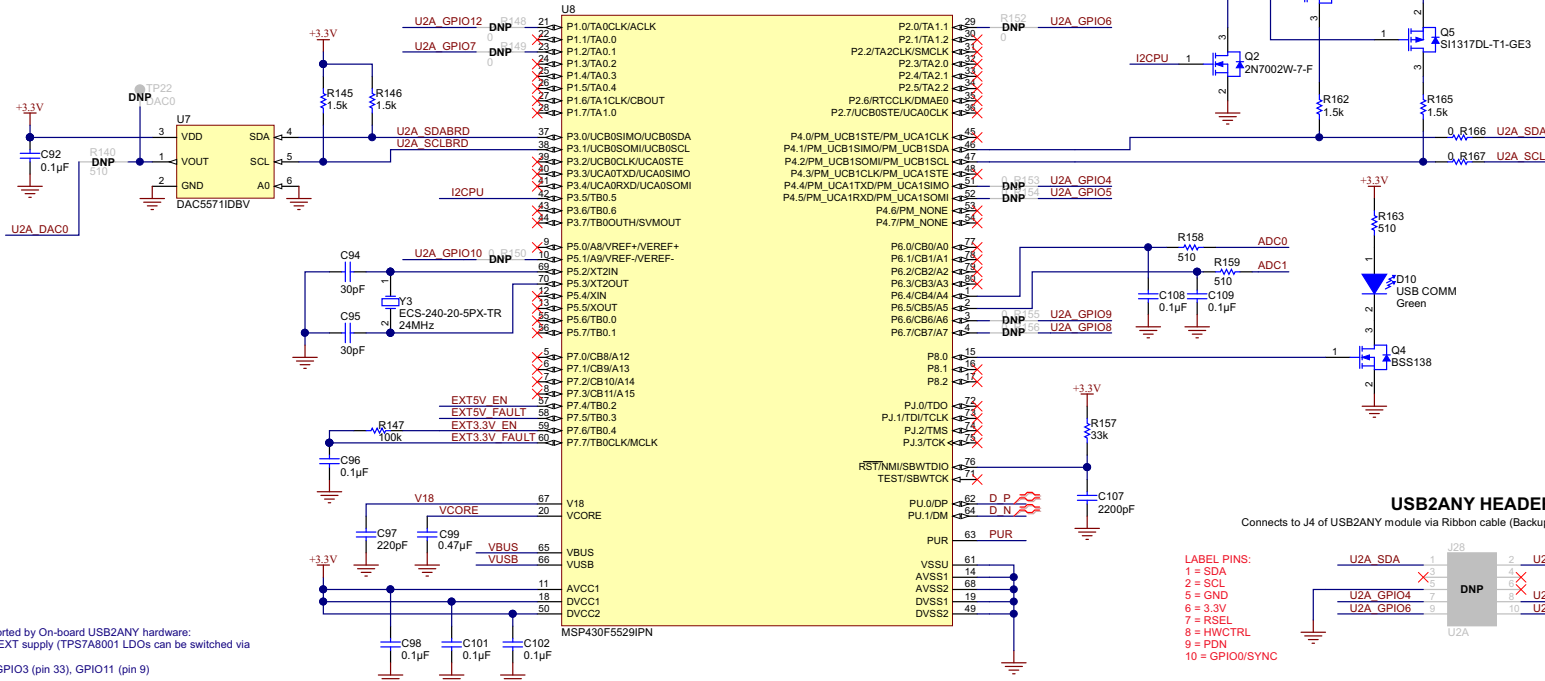
3.3V, 150mA REGULATOR



SWITCHED 5V, 0.5A USB SOURCE TO LDO REGULATORS



MSP430 MCU (USB2ANY)



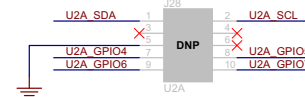
- Features not supported by On-board USB2ANY hardware:
- Switched +3.3V_EXT supply (TPS7A8001 LDOs can be switched via USB5V supply)
 - GPIO2 (pin 45), GPIO3 (pin 33), GPIO11 (pin 9)
 - ADC2, ADC3
 - DAC1
 - PWMs 0-3
 - SPI interface (I2C/SMBus only)

USER NOTE:
0R resistors between MSP430 and "U2A_GPIO[4-7]" nets should be de-populated before attaching the External USB2ANY module to the USB2ANY Header.

USB2ANY HEADER

Connects to J4 of USB2ANY module via Ribbon cable (Backup Host Interface if on-board MCU fails)

- LABEL PINS:
- 1 = SDA
 - 2 = SCL
 - 3 = GND
 - 4 = 3.3V
 - 5 = RSEL
 - 6 = HWCTRL
 - 7 = PDN
 - 8 = GPIO0/SYNC
 - 9 = PDN
 - 10 = GPIO0/SYNC



8 EVM Bill of Materials

DESIGNATOR	DESCRIPTION	MFR	PART NUMBER	QTY
!PCB1	Printed Circuit Board	Any	SV601123	1
C1, C2, C6, C89, C92, C93, C96, C98, C101, C102, C105, C108, C109	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	Kemet	C0603C104J4RACTU	13
C103	CAP, CERM, 22uF, 10V, +/-20%, X5R, 0805	Taiyo Yuden	LMK212BJ226MG-T	1
C104, C110	CAP, CERM, 10uF, 10V, +/-20%, X5R, 0603	TDK	C1608X5R1A106M	2
C107	CAP, CERM, 2200pF, 50V, +/-10%, X7R, 0603	Kemet	C0603C222K5RACTU	1
C13, C14	CAP, CERM, 1 µF, 10 V, +/- 10%, X5R, 0603	Kemet	C0603C105K8PACTU	2
C15, C16, C17, C18, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C43, C44, C45, C46, C47, C48, C51, C52, C53, C54, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C86, C87	CAP, CERM, 0.1uF, 10V, +/-10%, X5R, 0402	TDK	C1005X5R1A104K	42
C19, C20	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0603	Kemet	C0603C103K5RACTU	2
C21, C22, C23, C24, C37, C38, C39, C40, C41, C42, C55, C56, C57, C106	CAP, CERM, 10 µF, 6.3 V, +/- 20%, X5R, 0603	Kemet	C0603C106M9PACTU	14
C25, C26	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X5R, 0603	Kemet	C0603C475K8PACTU	2
C3, C4, C5, C7, C8	CAP, CERM, 10 µF, 10 V, +/- 20%, X7R, 1206	TDK	C3216X7R1A106M	5
C49, C50, R29, R30, R31, R32, R40, R41, R44, R45	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	10
C62	CAP, CERM, 22 µF, 6.3 V, +/- 20%, X5R, 0603	TDK	C1608X5R0J226M080AC	1
C64	CAP, CERM, 0.033 µF, 16 V, +/- 10%, X7R, 0603	MuRata	GRM188R71C333KA01D	1
C66	CAP, CERM, 3300 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H332JA01D	1
C9, C10, C11, C12, C88	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	Kemet	C0603C105K8PACTU	5
C94, C95	CAP, CERM, 30pF, 100V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C2A300JA01D	2
C97, C100	CAP, CERM, 220pF, 50V, +/-1%, C0G/NP0, 0603	AVX	06035A221FAT2A	2
C99	CAP, CERM, 0.47uF, 10V, +/-10%, X7R, 0603	MuRata	GRM188R71A474KA61D	1
D1, D2	Diode, Schottky, 20V, 2A, SMA	Diodes Inc.	B220A-13-F	2
D3, D4, D5, D10	LED, Green, SMD	Lite-On	LTST-C190GKT	4
D6, D7, D8	LED, Yellow, SMD	Lite-On	LTST-C170KSKT	3
D9	Diode, Zener, 7.5V, 550mW, SMB	ON Semiconductor	1SMB5922BT3G	1
FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9, FB10	Ferrite Bead, 220 ohm @ 100 MHz, 0.45 A, 0402	MuRata	BLM15AG221SN1D	10
FB11	3.5A Ferrite Bead, 60 ohm @ 100MHz, SMD	TDK	MPZ1608S600A	1
FID1, FID2, FID3, FID4, FID5, FID6, FID7, FID8	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	8

DESIGNATOR	DESCRIPTION	MFR	PART NUMBER	QTY
H1, H2, H3, H4, H5, H6	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B and F Fastener Supply	NY PMS 440 0025 PH	6
H7, H8, H9, H10, H11, H12	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	6
J1, J2, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26	Connector, End launch SMA, 50 ohm, SMT	Emerson Network Power	142-0701-851	24
J27	Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	TE Connectivity	1734035-2	1
J3, JP1, JP2, JP3, JP8, JP17, JP18, JP19, JP20, JP21, JP22, JP23, JP24	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-103-07-G-S	13
J4	Header, TH, 100mil, 1pos, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-101-07-G-S	1
JP15, JP16	Header, 100mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S	2
Q1, Q4	MOSFET, N-CH, 50V, 0.22A, SOT-23	Fairchild Semiconductor	BSS138	2
Q2	MOSFET, N-CH, 60V, 0.115A, SOT-323	Diodes Inc.	2N7002W-7-F	1
Q3, Q5	MOSFET, P-CH, -20V, 1.4A, SOT-323	Vishay-Siliconix	SI1317DL-T1-GE3	2
R1, R2	RES, 0.015, 1%, 0.5 W, 1206	Stackpole Electronics Inc	CSR1206FK15L0	2
R103	RES, 270, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603270RJNEA	1
R118	RES, 2.32 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06032K32FKEA	1
R119	RES, 5.62 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06035K62FKEA	1
R120	RES, 10.5 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K5FKEA	1
R121	RES, 18.7 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060318K7FKEA	1
R122	RES, 34.8 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060334K8FKEA	1
R123	RES, 84.5 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060384K5FKEA	1
R13, R15	RES, 4.99 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06034K99FKEA	2
R14	RES, 1.62 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K62FKEA	1
R141, R142	RES, 33 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040233R0JNED	2
R143	RES, 1.5k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04021K50JNED	1
R144	RES, 1.2Meg ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031M20JNEA	1
R145, R146, R162, R165	RES, 1.5k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031K50JNEA	4
R147, R160, R161	RES, 100k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603100KJNEA	3
R16	RES, 3.92 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06033K92FKEA	1
R164	RES, 52.3 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060352K3FKEA	1
R166, R167	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	2
R17	RES, 5.76 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06035K76FKEA	1
R18	RES, 2.67 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06032K67FKEA	1
R25, R27	RES, 4.32 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06034K32FKEA	2
R26, R28	RES, 2.49 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06032K49FKEA	2
R3, R4	RES, 1.5 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031K50JNEA	2
R33, R34	RES, 49.9, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040249R9FKED	2
R42, R43, R46, R47, R48, R49, R50, R51, R64, R65, R66, R67, R68, R69, R70, R71, R84, R85, R88, R90	RES, 0 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04020000Z0ED	20
R5, R6, R86, R87, R103, R158, R159, R163	RES, 510, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603510RJNEA	8
R52, R53, R54, R55, R72, R73, R74, R75	RES, 100, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402100RFKED	8
R7, R8, R139, R151, R157	RES, 33k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060333K0JNEA	5

DESIGNATOR	DESCRIPTION	MFR	PART NUMBER	QTY
R9, R10, R11, R12, R19, R20, R21, R22, R23, R24, R109, R110, R117, R126, R129, R130, R131, R132, R133, R134, R135, R136, R137	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	23
R92, R95, R100, R104, R111, R114	RES, 1.00 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00FKEA	6
R93, R98, R101, R106, R112, R125, R127	RES, 13.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060313K0FKEA	7
R94, R102, R107, R113	RES, 4.99k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034K99FKEA	4
R99, R128	RES, 1.0 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00JNEA	2
S1	Switch, Slide, SPST 3 poles, SMT	CTS Electrocomponents	219-3LPST	1
S3	Switch, Slide, SPST 2 poles, SMT	CTS Electrocomponents	219-2LPST	1
S4, S6, S7	Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	TE Connectivity	4-1437565-1	3
S5	Switch, Slide, SPST 8 poles, SMT	CTS Electrocomponents	219-8MST	1
SH1_2-3, SH2_1-2, SH3_1-2, SH15_1-2, SH16_1-2, SH17_2-3, SH18_2-3, SH19_1-2, SH20_2-3, SH21_2-3, SH22_2-3, SH23_2-3, SH24_2-3	Shunt, 100mil, Gold plated, Black	3M	969102-0000-DA	13
U1, U2	Voltage Output, High or Low Side Measurement, Bi-Directional Zero-Drift Series Current-Shunt Monitor, DCK0006A	Texas Instruments	INA214BIDCK	2
U10	PRECISION ADJUSTABLE CURRENT-LIMITED POWER-DISTRIBUTION SWITCHES, DBV0006A	Texas Instruments	TPS2553DBV-1	1
U3, U4	Low-Noise, Wide-Bandwidth, High PSRR, Low-Dropout 1A Linear Regulator, DRB0008A	Texas Instruments	TPS7A8001DRB	2
U5	Ultra-Low Jitter Clock Generator Family with Two Independent PLLs, Up to 8 Differential Outputs, Two Inputs, RHS0048A	Texas Instruments	LMK03318RHSR	1
U6	4-CHANNEL ESD-PROTECTION ARRAY FOR HIGH-SPEED DATA INTERFACES, DRY006A	Texas Instruments	TPD4E004DRY	1
U7	2.7 V to 5.5 V, I2C INTERFACE, VOLTAGE OUTPUT, 8-BIT DIGITAL TO ANALOG CONVERTER, DBV0006A	Texas Instruments	DAC5571IDBV	1
U8	Mixed Signal MicroController, PN0080A	Texas Instruments	MSP430F5529IPN	1
U9	Ultra Low Noise, 150mA Linear Regulator, 6-pin LLP, Pb-Free	Texas Instruments	LP5900SD-3.3/NOPB	1
Y1	Crystal, 50 MHz, 9 pF, SMD	TXC Corporation	7M50072001	1
Y3	Crystal, 24.000MHz, 20pF, SMD	ECS Inc.	ECS-240-20-5PX-TR	1
DNP COMPONENTS BELOW				
C58, C59	CAP, CERM, 1 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H1R0CA01D	0
C60, C61	CAP, CERM, 3000 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H302JA01D	0
C63	CAP, CERM, 22 µF, 6.3 V, +/- 20%, X5R, 0603	TDK	C1608X5R0J226M080AC	0
C65	CAP, CERM, 0.033 µF, 16 V, +/- 10%, X7R, 0603	MuRata	GRM188R71C333KA01D	0

DESIGNATOR	DESCRIPTION	MFR	PART NUMBER	QTY
C67	CAP, CERM, 3300 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H332JA01D	0
C84, C85	CAP, CERM, 8.2 pF, 25 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1E8R2CA01D	0
C90, C91	CAP, CERM, 10pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C100J5GACTU	0
J28	Header, 100mil, 5x2, Tin plated, TH	Sullins Connector Solutions	PEC05DAAN	0
JP4, JP5, JP6, JP7, JP9, JP10, JP11, JP12, JP13, JP14	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-103-07-G-S	0
LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	0
R105, R108	RES, 1.5k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031K50JNEA	0
R124	RES, 1.00 M, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031M00FKEA	0
R140	RES, 510, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603510RJNEA	0
R148, R149, R150, R152, R153, R154, R155, R156	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	0
R35, R38, R138	RES, 49.9, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040249R9FKED	0
R36, R37, R56, R57, R58, R59, R60, R61, R62, R63, R76, R77, R78, R79, R80, R81, R82, R83	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	0
R89, R91, R97, R116	RES, 4.99k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034K99FKEA	0
R96, R115	RES, 13.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060313K0FKEA	0
S2	Switch, Slide, SPST 3 poles, SMT	CTS Electrocomponents	219-3LPST	0
SH4, SH5, SH6, SH7, SH8, SH9, SH10, SH11, SH12, SH13, SH14	Shunt, 100mil, Gold plated, Black	3M	969102-0000-DA	0
TP1, TP2, TP3, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP23	Test Point, Miniature, Red, TH	Keystone	5000	0
TP20, TP21, TP22	Test Point, Miniature, Orange, TH	Keystone	5003	0
TP4, TP5, TP6, TP7	Test Point, Compact, Black, TH	Keystone	5006	0

9 Recommended Test Instruments

For making accurate measurements on ultra-low noise/jitter, high-speed clock signals, the following instruments are recommended:

- Source Signal Analyzer: Keysight/Agilent E5052 for phase noise/jitter measurements
- Oscilloscope: Agilent DSA90000A series (or equivalent) for AC measurements and time-domain jitter analysis with jitter software package
- Reference Oscillator (optional): Low-jitter clock source with LVCMOS or Differential output to SMA connector(s) to interface to PRIREF or SECREF inputs
 - Crystek CPRO33 Pocket Reference Oscillator, 3.3V HCMOS crystal oscillator, various standard frequencies, ± 25 ppm stability, SMA connectors
- Balun: M/A-COM H-183-4 (30-3000 MHz) 180° coupler, or equivalent

10 Example Performance Measurements

RMS Jitter and phase noise measurements were taken on the output clocks measured using **Soft Pin Mode, EEPROM Page 5** with the on-board 50-MHz crystal as the PLL reference input. The differential output clocks were measured using a balun to a Keysight/Agilent E5052B. Some phase noise plots are provided below.

Table 7. Output RMS Jitter Summary – Soft Pin Mode, EEPROM Page 5

Output	Output Frequency / Type	RMS Jitter (fs), 12k-20M band, spurs excluded	RMS Jitter (fs), 12k-20M band, spurs in included	Reference Plot
OUT0 (OUT1 similar)	156.25 MHz LVPECL	118	119	Figure 19
OUT2 (OUT3 similar)	125 MHz LVPECL	109	110	Figure 20
OUT4 (OUT5 similar)	100 MHz LVPECL	118	122	Figure 21
OUT6 (OUT7 similar)	25 MHz LVPECL	109 12k-5M band	109 12k-5M band	Figure 22

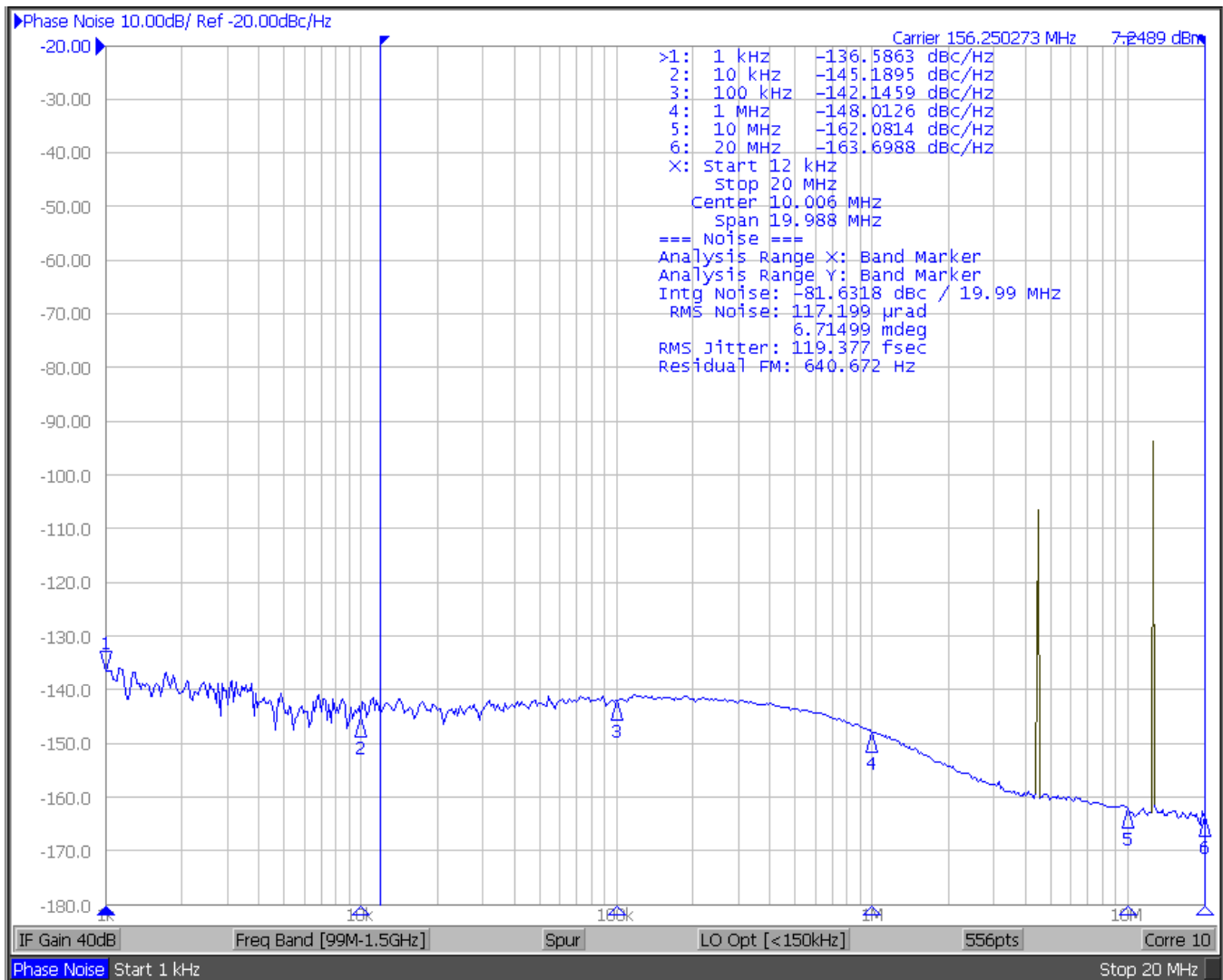


Figure 19. Soft Pin Mode, EEPROM Page 5, OUT0 – 156.25 MHz LVPECL (Spurs in dBc)

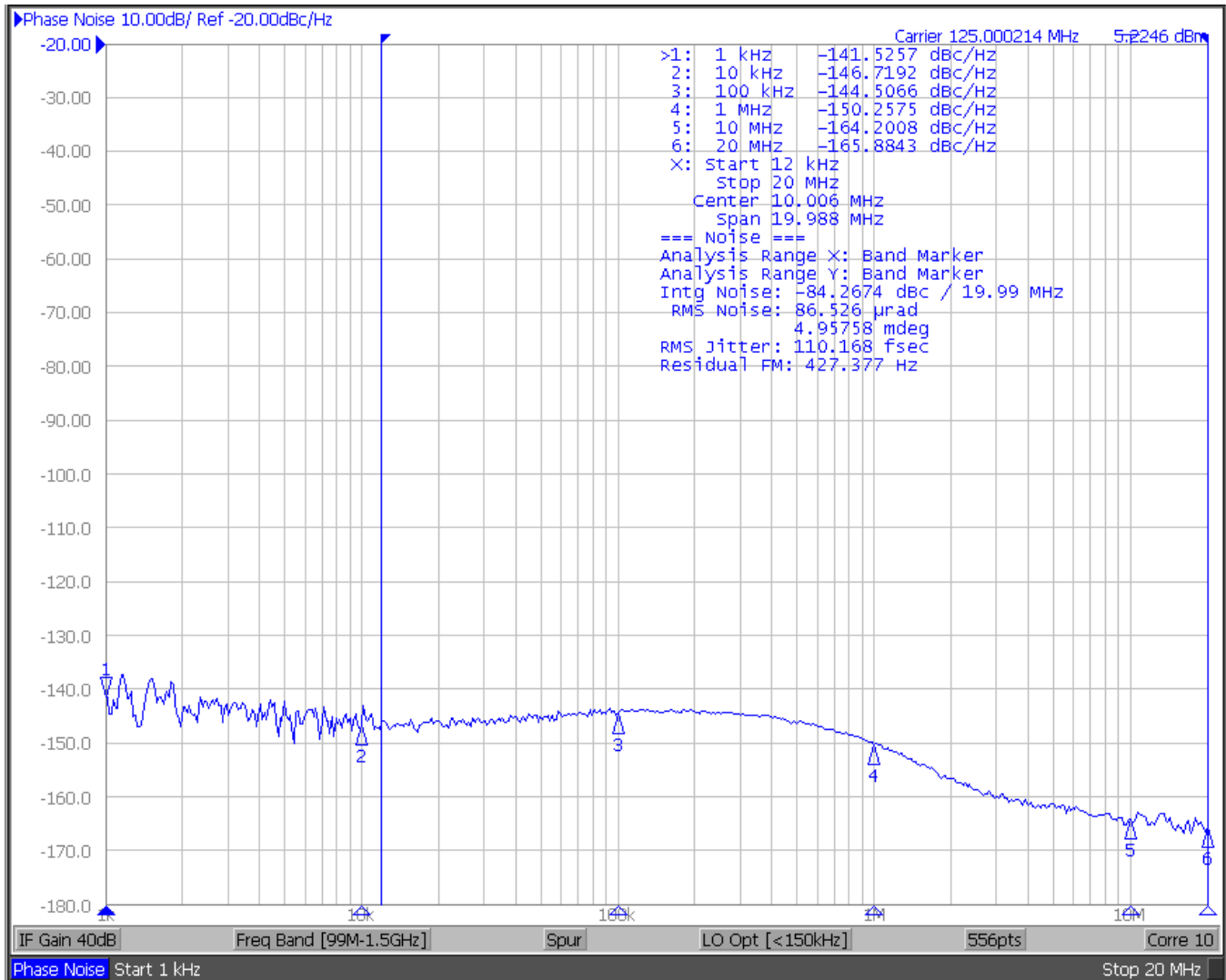


Figure 20. Soft Pin Mode, EEPROM Page 5, OUT2 – 125 MHz LVPECL (Spurs in dBc)

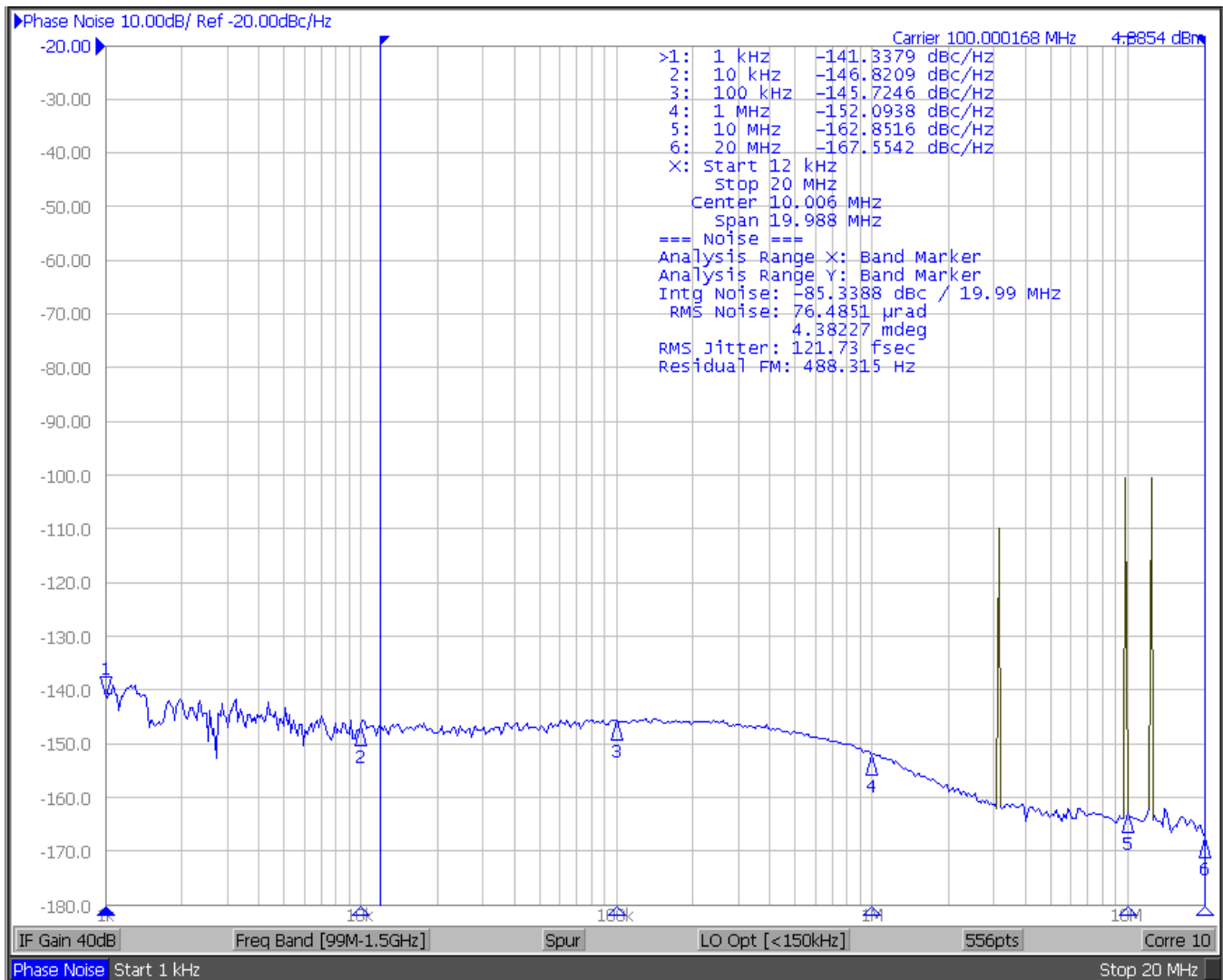


Figure 21. Soft Pin Mode, EEPROM Page 5, OUT4 – 100 MHz LVPECL (Spurs in dBc)

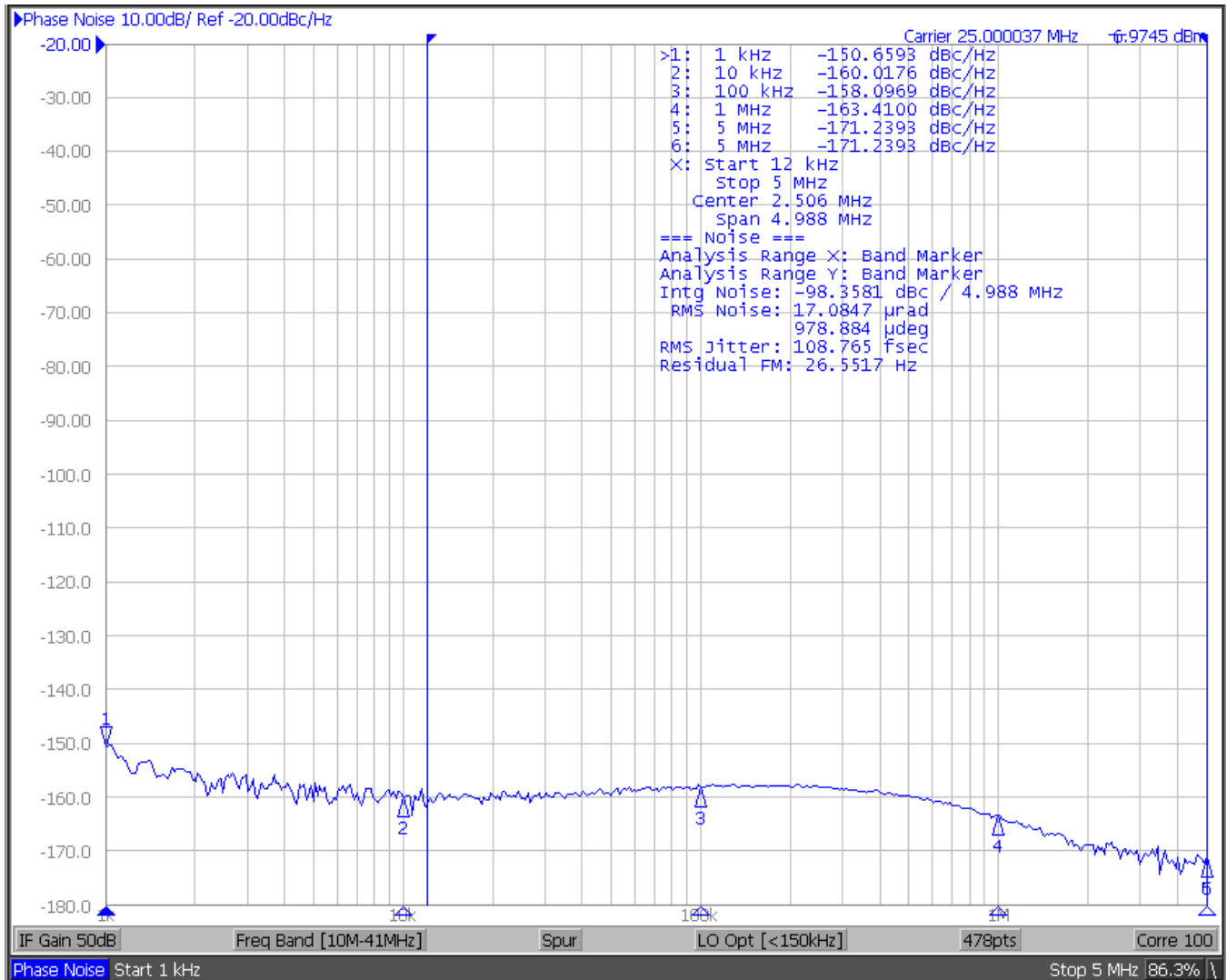


Figure 22. Soft Pin Mode, EEPROM Page 5, OUT6 – 25 MHz LVPECL (Spurs in dBc)

11 Using TI's USB2ANY Module for In-System Programming of LMK03318

When designing in the LMK03318 into a system application board, it is recommended to provision a **dedicated** header to access the I2C lines of the device to support external programming from Texas Instruments' USB2ANY module (see [Figure 23](#)). The USB2ANY module can be very useful to support in-system programming of the initial clock configuration (e.g. before the system software/firmware is enabled) and rapid clock prototyping, optimization, and debugging.



Figure 23. USB2ANY Module

Because the USB2ANY module implements the same MSP430-based USB-to-I2C interface/firmware as the one integrated on the LMK03318EVM, the same EVM GUI platform can be used to easily program the device in-system.

Once the customer's system software/firmware is enabled and can provide reliable configuration of the LMK03318, then the provisional I2C header may be removed or superseded in the next iteration of the hardware design.

11.1 USB2ANY Board Connections

The USB2ANY has four interface connectors: one USB 2.0 connector (J2) and three I/O connectors (J3, J4, and J5). The USB connector is a standard 'A' type mini USB receptacle. The I/O connectors are standard dual-row, 0.1" center, pin headers.

I/O connectors J3 and J5 are 8-pin type and J4 is a 10-pin type. They are configured such that they will accept either individual cable connections or a single 30-pin connection.

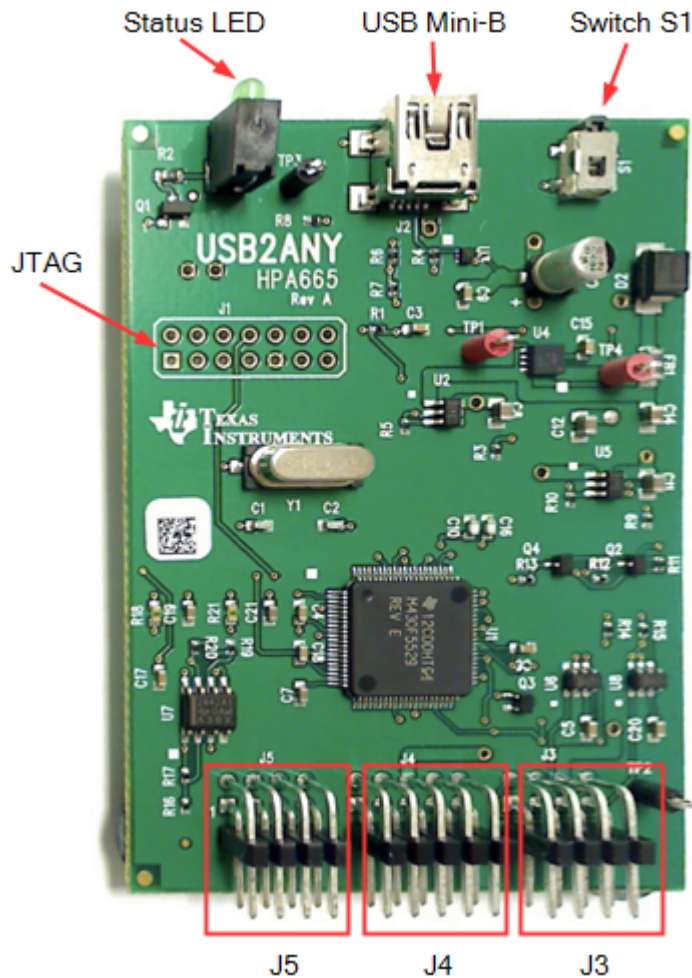


Figure 24. USB2ANY Board Connections

The standard USB2ANY Kit (HPA665-001) includes both a 10-pin cable and a 30-pin cable. The 10-pin cable is intended to be connected to J4. J4 provides the SDA, SCL, and GND connections of interest.

NOTE: J5 and J6 supply other connections that are NOT required and therefore, outside the scope of this document.

When the USB2ANY board is in the enclosure, there is a key notch above J4 that will prevent the cable connector from being plugged in upside-down. With the notch at the top, pin 1 of the 10-pin cable connector is located at the upper-right corner.

The 10-pin cable is about 6 inches in length and has a keyed female 10-pin IDC connector on each end. The cable should be connected to the USB2ANY board as shown in [Figure 25](#) (note that the key must be facing up, away from the board). The opposite end of the cable should be connected to the target board. The red stripe on the cable indicates pin 1 as shown in [Figure 26](#).

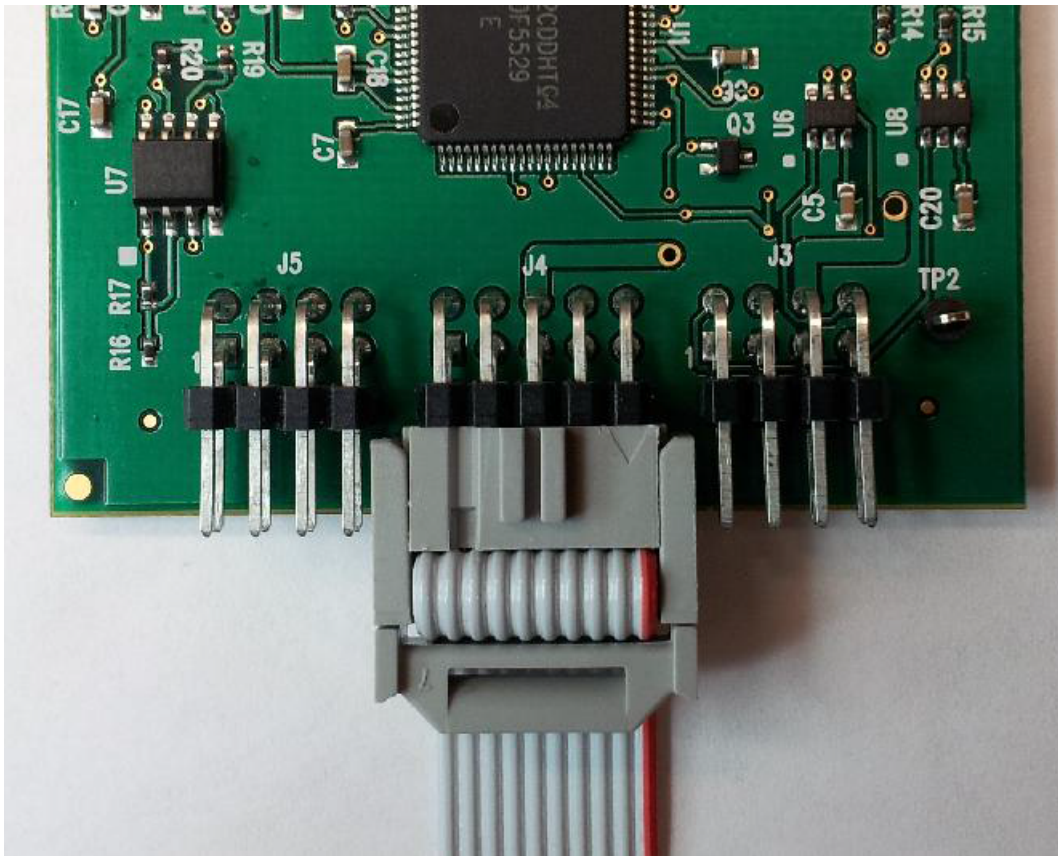


Figure 25. 10-pin Cable Connection to J4

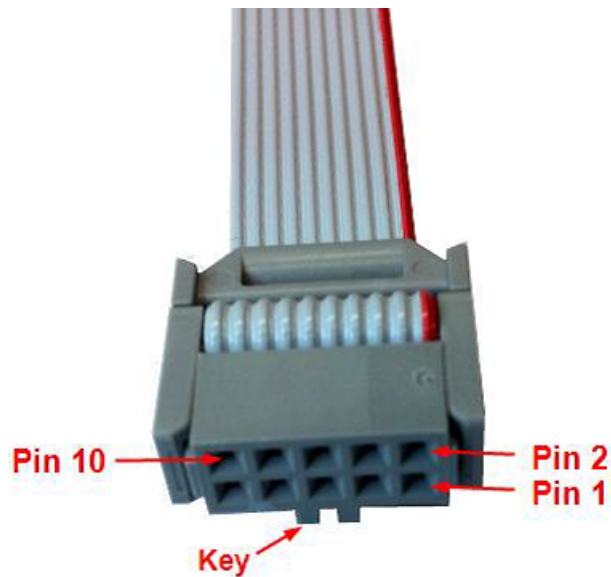


Figure 26. 10-pin Cable Pinout

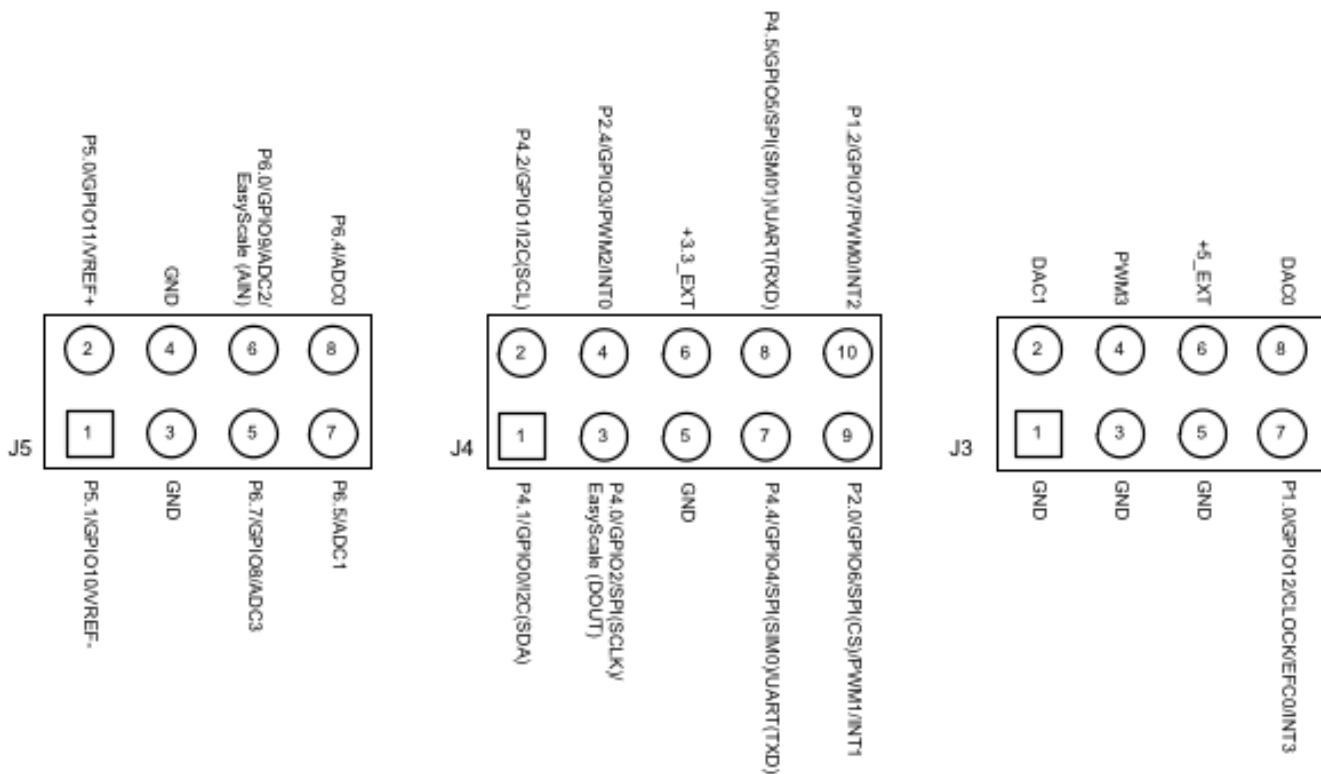


Figure 27. USB2ANY Board Connector Pinout Diagram

Table 8. USB2ANY Board Connector J4 and 10-pin Cable Pinouts

Pin Name	J4 Pin #	Cable Pin #	Description
P4.1/GPIO0/I2C(SDA)	1	10	I2C Data
P4.2/GPIO1/I2C(SCL)	2	9	I2C Clock
P4.0/GPIO2/SPI(SCLK)	3	8	General-purpose digital I/O (not required)
P2.4/GPIO3	4	7	General-purpose digital I/O (not required)
GND	5	6	Common Ground
+3.3_EXT	6	5	+3.3V output power supply (100 mA limit)
P4.4/GPIO4/SPI(SIM0)	7	4	General-purpose digital I/O (not required)
P4.5/GPIO5/SPI(SM01)	8	3	General-purpose digital I/O (not required)
P2.0/GPIO6/SPI(CS)	9	2	General-purpose digital I/O (not required)
P1.2/GPIO7	10	1	General-purpose digital I/O (not required)

Instead of using the 10-pin header and supplied cable, a board designer may alternatively choose to use a 3-pin "I2C header" on the application board and 3 jumper wires to connect the SDA, SCL, and GND signals from J4 of USB2ANY to the I2C header.

11.2 Ordering a USB2ANY Module

To order a USB2ANY module, submit a request to clock_support@list.ti.com with the following information:

1. Request/Reason: 1 pc. USB2ANY module for LMK03318 in-system programming/prototyping
2. Company Name:
3. Application/End-Equipment:
4. LMK03318 Est. Annual Volume/Year:
5. Ship-To Address:

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.
 - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software
 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
 - 2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.
 - 2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
3. *Regulatory Notices:*
 - 3.1 *United States*
 - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
 - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/llds/ti_ja/general/eStore/notice_02.page

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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