Programmer's Guide

LMH1229 and LMH1239 Programming Guide

ABSTRACT

This document provides a reference for the LMH12x9 cable equalizer with a reclocker from a programming model perspective including detailed information relating to programming and different configuration options. The intended audience includes software as well as hardware engineers working on system diagnostics and control software.

The reader should be familiar with the collateral related to the LMH12x9 cable equalizer with reclocker and the LMH1239EVM (LMH12x9 data sheet, EVM user's guide, EVM GUI, and others).

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Trademarks

1 Access Methods

Two methods are provided for accessing the LMH12x9 registers. These are:

- Register control through the Serial Management Bus (SMBus)
- Register control through the Serial Parallel Interface (SPI)

In a typical system, either SMBus or SPI access is used to configure and monitor the device status. Unless specified, the register configurations for SPI and SMBus are the same.

1.1 Register Programming Through SMBus

The LMH12x9 internal registers can be accessed through standard SMBus or SPI protocol. The SMBus Mode is enabled by setting MODE_SEL = L (1kΩ to GND). The pins associated with the LMH12x9 SMBus interface are:

- ADDR0 (Pin 11): Strap pin used to set the SMBus address
- ADDR1 LMH1239 (Pin 26), ADDR1 LMH1229 (Pin 28): Strap pin used to set the SMBus address
- SDA (Pin 13): SMBus data pin
- SCL LMH1239 (Pin 27), SCL LMH1229 (Pin 29): SMBus clock pin

The SMBus target address is strapped at power up based on the configuration of the ADDR0 and ADDR1 pins. The state of these two pins are read on power up, after the internal power-on reset signal is deasserted. The maximum operating speed supported on the SMBus is 400kHz.

There are 16 unique SMBus addresses that can be assigned to each device by placing external resistor straps on the ADDR0 and ADDR1 pins (Pin 11 and 26/28).

Table 1-1. SMBus Addresses

ADDR0 (LEVEL)	ADDR1 (LEVEL)	7-BIT ADDRESS [HEX]	8-BIT WRITE COMMAND [HEX](1)
L	L	3D	7A
L	R	3E	7C
L	F	3F	7E
L	H	40	80
R	L	41	82
R	R	42	84
R	F	43	86
R	H	44	88
F	L	45	8A
F	R	46	8C
F	F	47	8E
F	H	48	90
H	L	49	92
H	R	4A	94
H	F	4B	96
H	H	4C	98

(1) The 8-bit write command consists of the 7-bit target address (Bits 7:1) with 0 appended to the LSB to indicate an SMBus write. For example, if the 7-bit target address is 0x2D (8'b00101101), the 8-bit write command is 0x5A (8'b01011010).

1.2 Register Programming Through SPI

Alternatively, when MODE_SEL = F, SPI is used to configure the LMH12x9 for different configurations. Pins associated with SPI are:

- PICO (Pin 13): Peripheral Input, Controller Output
- LMH1239 POCI (Pin 26), LMH1229 POCI (Pin 28): Peripheral Output, Controller Input
- CS_N (Pin 11): Chip Select (Active Low)
- LMH1239 SCK (Pin 27), LMH1229 SCK (Pin 29): Serial clock (Input to the LMH12x9 Peripheral Device)

The maximum operating speed supported on the SPI bus is 10MHz.

1.3 Register Pages

The LMH12x9 register map is divided into three register pages. These register pages are used to control different aspects of the LMH12x9 functionality. A brief summary of the pages is shown below:

1. **Share Register Page:** This page corresponds to global parameters. This is the default page at device power on. Access this page by setting Reg 0xFF[2:0] = 000’b.
2. **CDR Register Page:** This page corresponds to CDR settings and output interrupt overrides. Access this page by setting Reg 0xFF[2:0] = 100’b.
3. **EQ/Drivers Page:** This page corresponds to equalizer and OUT0±, OUT1±, and SDI_OUT± driver output settings. Access this page by setting Reg 0xFF[2:0] = 101’b.

2 Register Command Syntax

Unless otherwise specified, the settings below apply to both SMBus and SPI register programming. Operations are read-modify-write. This requires that the register is read first and then modified by applying the specific bit mask.

Command Syntax:

RAW	Register Address	Register Content	Register Mask	//Comments

- RAW: This defines a Read/Write command
- Register Address: Specifies the register address in hex format
- Register Content: Specifies the value in hex that is going to be written
- Register Mask: Specifies the bits to be modified within the register content
- // Text comments

Example: RAW 80 01 01 //Enable override

In this command Register 0x80[0] = 1’b. Reg 0x80[7:1] are not modified since mask = 0x01.

RAR	Register Address	Register Content	Register Mask	//Comments

- RAR: This defines a Read-Only command
- Register Address: Specifies the register address in hex format
- Register Content: Specifies the value in hex that is being read
- Defines the mask for register content. For example, 1 in a mask defines bits being read
- // Text comments

Example: RAR 02 10 10 // Read Bit 4 only

In this command, Reg 0x02[4] is read to check if Bit 4 is set.

Important Notes:

- When using SMBus or SPI, the user may need to set override enable bits prior to setting the control bits of the corresponding register.
- TI recommends toggling the ENABLE pin after changing the input data rate
- See Section 4 for further details on register bit definitions.

3 Device Configurations

The following sections provide guidance for programming the LMH12x9 for common applications. Throughout the rest of the document, macro examples are given to set up the device for different configurations and settings.

To clarify terminology of data rates throughout this document, the following terms are considered interchangeable:

Table 3-1. Commonly Used Alternate Terms for Operating SDI Data Rates

OPERATING DATA RATE	COMMONLY USED ALTERNATE TERMS
11.88/11.868Gbps	12G, 12G UHD-SDI
5.94/5.934Gbps	6G, 6G UHD-SDI
2.97/2.967Gbps	3G, 3G HD-SDI
1.485/1.4835Gbps	1.5G, 1.5G HD-SDI
270Mbps	270M, SD

3.1 Common Device Configuration

The LMH12x9 supports SMPTE applications up to 11.88Gbps (12G UHD-SDI). The choice of the input (SDI_IN± or SDI_IN1±, LMH1239 only), output controls, and reclocker enable are determined by the SDI_IN_SEL, SDI_OUT_ENA, OUT0_OUT1_SEL, and OUT_CTRL pins, respectively. A common configuration of the device is outlined in Table 3-2. If access to these pins is not available, the desired device configurations can still be accomplished by register override. Further details about specific configurations are provided in later sections of the programming guide.

Table 3-2. Select SDI_IN± or SDI_IN1± to OUT0± (Retimed Data) and OUT1± (Retimed Data)

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Enable EQ/Drivers Register Page
RAR	08	04	04	//Read back signal detect for SDI_IN±
RAR	08	01	01	//Read back signal detect for SDI_IN1±
RAW	FF	00	07	//Enable Share Register Page
RAW	FE	02	02	//Set IN_MUX_SEL pin override
RAW	FE	00	01	//Assuming signal is present on SDI_IN1±, select SDI_IN1±. To select SDI_IN±, write 0x01 to reg_FE[0]
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	34	40	40	//Enable OUT0± Power Down Override
RAW	34	20	20	//Disable OUT0± channels
RAW	34	00	20	//Enable OUT0± channels
RAW	36	40	40	//Enable OUT1± Power Down Override
RAW	36	20	20	//Disable OUT1± channels
RAW	36	00	20	//Enable OUT1± channels

3.2 Common Register Commands

The following macros specify register settings for common operations.

3.2.1 Channel Control

The control registers in the LMH12x9 are grouped into three pages: the share page, the CDR page and the Cable/EQ Drivers page. The user can access any number of registers in the selected page until a new page is selected by writing a different value to register 0xFF.

Table 3-3. Enable CDR Register Page

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Enable CDR Register Page

Table 3-4. Enable EQ/Driver Register Page

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Enable EQ/Driver Register Page

Note

Share Register 0xFF can be written or read at any time and does not require selection of Share Register bank.

3.2.2 LMH12x9 Resets

To restart the LMH12x9, the user can override the ENABLE pin. The LMH12x9 can be disabled and re-enabled to restart the signal adaptation processes like the cable equalizer value and CDR lock. Additionally, the user can reset the device registers to the factory default values.

3.2.2.1 LMH12x9 ENABLE Pin Override

Using share page 0xFA, the user can override the ENABLE pin to restart the LMH12x9 state machine. The ENABLE pin can be used to force the LMH12x9 into power down. While the ENABLE pin is low, register access remains active. Disabling and re-enabling the device restarts the cable equalizer adaptation process and CDR lock.

Table 3-5. LMH12x9 ENABLE Pin Override

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	00	07	//Enable Share Register Page
RAW	FA	80	80	//Override the ENABLE pin
RAW	FA	00	40	//Disable the device
RAW	FA	40	40	//Enable the device
RAW	FA	00	80	//Disable the ENABLE pin override

3.2.2.2 LMH12x9 Share, CDR, and EQ/Drivers Page Resets

If a soft reset is performed by selecting the *Reset Registers* bit (regardless of the specific register page), users must re-initialize the LMH12x9 in order for the device to function properly. The LMH12x9 uses reserved SMBus accessible memory to control the internal state machine. At power up, this memory is automatically initialized; however, when resetting any register page, the state machine memory requires reinitialization.

Re-initialize the state machine by writing data 0x01 to register 0xE2 in the Share Register Page. Reinitialization of the state machine occurs in less than 100µs (maximum).

Reset and restore default register settings for the Share, the CDR, and the EQ/Drivers register pages:

Table 3-6. LMH12x9 Share, CDR, and EQ/Drivers Page Resets

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	00	07	//Select Share Register Page
RAW	04	40	40	//Reset Share Registers
RAW	FF	04	07	//Select CDR Register Page
RAW	00	04	04	//Reset CDR Registers
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	00	04	04	//Reset EQ/Drivers Registers
RAW	FF	00	07	//Select Share Register Page
RAW	E2	01	01	//Reinitialize internal state machine register settings. Note: 0xE2[0] is not self-clearing. Any write of logic high triggers the initialization.
RAR	E2	10	10	//Poll and wait until 0xE2[4] is set to indicate internal state machine registers are initialized

3.3 IN_MUX_SEL Override

To select SDI_IN± or SDI_IN1±, use the following sequence:

Table 3-7. IN_MUX_SEL Override

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	00	07	//Enable Share Register Page
RAW	FE	02	02	//Enable the IN_MUX_SEL pin override
RAW	FE	00	01	//Assuming signal is present on SDI_IN1±, select SDI_IN1±. To select SDI_IN±, enable 0xFE[0].

3.4 Signal Detect Status for SDI_IN± and SDI_IN1±

The LMH1239 has two inputs, and each input has a signal detector. Based on Signal Detect status and input channel selected, the device automatically goes into power down. For example, if SDI_IN± is selected and there is no signal on SDI_IN1±, the CDR and output drivers go into power down. Note that the unselected input always goes into power down. The following macros checks the status of the signal detects on SDI_IN± or SDI_IN1±.

Table 3-8. Check Signal Detect Status on SDI_IN±

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAR	08	04	04	//Read Signal Detect status of SDI_IN±. A value of 1’b indicates signal present.

Table 3-9. Check Signal Detect Status on SDI_IN1±

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAR	08	01	01	//Read Signal Detect status of SDI_IN1±. A value of 1’b indicates signal present.

3.4.1 Force Signal Detect Power Down

The LMH12x9 automatically powers down when there is a loss of signal (that is, the selected channel Signal Detect is not asserted). When there is an active signal the device can be forced to power down by manually deasserting the Signal Detect on a given input channel.

To force SDI_IN± Signal Detect off:

Table 3-10. Disable Signal Detect for SDI_IN±

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	06	08	08	//Enable Signal Detect power down override for SDI_IN±
RAW	06	00	04	//Force Signal Detect off for SDI_IN±

To force SDI_IN1± Signal Detect off:

Table 3-11. Disable Signal Detect for SDI_IN1±

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	07	08	08	//Enable Signal Detect power down override for SDI_IN1±
RAW	07	00	04	//Force Signal Detect off for SDI_IN1±

3.5 Lock Data Rate Indication

If there is a need to see what data rate the device is locked to read CDR Register Page Reg 0x06 to ensure that the device is locked, then review the VCO divisor setting in CDR Register Page Reg 0x72[6:4] to see the data rate.

Table 3-12. Lock Data Rate Indication

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAR	06	39	3F	//Readback is 0x39h if the CDR is locked and the initial adaptation is complete.
RAR	72	xx	70	//Reg 0x72[6:4] = 3'b000 is 11.88Gbps
				//Reg 0x72[6:4] = 3'b001 is 5.94Gbps
				//Reg 0x72[6:4] = 3'b010 is 2.97Gbps
				//Reg 0x72[6:4] = 3'b011 is 1.485Gbps
				//Reg 0x72[6:4] = 3'b100 is 270Mbps

3.6 CDR Loop Bandwidth Override

The LMH12x9 can be configured to a target CDR loop bandwidth through register control in the CDR page. To optimize jitter between the phase-locked loop (PLL) and voltage-controlled oscillator (VCO) the loop bandwidth can be adjusted over all data rates. TI recommends to leave the CDR loop bandwidth at default for the majority of cases.

Note

An external 470nF loop filter capacitor is needed when LOOP_BW_SEL is R or L.

Table 3-13. Loop Bandwidth Table

DATA RATE (Gbps)	LOOP_BW_SEL	EXTERNAL CAPACITOR	OVERRIDE & REG 0x23[6:7]	TARGET CDR LOOP BW (0.2 UI SINUSOIDAL JITTER)
11.88	H	No	11	7MHz
	F	No	01	7MHz
	R	Yes	10	700kHz
	L	Yes	00	350kHz
5.94	H	No	11	7MHz
	F	No	01	7MHz
	R	Yes	10	600kHz
	L	Yes	00	300kHz
2.97	H	No	11	5MHz
	F	No	01	5MHz
	R	Yes	10	460kHz
	L	Yes	00	230kHz
1.485	H	No	11	3MHz
	F	No	01	3MHz
	R	Yes	10	240kHz
	L	Yes	00	120kHz
0.27	H	No	11	800kHz
	F	No	01	800kHz
	R	Yes	10	50kHz
	L	Yes	00	30kHz

Table 3-14. Override the LOOP_BW_SEL pin

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	24	80	80	//Override Loop_BW_SEL pin.
RAW	23	00	C0	//Set the Loop_BW_SEL in to L mode. **Requires an external 470nF filter capacitor.**
RAW	23	60	C0	//Set the Loop_BW_SEL in to R mode. **Requires an external 470nF filter capacitor.**
RAW	23	80	C0	//Set the Loop_BW_SEL in to F mode
RAW	23	C0	C0	//Set the Loop_BW_SEL in to H mode

3.7 Selective SMPTE Data Rate Lock

By default, the LMH12x9 searches to lock to different data rates starting with 12G, followed by 6G, 3G, HD and ending with SD. To reduce the CDR lock adaptation search time the user can program the LMH12x9 to search within a subset of rates. For example, the user can adjust the starting and ending rates to 6G and HD, respectively, to make the LMH12x9 search to lock starting with 6G, then to 3G, and end with HD.

Note

The start and end rate can be set to the same value.

Table 3-15. Enable Selective SMPTE CDR Data Rate Lock

REGISTER	FUNCTION
Reg 0x7E[7]	Reserved
Reg 0x7E[6:4]	//Reg 0x7E[6:4] = 3'b000 sets the CDR lock search end rate to 11.88Gbps
	//Reg 0x7E[6:4] = 3'b001 sets the CDR lock search end rate to 5.94Gbps
	//Reg 0x7E[6:4] = 3'b010 sets the CDR lock search end rate to 2.97Gbps
	//Reg 0x7E[6:4] = 3'b011 sets the CDR lock search end rate to 1.485Gbps
	//Reg 0x7E[6:4] = 3'b100 sets the CDR lock search end rate to 270Mbps
Reg 0x7E[3]	Reserved
Reg 0x7E[2:0]	//Reg 0x7E[2:0] = 3'b000 sets the CDR lock search start rate to 11.88Gbps
	//Reg 0x7E[2:0] = 3'b001 sets the CDR lock search start rate to 5.94Gbps
	//Reg 0x7E[2:0] = 3'b010 sets the CDR lock search start rate to 2.97Gbps
	//Reg 0x7E[2:0] = 3'b011 sets the CDR lock search start rate to 1.485Gbps
	//Reg 0x7E[2:0] = 3'b100 sets the CDR lock search start rate to 270Mbps

For example, the user can set the starting rate for the search to 12G and the ending rate to 270M (default setting).

Table 3-16. Search All Data Rates

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	7E	00	07	//Coarse EQ search start rate is 12G
RAW	7E	40	70	//Coarse EQ search end rate is 270M
				//Toggle the ENABLE pin

Alternatively, the user can restrict the data rate search.

Table 3-17. Restrict the Data Rate Search

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	7E	02	07	//Coarse EQ search start rate is 3G
RAW	7E	40	70	//Coarse EQ search end rate is 270M
				//Toggle the ENABLE pin

3.7.1 Digital Mute Reference Threshold

In some applications, users may want to limit the length of cable to equalize. This is accomplished by the mute reference threshold. If the cable EQ index exceeds the mute reference threshold by two the LMH12x9 automatically mutes OUT0/OUT1.

Table 3-18. Disable Mute Reference

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	30	3F	3F	//Set the MUTERef value to 0x3F. 0x3F is the maximum possible coarse EQ adaptation value, therefore the output never auto-mutes

Table 3-19. Enable Mute Reference

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	30	00	3F	//Set the MUTERef value to 0x00. An adapted CTLE index of 2h or greater mutes OUT0 and OUT1

3.7.2 CTLE Index Check and Manual CTLE Override

There is a register than can be read to determine the adapted CTLE index for a given input cable length.

Table 3-20. Check the CTLE Index

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAR	9C	xx	3F	//Read back of final CTLE index from adaptive cable EQ

In cases where the user is sending non-SMPTE data rates, like 125Mbps MADI, the user can manually set the CTLE index. The steps required to perform this operation are listed below.

Table 3-21. Override the CTLE Index

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAR	9C	3F	3F	//Read back of final CTLE index from adaptive cable EQ
RAW	16	80	80	//Enable manual CTLE index selection
RAW	16	00	7F	//Set the CTLE index to the minimum value
RAW	16	37	7F	//Set the CTLE index to the maximum value

Note

If there is no signal at the selected input, the LMH12x9 auto-mutes.

3.8 Eye Opening Monitoring Operation

The LMH12x9 has an on-chip eye opening monitor (EOM) which can be used to analyze, monitor, and diagnose the performance of the link. The EOM operates on the post-equalized waveform, just prior to the reclocker. Therefore, the EOM captures the effects of all the equalization circuits within the receiver.

The EOM monitors the post-equalized waveform in a time window that spans one unit interval and a configurable voltage range that spans up to ±400mV. The time window and voltage range are divided into 64 steps, so the result of the eye capture is a 64 × 64 matrix of *hits*, where each point represents a specific voltage and phase offset relative to the main data sampler. The number of *hits* registered at each point needs to be put into context with the total number of bits observed at that voltage and phase offset to determine the corresponding probability for that point.

3.8.1 Fast EOM

Fast EOM is a mechanism that provides an option to read out the EOM through SPI or SMBus interfaces by reading the hits observed for each point in the 64 × 64 points matrix. The SPI operates at a faster clock rate than a SMBus interface, therefore a SPI controller must wait until the EOM start bit, register 0x67[0], goes low. This bit indicates that EOM samples are available, and the SPI controller can proceed to read register 0x68 and 0x69. For more information on how to build an eye diagram from raw data captured in the Fast EOM procedure, review some of our TI content on the EOM.

3.8.1.1 Fast EOM Operation

The following steps use Fast EOM to perform an eye capture for the 64 × 64 matrix.

Table 3-22. Eye Opening Monitor (EOM)

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	00	FF	//Select Share Register Page
RAW	0B	02	02	//Force enable VCO clock to enable EOM counting
RAW	FF	04	FF	//Select CDR Register Page
RAW	64	00	80	//Sets EOM Power Down to 0
RAW	65	40	40	//Enables Fast EOM
RAW	67	01	01	//Self-clearing bit to start EOM
RAR	67	00	01	//Wait for 0x67[0] to clear to 0
RAW	64	00	40	//Scale EOM range - Custom Scaling
RAW	64	30	30	//12.5mV step plots 800mVpp sets 0x64[4:5] to 11
RAR	68/69	xx	00	//Read Reg 0x68 then 0x69 and discard contents
RAR	68/69	xx	00	//Read Reg 0x68 then 0x69 and discard contents
RAR	68	xx	FF	//Read MSBs of cell and save number of eye hits
RAR	69	xx	FF	//Read LSBs of cell and save number of eye hits
				//Execute the above two commands for 4095 more times (total 4096 cells)
RAW	64	80	80	//Power down EOM

3.8.2 Read Horizontal and Vertical Eye Opening

A common measurement performed by the EOM is the horizontal and vertical eye opening. The Horizontal Eye Opening (HEO) represents the width of the post-equalized eye at the zero-crossing, typically measured in unit intervals or picoseconds (ps). The Vertical Eye Opening (VEO) represents the height of the post-equalized eye, measured midway between the mean zero crossing of the eye. This position in time approximates that of the CDR sampling phase.

The LMH12x9 produces two readings to indicate line signal quality. These parameters can be read by the host processor, or the LMH12x9 can be optioned to cause an interrupt if HEO/VEO reaches a predetermined threshold. See the equation below to convert the HEO reading to UI (Unit Interval) eye opening.

$$\text{HEO} = (\text{Decimal Reg 0x6A}) / 64 \quad (1)$$

For example, if the HEO reading is 0x31 (49 decimal), then the HEO UI eye opening is 49/64 = 0.77 UI. This means the HEO is about 77% open.

Similarly, VEO has 64 steps as well. The chip automatically covers ±400mV thus, each step is 800/64, or 12.5mV. See the equation below to convert the VEO reading to a voltage measurement.

$$\text{VEO inmV} = (\text{Decimal Reg 0x6B}) \times 12.5 \quad (2)$$

For example, if we read 0x50 (32 decimal) for the VEO reading, this corresponds to 32 × 12.5mV = 800mV vertical eye opening.

Table 3-23. Horizontal and Vertical Eye Opening (HEO and VEO)

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	00	07	//Select Share Register Page
RAW	0B	02	02	//Force enable VCO clock to enable EOM counting
RAW	FF	04	07	//Select CDR Register Page
RAW	64	00	80	//Sets EOM power down to low, enabling EOM
RAW	64	00	40	//Scale EOM range - Custom scaling
RAW	64	30	30	//12.5mV step
RAW	65	00	40	//Disables Fast EOM
RAW	67	02	02	//Enable eom_get_heo_veo to start HEO/VEO capture
RAW	FF	00	80	//Select Share Register Page
RAW	0B	00	02	//Force disable VCO clock to disable EOM counting
RAW	FF	04	07	//Select CDR Register Page
RAW	64	80	80	//Power down EOM capture
RAR	6A	FF	FF	//Read 8 bits of HEO
RAR	6B	FF	FF	//Read 8 bits of VEO
RAR	67	18	18	//Read Reg 0x67[4:3] for vrange setting

3.9 SDI_OUT±, OUT0± and OUT1± Default Mode of Operation

By default, the OUT_CTRL pin (Pin 19) controls the OUT0±/SDI_OUT± and OUT1± mode behavior. To override this pin set the following register configuration.

Table 3-24. Override OUT_CTRL

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	53	40	40	//Override OUT_CTRL pin. Output modes determined by register control.

When 0x53[6] is '1', 0x53[5:4] overwrites the selection from the OUT_CTRL pin.

Table 3-25. OUT_CTRL Settings

REG 0x53[5:4]	OUT0±, SDIOUT±	OUT1±
00	Cable EQ (CTLE, DFE) enabled and reclocker bypassed.	Cable EQ (CTLE, DFE) enabled and reclocker bypassed.
01	Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled	Full-Rate Recovered Clock if Data Rate ≤ 2.97Gbps. 297MHz Recovered Clock if Data Rate > 2.97Gbps
10	Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled	Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled
11	Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled	Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled

The following example can be used as a template to set the OUT0±/SDI_OUT± and OUT1± configuration:

Table 3-26. Override OUT_CTRL Settings

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	53	40	40	//Override OUT_CTRL pin. Output modes determined by register control.
RAW	53	00	30	//L mode: Enable Bypass, Debug Only. OUT0, SDI_OUT, and OUT1: Equalized Data, Cable EQ (CTLE, DFE) enabled and reclocker bypassed
RAW	53	10	30	//R mode: Enable OUT0 and SDI_OUT: Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled OUT1: Full-Rate Recovered Clock if Data Rate ≤ 2.97Gbps. 297MHz Recovered Clock if Data Rate > 2.97Gbps
RAW	53	20	30	//F mode: Enable Normal operation OUT0, SDI_OUT, and OUT1: Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled
RAW	53	30	30	//H mode: Enable Normal operation OUT0, SDI_OUT, and OUT1: Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled

3.9.1 SDI_OUT±, OUT0± and OUT1± Independent Control

The LMH12x9 allows independent control of SDI_OUT±, OUT0± and OUT1±. The possible outputs are 10MHz clock for all three outputs, this requires an override in the share page to select 10MHz clock as an output, raw data, reclocked data, and mute. See the register writes below and the LMH1239EVM GUI for a simpler way of configuring the outputs.

To output a 10MHz clock, the LMH12x9 Signal Detect must detect an active signal at the selected input.

Table 3-27. SDI_OUT± 10MHz Clock

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	00	07	//Select Share Register Page
RAW	0C	80	80	//Selects 10MHz clock on outputs as opposed to VCO/40 rate clock
RAW	FF	04	07	//Select CDR Register Page
RAW	53	62	72	//Enable Independent Output Control Override and ensure that CDR and EQ blocks operate normally
RAW	54	02	03	//Enable 10MHz clock output on SDI_OUT±

Table 3-28. SDI_OUT± Raw Data

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	53	62	72	//Enable Independent Output Control Override and ensure that CDR and EQ blocks operate normally
RAW	54	00	03	//Output Raw data (EQ only) on SDI_OUT±

Table 3-29. SDI_OUT± Reclocked Data

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	53	62	72	//Enable Independent Output Control Override and ensure that CDR and EQ blocks operate normally
RAW	54	01	03	//Output reclocked data on SDI_OUT± (valid only in locked condition)

Table 3-30. OUT0± Raw Data

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	53	62	72	//Enable Independent Output Control Override and ensure that CDR and EQ blocks operate normally
RAW	54	00	E0	//Output raw data (EQ only) on OUT0±

Table 3-31. OUT0± Mute

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	53	62	72	//Enable Independent Output Control Override and ensure that CDR and EQ blocks operate normally
RAW	54	E0	E0	//Mute OUT0±

Table 3-32. OUT0± Reclocked Data

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	53	02	02	//Enable Independent Output Control Override
RAW	54	20	E0	//Output reclocked data on OUT0± (valid only in locked condition)

To output a 10MHz clock, the LMH12x9 Signal Detect must detect an active signal at the selected input. However, the LMH12x9 does not need to be locked. SDI_OUT± does *not* need to output a 10MHz clock for OUT0± to output a 10MHz clock. To set the independent output control settings for OUT1±, see the register map and EVM GUI.

Table 3-33. OUT0± 10MHz Clock

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	00	07	//Select Share Register Page
RAW	0C	80	80	//Selects 10MHz clock on outputs as opposed to VCO/40 rate clock
RAW	FF	04	07	//Select CDR Register Page
RAW	53	62	72	//Enable Independent Output Control Override and ensure that CDR and EQ blocks operate normally
RAW	54	A0	E0	//Output 10MHz on OUT0±

3.10 Invert OUT0±, OUT1±, and SDI_OUT± Data Polarity

For ease of layout convenience, all outputs can be inverted.

Table 3-34. OUT0± Polarity Inversion

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	34	80	80	//Invert OUT0± driver polarity

Table 3-35. OUT1± Polarity Inversion

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	36	80	80	//Invert OUT1± driver polarity

Table 3-36. SDI_OUT± Polarity Inversion

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	3F	01	01	//Invert SDI_OUT± driver polarity

3.11 OUT0±, OUT1±, and SDI_OUT± Driver Settings

The LMH12x9 has programmable output driver settings for OUT0±, OUT1±, and SDI_OUT±. Register control can be used to set the VOD (Voltage Output Differential) and power down the outputs.

3.11.1 OUT0± and OUT1± VOD Settings

The OUT0± and OUT1± 100Ω driver has programmable peak-to-peak settings ranging from 410mVpp to 810mVpp. In default mode, the output voltage setting is determined by the VOD_DE pin. Overriding this pin setting enables register control of the output VOD settings.

Table 3-37. OUT0± VOD Settings

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	33	08	08	//Override VOD pin for OUT0±
RAW	33	00	07	//Set output VOD to 000’b (410mVpp typical)
RAW	33	02	07	//Set output VOD to 010’b (560mVpp typical)
RAW	33	04	07	//Set output VOD to 100’b (635mVpp typical)
RAW	33	06	07	//Set output VOD to 110’b (810mVpp typical)

Table 3-38. OUT1± VOD Settings

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	35	08	08	//Override VOD pin for OUT1±
RAW	35	00	07	//Set output VOD to 000’b (410mVpp typical)
RAW	35	02	07	//Set output VOD to 010’b (560mVpp typical)
RAW	35	04	07	//Set output VOD to 100’b (635mVpp typical)
RAW	35	06	07	//Set output VOD to 110’b (810mVpp typical)

3.11.2 OUT0± and OUT1± De-Emphasis Settings

The LMH12x9 features the ability to provide Tx equalization de-emphasis for OUT0± and OUT1±. By default, de-emphasis values for OUT0± and OUT1± are applied depending on the VOD_DE pin setting.

The default de-emphasis settings can be overridden by register control.

Table 3-39. OUT0± and OUT1± De-Emphasis Settings

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	34	10	10	//Override de-emphasis control from VOD_DEM_SEL pin for OUT0±
RAW	34	00	07	//OUT0 de-emphasis setting set to 0.0dB
RAW	34	02	07	//OUT0 de-emphasis setting set to –1.0dB
RAW	34	04	04	//OUT0 de-emphasis setting set to –2.4dB
RAW	34	06	06	//OUT0 de-emphasis setting set to –6.1dB
RAW	36	10	10	//Override de-emphasis control from VOD_DEM_SEL pin for OUT1±
RAW	36	00	07	//OUT1± de-emphasis setting set to 0.0dB
RAW	36	02	07	//OUT1± de-emphasis setting set to –1.0dB
RAW	36	04	04	//OUT1± de-emphasis setting set to –2.4dB
RAW	36	06	06	//OUT1± de-emphasis setting set to –6.1dB

3.11.3 SDI_OUT± VOD Settings

The SDI_OUT± 75Ω driver has a programmable peak-to-peak voltage setting ranging from 720mVp-p to 880mVp-p. By default, the baseline VOD amplitude is determined by register control, and the outputs are also changed in steps of ±5% or +10% depending on the SDI_VOD pin setting. Figure 3-1 illustrates the control logic for SDI_OUT VOD settings.

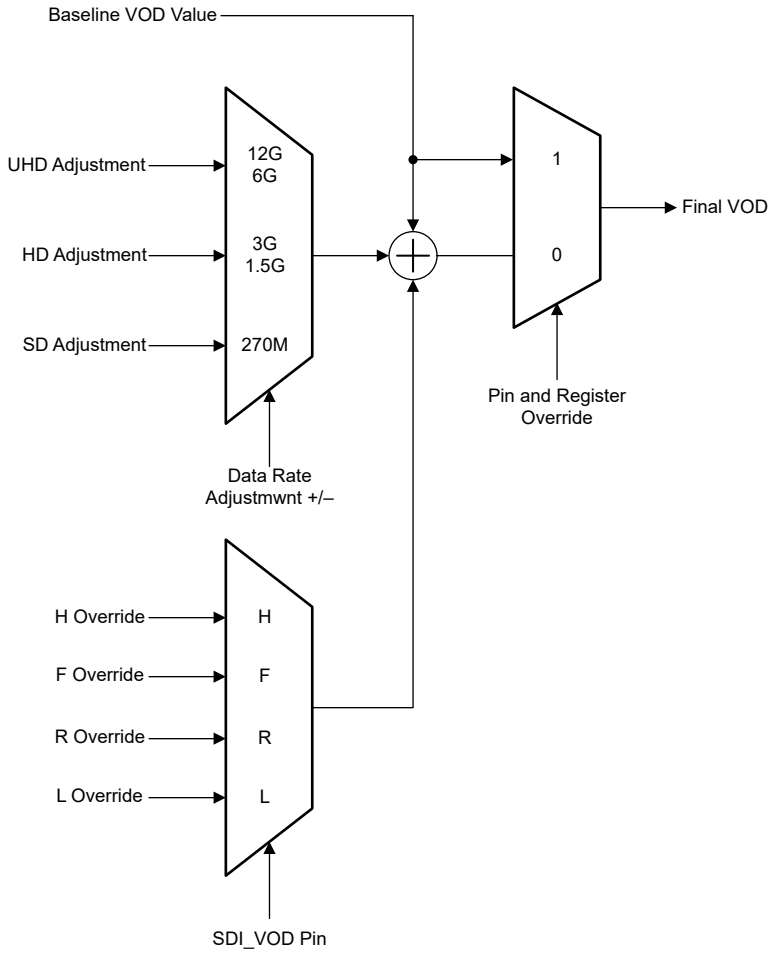

Figure 3-1. SDI VOD Amplitude Control Logic Block Diagram

To apply a baseline increase in SDI_OUT± VOD, the user can override the SDI_VOD pin and apply VOD decreases down to –5% of nominal and up to +10% of nominal VOD.

Table 3-40. SDI_OUT± VOD Settings

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	00	07	//Select Share Register Page
RAW	FA	20	20	//Override SDI_VOD pin setting for SDI_OUT±.
RAW	FA	18	18	//Set baseline SDI_OUT± output VOD to about +5% of nominal.
RAW	FA	10	18	//Set baseline SDI_OUT± output VOD to about 800mVpp (nominal).
RAW	FA	08	18	//Set baseline SDI_OUT± output VOD to about +10% of nominal.
RAW	FA	00	18	//Set baseline SDI_OUT± output VOD to about –5% of nominal.

The VOD adjustment knobs are used to increase or decrease the baseline VOD of the LMH12x9 on a rate dependent basis. The rates and associated VOD registers are: UHD (11.88Gbps and 5.94Gbps) adjusted with EQ/Drivers register 0x3A, HD (2.97Gbps and 1.485Gbps) with EQ/Drivers register 0x3B, and SD (270Mbps) with EQ/Drivers register 0x3C.

Table 3-41. Data Rate Dependent VOD Adjustment

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAR	3A	xx	1F	//Read and store the VOD adjustment value for UHD
RAW	3A	00	20	//Set addition to (+) VOD when 0x3A[5] = 0 or subtraction from (-) VOD 0x3A[5] = 1
RAW	3A	xx	1F	//Each unit increase of 0x3A[4:0] from the default value corresponds to a 6mV change in VOD from the baseline

Note

The LMH12x9 is optimized such that the default baseline VOD amplitude is nominally 800mVp-p. Each one-step increment or decrement corresponds to approximately 4mV to 6mV per step.

3.11.4 SDI_OUT± Pre-Emphasis

By default, pre-emphasis values are applied to the SDI outputs according to the detected data rate by the integrated reclocker. The pre-emphasis value is determined in the EQ/Drivers page register 0x3F[6:5]. The user can set the pre-emphasis value for both UHD and HD data rates by enabling 0x3F[7]. Alternatively, the user can set the pre-emphasis on a rate dependent basis by enabling either 0x3F[4] for UHD or enabling 0x3F[3] for HD, while 0x3F[7] is 0.

Table 3-42. SDI_OUT± Pre-Emphasis

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Registers Page
RAW	3F	80	80	//Enable pre-emphasis for UHD and HD data rates
RAW	3F	xx	60	//Choice of the pre-emphasis value
RAW	3F	08	08	//Enable pre-emphasis for HD
RAW	3F	10	10	//Enable pre-emphasis for UHD

3.11.5 Output Driver Power Down

The LMH12x9 OUT0±, OUT1±, and SDI_OUT± current mode outputs draw high current when operational. These outputs can be powered down to save energy when unused.

OUT0± can be powered down by overriding the OUT0_SEL pin in register control.

Table 3-43. OUT0± Power Down

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	34	40	40	//Override OUT0± power down control
RAW	34	20	20	//Force power down OUT0±

OUT1± can be powered down by overriding the OUT0_SEL pin in register control.

Table 3-44. OUT1± Power Down

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	36	40	40	//Override OUT1± power down control

Table 3-44. OUT1± Power Down (continued)

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	36	20	20	//Force power down OUT1±

Table 3-45. SDI_OUT± Power Down

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select Share Register Page
RAW	38	80	80	//Override SDI_OUT± power down control
RAW	38	40	40	//Force power down SDI_OUT±

3.11.6 Cable Fault Detection (CFD)

The Cable Fault Detection (CFD) state machine can be used to verify if SDI_OUT+ is open (fault) or terminated by 75Ω. When CFD is started, EQ/Drivers register 0xAC[3] is asserted if the cable is terminated and deasserted otherwise.

Table 3-46. Cable Termination Detection Procedure

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	A8	00	80	//Disable the CFD bypass
RAW	A8	00	20	//Ensure that CFD is not disabled
RAW	A8	40	40	//Start cable fault detection (CFD)
RAR	AC	08	08	//0xAC[3]= 0 - SDI_OUT+ is open, 0xAC[3] = 1 - SDI_OUT+ is terminated 75Ω

Additionally, the CFD state machine can be utilized to estimate the length of cable at the unterminated output of SDI_OUT+. After verifying that the cable length is open (0xAC[3] = 0) it is possible to calculate the unterminated cable length with the following equation:

$$\frac{\text{Decimal}[(\text{AC}[2:0]'\text{b}\quad \text{MSB})\quad (\text{AD}[7:0]'\text{b}\quad \text{LSB})]}{0.75} = \text{Typical}\quad \text{B1694A}\quad \text{cable}\quad \text{length}\quad \left(\text{m}\right) \tag{3}$$

Note

0xAC[2:0] and AD[7:0] makes up an 11-bit binary value and the denominator changes based on the cable type or insertion loss.

Table 3-47. Cable Fault Detection Procedure

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	A8	40	40	//Start cable fault detection (CFD)
RAR	AC	xx	0F	//Read SDI_OUT+ cable length MSB from bits [2:0] of 0xAC. Also, 0xAC[3] =0
RAR	AD	xx	FF	//Read SDI_OUT+ cable length LSB from bits [7:0] of 0xAD

3.12 LOCK_N Pin Output Settings

All outputs on the LOCK_N pin are active low.

Table 3-48. Lock Status From Reclocker or Cable EQ Adaption Status

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	06	00	C0	//Set the LOCK_N pin to output the CDR lock status
RAW	06	80	C0	//Set LOCK_N pin to output cable EQ adaptation status
RAW	06	C0	C0	//Set LOCK_N pin to output cable EQ adaptation status AND the status of the lock monitor

3.12.1 Interrupt Outputs Programmed by Interrupt Registers

The following example enables all possible interrupts as outputs for the LOCK_N pin. The interrupts are treated as a logical OR function, so if at least one interrupt occurs, the LOCK_N pin asserts low.

Table 3-49. Interrupt Outputs Programmed by Interrupt Registers

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	30	30	//Interrupts are output on LOCK_N pin, determined by register settings
RAW	FF	04	07	//Select CDR Register Page
RAW	7F	40	40	//Enable interrupt if CDR lock is achieved
RAW	7F	20	20	//Enable interrupt if SDI_IN1± Signal Detect is asserted
RAW	7F	10	10	//Enable interrupt if SDI_IN± Signal Detect is asserted
RAW	7F	08	08	//Enable interrupt when SDI-OUT+ detects a termination
RAW	7F	04	04	//Enable interrupt if CDR loses lock
RAW	7F	02	02	//Enable interrupt if there is loss of signal (LOS) on SDI_IN1±
RAW	7F	01	01	//Enable interrupt if there is loss of signal (LOS) on SDI_IN±

Note

Interrupts are sticky bits. To clear the interrupt and thereby clear the LOCK_N pin, the user must read the corresponding bit in CDR Register Page Reg 0x7E. For example, if Reg 0x7F[6] = 1 to enable an interrupt for CDR lock, the interrupt remains asserted until Reg 0x7E[6] is read to clear the interrupt.

Table 3-50. Interrupt Outputs Programmed by Interrupt Registers

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAR	7E	40	40	//Read interrupt if CDR lock is achieved
RAR	7E	20	20	//Read interrupt if SDI_IN1± Signal Detect is asserted
RAR	7E	10	10	//Read interrupt if SDI_IN1± Signal Detect is asserted
RAR	7E	08	08	//Read interrupt when SDI-OUT+ detects a termination
RAR	7E	04	04	//Read interrupt if CDR loses lock
RAR	7E	02	02	//Read interrupt if there is loss of signal (LOS) on SDI_IN1±
RAR	7E	01	01	//Read interrupt if there is loss of signal (LOS) on SDI_IN±

3.13 PRBS Generator and Checker

The LMH12x9 can be configured to output PRBS-7, PRBS-9, PRBS-23 and PRBS-31. Based on the PRBS polynomial and polarity selected, data is generated after loading the initial seed. The 32-bit data generated is read by the serializer clock. The pattern can be output to SDI_OUT±, OUT0± and/or OUT1±.

Table 3-51. PRBS Generator

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	2C	80	C0	//Enable the VCO by enabling the VCO_PD override and writing 0 to VCO_PD
RAW	45	88	CE	//Enable PFD
RAW	41	80	C0	//Enable Deserializer
RAW	3F	00	20	//Enable PDIQ
RAW	3F	00	07	//Select VCO Scalar Divider
				//Reg0x3F[2:0] = 3'b000 Full-Rate
				//Reg0x3F[2:0] = 3'b001 Divide-by-2
				//Reg0x3F[2:0] = 3'b010 Divide-by-4
				//Reg0x3F[2:0] = 3'b011 Divide-by-8
				//Reg0x3F[2:0] = 3'b100 Divide-by-40
RAW	3F	08	08	//Enable PDIQ Override
RAW	3F	48	48	//Enable PDIQ PD Override
RAW	54	80	E0	//Reg0x54[7:5] = 3'b100 PRBS data on OUT0
		10	1C	//Reg0x54[4:2] = 3'b100 PRBS data on OUT1
		03	03	//Reg0x54[1:0] = 2'b11 PRBS data on SDI_OUT
RAW	53	02	02	//Override the independent output control
RAW	40	20	20	//Enable Serializer
RAW	82	40	40	//Allow serializer clock to drive PRBS-core
RAW	FF	05	07	//Select EQ/Drivers Register Page
RAW	34	40	40	//Disable ability to power down TX0
RAW	36	40	40	//Disable ability to power down TX1
RAW	38	80	80	//Disable ability to power down SDI_OUT±
RAW	FF	00	07	//Select SHARE Register Page
RAW	0C	04	04	//Hold serializer clock in reset state
RAW	0B	04	04	//Enable Serializer Clock
RAW	0C	00	04	//Bring serializer clock out of reset state
RAW	FF	04	07	//Select CDR Register Page
RAW	79	00	30	//Reg0x79[5:4] = 2'b00 PRBS7
		10	30	//Reg0x79[5:4] = 2'b01 PRBS9
		20	30	//Reg0x79[5:4] = 2'b10 PRBS23
		30	30	//Reg0x79[5:4] = 2'b11 PRBS31
RAW	7A	00	01	//Force no polarity inversion on gen data
RAW	79	02	02	//Make the logic as PRBS generator
RAW	79	01	01	//Enable PRBS functionality

Table 3-51. PRBS Generator (continued)

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	00	07	//Select SHARE Register Page
RAW	FE	08	0C	//Overrides for OUT0±

When the LMH12x9 is programmed in generator mode the device can generate error-free PRBS. It is possible to inject one bit of error to the generated data by flipping one of the bits in the generated data. The user can assign the error to one of the 32 bits by setting the self clearing inject-bit. After this action, the output data carries one bit error.

Table 3-52. Bit Error Injection

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	82	xx	1F	//0x82[4:0] = 5'bxxxxx Select 32-bit address for single-bit error injection
RAW	82	20	20	//Trigger the PRBS generator to inject just one bit of error in the generated data stream. Self-clearing.

If the module is set to check PRBS, the incoming deserializer data is first loaded to the device as a seed. Based on the PRBS polynomial and polarity *selected by the state machine*, the device generates a new value, and this value is compared against *the deserializer data in the next data clock cycle.* This process repeats for 64 clock cycles and if the data from device matches the deserializer data in *all 64 clock cycles,* the state machine (SM) declares a *PRBS-lock*, which means the SM finds a matching PRBS polynomial in the incoming data. Otherwise, the SM switch to test the opposite polarity, and then another polynomial. This process repeats until the SM finds a PRBS lock. However, if the incoming signal does not match any of the supported PRBS polynomial, this process goes on forever.

Table 3-53. PRBS Checker

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	40	20	20	//Initialize clock signals for PRBS checking
RAW	82	40	40	//Initialize clock signals for PRBS checking
RAW	82	00	40	//Initialize clock signals for PRBS checking
RAW	40	00	20	//Initialize clock signals for PRBS checking
RAW	8B	00	80	///Turn off power cycling
RAW	82	80	80	//Allow deserializer clock to drive PRBS-core
RAW	79	04	04	//Make the logic as PRBS Checker
RAW	79	10	10	//Enable PRBS functionality
RAR	73		0F	//Read PRBS_PATT_DET to detect which PRBS is being provided
				//Reg 0x73[3:0] = 4'b1000 PRBS-31 Detected
				//Reg 0x73[3:0] = 4'b0100 PRBS-23 Detected
				//Reg 0x73[3:0] = 4'b0010 PRBS-9 Detected
				//Reg 0x73[3:0] = 4'b0001 PRBS-7 Detected
RAR	74		07	//Read upper three bits of eleven-bit wide error sum. Maximum 2047 total errors.
				//Reg0x74[2:0] = 3'bxxx
RAR	75		FF	//Read lower eight bits of eleven-bit wide error sum
				//Reg0x75[7:0] = 8'bxxxxxxxx

3.14 CDR Lock Timing Control

The CDR page register 0x89 can be used to delay the onset of CDR lock after signal detect is asserted for SDI_IN or SDI_IN1. This functionality is especially useful when the incoming signal is initially unstable and requires a few milliseconds to stabilize.

Table 3-54. CDR Lock Delay

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	89	18	18	//Set the delay to 4ms
RAW	89	10	18	//Set the delay to 2ms
RAW	89	08	18	//Set the delay to 1ms
RAW	89	00	18	//Set the delay to 0ms

3.14.1 Watchdog Timer

Additionally, when CDR page_0x89[7] is asserted, a watchdog timer is implemented to extend the device lock time before entering CDR bypass mode. The value of the CDR page 0x89[6:5] determines the length of the timer in ms. When this timer expires twice, the LMH12x9 enters CDR bypass mode.

Table 3-55. Enable CDR Relock Attempts

COMMAND	REGISTER	VALUE	MASK	//COMMENTS
RAW	FF	04	07	//Select CDR Register Page
RAW	89	xx	60	//Timer value for the CDR relock functionality 2'd0: 32ms 2'd1: 36ms 2'd2: 44ms 2'd3: 60ms
RAW	89	80	80	//Enable timer to restart the CDR without enabling bypass

4 Register Maps

The LMH1239 register set is divided into three register pages: Share Register Page, CDR Register Page, and EQ/Drivers Register Page.

The register maps given in Section 4.1, Section 4.2, and Section 4.3 provide the following information:

- 8-bit register address, in hexadecimal format
- Bit positions within each register
- Field name to identify the register function
- Default register value on power up, in hexadecimal format
- Type for each bit:
  - R = Read-only
  - RW = Read/Write
  - RW1C = Read/Write 1 to clear
- Description of bit(s) functionality
  - Bit value notation in decimal and binary (For example: 3'd3 == 3'b011)

Please note the following about the LMH1239 default register values in the register map:

- Default register values were read after power-up with no active inputs applied to SDI_IN or SDI_IN1.
- Default register values for Reserved *Read-Only* bits can vary from part to part

4.1 Share Registers

Table 4-1 lists the memory-mapped registers for the Share registers. All register offset addresses not listed in Table 4-1 should be considered as reserved locations and the register contents should not be modified.

Table 4-1. SHARE Registers

Offset	Acronym	Register Name	Section
4h	Reset_Share	RST_SHR	Section 4.1.1
Bh	VCO_Clock_Divider	VCO_DIV	Section 4.1.2
Ch	Clock_Control	CLK_CTRL	Section 4.1.3
E2h	Reset_Channel	CH_RST	Section 4.1.4
FAh	Transmitter_VOD_Control	TX_VOD	Section 4.1.5
FEh	Input_Mux_Selection	IN_MUX	Section 4.1.6
FFh	Channel_Selection	CH_SEL4	Section 4.1.7

Complex bit access types are encoded to fit into small table cells. Table 4-2 shows the codes that are used for access types in this section.

Table 4-2. Share Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

4.1.1 Reset_Share Register (Offset = 4h) [Reset = 05h]

Reset_Share is shown in Table 4-3.

Return to the Summary Table.

This register is to reset the Share page registers.

Table 4-3. Reset_Share Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	rst_i2c_regs	R/W1C	0h	Reset Shared registers. Self-cleared after by the action of reset
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	1h	
1	RESERVED	R	0h	
0	RESERVED	R	1h	

4.1.2 VCO_Clock_Divider Register (Offset = Bh) [Reset = 00h]

VCO_Clock_Divider is shown in Table 4-4.

Return to the Summary Table.

This register is to force enable the VCO clock divider.

Table 4-4. VCO_Clock_Divider Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	clk_vco_en	R/W	0h	Force-ENABLE the VCO-DIV clock when set to 1, overriding the state machine control
0	RESERVED	R	0h	

4.1.3 Clock_Control Register (Offset = Ch) [Reset = 00h]

Clock_Control is shown in Table 4-5.

Return to the Summary Table.

This register is used to select the output as a 10 MHz or a VCO divided by 40 clock (VCO/40) depending on the value in ana_reset_control bit 2. See Output_Selection for output control.

Table 4-5. Clock_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	out_pfd_mux_clk_sel	R/W	0h	Selects which clock goes to OUT0 or OUT1 when the corresponding PFD mux selection is made: 1'b0 = VCO divided by 40 clock from analog, unfiltered 1'b1 = 10MHz clock
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.1.4 Reset_Channel Register (Offset = E2h) [Reset = 00h]

Reset_Channel is shown in Table 4-6.

Return to the Summary Table.

This register is used to reinitialize the default register values from the internal state machine.

Table 4-6. Reset_Channel Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	reset_done	R	0h	1'b0 = Internal state machine register initialization not done 1'b1 = Internal state machine register initialization done
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	

Table 4-6. Reset_Channel Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	reset_init	R/W	0h	1'b1 = Initialize internal state machine register settings

4.1.5 Transmitter_VOD_Control Register (Offset = FAh) [Reset = 00h]

Transmitter_VOD_Control is shown in Table 4-7.

Return to the Summary Table.

This register is the override for the ENABLE and SDI_VOD pins.

Table 4-7. Transmitter_VOD_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	mr_enable_ov_en	R/W	0h	When 1, the ENABLE pin is overridden by mr_enable_ov
6	mr_enable_ov	R/W	0h	Override for ENABLE pin when mr_enable_ov_en is 1
5	sdi_vod_ov_en	R/W	0h	When 1, SDI_VOD is configured by mr_sdi_vod[1] and mr_sdi_vod[0] in Share reg_FAh. Replacing the pin SDI_VOD
4	mr_sdi_vod_1	R/W	0h	Replace the setting from the pin SDI_VOD when sdi_vod_ov_en is 1: 2'b00 = about –5% of nominal 2'b01 = about +10% of nominal 2'b10 = 800mVpp (nominal) 2'b11 = about +5% of nominal
3	mr_sdi_vod_0	R/W	0h	see MSB
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.1.6 Input_Mux_Selection Register (Offset = FEh) [Reset = 00h]

Input_Mux_Selection is shown in Table 4-8.

Return to the Summary Table.

This register is for overriding IN_MUX_SEL.

Table 4-8. Input_Mux_Selection Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	in_mux_sel_ov	R/W	0h	Override for IN_MUX_SEL (LMH1239 only)
0	in_mux_sel	R/W	0h	1'b1 = SDI_IN is selected 1'b0 = SDI_IN1 is selected

4.1.7 Channel_Selection Register (Offset = FFh) [Reset = 00h]

Channel_Selection is shown in Table 4-9.

Return to the Summary Table.

This register is for channel selection and LOCK_N pin output control.

Table 4-9. Channel_Selection Register Field Descriptions

Bit	Field	Type	Reset	Description
7	lock_output_ctrl_1	R/W	0h	Controls the output on LOCK_N pin if Reg 0xFF[5:4] = 2'b01: 2'b00 = Lock status from reclocker (defined by cdr_reg_06h[7:6]) 2'b01 = Equalizer adaptation is complete 2'b10 = Logical OR of lock status from reclocker and equalizer adaptation completion 2'b11 = Logical AND of lock status from reclocker and equalizer adaptation completion
6	lock_output_ctrl_0	R/W	0h	See MSB
5	los_int_bus_sel_1	R/W	0h	Controls the output on LOCK_N pin: 2'b00 = Default behavior (LOCK_N outputs lock status from reclocker) 2'b01 = LOCK_N pin output status is determined by reg_FF[7:6] 2'b10 = LOS of selected input 2'b11 = Interrupts are output on LOCK_N pin
4	los_int_bus_sel_0	R/W	0h	See MSB
3	RESERVED	R	0h	
2	en_ch_SMB	R/W	0h	1'b1 = Enables SMBUS access to one of the channels specified in regFF[1:0] 1'b0 = Share page registers are enabled.
1	ensmb_ch_1	R/W	0h	ensmb[1:0] 2'b00 = CDR Register Page 2'b01 = CTLE Register Page Other values are invalid.
0	ensmb_ch_0	R/W	0h	See MSB

4.2 CDR Registers

Table 4-10 lists the memory-mapped registers for the CDR registers. All register offset addresses not listed in Table 4-10 should be considered as reserved locations and the register contents should not be modified.

Table 4-10. CDR Registers

Offset	Acronym	Register Name	Section
0h	CDR_Page_Reset	CDR_RST	Section 4.2.1
6h	CDR_Locked	CDR_LCK	Section 4.2.2
23h	Loop_Bandwidth_Control_1	LBW_CTRL1	Section 4.2.3
24h	Loop_Bandwidth_Control_2	LBW_CTRL2	Section 4.2.4
2Ch	VCO_Control	VCO_CTRL	Section 4.2.5
3Fh	Divider	DIV	Section 4.2.6
40h	PRBS_Serializer	SER	Section 4.2.7
41h	Deserializer	DES	Section 4.2.8
45h	PFD_Overrides	PFD_OV	Section 4.2.9
53h	PFD_Driver_Mux	PFD_CTRL	Section 4.2.10
54h	Output_Selection	OUT_SEL	Section 4.2.11
64h	EOM_Control_1	EOM_CTRL1	Section 4.2.12
65h	EOM_Control_2	EOM_CTRL2	Section 4.2.13
67h	EOM_Control_4	EOM_CTRL4	Section 4.2.14
68h	EOM_Control_5	EOM_CTRL5	Section 4.2.15
69h	EOM_Control_6	EOM_CTRL6	Section 4.2.16
6Ah	Eye_Opening_Monitor_1	EOM_VEO	Section 4.2.17
6Bh	Eye_Opening_Monitor_2	EOM_VEO	Section 4.2.18
72h	Rate_Detect	RT_DET	Section 4.2.19
73h	PRBS_Detect	PRBS_DET	Section 4.2.20
74h	PRBS_Error_Check_1	BEC	Section 4.2.21
75h	PRBS_Error_Check_2	BEC1	Section 4.2.22
79h	PRBS_Control_1	PRBS_CTRL1	Section 4.2.23
7Eh	Interrupt_Status	INT_STAT	Section 4.2.24
7Fh	Enable_Interrupts	EN_INT	Section 4.2.25
82h	PRBS_Error_Injection	BEI	Section 4.2.26
89h	Watchdog_Timer	WT	Section 4.2.27
8Bh	POWER_CYCLE	PRBS_CLK	Section 4.2.28

Complex bit access types are encoded to fit into small table cells. Table 4-11 shows the codes that are used for access types in this section.

Table 4-11. CDR Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

4.2.1 CDR_Page_Reset Register (Offset = 0h) [Reset = 00h]

CDR_Page_Reset is shown in Table 4-12.

Return to the Summary Table.

This register is to reset the CDR page registers.

Table 4-12. CDR_Page_Reset Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	rst_regs	R/W1C	0h	Reset all the CDR page registers
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.2.2 CDR_Locked Register (Offset = 6h) [Reset = 00h]

CDR_Locked is shown in Table 4-13.

Return to the Summary Table.

This register is to view the CDR locked status.

Table 4-13. CDR_Locked Register Field Descriptions

Bit	Field	Type	Reset	Description
7	cdr_locked_sel_1	R/W	0h	Select which signal is used to control LOCK_N pin: 2'b00 = CDR lock status 2'b01 = RESERVED 2'b10 = EQ adaptation status 2'b11 = Lock monitor completion status
6	cdr_locked_sel_0	R/W	0h	See MSB
5	cdr_pd2_locked	R/W	0h	1'b0 = CDR not locked 1'b1 = CDR locked
4	sslms_1done	R/W	0h	1'b0 = Equalizer adaptation incomplete 1'b1 = Equalizer adaptation complete
3	channel_controller_state_3	R/W	0h	Device Status: 4'd0 = RESET 4'd4 = Waiting for input signal 4'd6, 4d'7 = CDR lock acquisition in progress 4'd9 = CDR locked and equalizer adaptation complete 4'd10 =Equalizer adaptation in progress Other values = RESERVED
2	channel_controller_state_2	R/W	0h	See MSB
1	channel_controller_state_1	R/W	0h	See MSB
0	channel_controller_state_0	R/W	0h	See MSB

4.2.3 Loop_Bandwidth_Control_1 Register (Offset = 23h) [Reset = 2Ch]

Loop_Bandwidth_Control_1 is shown in Table 4-14.

Return to the Summary Table.

This register has the override for the LOOP_BW_SEL pin.

Table 4-14. Loop_Bandwidth_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	reg_loop_bw_sel_1	R/W	0h	Replaces the value from LOOP_BW_SEL pin when loop_bw_sel_pin_ov_en is 1
6	reg_loop_bw_sel_0	R/W	0h	See MSB
5	RESERVED	R	1h	
4	RESERVED	R	0h	
3	RESERVED	R	1h	
2	RESERVED	R	1h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.2.4 Loop_Bandwidth_Control_2 Register (Offset = 24h) [Reset = 32h]

Loop_Bandwidth_Control_2 is shown in Table 4-15.

Return to the Summary Table.

This register sets the value for the LOOP_BW_SEL pin when the override in reg_23h is enabled.

Table 4-15. Loop_Bandwidth_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	loop_bw_sel_pin_ov_en	R/W	0h	when 1, uses reg23[7:6] instead of the pin LOOP_BW_SEL
6	RESERVED	R	0h	
5	RESERVED	R	1h	
4	RESERVED	R	1h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	1h	
0	RESERVED	R	0h	

4.2.5 VCO_Control Register (Offset = 2Ch) [Reset = 04h]

VCO_Control is shown in Table 4-16.

Return to the Summary Table.

This register is for overriding the VCO power down.

Table 4-16. VCO_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	vco_PD_ov	R/W	0h	When set to 1, VCO power-down signal is controlled by vco_PD When set to 0, VCO power-down signal is controlled by state machine
6	vco_PD	R/W	0h	See MSB
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	1h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.2.6 Divider Register (Offset = 3Fh) [Reset = 04h]

Divider is shown in Table 4-17.

Return to the Summary Table.

This register is for PRBS divider control.

Table 4-17. Divider Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	pdiq_PD_ov	R/W	0h	When 1, the divider power-down signal is controlled by pdiq_PD (bit 5)
5	pdiq_PD	R/W	0h	Controls the divider power-down signal when pdiq_PD_ov (bit 6) is 1
4	RESERVED	R	0h	
3	reg_divsel_ov	R/W	0h	Enable bit to override divider ratio with value in bits [2:0]
2	pdiq_sel_div_2	R/W	1h	Sets the scalar divider ratio when override in bit 3 is set: 3'b000 = Full-rate 3'b001 = Divide-by-2 3'b010 = Divide-by-4 3'b011 = Divide-by-8 3'b100 = Divide-by-40
1	pdiq_sel_div_1	R/W	0h	See MSB
0	pdiq_sel_div_0	R/W	0h	See MSB

4.2.7 PRBS_Serializer Register (Offset = 40h) [Reset = 00h]

PRBS_Serializer is shown in Table 4-18.

Return to the Summary Table.

This register is for serializer control.

Table 4-18. PRBS_Serializer Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	serializer_en	R/W	0h	1'b0 = Disable the serializer block 1'b1 = Enable the serializer block
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.2.8 Deserializer Register (Offset = 41h) [Reset = 00h]

Deserializer is shown in Table 4-19.

Return to the Summary Table.

This register is for deserializer power down control.

Table 4-19. Deserializer Register Field Descriptions

Bit	Field	Type	Reset	Description
7	deser_pd_ov	R/W	0h	When 1, the deserializer power-down signal is controlled by deser_pd (bit 6)
6	deser_pd	R/W	0h	Controls the deserializer power-down signal when deser_pd_ov is 1 (bit 7)

Table 4-19. Deserializer Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.2.9 PFD_Overrides Register (Offset = 45h) [Reset = 10h]

PFD_Overrides is shown in Table 4-20.

Return to the Summary Table.

This register is for applying clock and PFD overrides.

Table 4-20. PFD_Overrides Register Field Descriptions

Bit	Field	Type	Reset	Description
7	mr_pfd_pd_ov	R/W	0h	When 1, PFD power-down signal is controlled by mr_pfd_pd (bit 6)
6	mr_pfd_pd	R/W	0h	Controls the PFD power-down signal when mr_pfd_pd_ov (bit 7) is 1
5	RESERVED	R	0h	
4	RESERVED	R	1h	
3	mr_pfd_pd_clk_path_ov	R/W	0h	Override to force the power down or power up of the retimer and clock path
2	mr_pfd_pd_ret	R/W	0h	Power-down control for retimer when reg_45h mr_pfd_pd_ret_clk_path_ov is 1
1	mr_pfd_pd_clk_path_pd	R/W	0h	Power-down control for clock path when reg_45h mr_pfd_pd_ret_clk_path_ov is 1
0	RESERVED	R	0h	

4.2.10 PFD_Driver_Mux Register (Offset = 53h) [Reset = 20h]

PFD_Driver_Mux is shown in Table 4-21.

Return to the Summary Table.

This register is for OUT_CTRL override and the independent output control override (PFD).

Table 4-21. PFD_Driver_Mux Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	out_ctrl_ov_en	R/W	0h	When '1', selection from OUT_CTRL pin is overwritten by reg_53h mr_out_ctrl[1] and mr_out_ctrl[0]
5	mr_out_ctrl_1	R/W	1h	2'b00 = Enable Bypass, Debug Only. OUT0, SDI_OUT, and OUT1 transmit Equalized Data, Cable EQ (CTLE, DFE) enabled and reclocker bypassed 2'b01 = Enable OUT0 and SDI_OUT transmit Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled OUT1 transmits Full-Rate Recovered Clock if Data Rate ≤ 2.97Gbps. 297MHz Recovered Clock if Data Rate > 2.97Gbps 2'b10 = Enable Normal operation OUT0, SDI_OUT, and OUT1 transmit Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled 2'b11 = Enable Normal operation OUT0, SDI_OUT, and OUT1 transmit Recovered Data, Cable EQ (CTLE, DFE) and reclocker enabled
4	mr_out_ctrl_0	R/W	0h	See MSB

Table 4-21. PFD_Driver_Mux Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	reg_bypass_pfd_ov	R/W	0h	PFD Output MUX control override: 1'b0 = Disable PFD output MUX control using reg_54h 1'b1 = Enable PFD output MUX control using reg_54h
0	RESERVED	R	0h	

4.2.11 Output_Selection Register (Offset = 54h) [Reset = FCh]

Output_Selection is shown in Table 4-22.

Return to the Summary Table.

This register is for independent output control for OUT0, OUT1, and SDI_OUT.

Table 4-22. Output_Selection Register Field Descriptions

Bit	Field	Type	Reset	Description
7	pfd_sel_mux_out0_2	R/W	1h	PFD Mux Selection for OUT0 when reg_bypass_pfd_ov is set Output on OUT0: 3'b000 = Raw Data 3'b001 = Retimed Data 3'b010 = Full-Rate VCO Clock 3'b100 = PRBS data 3'b101 = 10MHz clock or VCO/40 clock (see VCO_Clock_Divider) 3'b111 = Mute Other settings invalid
6	pfd_sel_mux_out0_1	R/W	1h	See MSB
5	pfd_sel_mux_out0_0	R/W	1h	See MSB
4	pfd_sel_mux_out1_2	R/W	1h	PFD Mux Selection for OUT1 when reg_bypass_pfd_ov is set Output on OUT0: 3'b000 = Raw Data 3'b001 = Retimed Data 3'b010 = Full-Rate VCO Clock 3'b100 = PRBS data 3'b101 = 10MHz clock or VCO/40 clock (see VCO_Clock_Divider) 3'b111 = Mute Other settings invalid
3	pfd_sel_mux_out1_1	R/W	1h	See MSB
2	pfd_sel_mux_out1_0	R/W	1h	See MSB
1	pfd_sel_cable_mux_1	R/W	0h	PFD Mux Selection for SDI_OUT when reg_bypass_pfd_ov is set. Output on SDI_OUT: 2'b00 = Raw Data 2'b01 = Retimed Data 2'b10 = 10MHz clock or VCO/40 clock (see VCO_Clock_Divider) 2'b11 = PRBS data
0	pfd_sel_cable_mux_0	R/W	0h	See MSB

4.2.12 EOM_Control_1 Register (Offset = 64h) [Reset = F0h]

EOM_Control_1 is shown in Table 4-23.

Return to the Summary Table.

This register is for EOM control.

Table 4-23. EOM_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	eom_PD	R/W	1h	Power down for EOM

Table 4-23. EOM_Control_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	veo_scale	R/W	1h	1'b0 = VEO scaling based on manual voltage range settings in bits[5:4] 1'b1 = Enable auto-VEO scaling
5	eom_sel_vrange_1	R/W	1h	Sets the expected incoming eye diagram vertical eye opening interval if veo_scale (bit 6) is 0: 2'b00 = 3.125mV (3.125mV × 64 = 200mV; ±100mV range) 2'b01 = 6.25mV (6.25mV × 64 = 400mV; ±200mV range) 2'b10 = 9.375mV (9.375mV × 64 = 600mV; ±300mV range) 2'b11 = 12.5mV (12.5mV × 64 = 800mV; ±400mV range)
4	eom_sel_vrange_0	R/W	1h	See MSB
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.2.13 EOM_Control_2 Register (Offset = 65h) [Reset = 00h]

EOM_Control_2 is shown in Table 4-24.

Return to the Summary Table.

This register is for EOM control.

Table 4-24. EOM_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	fast_eom	R/W	0h	1'b0 = Disable fast EOM mode 1'b1 = Enable fast EOM mode
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.2.14 EOM_Control_4 Register (Offset = 67h) [Reset = 00h]

EOM_Control_4 is shown in Table 4-25.

Return to the Summary Table.

This register is for EOM control.

Table 4-25. EOM_Control_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	eom_vrange_setting_1	R	0h	Readback of automatic EOM voltage range granularity: 2'b00 = 3.125mV 2'b01 = 6.25mV 2'b10 = 9.375mV 2'b11 = 12.5mV
3	eom_vrange_setting_0	R	0h	See MSB
2	RESERVED	R	0h	

Table 4-25. EOM_Control_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	eom_get_heo_veo	R/W1C	0h	1'b1 = Acquire HEO and VEO, self-clearing
0	eom_start	R/W1C	0h	1'b1 = Start EOM counter, self-clearing

4.2.15 EOM_Control_5 Register (Offset = 68h) [Reset = 00h]

EOM_Control_5 is shown in Table 4-26.

Return to the Summary Table.

This register is for the MSBs of the EOM counter.

Table 4-26. EOM_Control_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	eom_count_msb_7	R	0h	MSBs of EOM counter
6	eom_count_msb_6	R	0h	MSBs of EOM counter
5	eom_count_msb_5	R	0h	MSBs of EOM counter
4	eom_count_msb_4	R	0h	MSBs of EOM counter
3	eom_count_msb_3	R	0h	MSBs of EOM counter
2	eom_count_msb_2	R	0h	MSBs of EOM counter
1	eom_count_msb_1	R	0h	MSBs of EOM counter
0	eom_count_msb_0	R	0h	MSBs of EOM counter

4.2.16 EOM_Control_6 Register (Offset = 69h) [Reset = 00h]

EOM_Control_6 is shown in Table 4-27.

Return to the Summary Table.

This register is for the LSBs of the EOM counter.

Table 4-27. EOM_Control_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	eom_count_lsb_7	R	0h	LSBs of EOM counter
6	eom_count_lsb_6	R	0h	LSBs of EOM counter
5	eom_count_lsb_5	R	0h	LSBs of EOM counter
4	eom_count_lsb_4	R	0h	LSBs of EOM counter
3	eom_count_lsb_3	R	0h	LSBs of EOM counter
2	eom_count_lsb_2	R	0h	LSBs of EOM counter
1	eom_count_lsb_1	R	0h	LSBs of EOM counter
0	eom_count_lsb_0	R	0h	LSBs of EOM counter

4.2.17 Eye_Opening_Monitor_1 Register (Offset = 6Ah) [Reset = 00h]

Eye_Opening_Monitor_1 is shown in Table 4-28.

Return to the Summary Table.

This register is for viewing the HEO value.

Table 4-28. Eye_Opening_Monitor_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	heo_7	R	0h	HEO value. This is measured in 0-63 phase settings.
6	heo_6	R	0h	See MSB

Table 4-28. Eye_Opening_Monitor_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	heo_5	R	0h	See MSB
4	heo_4	R	0h	See MSB
3	heo_3	R	0h	See MSB
2	heo_2	R	0h	See MSB
1	heo_1	R	0h	See MSB
0	heo_0	R	0h	See MSB

4.2.18 Eye_Opening_Monitor_2 Register (Offset = 6Bh) [Reset = 00h]

Eye_Opening_Monitor_2 is shown in Table 4-29.

Return to the Summary Table.

This register is for viewing the VEO value.

Table 4-29. Eye_Opening_Monitor_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	veo_7	R	0h	VEO value. This is measured in 0-63 vertical steps.
6	veo_6	R	0h	See MSB
5	veo_5	R	0h	See MSB
4	veo_4	R	0h	See MSB
3	veo_3	R	0h	See MSB
2	veo_2	R	0h	See MSB
1	veo_1	R	0h	See MSB
0	veo_0	R	0h	See MSB

4.2.19 Rate_Detect Register (Offset = 72h) [Reset = 00h]

Rate_Detect is shown in Table 4-30.

Return to the Summary Table.

This register is used to detect the input data rate.

Table 4-30. Rate_Detect Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	rate_detected_2	R	0h	Read back the detected data rate: 3'b000 = 12G 3'b001 = 6G 3'b010 = 3G 3'b011 = 1.5G 3'b100 = 270M Other values invalid
5	rate_detected_1	R	0h	See MSB
4	rate_detected_0	R	0h	See MSB
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.2.20 PRBS_Detect Register (Offset = 73h) [Reset = 10h]

PRBS_Detect is shown in Table 4-31.

Return to the Summary Table.

This is a status register for PRBS generation and checking.

Table 4-31. PRBS_Detect Register Field Descriptions

Bit	Field	Type	Reset	Description
7	prbs_pol_inv	R	0h	Detects PRBS polarity inverted, read only 1'b1 = PRBS polarity is inverted
6	RESERVED	R	0h	
5	prbs_error	R	0h	Detects PRBS error, read only 1'b1 = PRBS error detected
4	RESERVED	R	1h	
3	prbs_patt_det_3	R	0h	PRBS-31 detected
2	prbs_patt_det_2	R	0h	PRBS-23 detected
1	prbs_patt_det_1	R	0h	PRBS-9 detected
0	prbs_patt_det_0	R	0h	PRBS-7 detected

4.2.21 PRBS_Error_Check_1 Register (Offset = 74h) [Reset = 00h]

PRBS_Error_Check_1 is shown in Table 4-32.

Return to the Summary Table.

This register is used to see the number of bit errors once a PRBS polynomial is found.

Table 4-32. PRBS_Error_Check_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	bit_err_sum_msb_2	R	0h	Number of bit errors once PRBS polynomial is found
1	bit_err_sum_msb_1	R	0h	see MSB
0	bit_err_sum_msb_0	R	0h	see MSB

4.2.22 PRBS_Error_Check_2 Register (Offset = 75h) [Reset = 00h]

PRBS_Error_Check_2 is shown in Table 4-33.

Return to the Summary Table.

This register is for PRBS bit error checking.

Table 4-33. PRBS_Error_Check_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	bit_err_sum_lsb_7	R	0h	LSB of bit errors once PRBS polynomial is found
6	bit_err_sum_lsb_6	R	0h	see MSB
5	bit_err_sum_lsb_5	R	0h	see MSB
4	bit_err_sum_lsb_4	R	0h	see MSB
3	bit_err_sum_lsb_3	R	0h	see MSB
2	bit_err_sum_lsb_2	R	0h	see MSB
1	bit_err_sum_lsb_1	R	0h	see MSB

Table 4-33. PRBS_Error_Check_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	bit_err_sum_lsb_0	R	0h	see MSB

4.2.23 PRBS_Control_1 Register (Offset = 79h) [Reset = 80h]

PRBS_Control_1 is shown in Table 4-34.

Return to the Summary Table.

This register is for PRBS control.

Table 4-34. PRBS_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	1h	
6	RESERVED	R	0h	
5	prbs_gen_sel_1	R/W	0h	PRBS generator pattern selection: 2'b00 = PRBS7 2'b01 = PRBS9 2'b10 = PRBS23 2'b11 = PRBS31
4	prbs_gen_sel_0	R/W	0h	See MSB
3	progpatt_en	R/W	0h	1'b1 = enable fixed pattern output and ignore prbs_gen_sel 1'b0 = Generate PRBS based on prbs_gen_sel when in generator mode
2	prbs_chk	R/W	0h	1'b0 = PRBS checker mode disabled 1'b1 = PRBS checker mode enabled
1	prbs_gen	R/W	0h	1'b1 = PRBS generator mode
0	prbs_en	R/W	0h	1'b1 = Enable PRBS functionality

4.2.24 Interrupt_Status Register (Offset = 7Eh) [Reset = 00h]

Interrupt_Status is shown in Table 4-35.

Return to the Summary Table.

This register serves as the interrupt observation point for the interrupt set in reg_7Fh, the condition for the given bit only applies if the corresponding bit interrupt in reg_7Fh is enabled.

Table 4-35. Interrupt_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	sigdet	R	0h	Raw signal detect observation point
6	cdr_lock_int	R	0h	1'b0 = No interrupt from CDR lock 1'b1 = Interrupt for CDR lock
5	signal_det1_int	R	0h	1'b0 = No signal detected on SDI_IN1 1'b1 = Signal detected on SDI_IN1
4	signal_det0_int	R	0h	1'b0 = No signal detected on SDI_IN 1'b1 = Signal detected on SDI_IN
3	sdi_out_term_det_int	R	0h	1'b0 = SDI_OUT is not terminated 1'b1 = SDI_OUT is terminated
2	cdr_lock_loss_int	R	0h	1'b0 = No interrupt for CDR loss of lock 1'b1 = Interrupt for CDR loss of lock
1	signal_det1_loss_int	R	0h	1'b0 = No interrupt for loss of signal on SDI_IN1 1'b1 = Interrupt for loss of signal on SDI_IN1
0	signal_det0_loss_int	R	0h	1'b0 = No interrupt for loss of signal on SDI_IN 1'b1 = Interrupt for loss of signal on SDI_IN

4.2.25 Enable_Interrupts Register (Offset = 7Fh) [Reset = 00h]

Enable_Interrupts is shown in Table 4-36.

Return to the Summary Table.

This register is to enable interrupts.

Table 4-36. Enable_Interrupts Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	cdr_lock_int_en	R/W	0h	Enable interrupt for CDR lock
5	signal_det1_int_en	R/W	0h	Enable interrupt for when signal detect triggers on SDI_IN1
4	signal_det0_int_en	R/W	0h	Enable interrupt for when signal detect triggers on SDI_IN
3	sdi_out_term_det_int_en	R/W	0h	Enable interrupt if SDI-OUT detects a termination
2	cdr_lock_loss_int_en	R/W	0h	Enable interrupt if the CDR loses lock
1	signal_det1_loss_int_en	R/W	0h	Enable interrupt to detect a loss of signal on SDI_IN1
0	signal_det0_loss_int_en	R/W	0h	Enable interrupt to detect a loss of signal on SDI_IN

4.2.26 PRBS_Error_Injection Register (Offset = 82h) [Reset = 00h]

PRBS_Error_Injection is shown in Table 4-37.

Return to the Summary Table.

This register is for applying a PRBS generator bit error injection.

Table 4-37. PRBS_Error_Injection Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	prbs_sel_ser_clk	R/W	0h	When set to 1, use serializer clock to drive PRBS-core
5	prbs_gen_bit_err_inject	R/W1C	0h	Trigger the PRBS generator to inject just one bit of error in the generated data stream. Self-clearing
4	prbs_gen_bit_err_pos_4	R/W	0h	Defines the position of the single-bit error in the 32-bit generated data
3	prbs_gen_bit_err_pos_3	R/W	0h	See MSB
2	prbs_gen_bit_err_pos_2	R/W	0h	See MSB
1	prbs_gen_bit_err_pos_1	R/W	0h	See MSB
0	prbs_gen_bit_err_pos_0	R/W	0h	See MSB

4.2.27 Watchdog_Timer Register (Offset = 89h) [Reset = 04h]

Watchdog_Timer is shown in Table 4-38.

Return to the Summary Table.

This register activates the watchdog timer functionality.

Table 4-38. Watchdog_Timer Register Field Descriptions

Bit	Field	Type	Reset	Description
7	wdog_restart_en	R/W	0h	Enable watchdog timer functionality to restart CDR without enabling bypass
6	wdog_restart_sel_1	R/W	0h	Timer value for wdog_restart_en: 2'b00 = 32ms 2'b01 = 36ms 2'b10 = 44ms 2'b11 = 60ms
5	wdog_restart_sel_0	R/W	0h	See MSB

Table 4-38. Watchdog_Timer Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	sigdet_delay_1	R/W	0h	Delay the onset of CDR lock after signal detect is asserted: 2'b00 = No delay 2'b01 = 1ms 2'b10 = 2ms 2'b11 = 4ms
3	sigdet_delay_0	R/W	0h	See MSB
2	RESERVED	R	1h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.2.28 POWER_CYCLE Register (Offset = 8Bh) [Reset = 83h]

POWER_CYCLE is shown in Table 4-39.

Return to the Summary Table.

This register is for power cycling the deserializer.

Table 4-39. POWER_CYCLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	power_cycle_en	R/W	1h	1'b1 = Turn the deserializer on and off periodically 1'b0 = Leave deserializer always on
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	1h	
0	RESERVED	R	1h	

4.3 EQ_Drivers Registers

Table 4-40 lists the memory-mapped registers for the EQ_Drivers registers. All register offset addresses not listed in Table 4-40 should be considered as reserved locations and the register contents should not be modified.

Table 4-40. EQ_DRIVERS Registers

Offset	Acronym	Register Name	Section
0h	General_Control	GEN_CTRL	Section 4.3.1
6h	Signal_Detect	SIG_DET1	Section 4.3.2
7h	Signal_Detect_2	SIG_DET2	Section 4.3.3
8h	Signal_Detect_3	SIG_DET3	Section 4.3.4
16h	CTLE_Index_Override	CTLE_OV	Section 4.3.5
30h	Mute_Reference_Threshold	MUTE_REF	Section 4.3.6
33h	OUT0_Controls	OUT0_CTRL	Section 4.3.7
34h	OUT0_Controls_2	OUT0_CTRL2	Section 4.3.8
35h	OUT1_Controls	OUT1_CTRL	Section 4.3.9
36h	OUT1_Controls_2	OUT1_CTRL2	Section 4.3.10
38h	SDI_OUT_Driver_Controls	SDI_OUTCTRL	Section 4.3.11
39h	Cable_Driver_VOD	CD_VOD	Section 4.3.12
3Ah	UHD_VOD_Adjustment	UHD_VOD	Section 4.3.13
3Bh	HD_VOD_Adjustment	HD_VOD	Section 4.3.14
3Ch	SD_VOD_Adjustment	SD_VOD	Section 4.3.15
3Fh	SDI_OUT_Pre-Emphasis	SDI_OUT_PE	Section 4.3.16
45h	DFE_Taps_1_Observation	DFE1	Section 4.3.17
47h	DFE_Taps_2_Observation	DFE2	Section 4.3.18
49h	DFE_Taps_3_Observation	DFE3	Section 4.3.19
7Eh	Coarse_Rate_Control	CRC	Section 4.3.20
9Ch	CTLE_Index	CTLE	Section 4.3.21
A8h	Cable_Fault_Detect	CFD	Section 4.3.22
ACh	Observation_Point_1	OBS1	Section 4.3.23
ADh	Observation_Point_2	OBS2	Section 4.3.24

Complex bit access types are encoded to fit into small table cells. Table 4-41 shows the codes that are used for access types in this section.

Table 4-41. EQ_Drivers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

4.3.1 General_Control Register (Offset = 0h) [Reset = 08h]

General_Control is shown in Table 4-42.

Return to the Summary Table.

This register is for general control of the EQ/Drivers page.

Table 4-42. General_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	1h	
2	register_reset	R/W1C	0h	Reset EQ/Drivers registers: 1'b0 = Normal operation 1'b1 = Reset EQ/Drivers registers
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.3.2 Signal_Detect Register (Offset = 6h) [Reset = 08h]

Signal_Detect is shown in Table 4-43.

Return to the Summary Table.

This register is for overriding the signal detect status on SDI_IN.

Table 4-43. Signal_Detect Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	dig_eq0_sd_ov	R/W	1h	Enable Override of Signal Detect on SDI_IN: 1'b0 = Normal operation 1'b1 = Override Signal Detect with value in bit 2 of this register
2	dig_eq0_sd	R/W	0h	Override Value for Signal Detect on SDI_IN: When bit 3 of this register is 1, this value is used in place of the Signal Detect. When bit 3 of this register is 0, this value is ignored.
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.3.3 Signal_Detect_2 Register (Offset = 7h) [Reset = 20h]

Signal_Detect_2 is shown in Table 4-44.

Return to the Summary Table.

This register is for overriding the signal detect status on SDI_IN1.

Table 4-44. Signal_Detect_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	1h	
4	RESERVED	R	0h	
3	dig_eq1_sd_ov	R/W	0h	Enable Override of Signal Detect on SDI_IN1: 1'b0 = Normal operation 1'b1 = Override Signal Detect with value in bit 2 of this register

Table 4-44. Signal_Detect_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	dig_eq1_sd	R/W	0h	Override Value for Signal Detect on SDI_IN1: When bit 3 of this register is 1, this value is used in place of the Signal Detect. When bit 3 of this register is 0, this value is ignored.
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.3.4 Signal_Detect_3 Register (Offset = 8h) [Reset = 20h]

Signal_Detect_3 is shown in Table 4-45.

Return to the Summary Table.

This register is for viewing the signal detect status on SDI_IN and SDI_IN1.

Table 4-45. Signal_Detect_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	1h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	eq0_sig_detect_filtered	R	0h	Signal detect status of SDI_IN: 1'b0 = No signal 1'b1 = Signal present
1	RESERVED	R	0h	
0	eq1_sig_detect_filtered	R	0h	Signal detect status of SDI_IN1: 1'b0 = No signal 1'b1 = Signal present

4.3.5 CTLE_Index_Override Register (Offset = 16h) [Reset = 00h]

CTLE_Index_Override is shown in Table 4-46.

Return to the Summary Table.

This register is for overriding the CTLE index value.

Table 4-46. CTLE_Index_Override Register Field Descriptions

Bit	Field	Type	Reset	Description
7	eq_index_ov	R/W	0h	CTLE Adaptation Mode: 1'b0 = Fully Automatic 1'b1 = Manual control using bits[6:0]
6	eq_index_val_6	R/W	0h	Override EQ index value
5	eq_index_val_5	R/W	0h	See MSB
4	eq_index_val_4	R/W	0h	See MSB
3	eq_index_val_3	R/W	0h	See MSB
2	eq_index_val_2	R/W	0h	See MSB
1	eq_index_val_1	R/W	0h	See MSB
0	eq_index_val_0	R/W	0h	See MSB

4.3.6 Mute_Reference_Threshold Register (Offset = 30h) [Reset = 00h]

Mute_Reference_Threshold is shown in Table 4-47.

Return to the Summary Table.

This register is for setting the mute reference threshold. The mute reference threshold is defined as the threshold CTLE index + 2 for which OUT0/1 mute. The mute reference threshold is a binary value at 26mV per step.

Table 4-47. Mute_Reference_Threshold Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	reg_muteref_threshl_5	R/W	0h	Mute reference threshold value in decimal: 6'd0 = Mute when CTLE Index (eq boost) ≥ 2 6'd63 = Mute Reference threshold exceeds maximum CTLE, so the outputs never mute
4	reg_muteref_threshl_4	R/W	0h	See MSB
3	reg_muteref_threshl_3	R/W	0h	See MSB
2	reg_muteref_threshl_2	R/W	0h	See MSB
1	reg_muteref_threshl_1	R/W	0h	See MSB
0	reg_muteref_threshl_0	R/W	0h	See MSB

4.3.7 OUT0_Controls Register (Offset = 33h) [Reset = 3Fh]

OUT0_Controls is shown in Table 4-48.

Return to the Summary Table.

This register is for OUT0 control.

Table 4-48. OUT0_Controls Register Field Descriptions

Bit	Field	Type	Reset	Description
7	reg_tx0_mute_ov	R/W	0h	OUT0 Mute Override Control: 1'b0 = Disable OUT0 Mute Override Control 1'b1 = Enable OUT0 Mute Override Control by value in bit 6
6	reg_tx0_mute_val	R/W	0h	1'b0 = Normal Operation 1'b1 = Mute OUT0 if bit 7 is 1
5	RESERVED	R	1h	
4	RESERVED	R	1h	
3	reg_tx0_vod_ov	R/W	1h	OUT0 VOD override control: 1'b0 = VOD settings determined by VOD_DE pin 1'b1 = VOD settings controlled by bits [2:0]
2	reg_tx0_vod_2	R/W	1h	Override VOD settings: 3'b000 = 410mVpp 3'b010 = 560mVpp 3'b100 = 635mVpp 3'b110 = 810mVpp
1	reg_tx0_vod_1	R/W	1h	See MSB
0	reg_tx0_vod_0	R/W	1h	See MSB

4.3.8 OUT0_Controls_2 Register (Offset = 34h) [Reset = 12h]

OUT0_Controls_2 is shown in Table 4-49.

Return to the Summary Table.

This is the second register for OUT0 control.

Table 4-49. OUT0_Controls_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	reg_tx0_sel_inv	R/W	0h	Inverts driver polarity

Table 4-49. OUT0_Controls_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	reg_tx0_PD_ov	R/W	0h	Overrides for powering down the TX.
5	reg_tx0_PD	R/W	0h	1'b0 = Normal Operation 1'b1 = Power Down OUT0 if bit 6 is 1
4	reg_tx0_dem_ov	R/W	1h	If low, the DEM is taken from the VOD_DE pin. Otherwise, the DEM is taken from [3:0]
3	reg_tx0_dem_range	R/W	0h	Compresses DEM settings in [2:0] to <6dB when asserted
2	reg_tx0_dem_2	R/W	0h	De-emphasis settings: 3'b000 = 0.0dB 3'b010 = –1.0dB 3'b100 = –2.4dB 3'b110 = –6.1dB
1	reg_tx0_dem_1	R/W	1h	See MSB
0	reg_tx0_dem_0	R/W	0h	See MSB

4.3.9 OUT1_Controls Register (Offset = 35h) [Reset = 01h]

OUT1_Controls is shown in Table 4-50.

Return to the Summary Table.

This register is for OUT1 control.

Table 4-50. OUT1_Controls Register Field Descriptions

Bit	Field	Type	Reset	Description
7	reg_tx1_mute_ov	R/W	0h	OUT1 Mute Override Control: 1'b0 = Disable OUT1 Mute Override Control 1'b1 = Enable OUT1 Mute Override Control by value in bit 6
6	reg_tx1_mute_val	R/W	0h	1'b0 = Normal Operation 1'b1 = Mute OUT1 if bit 7 is 1
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	reg_tx1_vod_ov	R/W	0h	OUT1 VOD override control: 1'b0 = VOD settings determined by VOD_DE pin 1'b1 = VOD settings controlled by bits [2:0]
2	reg_tx1_vod_2	R/W	0h	Override VOD settings: 3'b000 = 410mVpp 3'b010 = 560mVpp 3'b100 = 635mVpp 3'b110 = 810mVpp
1	reg_tx1_vod_1	R/W	0h	See MSB
0	reg_tx1_vod_0	R/W	1h	See MSB

4.3.10 OUT1_Controls_2 Register (Offset = 36h) [Reset = 12h]

OUT1_Controls_2 is shown in Table 4-51.

Return to the Summary Table.

This is the second register for OUT1 control.

Table 4-51. OUT1_Controls_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	reg_tx1_sel_inv	R/W	0h	Inverts driver polarity
6	reg_tx1_PD_ov	R/W	0h	Overrides for powering-down the TX.
5	reg_tx1_PD	R/W	0h	1'b0 = Normal Operation 1'b1 = Power Down OUT1 if bit 6 is 1

Table 4-51. OUT1_Controls_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	reg_tx1_dem_ov	R/W	1h	If low, de-emphasis is taken from VOD_DE pin. Else, de-emphasis is taken from [3:0].
3	reg_tx1_dem_range	R/W	0h	Compresses DEM settings in [2:0] to <6dB when asserted.
2	reg_tx1_dem_2	R/W	0h	De-emphasis settings: 3'b000 = 0.0dB 3'b010 = –1.0dB 3'b100 = –2.4dB 3'b110 = –6.1dB
1	reg_tx1_dem_1	R/W	1h	See MSB
0	reg_tx1_dem_0	R/W	0h	See MSB

4.3.11 SDI_OUT_Driver_Controls Register (Offset = 38h) [Reset = 01h]

SDI_OUT_Driver_Controls is shown in Table 4-52.

Return to the Summary Table.

This register is for SDI_OUT driver control.

Table 4-52. SDI_OUT_Driver_Controls Register Field Descriptions

Bit	Field	Type	Reset	Description
7	sdi_out_PD_ov	R/W	0h	Override for SDI_OUT power-down control: 1'b0 = Use SDI_OUT_SEL pin to control SDI_OUT driver power-down 1'b1 = SDI_OUT power-down is controlled by bit 6
6	sdi_out_PD_val	R/W	0h	When bit 7 of this register is set: 1'b0 = SDI_OUT+/- enabled 1'b1 = SDI_OUT+/- disabled
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	1h	

4.3.12 Cable_Driver_VOD Register (Offset = 39h) [Reset = 68h]

Cable_Driver_VOD is shown in Table 4-53.

Return to the Summary Table.

This register is for overriding VOD from pin control and rate trim values with a baseline VOD value. See the SDI VOD Amplitude Control Logic block diagram in this document for more information on VOD control.

Table 4-53. Cable_Driver_VOD Register Field Descriptions

Bit	Field	Type	Reset	Description
7	sdi_out_vod_ov	R/W	0h	1'b0 = SDI_VOD pin control + data rate adjustment value (See the SDI VOD Amplitude Control Logic block diagram in this document for reference) 1'b1 = sdi_out_vod_val[6:0]
6	sdi_out_vod_val_6	R/W	1h	Default vod baseline for pin ctrl
5	sdi_out_vod_val_5	R/W	1h	See MSB
4	sdi_out_vod_val_4	R/W	0h	See MSB
3	sdi_out_vod_val_3	R/W	1h	See MSB
2	sdi_out_vod_val_2	R/W	0h	See MSB

Table 4-53. Cable_Driver_VOD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	sdi_out_vod_val_1	R/W	0h	See MSB
0	sdi_out_vod_val_0	R/W	0h	See MSB

4.3.13 UHD_VOD_Adjustment Register (Offset = 3Ah) [Reset = 0Ch]

UHD_VOD_Adjustment is shown in Table 4-54.

Return to the Summary Table.

This register is to apply adjustments to the output VOD on SDI_OUT for UHD.

Table 4-54. UHD_VOD_Adjustment Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	sdi_out_vod_os_uhd_sign	R/W	0h	SDI_OUT VOD control for UHD rates: 1'b0 = Positive 1'b1 = Negative
4	sdi_out_vod_os_uhd_4	R/W	0h	[4:0] = Magnitude in the range of 0mV to 194mV
3	sdi_out_vod_os_uhd_3	R/W	1h	See MSB
2	sdi_out_vod_os_uhd_2	R/W	1h	See MSB
1	sdi_out_vod_os_uhd_1	R/W	0h	See MSB
0	sdi_out_vod_os_uhd_0	R/W	0h	See MSB

4.3.14 HD_VOD_Adjustment Register (Offset = 3Bh) [Reset = 00h]

HD_VOD_Adjustment is shown in Table 4-55.

Return to the Summary Table.

This register is to apply adjustments to the output VOD on SDI_OUT for HD.

Table 4-55. HD_VOD_Adjustment Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	sdi_out_vod_os_hd_sign	R/W	0h	SDI_OUT VOD control for HD rates: 1'b0 = Positive 1'b1 = Negative
4	sdi_out_vod_os_hd_4	R/W	0h	[4:0] = Magnitude in the range of 0mV to 194mV
3	sdi_out_vod_os_hd_3	R/W	0h	See MSB
2	sdi_out_vod_os_hd_2	R/W	0h	See MSB
1	sdi_out_vod_os_hd_1	R/W	0h	See MSB
0	sdi_out_vod_os_hd_0	R/W	0h	See MSB

4.3.15 SD_VOD_Adjustment Register (Offset = 3Ch) [Reset = 00h]

SD_VOD_Adjustment is shown in Table 4-56.

Return to the Summary Table.

This register is to apply adjustments to the output VOD on SDI_OUT for SD.

Table 4-56. SD_VOD_Adjustment Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	sdi_out_vod_os_sd_sign	R/W	0h	SDI_OUT VOD control for SD rates: 1'b0 = Positive 1'b1 = Negative
4	sdi_out_vod_os_sd_4	R/W	0h	[4:0] = Magnitude in the range of 0mV to 194mV
3	sdi_out_vod_os_sd_3	R/W	0h	See MSB
2	sdi_out_vod_os_sd_2	R/W	0h	See MSB
1	sdi_out_vod_os_sd_1	R/W	0h	See MSB
0	sdi_out_vod_os_sd_0	R/W	0h	See MSB

4.3.16 SDI_OUT_Pre-Emphasis Register (Offset = 3Fh) [Reset = 30h]

SDI_OUT_Pre-Emphasis is shown in Table 4-57.

Return to the Summary Table.

This register is to apply changes to pre-emphasis on SDI_OUT.

Table 4-57. SDI_OUT_Pre-Emphasis Register Field Descriptions

Bit	Field	Type	Reset	Description
7	sdi_out_sel_pre_ov	R/W	0h	SDI_OUT pre-emphasis override control: 1'b0 = Normal operation 1'b1 = SDI_OUT pre-emphasis is controlled by bits [6:5]
6	sdi_out_sel_pre_val_1	R/W	0h	Pre-emphasis value: 2'b11 = 2.5dB
5	sdi_out_sel_pre_val_0	R/W	1h	See MSB
4	sdi_out_sel_pre_uhd	R/W	1h	1'b0 = Disable pre-emphasis at UHD data rates 1'b1 = Enable pre-emphasis value programmed in bits[6:5] at UHD data rates
3	sdi_out_sel_pre_hd	R/W	0h	1'b0 = Disable pre-emphasis at HD data rates 1'b1 = Enable pre-emphasis value programmed in bits[6 :5] at HD data rates
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	sdi_out_sel_inv	R/W	0h	1'b0 = Noninverting SDI_OUT output 1'b1 = Inverting SDI_OUT output

4.3.17 DFE_Taps_1_Observation Register (Offset = 45h) [Reset = 20h]

DFE_Taps_1_Observation is shown in Table 4-58.

Return to the Summary Table.

This register is the first observation point for DFE Taps.

Table 4-58. DFE_Taps_1_Observation Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	dfe_pol_1_obs	R	1h	DFE tap 1 polarity: 1'b0 = Positive 1'b1 = Negative
4	dfe_wt1_obs_4	R	0h	DFE tap 1 magnitude [4:0]
3	dfe_wt1_obs_3	R	0h	See MSB

Table 4-58. DFE_Taps_1_Observation Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	dfe_wt1_obs_2	R	0h	See MSB
1	dfe_wt1_obs_1	R	0h	See MSB
0	dfe_wt1_obs_0	R	0h	See MSB

4.3.18 DFE_Taps_2_Observation Register (Offset = 47h) [Reset = 00h]

DFE_Taps_2_Observation is shown in Table 4-59.

Return to the Summary Table.

This register is the second observation point for DFE Taps.

Table 4-59. DFE_Taps_2_Observation Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	dfe_pol_2_obs	R	0h	DFE tap 2 polarity: 1'b0 = Positive 1'b1 = Negative
3	dfe_wt2_obs_3	R	0h	DFE tap 2 magnitude [3:0]
2	dfe_wt2_obs_2	R	0h	See MSB
1	dfe_wt2_obs_1	R	0h	See MSB
0	dfe_wt2_obs_0	R	0h	See MSB

4.3.19 DFE_Taps_3_Observation Register (Offset = 49h) [Reset = 00h]

DFE_Taps_3_Observation is shown in Table 4-60.

Return to the Summary Table.

This register is the third observation point for DFE Taps.

Table 4-60. DFE_Taps_3_Observation Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	dfe_pol_3_obs	R	0h	DFE tap 3 polarity: 1'b0 = Positive 1'b1 = Negative
3	dfe_wt3_obs_3	R	0h	DFE tap 3 magnitude [3:0]
2	dfe_wt3_obs_2	R	0h	See MSB
1	dfe_wt3_obs_1	R	0h	See MSB
0	dfe_wt3_obs_0	R	0h	See MSB

4.3.20 Coarse_Rate_Control Register (Offset = 7Eh) [Reset = 00h]

Coarse_Rate_Control is shown in Table 4-61.

Return to the Summary Table.

This register is to set the coarse EQ ending rate and the coarse EQ starting rate.

Table 4-61. Coarse_Rate_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	ending_rate_det_register_reg_2	R/W	0h	Coarse EQ ending rate: 3'b000 = 12G 3'b001 = 6G 3'b010 = 3G 3'b011 = 1.5G 3'b100 = 270M (default) 3'b101, 3'b110, 3'b111 = Invalid
5	ending_rate_det_register_reg_1	R/W	0h	See MSB
4	ending_rate_det_register_reg_0	R/W	0h	See MSB
3	RESERVED	R	0h	
2	starting_rate_det_register_reg_2	R/W	0h	Coarse EQ starting rate: 3'b000 = 12G (default) 3'b001 = 6G 3'b010 = 3G 3'b011 = 1.5G 3'b100 = 270M 3'b101, 3'b110, 3'b111 = Invalid
1	starting_rate_det_register_reg_1	R/W	0h	See MSB
0	starting_rate_det_register_reg_0	R/W	0h	See MSB

4.3.21 CTLE_Index Register (Offset = 9Ch) [Reset = 00h]

CTLE_Index is shown in Table 4-62.

Return to the Summary Table.

This register is to view the final CTLE index.

Table 4-62. CTLE_Index Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	ctle_index_5	R	0h	Adapted CTLE index from 0 to 55 in decimal notation
4	ctle_index_4	R	0h	See MSB
3	ctle_index_3	R	0h	See MSB
2	ctle_index_2	R	0h	See MSB
1	ctle_index_1	R	0h	See MSB
0	ctle_index_0	R	0h	See MSB

4.3.22 Cable_Fault_Detect Register (Offset = A8h) [Reset = 80h]

Cable_Fault_Detect is shown in Table 4-63.

Return to the Summary Table.

This register is used to enable the cable fault detector state machine.

Table 4-63. Cable_Fault_Detect Register Field Descriptions

Bit	Field	Type	Reset	Description
7	cfd_bypass	R/W	1h	Bypass the cable fault detector state machine
6	cfd_start	R/W1C	0h	Manual start cable fault detector state machine, self-cleared

Table 4-63. Cable_Fault_Detect Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	cfd_disable	R/W	0h	Disable the cable fault detector state machine
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

4.3.23 Observation_Point_1 Register (Offset = ACh) [Reset = 00h]

Observation_Point_1 is shown in Table 4-64.

Return to the Summary Table.

This register is the cable fault detection observation point.

Table 4-64. Observation_Point_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	sdi_out_term_status	R	0h	Cable fault detection status: 1'b0 = No termination detected on SDI_OUT 1'b1 = Termination detected on SDI_OUT
2	cfd_length_cnt_msb_2	R	0h	Cable length count MSB
1	cfd_length_cnt_msb_1	R	0h	MSB
0	cfd_length_cnt_msb_0	R	0h	MSB

4.3.24 Observation_Point_2 Register (Offset = ADh) [Reset = 00h]

Observation_Point_2 is shown in Table 4-65.

Return to the Summary Table.

This register is the second cable fault detect observation point.

Table 4-65. Observation_Point_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	cfd_length_cnt_lsb_7	R	0h	Cable length count LSB
6	cfd_length_cnt_lsb_6	R	0h	LSB
5	cfd_length_cnt_lsb_5	R	0h	LSB
4	cfd_length_cnt_lsb_4	R	0h	LSB
3	cfd_length_cnt_lsb_3	R	0h	LSB
2	cfd_length_cnt_lsb_2	R	0h	LSB
1	cfd_length_cnt_lsb_1	R	0h	LSB
0	cfd_length_cnt_lsb_0	R	0h	LSB

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