Application Note

LMK3H0102 PCI Express Compliance Report

Kadeem Samuel

ABSTRACT

Enterprise systems are demanding cleaner clocks since data centers are using higher data rates. This report demonstrates PCI Express (PCIe) compliance for the LMK3H0102 family of clock generators, which verify these devices can be used in such systems.

Table of Contents

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

This document presents a test report of PCI Express (PCIe) reference clock compliance for the LMK3H0102 family. The report contains the test setup, test procedure, TI's PCIe Compliance Tool explanation, and the test results demonstrating PCIe compliance. The test setup was arranged to obtain both the phase noise and time domain jitter analysis required for PCIe compliance. Then, the test procedure was followed to obtain the results. The data from this test is then uploaded onto TI's PCIe Compliance Tool within TICS Pro to determine PCIe compliance.

2 Test Setup

TI's PCIe Compliance Reports display the analysis of a device's phase noise or jitter in regards to meeting PCIe requirements. The LMK3H0102 family is characterized at max operating temperature of 85°C and a lowest supply voltage of 1.71 V. This PCIe compliance report displays test results under typical conditions. For the LMK3H0102 family the operating temperature is at 25°C and the supply voltage is at 3.3 V.

The hardware setup consists of a device under test, power supply, attenuators, limiter, balun (for frequency domain only), thermal force unit, test load board, and phase noise analyzer (PNA, for frequency domain) or oscilloscope (for time domain). The device is reference-less, and does not require signal from a signal generator. The internal BAW resonator is the clock source for the device.

For the frequency domain measurements, the differential outputs of the device are connected to a balun to convert them to a single-ended signal and then route that signal to a PNA, as shown on Figure 2-1.

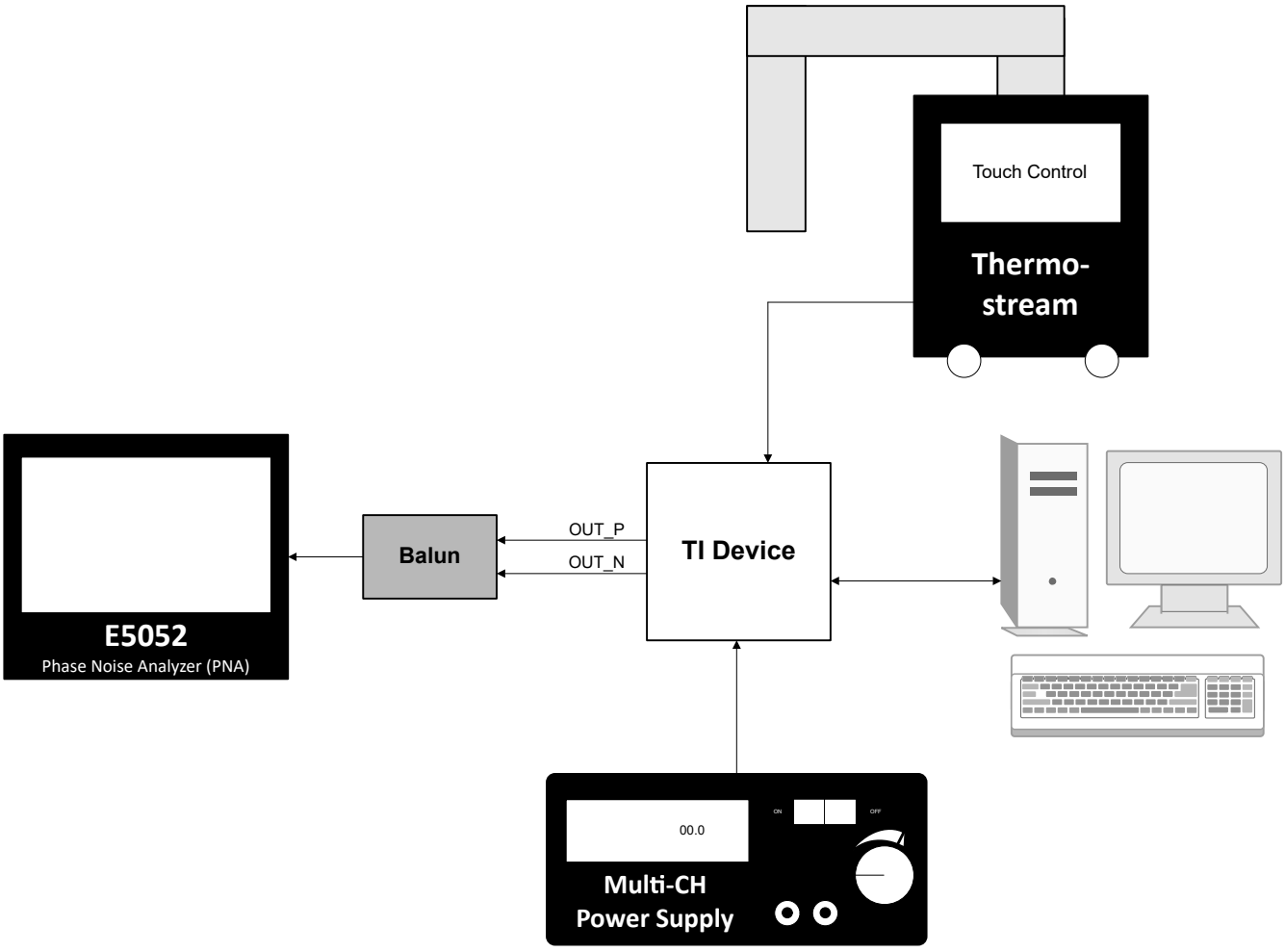

Figure 2-1. TI's PCIe Compliance Test Hardware Setup for Frequency Domain Measurements

For time domain measurements, the differential outputs (both positive and negative pins) of the device are routed directly to an oscilloscope, as shown on Figure 2-2. Also, when obtaining data for the time domain measurements, the PCIe test load is a 15 dB loss trace at 4 GHz.

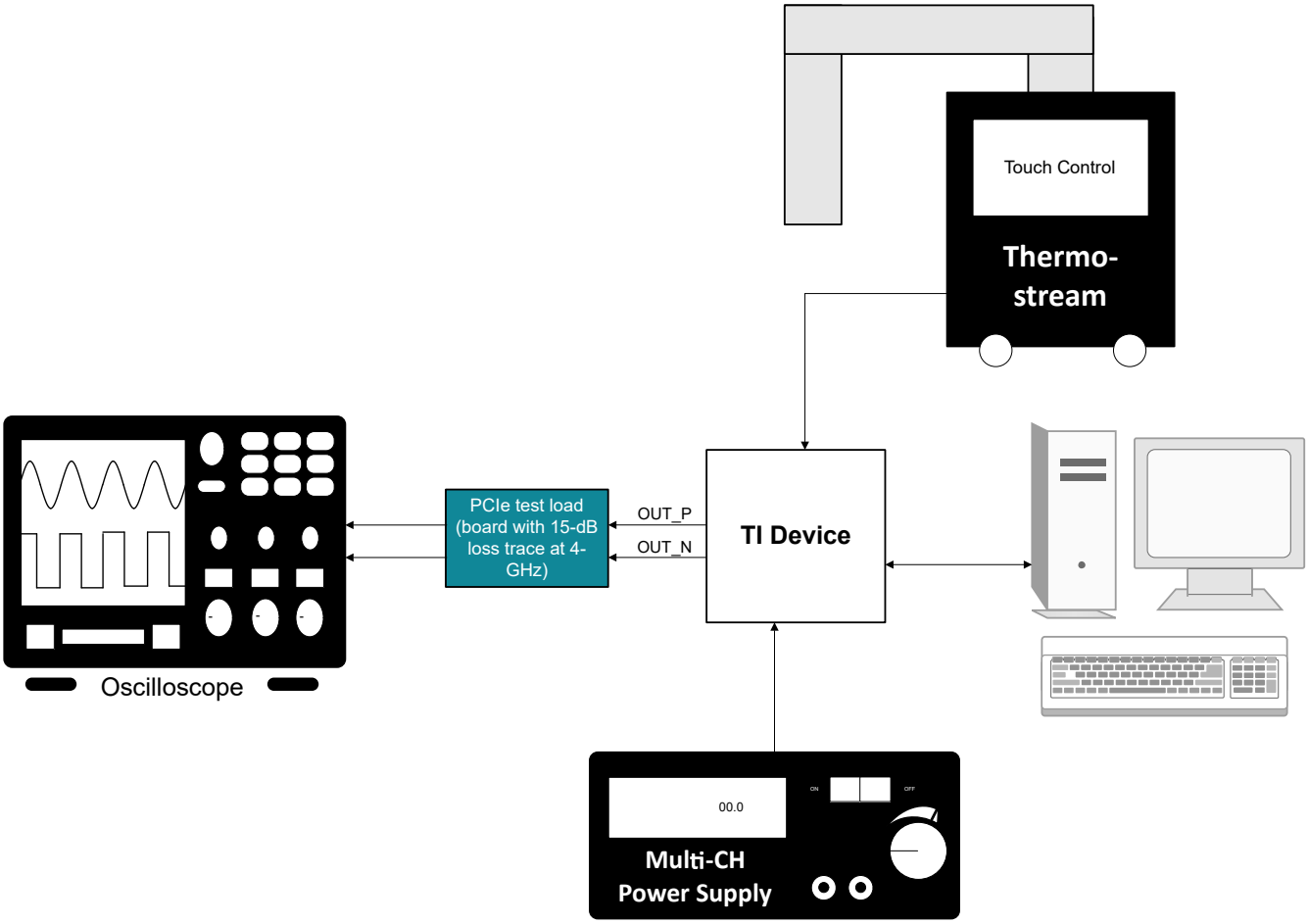

Figure 2-2. TI's PCIe Compliance Test Hardware Setup for Time Domain Measurements

3 Test Procedure

Test procedure used to obtain LMK3H0102's PCIe compliance report results is as follows:

1. After powering up the device, the differential outputs are connected directly to an oscilloscope for time domain measurements, or to a PNA through a balun for frequency domain measurements.
2. An output trace file is captured from the PNA or oscilloscope. Note that the oscilloscope capture requires both the positive and negative traces, so two output trace files from the oscilloscope are required.
3. The file/files generated is/are run through TI's PCIe Compliance Tool (Section 4 contains more information about this tool).

4 Explanation of TI's PCIe Compliance Tool

TI's PCIe Compliance Tool can be found within TI's TICS Pro Software. To access the tool, first download *TI's TICS Pro Software*. Under the *Tools* tab, select *PCIe Report Generator* (steps shown in Figure 4-1). After a few seconds, the tool appears, as shown on Figure 4-2, which can then be used to analyze frequency domain traces (such as Figure 4-3) and time domain traces (such as Figure 4-4) to determine PCIe compliance.

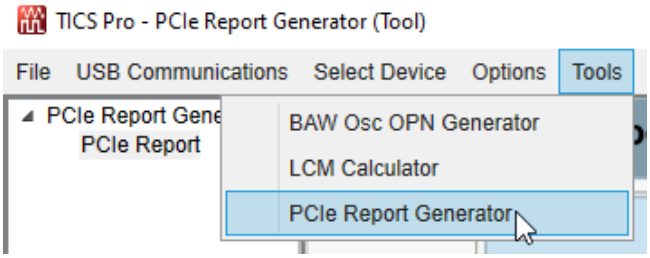

Figure 4-1. TICS Pro Steps to Access the *PCIe Reference Clock Analysis Tool*

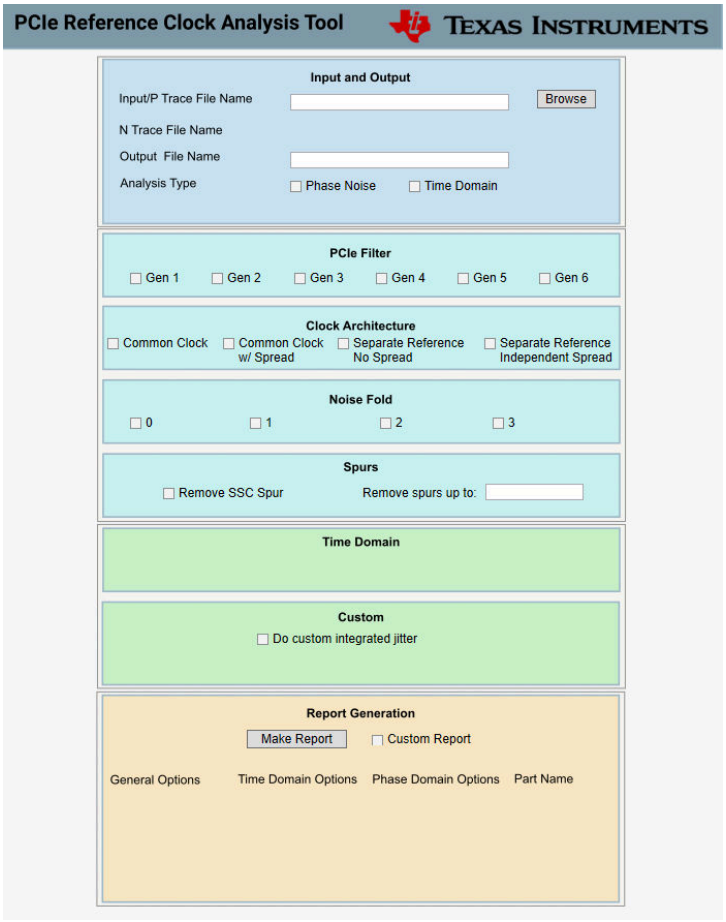

Figure 4-2. PCIe Tool Home Page

For frequency domain data analysis, the tool runs frequency domain input traces through PCIe filters, taking other parameters such as PCIe generation, clock architecture, noise fold, and presence of SSC into considerations to determine if the trace meets PCIe requirements. Then, the tool assign a PASS, FAIL, or N/A status based on the results.

For time domain data analysis, the tool runs time domain input traces, and takes into account Vcross, period, duty cycle, and other parameters specified by PCIe standards to determine and assign a PASS or FAIL to the traces being analyzed.

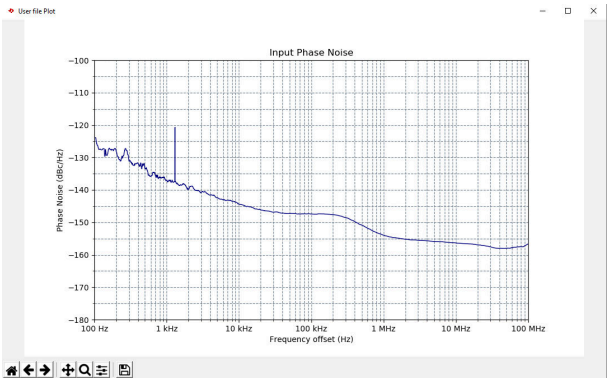

Figure 4-3. Example of PNA Plot

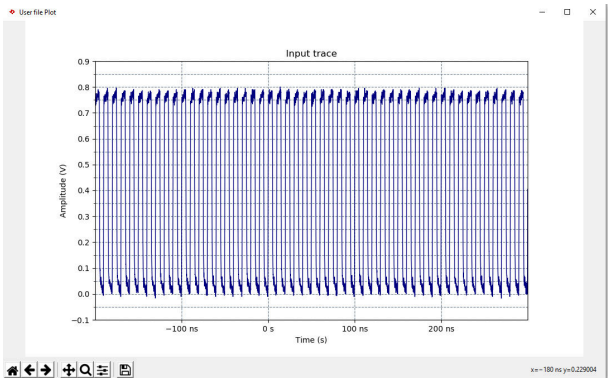

Figure 4-4. Example of Time Domain Plot

5 LMK3H0102 Test Results

The LMK3H0102 PCIe Compliance test results are detailed in this section.

5.1 LMK3H0102 Test Results Summary

Table 5-1 is the PCIe compliance results summary for the LMK3H0102 100-MHz LP-HCSL no SSC phase noise measurement. Figure 5-1 displays the phase noise capture used for the analysis.Table 5-2 is the PCIe compliance results summary for the LMK3H0102 100-MHz LP-HCSL –0.5% down-spread SSC phase noise measurement. Figure 5-2 displays the phase noise capture used for the analysis. The jitter compliance of the device for PCIe Gen 1 through 6, noise folds 0 and 3, and clock architectures Common Clock with Spread (CCS) and Separate Reference Independent Spread (SRIS) is displayed.

A PCIe jitter spec or time domain calculation can have one of the following statuses:

- PASS: within specifications/limits
- FAIL: outside specifications/limits
- N/A: no specifications/limits available

Table 5-1. Frequency Domain LMK3H0102 PCIe Tool Test Results Summary, No SSC

Jitter Filter	Clock Arch.	Noise Fold	Min (ps)	Max (ps)	Limit	Status
PCIe1[1]	CC	0	0.0	2.202	86 ps pp	PASS
		3	0.0	2.27	86 ps pp	PASS
PCIe2	CC	0	0.053	0.273	3.1 ps RMS	PASS
		3	0.101	0.279	3.1 ps RMS	PASS
	SRNS	0	0.095	0.216	N/A	N/A
		3	0.146	0.225	N/A	N/A
PCIe3	CC	0	0.024	0.082	1 ps RMS	PASS
		3	0.041	0.084	1 ps RMS	PASS
	SRNS	0	0.249	0.067	N/A	N/A
		3	0.273	0.07	N/A	N/A
PCIe4	CC	0	0.024	0.082	0.5 ps RMS	PASS
		3	0.041	0.084	0.5 ps RMS	PASS
	SRNS	0	0.17	0.067	N/A	N/A
		3	0.18	0.07	N/A	N/A
PCIe5	CC	0	0.004	0.036	0.15 ps RMS	PASS
		3	0.004	0.037	0.15 ps RMS	PASS
	SRNS	0	0.052	0.029	N/A	N/A
		3	0.053	0.030	N/A	N/A
PCIe6	CC	0	0.004	0.020	0.10 ps RMS	PASS
		3	0.008	0.020	0.10 ps RMS	PASS
	SRNS	0	0.036	0.017	N/A	N/A
		3	0.039	0.018	N/A	N/A

Table 5-2. Frequency Domain LMK3H0102 PCIe Tool Test Results Summary, –0.5% Down-Spread SSC

Jitter Filter	Clock Arch.	Noise Fold	Min (ps)	Max (ps)	Limit	Status
PCIe1[1]	CCS	0	0.0	3.886	86 ps pp	PASS
		3	0.0	4.654	86 ps pp	PASS
PCIe2	CCS	0	0.053	0.161	3.1 ps RMS	PASS
		3	0.101	0.312	3.1 ps RMS	PASS
	SRIS	0	0.095	0.169	N/A	N/A
		3	0.146	0.334	N/A	N/A
PCIe3	CCS	0	0.024	0.078	1 ps RMS	PASS
		3	0.041	0.101	1 ps RMS	PASS
	SRIS	0	0.249	0.289	N/A	N/A
		3	0.273	0.376	N/A	N/A
PCIe4	CCS	0	0.024	0.078	0.5 ps RMS	PASS
		3	0.041	0.101	0.5 ps RMS	PASS
	SRIS	0	0.17	0.185	N/A	N/A
		3	0.18	0.217	N/A	N/A
PCIe5	CCS	0	0.004	0.031	0.15 ps RMS	PASS
		3	0.004	0.04	0.15 ps RMS	PASS
	SRIS	0	0.052	0.066	N/A	N/A
		3	0.053	0.072	N/A	N/A
PCIe6	CCS	0	0.004	0.016	0.10 ps RMS	PASS
		3	0.008	0.024	0.10 ps RMS	PASS
	SRIS	0	0.036	0.047	N/A	N/A
		3	0.039	0.05	N/A	N/A

1. PCIe1 is measured using peak-to-peak jitter instead of RMS jitter using a conversion ratio of 8.83, as specified by the PCIe standard.

Table 5-3 is the PCIe compliance summary for the LMK3H0102 time domain analysis which demonstrates the time domain compliance of the device.

Table 5-3. Time Domain LMK3H0102 PCIe Tool Test Results Summary

Calculation	Min	Avg	Max	Limit	Status
V_{cross}	396.62 mV	407.61 mV	416.73 mV	250 mV to 550 mV	PASS
V_{high}	720 mV	720 mV		150 mV	PASS
V_{low}		-12.0 mV	-12.0 mV	–150 mV	PASS
Period	9.9 ns	9.996 ns	10.1 ns	9.847 ns to 10.203 ns	PASS
Duty Cycle	50.02%	50.58%	51.021%	40% to 60%	PASS
Overshoot Voltage		28.26 mV	40.0 mV	300 mV	PASS
Undershoot Voltage		-32.28 mV	-48.0 mV	–300 mV	PASS
Rising Edge Rate	2.24 V/ns	2.584 V/ns	2.92 V/ns	0.6 V/ns to 0.4 V/ns	PASS
Falling Edge Rate	2.12 V/ns	2.612 V/ns	3.08 V/ns	0.6 V/ns to 0.4 V/ns	PASS

5.2 PCIe Tool Input File Waveforms for the LMK3H0102 Family

Figure 5-1 illustrates output phase noise curve of the LMK3H0102 with a 100-MHz LP-HCSL –0.5% down-spread SSC output.Figure 5-2 illustrates output phase noise curve of the LMK3H0102 with a 100-MHz LP-HCSL –0.5% down-spread SSC output. Figure 5-3 illustrates the input trace waveform. All of these waveforms are inputted into TI's PCIe Compliance Tool (found within TI's TICS Pro Software, more information in Section 4) to determine PCIe compliance.

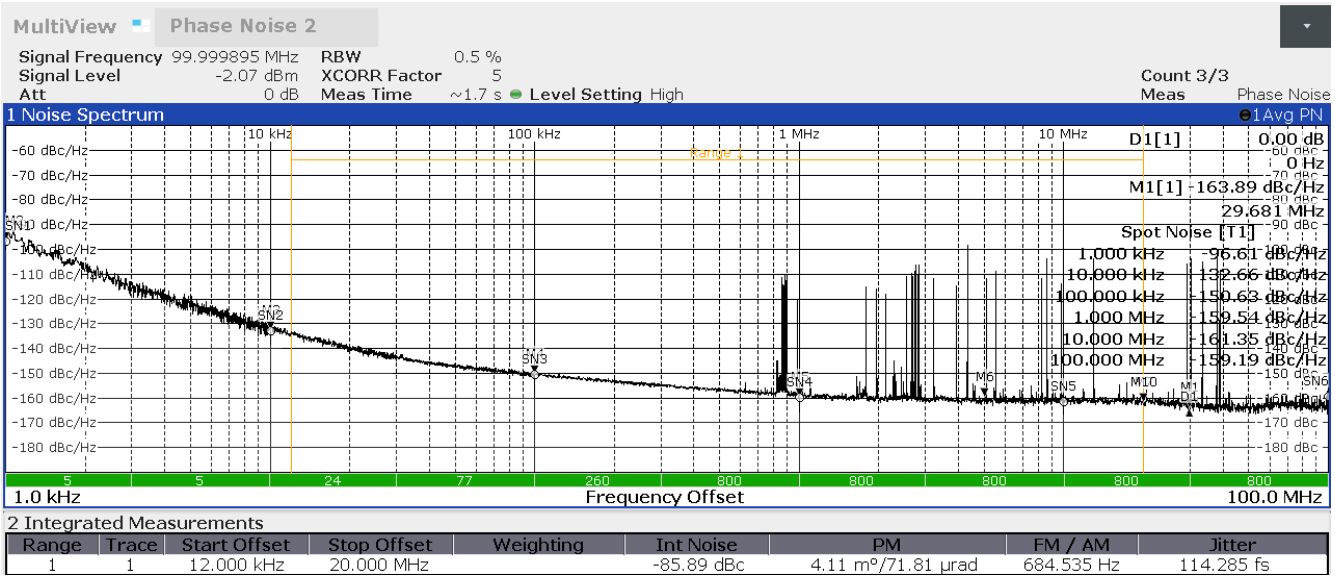

Figure 5-1. Output Phase Noise Curve from the LMK3H0102, 100-MHz LP-HCSL, No SSC

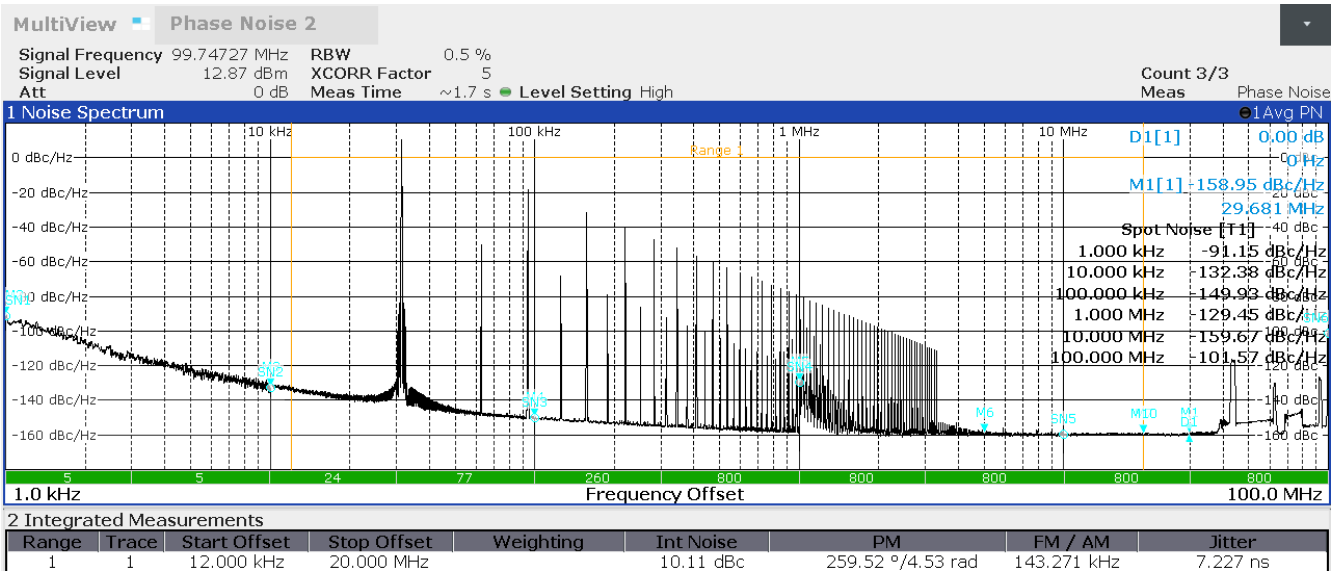

Figure 5-2. Output Phase Noise Curve from the LMK3H0102, 100-MHz LP-HCSL, –0.5% Down-Spread SSC

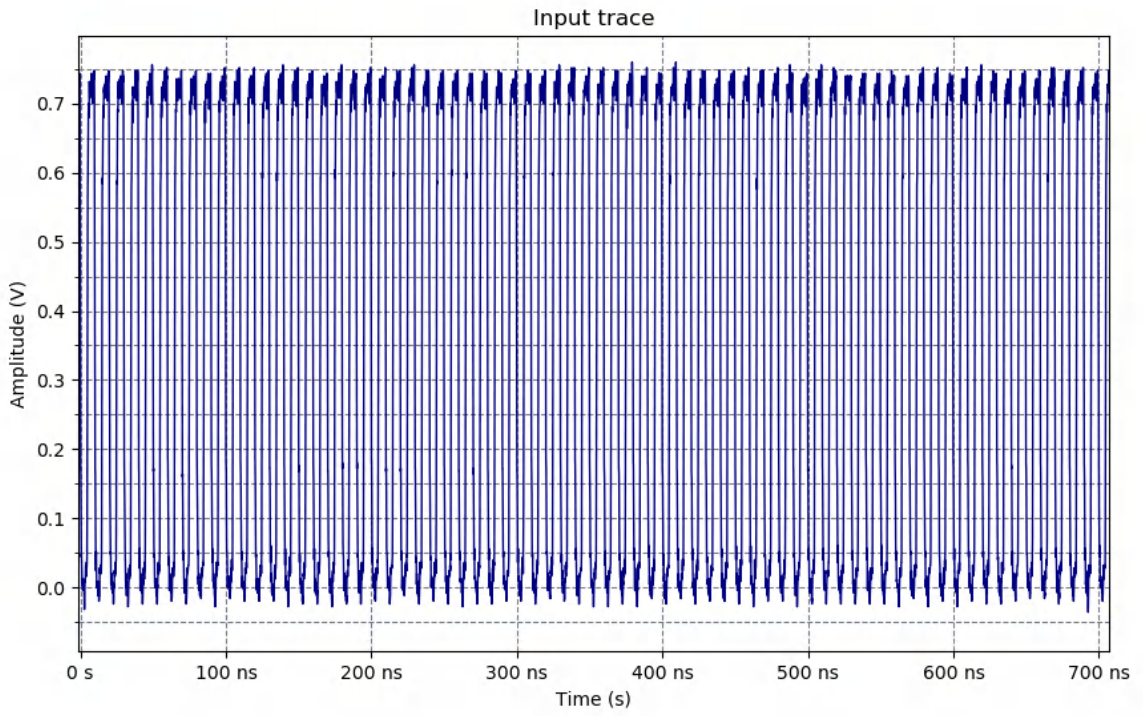

Figure 5-3. Output Time Domain Plot from the LMK3H0102

5.3 LMK3H0102 Detailed Jitter Measurements

Table 5-4 outlines specific jitter measurement results for PCIe generations 1 through 6 with noise folds 0 and 3 and clock architectures CCS and SRIS. These results are summarized in Table 5-2.

Table 5-4. LMK3H0102 Detailed Jitter Measurements

PCIe Gen	Clock Arch.	Noise Fold	Filter Comb.	f1	zeta1	f2	zeta2	f3	Value (ps)	Limit (ps)	Status
1	CCS	0	1	1.50E+06	0.54	1.50E+06	0.54	1.50E+06	0.498	86.000	PASS
1	CCS	0	2	1.50E+06	0.54	2.20E+07	0.54	1.50E+06	3.886	86.000	PASS
1	CCS	0	3	2.20E+07	0.54	1.50E+06	0.54	1.50E+06	3.886	86.000	PASS
1	CCS	0	4	2.20E+07	0.54	2.20E+07	0.54	1.50E+06	1.473	86.000	PASS
1	CCS	0	5	1.50E+06	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	6	1.50E+06	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	7	2.20E+07	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	8	2.20E+07	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	9	1.50E+06	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	10	1.50E+06	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	11	2.20E+07	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	12	2.20E+07	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	13	1.50E+06	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	14	1.50E+06	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	15	2.20E+07	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	16	2.20E+07	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	17	1.50E+06	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	18	1.50E+06	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	0	19	2.20E+07	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS

Table 5-4. LMK3H0102 Detailed Jitter Measurements (continued)

PCIe Gen	Clock Arch.	Noise Fold	Filter Comb.	f1	zeta1	f2	zeta2	f3	Value (ps)	Limit (ps)	Status
1	CCS	0	20	2.20E+07	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	1	1.50E+06	0.54	1.50E+06	0.54	1.50E+06	0.519	86.000	PASS
1	CCS	3	2	1.50E+06	0.54	2.20E+07	0.54	1.50E+06	4.654	86.000	PASS
1	CCS	3	3	2.20E+07	0.54	1.50E+06	0.54	1.50E+06	4.654	86.000	PASS
1	CCS	3	4	2.20E+07	0.54	2.20E+07	0.54	1.50E+06	2.746	86.000	PASS
1	CCS	3	5	1.50E+06	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	6	1.50E+06	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	7	2.20E+07	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	8	2.20E+07	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	9	1.50E+06	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	10	1.50E+06	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	11	2.20E+07	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	12	2.20E+07	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	13	1.50E+06	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	14	1.50E+06	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	15	2.20E+07	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	16	2.20E+07	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	17	1.50E+06	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	18	1.50E+06	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	19	2.20E+07	14	2.20E+07	0.54	1.50E+06	0	86.000	PASS
1	CCS	3	20	2.20E+07	0.54	2.20E+07	0.54	1.50E+06	0	86.000	PASS
2	CCS	0	10	5.00E+06	14	5.00E+06	14	5.00E+06	0.061	3.100	PASS
2	CCS	0	11	5.00E+06	14	5.00E+06	0.54	5.00E+06	0.082	3.100	PASS
2	CCS	0	12	5.00E+06	14	1.60E+07	14	5.00E+06	0.135	3.100	PASS
2	CCS	0	13	5.00E+06	14	1.60E+07	0.54	5.00E+06	0.127	3.100	PASS
2	CCS	0	14	5.00E+06	1.16	5.00E+06	14	5.00E+06	0.082	3.100	PASS
2	CCS	0	15	5.00E+06	1.16	5.00E+06	0.54	5.00E+06	0.053	3.100	PASS
2	CCS	0	16	5.00E+06	1.16	1.60E+07	14	5.00E+06	0.126	3.100	PASS
2	CCS	0	17	5.00E+06	1.16	1.60E+07	0.54	5.00E+06	0.114	3.100	PASS
2	CCS	0	18	1.60E+07	14	5.00E+06	14	5.00E+06	0.135	3.100	PASS
2	CCS	0	19	1.60E+07	14	5.00E+06	0.54	5.00E+06	0.124	3.100	PASS
2	CCS	0	20	1.60E+07	14	1.60E+07	14	5.00E+06	0.161	3.100	PASS
2	CCS	0	21	1.60E+07	14	1.60E+07	0.54	5.00E+06	0.155	3.100	PASS
2	CCS	0	22	1.60E+07	1.16	5.00E+06	14	5.00E+06	0.135	3.100	PASS
2	CCS	0	23	1.60E+07	1.16	5.00E+06	0.54	5.00E+06	0.121	3.100	PASS
2	CCS	0	24	1.60E+07	1.16	1.60E+07	14	5.00E+06	0.157	3.100	PASS
2	CCS	0	25	1.60E+07	1.16	1.60E+07	0.54	5.00E+06	0.145	3.100	PASS
2	CCS	3	10	5.00E+06	14	5.00E+06	14	5.00E+06	0.111	3.100	PASS
2	CCS	3	11	5.00E+06	14	5.00E+06	0.54	5.00E+06	0.120	3.100	PASS
2	CCS	3	12	5.00E+06	14	1.60E+07	14	5.00E+06	0.251	3.100	PASS
2	CCS	3	13	5.00E+06	14	1.60E+07	0.54	5.00E+06	0.232	3.100	PASS
2	CCS	3	14	5.00E+06	1.16	5.00E+06	14	5.00E+06	0.116	3.100	PASS
2	CCS	3	15	5.00E+06	1.16	5.00E+06	0.54	5.00E+06	0.101	3.100	PASS
2	CCS	3	16	5.00E+06	1.16	1.60E+07	14	5.00E+06	0.247	3.100	PASS
2	CCS	3	17	5.00E+06	1.16	1.60E+07	0.54	5.00E+06	0.232	3.100	PASS
2	CCS	3	18	1.60E+07	14	5.00E+06	14	5.00E+06	0.251	3.100	PASS

Table 5-4. LMK3H0102 Detailed Jitter Measurements (continued)

PCIe Gen	Clock Arch.	Noise Fold	Filter Comb.	f1	zeta1	f2	zeta2	f3	Value (ps)	Limit (ps)	Status
2	CCS	3	19	1.60E+07	14	5.00E+06	0.54	5.00E+06	0.250	3.100	PASS
2	CCS	3	20	1.60E+07	14	1.60E+07	14	5.00E+06	0.290	3.100	PASS
2	CCS	3	21	1.60E+07	14	1.60E+07	0.54	5.00E+06	0.312	3.100	PASS
2	CCS	3	22	1.60E+07	1.16	5.00E+06	14	5.00E+06	0.243	3.100	PASS
2	CCS	3	23	1.60E+07	1.16	5.00E+06	0.54	5.00E+06	0.245	3.100	PASS
2	CCS	3	24	1.60E+07	1.16	1.60E+07	14	5.00E+06	0.295	3.100	PASS
2	CCS	3	25	1.60E+07	1.16	1.60E+07	0.54	5.00E+06	0.289	3.100	PASS
2	SRIS	0	10	5.00E+06	14	5.00E+06	14	5.00E+06	0.099	N/A	N/A
2	SRIS	0	11	5.00E+06	14	5.00E+06	0.54	5.00E+06	0.095	N/A	N/A
2	SRIS	0	12	5.00E+06	14	1.60E+07	14	5.00E+06	0.136	N/A	N/A
2	SRIS	0	13	5.00E+06	14	1.60E+07	0.54	5.00E+06	0.137	N/A	N/A
2	SRIS	0	14	5.00E+06	1.16	5.00E+06	14	5.00E+06	0.098	N/A	N/A
2	SRIS	0	15	5.00E+06	1.16	5.00E+06	0.54	5.00E+06	0.095	N/A	N/A
2	SRIS	0	16	5.00E+06	1.16	1.60E+07	14	5.00E+06	0.134	N/A	N/A
2	SRIS	0	17	5.00E+06	1.16	1.60E+07	0.54	5.00E+06	0.135	N/A	N/A
2	SRIS	0	18	1.60E+07	14	5.00E+06	14	5.00E+06	0.136	N/A	N/A
2	SRIS	0	19	1.60E+07	14	5.00E+06	0.54	5.00E+06	0.131	N/A	N/A
2	SRIS	0	20	1.60E+07	14	1.60E+07	14	5.00E+06	0.169	N/A	N/A
2	SRIS	0	21	1.60E+07	14	1.60E+07	0.54	5.00E+06	0.164	N/A	N/A
2	SRIS	0	22	1.60E+07	1.16	5.00E+06	14	5.00E+06	0.135	N/A	N/A
2	SRIS	0	23	1.60E+07	1.16	5.00E+06	0.54	5.00E+06	0.130	N/A	N/A
2	SRIS	0	24	1.60E+07	1.16	1.60E+07	14	5.00E+06	0.167	N/A	N/A
2	SRIS	0	25	1.60E+07	1.16	1.60E+07	0.54	5.00E+06	0.165	N/A	N/A
2	SRIS	3	10	5.00E+06	14	5.00E+06	14	5.00E+06	0.166	N/A	N/A
2	SRIS	3	11	5.00E+06	14	5.00E+06	0.54	5.00E+06	0.149	N/A	N/A
2	SRIS	3	12	5.00E+06	14	1.60E+07	14	5.00E+06	0.250	N/A	N/A
2	SRIS	3	13	5.00E+06	14	1.60E+07	0.54	5.00E+06	0.272	N/A	N/A
2	SRIS	3	14	5.00E+06	1.16	5.00E+06	14	5.00E+06	0.161	N/A	N/A
2	SRIS	3	15	5.00E+06	1.16	5.00E+06	0.54	5.00E+06	0.146	N/A	N/A
2	SRIS	3	16	5.00E+06	1.16	1.60E+07	14	5.00E+06	0.245	N/A	N/A
2	SRIS	3	17	5.00E+06	1.16	1.60E+07	0.54	5.00E+06	0.267	N/A	N/A
2	SRIS	3	18	1.60E+07	14	5.00E+06	14	5.00E+06	0.250	N/A	N/A
2	SRIS	3	19	1.60E+07	14	5.00E+06	0.54	5.00E+06	0.236	N/A	N/A
2	SRIS	3	20	1.60E+07	14	1.60E+07	14	5.00E+06	0.324	N/A	N/A
2	SRIS	3	21	1.60E+07	14	1.60E+07	0.54	5.00E+06	0.326	N/A	N/A
2	SRIS	3	22	1.60E+07	1.16	5.00E+06	14	5.00E+06	0.255	N/A	N/A
2	SRIS	3	23	1.60E+07	1.16	5.00E+06	0.54	5.00E+06	0.239	N/A	N/A
2	SRIS	3	24	1.60E+07	1.16	1.60E+07	14	5.00E+06	0.324	N/A	N/A
2	SRIS	3	25	1.60E+07	1.16	1.60E+07	0.54	5.00E+06	0.334	N/A	N/A
3	CCS	0	1	2.00E+06	14	2.00E+06	14	1.00E+07	0.024	1.000	PASS
3	CCS	0	2	2.00E+06	14	2.00E+06	1.15	1.00E+07	0.061	1.000	PASS
3	CCS	0	3	2.00E+06	14	5.00E+06	14	1.00E+07	0.063	1.000	PASS
3	CCS	0	4	2.00E+06	14	5.00E+06	1.15	1.00E+07	0.078	1.000	PASS
3	CCS	0	5	2.00E+06	0.73	2.00E+06	14	1.00E+07	0.070	1.000	PASS
3	CCS	0	6	2.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.032	1.000	PASS
3	CCS	0	7	2.00E+06	0.73	5.00E+06	14	1.00E+07	0.057	1.000	PASS

Table 5-4. LMK3H0102 Detailed Jitter Measurements (continued)

PCIe Gen	Clock Arch.	Noise Fold	Filter Comb.	f1	zeta1	f2	zeta2	f3	Value (ps)	Limit (ps)	Status
3	CCS	0	8	2.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.053	1.000	PASS
3	CCS	0	9	4.00E+06	14	2.00E+06	14	1.00E+07	0.054	1.000	PASS
3	CCS	0	10	4.00E+06	14	2.00E+06	1.15	1.00E+07	0.052	1.000	PASS
3	CCS	0	11	4.00E+06	14	5.00E+06	14	1.00E+07	0.052	1.000	PASS
3	CCS	0	12	4.00E+06	14	5.00E+06	1.15	1.00E+07	0.059	1.000	PASS
3	CCS	0	13	4.00E+06	0.73	2.00E+06	14	1.00E+07	0.075	1.000	PASS
3	CCS	0	14	4.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.055	1.000	PASS
3	CCS	0	15	4.00E+06	0.73	5.00E+06	14	1.00E+07	0.053	1.000	PASS
3	CCS	0	16	4.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.043	1.000	PASS
3	CCS	3	1	2.00E+06	14	2.00E+06	14	1.00E+07	0.043	1.000	PASS
3	CCS	3	2	2.00E+06	14	2.00E+06	1.15	1.00E+07	0.069	1.000	PASS
3	CCS	3	3	2.00E+06	14	5.00E+06	14	1.00E+07	0.097	1.000	PASS
3	CCS	3	4	2.00E+06	14	5.00E+06	1.15	1.00E+07	0.101	1.000	PASS
3	CCS	3	5	2.00E+06	0.73	2.00E+06	14	1.00E+07	0.076	1.000	PASS
3	CCS	3	6	2.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.041	1.000	PASS
3	CCS	3	7	2.00E+06	0.73	5.00E+06	14	1.00E+07	0.094	1.000	PASS
3	CCS	3	8	2.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.084	1.000	PASS
3	CCS	3	9	4.00E+06	14	2.00E+06	14	1.00E+07	0.081	1.000	PASS
3	CCS	3	10	4.00E+06	14	2.00E+06	1.15	1.00E+07	0.080	1.000	PASS
3	CCS	3	11	4.00E+06	14	5.00E+06	14	1.00E+07	0.096	1.000	PASS
3	CCS	3	12	4.00E+06	14	5.00E+06	1.15	1.00E+07	0.091	1.000	PASS
3	CCS	3	13	4.00E+06	0.73	2.00E+06	14	1.00E+07	0.087	1.000	PASS
3	CCS	3	14	4.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.071	1.000	PASS
3	CCS	3	15	4.00E+06	0.73	5.00E+06	14	1.00E+07	0.094	1.000	PASS
3	CCS	3	16	4.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.081	1.000	PASS
3	SRIS	0	1	2.00E+06	14	2.00E+06	14	1.00E+07	0.249	N/A	N/A
3	SRIS	0	2	2.00E+06	14	2.00E+06	1.15	1.00E+07	0.256	N/A	N/A
3	SRIS	0	3	2.00E+06	14	5.00E+06	14	1.00E+07	0.274	N/A	N/A
3	SRIS	0	4	2.00E+06	14	5.00E+06	1.15	1.00E+07	0.269	N/A	N/A
3	SRIS	0	5	2.00E+06	0.73	2.00E+06	14	1.00E+07	0.255	N/A	N/A
3	SRIS	0	6	2.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.263	N/A	N/A
3	SRIS	0	7	2.00E+06	0.73	5.00E+06	14	1.00E+07	0.280	N/A	N/A
3	SRIS	0	8	2.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.275	N/A	N/A
3	SRIS	0	9	4.00E+06	14	2.00E+06	14	1.00E+07	0.264	N/A	N/A
3	SRIS	0	10	4.00E+06	14	2.00E+06	1.15	1.00E+07	0.271	N/A	N/A
3	SRIS	0	11	4.00E+06	14	5.00E+06	14	1.00E+07	0.289	N/A	N/A
3	SRIS	0	12	4.00E+06	14	5.00E+06	1.15	1.00E+07	0.284	N/A	N/A
3	SRIS	0	13	4.00E+06	0.73	2.00E+06	14	1.00E+07	0.258	N/A	N/A
3	SRIS	0	14	4.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.265	N/A	N/A
3	SRIS	0	15	4.00E+06	0.73	5.00E+06	14	1.00E+07	0.283	N/A	N/A
3	SRIS	0	16	4.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.279	N/A	N/A
3	SRIS	3	1	2.00E+06	14	2.00E+06	14	1.00E+07	0.273	N/A	N/A
3	SRIS	3	2	2.00E+06	14	2.00E+06	1.15	1.00E+07	0.276	N/A	N/A
3	SRIS	3	3	2.00E+06	14	5.00E+06	14	1.00E+07	0.340	N/A	N/A
3	SRIS	3	4	2.00E+06	14	5.00E+06	1.15	1.00E+07	0.324	N/A	N/A
3	SRIS	3	5	2.00E+06	0.73	2.00E+06	14	1.00E+07	0.273	N/A	N/A

Table 5-4. LMK3H0102 Detailed Jitter Measurements (continued)

PCIe Gen	Clock Arch.	Noise Fold	Filter Comb.	f1	zeta1	f2	zeta2	f3	Value (ps)	Limit (ps)	Status
3	SRIS	3	6	2.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.277	N/A	N/A
3	SRIS	3	7	2.00E+06	0.73	5.00E+06	14	1.00E+07	0.340	N/A	N/A
3	SRIS	3	8	2.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.324	N/A	N/A
3	SRIS	3	9	4.00E+06	14	2.00E+06	14	1.00E+07	0.314	N/A	N/A
3	SRIS	3	10	4.00E+06	14	2.00E+06	1.15	1.00E+07	0.317	N/A	N/A
3	SRIS	3	11	4.00E+06	14	5.00E+06	14	1.00E+07	0.376	N/A	N/A
3	SRIS	3	12	4.00E+06	14	5.00E+06	1.15	1.00E+07	0.361	N/A	N/A
3	SRIS	3	13	4.00E+06	0.73	2.00E+06	14	1.00E+07	0.292	N/A	N/A
3	SRIS	3	14	4.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.295	N/A	N/A
3	SRIS	3	15	4.00E+06	0.73	5.00E+06	14	1.00E+07	0.355	N/A	N/A
3	SRIS	3	16	4.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.341	N/A	N/A
4	CCS	0	1	2.00E+06	14	2.00E+06	14	1.00E+07	0.024	0.500	PASS
4	CCS	0	2	2.00E+06	14	2.00E+06	1.15	1.00E+07	0.061	0.500	PASS
4	CCS	0	3	2.00E+06	14	5.00E+06	14	1.00E+07	0.063	0.500	PASS
4	CCS	0	4	2.00E+06	14	5.00E+06	1.15	1.00E+07	0.078	0.500	PASS
4	CCS	0	5	2.00E+06	0.73	2.00E+06	14	1.00E+07	0.070	0.500	PASS
4	CCS	0	6	2.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.032	0.500	PASS
4	CCS	0	7	2.00E+06	0.73	5.00E+06	14	1.00E+07	0.057	0.500	PASS
4	CCS	0	8	2.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.053	0.500	PASS
4	CCS	0	9	4.00E+06	14	2.00E+06	14	1.00E+07	0.054	0.500	PASS
4	CCS	0	10	4.00E+06	14	2.00E+06	1.15	1.00E+07	0.052	0.500	PASS
4	CCS	0	11	4.00E+06	14	5.00E+06	14	1.00E+07	0.052	0.500	PASS
4	CCS	0	12	4.00E+06	14	5.00E+06	1.15	1.00E+07	0.059	0.500	PASS
4	CCS	0	13	4.00E+06	0.73	2.00E+06	14	1.00E+07	0.075	0.500	PASS
4	CCS	0	14	4.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.055	0.500	PASS
4	CCS	0	15	4.00E+06	0.73	5.00E+06	14	1.00E+07	0.053	0.500	PASS
4	CCS	0	16	4.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.043	0.500	PASS
4	CCS	3	1	2.00E+06	14	2.00E+06	14	1.00E+07	0.043	0.500	PASS
4	CCS	3	2	2.00E+06	14	2.00E+06	1.15	1.00E+07	0.069	0.500	PASS
4	CCS	3	3	2.00E+06	14	5.00E+06	14	1.00E+07	0.097	0.500	PASS
4	CCS	3	4	2.00E+06	14	5.00E+06	1.15	1.00E+07	0.101	0.500	PASS
4	CCS	3	5	2.00E+06	0.73	2.00E+06	14	1.00E+07	0.076	0.500	PASS
4	CCS	3	6	2.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.041	0.500	PASS
4	CCS	3	7	2.00E+06	0.73	5.00E+06	14	1.00E+07	0.094	0.500	PASS
4	CCS	3	8	2.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.084	0.500	PASS
4	CCS	3	9	4.00E+06	14	2.00E+06	14	1.00E+07	0.081	0.500	PASS
4	CCS	3	10	4.00E+06	14	2.00E+06	1.15	1.00E+07	0.080	0.500	PASS
4	CCS	3	11	4.00E+06	14	5.00E+06	14	1.00E+07	0.096	0.500	PASS
4	CCS	3	12	4.00E+06	14	5.00E+06	1.15	1.00E+07	0.091	0.500	PASS
4	CCS	3	13	4.00E+06	0.73	2.00E+06	14	1.00E+07	0.087	0.500	PASS
4	CCS	3	14	4.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.071	0.500	PASS
4	CCS	3	15	4.00E+06	0.73	5.00E+06	14	1.00E+07	0.094	0.500	PASS
4	CCS	3	16	4.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.081	0.500	PASS
4	SRIS	0	1	2.00E+06	14	2.00E+06	14	1.00E+07	0.170	N/A	N/A
4	SRIS	0	2	2.00E+06	14	2.00E+06	1.15	1.00E+07	0.177	N/A	N/A
4	SRIS	0	3	2.00E+06	14	5.00E+06	14	1.00E+07	0.176	N/A	N/A

Table 5-4. LMK3H0102 Detailed Jitter Measurements (continued)

PCIe Gen	Clock Arch.	Noise Fold	Filter Comb.	f1	zeta1	f2	zeta2	f3	Value (ps)	Limit (ps)	Status
4	SRIS	0	4	2.00E+06	14	5.00E+06	1.15	1.00E+07	0.177	N/A	N/A
4	SRIS	0	5	2.00E+06	0.73	2.00E+06	14	1.00E+07	0.178	N/A	N/A
4	SRIS	0	6	2.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.185	N/A	N/A
4	SRIS	0	7	2.00E+06	0.73	5.00E+06	14	1.00E+07	0.184	N/A	N/A
4	SRIS	0	8	2.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.185	N/A	N/A
4	SRIS	0	9	4.00E+06	14	2.00E+06	14	1.00E+07	0.174	N/A	N/A
4	SRIS	0	10	4.00E+06	14	2.00E+06	1.15	1.00E+07	0.181	N/A	N/A
4	SRIS	0	11	4.00E+06	14	5.00E+06	14	1.00E+07	0.181	N/A	N/A
4	SRIS	0	12	4.00E+06	14	5.00E+06	1.15	1.00E+07	0.182	N/A	N/A
4	SRIS	0	13	4.00E+06	0.73	2.00E+06	14	1.00E+07	0.175	N/A	N/A
4	SRIS	0	14	4.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.182	N/A	N/A
4	SRIS	0	15	4.00E+06	0.73	5.00E+06	14	1.00E+07	0.182	N/A	N/A
4	SRIS	0	16	4.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.184	N/A	N/A
4	SRIS	3	1	2.00E+06	14	2.00E+06	14	1.00E+07	0.180	N/A	N/A
4	SRIS	3	2	2.00E+06	14	2.00E+06	1.15	1.00E+07	0.185	N/A	N/A
4	SRIS	3	3	2.00E+06	14	5.00E+06	14	1.00E+07	0.203	N/A	N/A
4	SRIS	3	4	2.00E+06	14	5.00E+06	1.15	1.00E+07	0.200	N/A	N/A
4	SRIS	3	5	2.00E+06	0.73	2.00E+06	14	1.00E+07	0.185	N/A	N/A
4	SRIS	3	6	2.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.191	N/A	N/A
4	SRIS	3	7	2.00E+06	0.73	5.00E+06	14	1.00E+07	0.207	N/A	N/A
4	SRIS	3	8	2.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.205	N/A	N/A
4	SRIS	3	9	4.00E+06	14	2.00E+06	14	1.00E+07	0.195	N/A	N/A
4	SRIS	3	10	4.00E+06	14	2.00E+06	1.15	1.00E+07	0.199	N/A	N/A
4	SRIS	3	11	4.00E+06	14	5.00E+06	14	1.00E+07	0.217	N/A	N/A
4	SRIS	3	12	4.00E+06	14	5.00E+06	1.15	1.00E+07	0.215	N/A	N/A
4	SRIS	3	13	4.00E+06	0.73	2.00E+06	14	1.00E+07	0.190	N/A	N/A
4	SRIS	3	14	4.00E+06	0.73	2.00E+06	1.15	1.00E+07	0.195	N/A	N/A
4	SRIS	3	15	4.00E+06	0.73	5.00E+06	14	1.00E+07	0.212	N/A	N/A
4	SRIS	3	16	4.00E+06	0.73	5.00E+06	1.15	1.00E+07	0.211	N/A	N/A
5	CCS	0	1	5.00E+05	14	5.00E+05	14	2.00E+07	0.006	0.150	PASS
5	CCS	0	2	5.00E+05	14	5.00E+05	0.73	2.00E+07	0.013	0.150	PASS
5	CCS	0	3	5.00E+05	14	1.80E+06	14	2.00E+07	0.022	0.150	PASS
5	CCS	0	4	5.00E+05	14	1.80E+06	0.73	2.00E+07	0.024	0.150	PASS
5	CCS	0	5	5.00E+05	0.73	5.00E+05	14	2.00E+07	0.013	0.150	PASS
5	CCS	0	6	5.00E+05	0.73	5.00E+05	0.73	2.00E+07	0.004	0.150	PASS
5	CCS	0	7	5.00E+05	0.73	1.80E+06	14	2.00E+07	0.028	0.150	PASS
5	CCS	0	8	5.00E+05	0.73	1.80E+06	0.73	2.00E+07	0.031	0.150	PASS
5	CCS	0	9	1.80E+06	14	5.00E+05	14	2.00E+07	0.022	0.150	PASS
5	CCS	0	10	1.80E+06	14	5.00E+05	0.73	2.00E+07	0.028	0.150	PASS
5	CCS	0	11	1.80E+06	14	1.80E+06	14	2.00E+07	0.022	0.150	PASS
5	CCS	0	12	1.80E+06	14	1.80E+06	0.73	2.00E+07	0.020	0.150	PASS
5	CCS	0	13	1.80E+06	0.73	5.00E+05	14	2.00E+07	0.024	0.150	PASS
5	CCS	0	14	1.80E+06	0.73	5.00E+05	0.73	2.00E+07	0.031	0.150	PASS
5	CCS	0	15	1.80E+06	0.73	1.80E+06	14	2.00E+07	0.020	0.150	PASS
5	CCS	0	16	1.80E+06	0.73	1.80E+06	0.73	2.00E+07	0.015	0.150	PASS
5	CCS	3	1	5.00E+05	14	5.00E+05	14	2.00E+07	0.011	0.150	PASS

Table 5-4. LMK3H0102 Detailed Jitter Measurements (continued)

PCIe Gen	Clock Arch.	Noise Fold	Filter Comb.	f1	zeta1	f2	zeta2	f3	Value (ps)	Limit (ps)	Status
5	CCS	3	2	5.00E+05	14	5.00E+05	0.73	2.00E+07	0.016	0.150	PASS
5	CCS	3	3	5.00E+05	14	1.80E+06	14	2.00E+07	0.034	0.150	PASS
5	CCS	3	4	5.00E+05	14	1.80E+06	0.73	2.00E+07	0.031	0.150	PASS
5	CCS	3	5	5.00E+05	0.73	5.00E+05	14	2.00E+07	0.016	0.150	PASS
5	CCS	3	6	5.00E+05	0.73	5.00E+05	0.73	2.00E+07	0.008	0.150	PASS
5	CCS	3	7	5.00E+05	0.73	1.80E+06	14	2.00E+07	0.038	0.150	PASS
5	CCS	3	8	5.00E+05	0.73	1.80E+06	0.73	2.00E+07	0.036	0.150	PASS
5	CCS	3	9	1.80E+06	14	5.00E+05	14	2.00E+07	0.034	0.150	PASS
5	CCS	3	10	1.80E+06	14	5.00E+05	0.73	2.00E+07	0.038	0.150	PASS
5	CCS	3	11	1.80E+06	14	1.80E+06	14	2.00E+07	0.040	0.150	PASS
5	CCS	3	12	1.80E+06	14	1.80E+06	0.73	2.00E+07	0.036	0.150	PASS
5	CCS	3	13	1.80E+06	0.73	5.00E+05	14	2.00E+07	0.031	0.150	PASS
5	CCS	3	14	1.80E+06	0.73	5.00E+05	0.73	2.00E+07	0.036	0.150	PASS
5	CCS	3	15	1.80E+06	0.73	1.80E+06	14	2.00E+07	0.036	0.150	PASS
5	CCS	3	16	1.80E+06	0.73	1.80E+06	0.73	2.00E+07	0.028	0.150	PASS
5	SRIS	0	1	5.00E+05	14	5.00E+05	14	2.00E+07	0.052	N/A	N/A
5	SRIS	0	2	5.00E+05	14	5.00E+05	0.73	2.00E+07	0.058	N/A	N/A
5	SRIS	0	3	5.00E+05	14	1.80E+06	14	2.00E+07	0.056	N/A	N/A
5	SRIS	0	4	5.00E+05	14	1.80E+06	0.73	2.00E+07	0.057	N/A	N/A
5	SRIS	0	5	5.00E+05	0.73	5.00E+05	14	2.00E+07	0.058	N/A	N/A
5	SRIS	0	6	5.00E+05	0.73	5.00E+05	0.73	2.00E+07	0.064	N/A	N/A
5	SRIS	0	7	5.00E+05	0.73	1.80E+06	14	2.00E+07	0.060	N/A	N/A
5	SRIS	0	8	5.00E+05	0.73	1.80E+06	0.73	2.00E+07	0.061	N/A	N/A
5	SRIS	0	9	1.80E+06	14	5.00E+05	14	2.00E+07	0.056	N/A	N/A
5	SRIS	0	10	1.80E+06	14	5.00E+05	0.73	2.00E+07	0.060	N/A	N/A
5	SRIS	0	11	1.80E+06	14	1.80E+06	14	2.00E+07	0.062	N/A	N/A
5	SRIS	0	12	1.80E+06	14	1.80E+06	0.73	2.00E+07	0.064	N/A	N/A
5	SRIS	0	13	1.80E+06	0.73	5.00E+05	14	2.00E+07	0.057	N/A	N/A
5	SRIS	0	14	1.80E+06	0.73	5.00E+05	0.73	2.00E+07	0.061	N/A	N/A
5	SRIS	0	15	1.80E+06	0.73	1.80E+06	14	2.00E+07	0.064	N/A	N/A
5	SRIS	0	16	1.80E+06	0.73	1.80E+06	0.73	2.00E+07	0.066	N/A	N/A
5	SRIS	3	1	5.00E+05	14	5.00E+05	14	2.00E+07	0.053	N/A	N/A
5	SRIS	3	2	5.00E+05	14	5.00E+05	0.73	2.00E+07	0.058	N/A	N/A
5	SRIS	3	3	5.00E+05	14	1.80E+06	14	2.00E+07	0.062	N/A	N/A
5	SRIS	3	4	5.00E+05	14	1.80E+06	0.73	2.00E+07	0.061	N/A	N/A
5	SRIS	3	5	5.00E+05	0.73	5.00E+05	14	2.00E+07	0.058	N/A	N/A
5	SRIS	3	6	5.00E+05	0.73	5.00E+05	0.73	2.00E+07	0.064	N/A	N/A
5	SRIS	3	7	5.00E+05	0.73	1.80E+06	14	2.00E+07	0.065	N/A	N/A
5	SRIS	3	8	5.00E+05	0.73	1.80E+06	0.73	2.00E+07	0.064	N/A	N/A
5	SRIS	3	9	1.80E+06	14	5.00E+05	14	2.00E+07	0.062	N/A	N/A
5	SRIS	3	10	1.80E+06	14	5.00E+05	0.73	2.00E+07	0.065	N/A	N/A
5	SRIS	3	11	1.80E+06	14	1.80E+06	14	2.00E+07	0.072	N/A	N/A
5	SRIS	3	12	1.80E+06	14	1.80E+06	0.73	2.00E+07	0.071	N/A	N/A
5	SRIS	3	13	1.80E+06	0.73	5.00E+05	14	2.00E+07	0.061	N/A	N/A
5	SRIS	3	14	1.80E+06	0.73	5.00E+05	0.73	2.00E+07	0.064	N/A	N/A
5	SRIS	3	15	1.80E+06	0.73	1.80E+06	14	2.00E+07	0.071	N/A	N/A

Table 5-4. LMK3H0102 Detailed Jitter Measurements (continued)

PCIe Gen	Clock Arch.	Noise Fold	Filter Comb.	f1	zeta1	f2	zeta2	f3	Value (ps)	Limit (ps)	Status
5	SRIS	3	16	1.80E+06	0.73	1.80E+06	0.73	2.00E+07	0.071	N/A	N/A
6	CCS	0	1	5.00E+05	14	5.00E+05	14	1.00E+07	0.006	0.100	PASS
6	CCS	0	2	5.00E+05	14	5.00E+05	0.73	1.00E+07	0.010	0.100	PASS
6	CCS	0	3	5.00E+05	14	1.00E+06	14	1.00E+07	0.012	0.100	PASS
6	CCS	0	4	5.00E+05	14	1.00E+06	0.73	1.00E+07	0.013	0.100	PASS
6	CCS	0	5	5.00E+05	0.73	5.00E+05	14	1.00E+07	0.010	0.100	PASS
6	CCS	0	6	5.00E+05	0.73	5.00E+05	0.73	1.00E+07	0.004	0.100	PASS
6	CCS	0	7	5.00E+05	0.73	1.00E+06	14	1.00E+07	0.016	0.100	PASS
6	CCS	0	8	5.00E+05	0.73	1.00E+06	0.73	1.00E+07	0.016	0.100	PASS
6	CCS	0	9	1.00E+06	14	5.00E+05	14	1.00E+07	0.012	0.100	PASS
6	CCS	0	10	1.00E+06	14	5.00E+05	0.73	1.00E+07	0.016	0.100	PASS
6	CCS	0	11	1.00E+06	14	1.00E+06	14	1.00E+07	0.012	0.100	PASS
6	CCS	0	12	1.00E+06	14	1.00E+06	0.73	1.00E+07	0.013	0.100	PASS
6	CCS	0	13	1.00E+06	0.73	5.00E+05	14	1.00E+07	0.013	0.100	PASS
6	CCS	0	14	1.00E+06	0.73	5.00E+05	0.73	1.00E+07	0.016	0.100	PASS
6	CCS	0	15	1.00E+06	0.73	1.00E+06	14	1.00E+07	0.013	0.100	PASS
6	CCS	0	16	1.00E+06	0.73	1.00E+06	0.73	1.00E+07	0.009	0.100	PASS
6	CCS	3	1	5.00E+05	14	5.00E+05	14	1.00E+07	0.012	0.100	PASS
6	CCS	3	2	5.00E+05	14	5.00E+05	0.73	1.00E+07	0.014	0.100	PASS
6	CCS	3	3	5.00E+05	14	1.00E+06	14	1.00E+07	0.022	0.100	PASS
6	CCS	3	4	5.00E+05	14	1.00E+06	0.73	1.00E+07	0.019	0.100	PASS
6	CCS	3	5	5.00E+05	0.73	5.00E+05	14	1.00E+07	0.014	0.100	PASS
6	CCS	3	6	5.00E+05	0.73	5.00E+05	0.73	1.00E+07	0.008	0.100	PASS
6	CCS	3	7	5.00E+05	0.73	1.00E+06	14	1.00E+07	0.024	0.100	PASS
6	CCS	3	8	5.00E+05	0.73	1.00E+06	0.73	1.00E+07	0.020	0.100	PASS
6	CCS	3	9	1.00E+06	14	5.00E+05	14	1.00E+07	0.022	0.100	PASS
6	CCS	3	10	1.00E+06	14	5.00E+05	0.73	1.00E+07	0.024	0.100	PASS
6	CCS	3	11	1.00E+06	14	1.00E+06	14	1.00E+07	0.024	0.100	PASS
6	CCS	3	12	1.00E+06	14	1.00E+06	0.73	1.00E+07	0.023	0.100	PASS
6	CCS	3	13	1.00E+06	0.73	5.00E+05	14	1.00E+07	0.019	0.100	PASS
6	CCS	3	14	1.00E+06	0.73	5.00E+05	0.73	1.00E+07	0.020	0.100	PASS
6	CCS	3	15	1.00E+06	0.73	1.00E+06	14	1.00E+07	0.023	0.100	PASS
6	CCS	3	16	1.00E+06	0.73	1.00E+06	0.73	1.00E+07	0.017	0.100	PASS
6	SRIS	0	1	5.00E+05	14	5.00E+05	14	1.00E+07	0.036	N/A	N/A
6	SRIS	0	2	5.00E+05	14	5.00E+05	0.73	1.00E+07	0.040	N/A	N/A
6	SRIS	0	3	5.00E+05	14	1.00E+06	14	1.00E+07	0.039	N/A	N/A
6	SRIS	0	4	5.00E+05	14	1.00E+06	0.73	1.00E+07	0.041	N/A	N/A
6	SRIS	0	5	5.00E+05	0.73	5.00E+05	14	1.00E+07	0.040	N/A	N/A
6	SRIS	0	6	5.00E+05	0.73	5.00E+05	0.73	1.00E+07	0.045	N/A	N/A
6	SRIS	0	7	5.00E+05	0.73	1.00E+06	14	1.00E+07	0.042	N/A	N/A
6	SRIS	0	8	5.00E+05	0.73	1.00E+06	0.73	1.00E+07	0.044	N/A	N/A
6	SRIS	0	9	1.00E+06	14	5.00E+05	14	1.00E+07	0.039	N/A	N/A
6	SRIS	0	10	1.00E+06	14	5.00E+05	0.73	1.00E+07	0.042	N/A	N/A
6	SRIS	0	11	1.00E+06	14	1.00E+06	14	1.00E+07	0.041	N/A	N/A
6	SRIS	0	12	1.00E+06	14	1.00E+06	0.73	1.00E+07	0.044	N/A	N/A
6	SRIS	0	13	1.00E+06	0.73	5.00E+05	14	1.00E+07	0.041	N/A	N/A

Table 5-4. LMK3H0102 Detailed Jitter Measurements (continued)

PCIe Gen	Clock Arch.	Noise Fold	Filter Comb.	f1	zeta1	f2	zeta2	f3	Value (ps)	Limit (ps)	Status
6	SRIS	0	14	1.00E+06	0.73	5.00E+05	0.73	1.00E+07	0.044	N/A	N/A
6	SRIS	0	15	1.00E+06	0.73	1.00E+06	14	1.00E+07	0.044	N/A	N/A
6	SRIS	0	16	1.00E+06	0.73	1.00E+06	0.73	1.00E+07	0.047	N/A	N/A
6	SRIS	3	1	5.00E+05	14	5.00E+05	14	1.00E+07	0.039	N/A	N/A
6	SRIS	3	2	5.00E+05	14	5.00E+05	0.73	1.00E+07	0.042	N/A	N/A
6	SRIS	3	3	5.00E+05	14	1.00E+06	14	1.00E+07	0.044	N/A	N/A
6	SRIS	3	4	5.00E+05	14	1.00E+06	0.73	1.00E+07	0.044	N/A	N/A
6	SRIS	3	5	5.00E+05	0.73	5.00E+05	14	1.00E+07	0.042	N/A	N/A
6	SRIS	3	6	5.00E+05	0.73	5.00E+05	0.73	1.00E+07	0.046	N/A	N/A
6	SRIS	3	7	5.00E+05	0.73	1.00E+06	14	1.00E+07	0.047	N/A	N/A
6	SRIS	3	8	5.00E+05	0.73	1.00E+06	0.73	1.00E+07	0.047	N/A	N/A
6	SRIS	3	9	1.00E+06	14	5.00E+05	14	1.00E+07	0.044	N/A	N/A
6	SRIS	3	10	1.00E+06	14	5.00E+05	0.73	1.00E+07	0.047	N/A	N/A
6	SRIS	3	11	1.00E+06	14	1.00E+06	14	1.00E+07	0.050	N/A	N/A
6	SRIS	3	12	1.00E+06	14	1.00E+06	0.73	1.00E+07	0.050	N/A	N/A
6	SRIS	3	13	1.00E+06	0.73	5.00E+05	14	1.00E+07	0.044	N/A	N/A
6	SRIS	3	14	1.00E+06	0.73	5.00E+05	0.73	1.00E+07	0.047	N/A	N/A
6	SRIS	3	15	1.00E+06	0.73	1.00E+06	14	1.00E+07	0.050	N/A	N/A
6	SRIS	3	16	1.00E+06	0.73	1.00E+06	0.73	1.00E+07	0.050	N/A	N/A

6 Summary

This report outlines TI's PCIe Compliance Tool, how the test results are obtained, and demonstrates PCIe compliance based on the results in Section 5.1. This report demonstrates that the LMK3H0102 clock generator family is an excellent choice for the PCIe REFCLK in enterprise systems.

7 References

- Texas Instruments, *LMK3H0102 Dual Output Reference-less PCIe Gen 1 to Gen 6 Clock Generator*, data sheet.
- Texas Instruments, *TICSPRO-SW*, Clocks and Synthesizers (TICS) Pro Software.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265