TUSB8044AEVM User's guide

TI's TUSB8044AEVM evaluation module (EVM) is a functional board design that implements both a USB 3.0 hub and a USB 2.0 hub. The EVM can support both USB SuperSpeed (SS) and USB 2.0 high-speed (HS), full-speed (FS), or low-speed (LS) operation on its USB ports. The EVM enumerates a *Billboard* device on a virtual downstream port for USB Type-C™ applications with alternate mode support. It has an I^2C Master controllable through an HID-compliant device enumerated on a virtual downstream port. This EVM is intended for use in evaluating system compatibility, developing optional EEPROM firmware, and validating interoperability. This EVM also acts as a hardware reference design for any implementation of the TUSB8044.

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1 Introduction

Upon request, layout files for the EVM can be provided to illustrate techniques used to route the differential pairs, use of split power planes, placement of filters and other critical components, and methods used to achieve length matching of critical signals.

NOTE: The EVM accommodates various lab test components; actual production implementations can be much smaller.

Figure 1 illustrates the *TUSB8044AEVM* top layer layout.

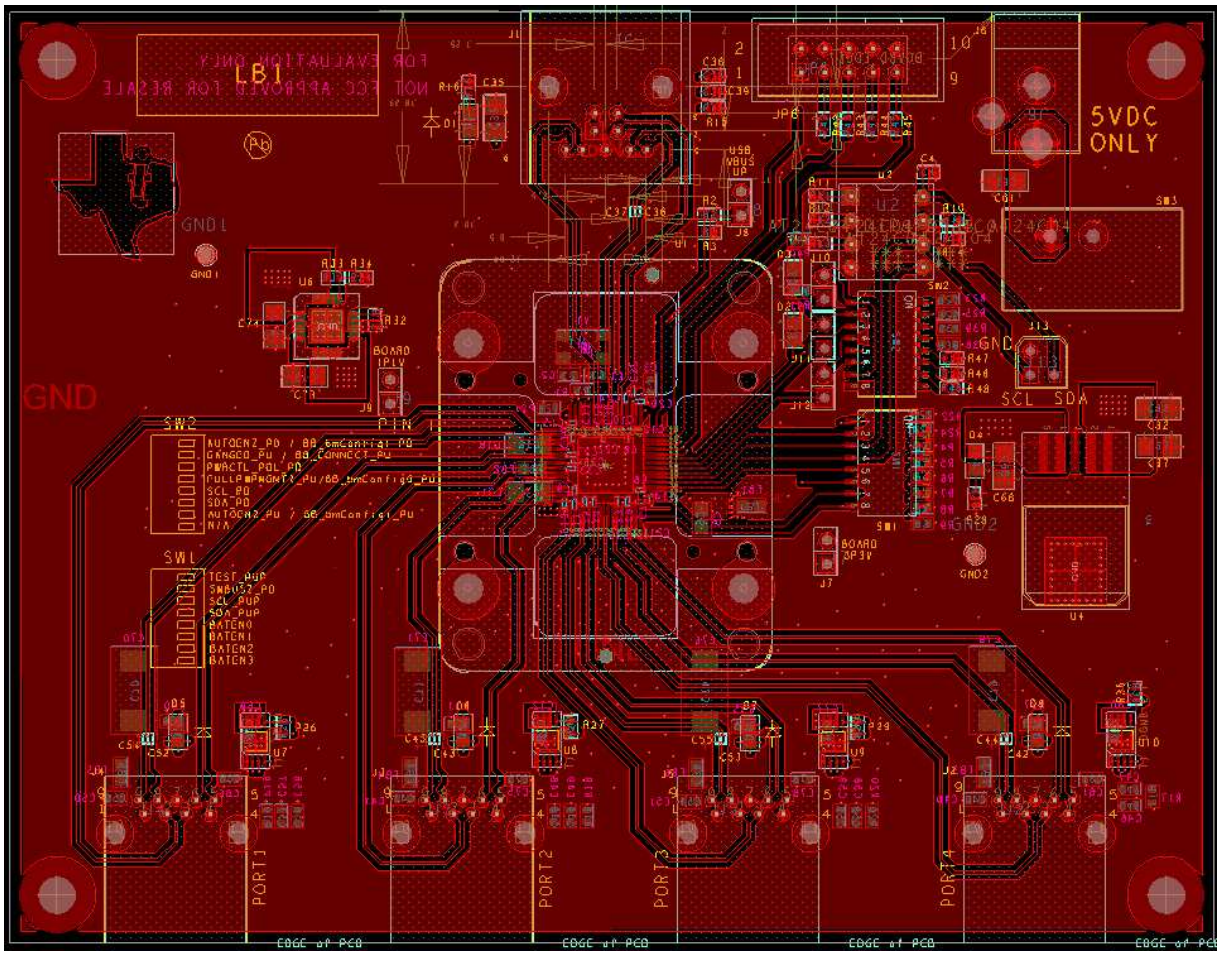

Figure 1. TUSB8044AEVM Top Layer Layout

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2 Hardware Overview

The TUSB8044AEVM board hardware can be divided into the following functional areas:

2.1 TUSB8044AEVM

The TUSB8044A on the TUSB8044A EVM (U1 on the schematic) operates as a functional interconnect between an upstream connection to a USB host or hub and up to four directly connected downstream devices or hubs. More devices and hubs can be supported if arranged in tiers. The TUSB8044A is capable of supporting operation at USB SuperSpeed (SS), high speed (HS), full speed (FS), or low speed (LS). In general, the speed of the upstream connection of the TUSB8044AEVM limits the downstream connections to that speed (SS, HS, and FS), or lower.

The TUSB8044A enumerates a *Billboard* device on a virtual downstream port for USB Type-C applications with alternate mode support. It also has an *I^2C Master* controllable through an HID compliant device enumerated on a virtual downstream port.

The TUSB8044A requires a 24-MHz low-ESR crystal, Y1, with a 1-MΩ feedback resistor. The crystal must be in fundamental mode with a load capacitance of 12 to 24 pF and a frequency stability rating of ±100 PPM or better. To ensure a proper startup oscillation condition, TI recommends a maximum crystal equivalent series resistance (ESR) of 50 Ω.

The TUSB8044A can also use an oscillator or other clock source. When using an external clock source such as an oscillator, the reference clock must have ±100 PPM (or better) frequency stability and have less than 50-ps absolute peak-to-peak jitter (or less) than 25-ps peak-to-peak jitter after applying the USB 3.0 jitter transfer function.

2.2 USB Port Connectors

The TUSB8044A EVM is equipped with five standard 9-pin USB 3.0 port connectors. One of these five connectors, J1, is a Type B connector designed to interface with an upstream USB host or hub. The remaining connectors, J2, J3, J4, and J5, are Type A connectors for connection to downstream devices or hubs. Standard size connectors were used on the EVM design, but USB micro connectors can be used, if desired.

The USB ports can be attached through a standard USB cable to any USB 3.0 or legacy USB host, hub, or device. The TUSB8044A will automatically connect to any upstream USB 3.0 host or hub at both SS and HS. Using a legacy USB cable between the TUSB8044A EVM and a USB 3.0 host or hub forces it to HS operation. The same is true if a legacy USB cable is used between the TUSB8044A EVM and a downstream SS-capable device; operation will be limited to USB 2.0 HS.

2.3 USB Port Connector – Power

VBUS is received from the upstream host or hub on J1. The TUSB8044A is configured as a self-powered hub, so there is not any significant current draw by the EVM from VBUS. The TUSB8044A does monitor the VBUS input after filtering through a resistor divider network of a 90.9-kΩ, 1% resistor, R2, and a 10-kΩ, 1% resistor, R3. VBUS cannot be directly connected to the TUSB8044A device. A bulk capacitor of at least 1 μF is required on the upstream port VBUS input to comply with the USB specification. The TUSB8044AEVM uses a 10-μF capacitor, C35.

VBUS, sourced by the 5-V wall power input, J6, is provided to the downstream port connectors. The USB 3.0 specification limits the current consumption of a USB 3.0 device to 900 mA at 5 V. The current limiting parameter of the TPS2001C devices, U7, U8, U9, and U10, is 2 A to avoid any spurious overcurrent events due to bus-powered HDD spin-up power fluctuations or unnecessary limiting during USB charging. A production implementation could place stricter limits on this power consumption. An overcurrent event on any of the downstream port connectors will be reported to the TUSB8044A through the OVERCURxZ inputs.

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2.4 USB Port Connector – Noise Filtering

Each downstream VBUS output has a 150-µF bulk capacitor (C70, C71, C76, C79) as recommended by the TPS2001C data manual (SLVSAU6) to prevent in-rush current events on the downstream devices. In addition, there are ferrite beads and small capacitors on the VBUS lines to reduce noise and address ESD and EMI concerns.

The TUSB8044AEVM also implements optional isolation using two small noise-filtering capacitors and a 1-MΩ resistor between the earth ground of each connector and the digital ground of the EVM; this is not a requirement, but must be used if ground isolation is desired.

NOTE: Note that the series capacitors implemented on the SS TX pairs are incorporated to satisfy the USB 3.0 requirement that differential links be AC coupled on the transmit pair.

2.5 Optional Serial EEPROM

Each TUSB8044AEVM is equipped with an onboard EEPROM or socket placeholder, U2. A small I^2C EEPROM can be installed to set the configuration registers as defined in the TUSB8044A data manual (SLLSEW5). In its default setting, the EVM does not have an EEPROM installed and instead uses the configuration inputs to determine any optional settings of the TUSB8044.

The EEPROM interface defaults to programmable (not write-protected) so that any installed contents on the EEPROM may be modified to test various settings. If an EEPROM data change is required, the values may be changed using the register access methods outlined in the TUSB8044A data sheet. In addition, a Microsoft® Windows® based EEPROM utility is available upon request.

2.6 Power

The TUSB8044A EVM operates from the power provided by a 5-V wall power adapter, J6, not bus power supplied by a USB host. TI recommends to use a wall power adapter that is capable of sourcing 2 to 3 A because the hub must be able to source significant power on its downstream ports (900 mA per port).

The TUSB8044A EVM uses a single-channel LDO voltage regulator to drop 5 V to 3.3 V. The TPS7A4533, U4, is a 1.5-A output linear regulator (SLVS720). The 1.1-V core voltage required by the TUSB8044A is sourced by the 3.3-V rail to reduce unnecessary heat dissipation. The TPS74801, U6, is a 1.5-A output single channel LDO linear regulator (SBVS074). Both regulators require few external passive components and are appropriately rated for heat dissipation.

2.7 Hub Configuration

The TUSB8044AEVM can be configured by setting several inputs to the TUSB8044A that are sampled at power-on reset or using an optional serial EEPROM or SMBUS host. A production implementation without EEPROM or SMBUS could either rely on the default internal pullup or pulldown resistor for each configuration input or override it with an external pullup or pulldown resistor. The settings can be modified using SW1 and SW2 on the EVM. Descriptions of the possible configuration changes are included in Section 3.1.

2.8 Optional Circuitry

The TUSB8044A EVM design implements a variety of LEDs, none of which are required by the USB specification. They are provided to make testing and debugging easier.

- D1 – indicates that the upstream USB port power is on
- D4 – indicates that 3.3 V is being applied to the TUSB8044A EVM
- D5 – indicates downstream USB port 1 power is on
- D6 – indicates downstream USB port 2 power is on
- D7 – indicates downstream USB port 3 power is on
- D8 – indicates downstream USB port 4 power is on

The switches (SW1, SW2, and SW3) and headers (J7, J8, J9, JP6) present on the TUSB8044A EVM are intended only for lab evaluation and are not required for production designs.

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3 Hardware Setup

3.1 Configuration Switch

The TI TUSB8044AEVM has a set of switches to facilitate configuration changes. TI does not recommend changing these switch settings without a complete understanding of the result. Configuration inputs are only read by the TUSB8044A during power-on reset, changing the switch settings while the EVM is powered on will have no effect. For additional information, refer to the EVM schematic in Appendix B.

The switch definitions are shown in Table 1.

Table 1. Switch Definitions

Switch	Standard	Definition
SW1_1	Off	TEST_TRSTz Switch The TUSB8044A has an internal pulldown on this terminal. If the switch is set to the ON position, the terminal is pulled high and test mode is enabled. This is a production test mode only.
SW1_2	Off	SMBUSz Switch The TUSB8044A has an internal pullup on this terminal, so I^2C interface mode is enabled by default. If the switch is set to the ON position, the terminal is pulled low and SMBUS mode is enabled.
SW1_3	Off	SCL_SMBCLK Switch The TUSB8044A has an internal pulldown on this terminal, so the serial EEPROM or SMBUS interface is disabled. If the switch is set to the ON position, a pullup resistor is connected to the serial clock terminal to indicate that an I^2C EEPROM may be attached (along with a pullup resistor on SDA).
SW1_4	Off	SDA_SMBDAT Switch The TUSB8044A has an internal pulldown on this terminal, so the serial EEPROM or SMBUS interface is disabled. If the switch is set to the ON position, a pullup resistor is connected to the serial clock terminal to indicate that an I^2C EEPROM may be attached (along with a pullup resistor on SCL).
SW1_5	Off	PWRON1_BATEN1 Switch The TUSB8044A has an internal pulldown on this terminal, so USB battery charging mode on Port 1 is disabled by default. If the switch is set to the ON position, the terminal is pulled high and battery charging is enabled on downstream port 1.
SW1_6	Off	PWRON2_BATEN2 Switch The TUSB8044A has an internal pulldown on this terminal, so USB battery charging mode on Port 2 is disabled by default. If the switch is set to the ON position, the terminal is pulled high and battery charging is enabled on downstream port 2.
SW1_7	Off	PWRON3_BATEN3 Switch The TUSB8044A has an internal pulldown on this terminal, so USB battery charging mode on Port 3 is disabled by default. If the switch is set to the ON position, the terminal is pulled high and battery charging is enabled on downstream port 3.
SW1_8	Off	PWRON4_BATEN4 Switch The TUSB8044A has an internal pulldown on this terminal, so USB battery charging mode on Port 4 is disabled by default. If the switch is set to the ON position, the terminal is pulled high and battery charging is enabled on downstream port 4.
SW2_1, SW2_7	Off	AUTOENZ_PD/BB_bmConfig1_PD Switch When configured for I^2C mode, this pin along with BBbmConfigured0 directly controls the bmConfigurated field in the *Billboard Capability* descriptor. If SMBus is selected, then bmConfigured[1] field is determined by a register. If SMBus is selected, the sampled value of this pin will set or clear the autoEnz bit in the *Battery Charging Support Register*. SMBus master can at a later time override the register. If SMBus is selected and stsOutputEn bit is set, this pin will function as a HS_SUSPEND (upstream HS suspend indicator). When enabled, a value of 1 indicates the connection is suspended.
SW2_2	Off	GANGED_HS_UP/BB_CONNECT Switch When configured for I^2C mode, this pin functions as *Billboard Enable*. When high, the billboard device is enabled and presented to system. When low, the billboard device is disabled. If SMBus is selected, then *Billboard Enable* is controlled by a register. If SMBus is selected and stsOutputEn bit is set, this pin will function as a HS_UP (upstream HS connection indicator). When enabled, a value of 1 indicates the upstream port is connected to a HS USB-capable port. If SMBus is selected, the value of the pin is sampled at the de-assertion of reset to set the power switch and overcurrent detection mode as follows: 0 = Individual port power control supported. 1 = Ganged port power control supported. SMBus master can at a later time override the register.
SW2_3	Off	PWRCTL_POL Switch The TUSB8044A has an internal pullup on this terminal, so port power control polarity defaults to active high. If the switch is set to the ON position, the terminal is pulled low and the port power control polarity changes to active low.
SW2_4	Off	FULLPWRMGMTZ_SS_UP/BB_bmConfig0 Switch When configured for I^2C mode, this pin along with BBbmConfigured1 directly controls the bmConfigurated field in the *Billboard Capability* descriptor. If SMBus is selected, then bmConfigured[0] field is determined by a register. If SMBus is selected and battery charging is enabled on any port, the sampled state of this pin will set or clear the FullAutoEn bit in the *Device Configuration Register 3*. SMBus master can at a later time override the register. If SMBus is selected and battery charging is disabled, then the value of the pin is sampled at the de-assertion of reset to set the power switch control: SMBus master can override this function at a later time. 0 = Power Switching and over current inputs supported. 1= Power Switch and over current inputs not supported. If SMBus is selected and stsOutputEn bit is set, ths pin will function as an SS_UP (upstream SS connection indicator). When enabled, a value of '1' indicates the upstream port is connected to a SuperSpeed USB capable port.

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Table 1. Switch Definitions (continued)

Switch	Standard	Definition
SW2_5	Off	SCL_SMBCLK PD Switch The TUSB8044A has an internal pulldown on this terminal, so the serial EEPROM or SMBUS interface is disabled. If the switch is set to the ON position, an external pulldown resistor is connected to the serial clock terminal for test purposes.
SW2_6	Off	SDA_SMBDAT PD Switch The TUSB8044A has an internal pulldown on this terminal, so the serial EEPROM or SMBUS interface is disabled. If the switch is set to the ON position, an external pulldown resistor is connected to the serial clock terminal for test purposes.

3.2 EVM Installation

To install the EVM, perform the following steps:

1. Attach a 5-V, 3-A wall power source to J6.
2. Turn on switch SW3, LED D4 must be lit.
3. Attach a USB cable between J3 and a USB host. LEDs D1, D5, D6, D7 and D8 must be lit.

3.3 Troubleshooting

Case 1: Device function or functions are “banged out” in Device Manager.

- Make sure that the latest updates are installed for the operating system.
- Make sure that the latest drivers are installed for the host controller.

Case 2: The EVM does not work at all.

- Verify that all switches are in their default state and the EVM is powered on with a 5-V source with adequate current to support any bus-powered devices (3 A+).
- If installed, remove the serial EEPROM from the EEPROM socket. The EVM does not require an EEPROM to operate.
- Make sure shunts are installed on J7, J8, and J9.
- In the case where a 12-V power supply has been attached to the EVM, the fault is non-recoverable.

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TUSB8044AEVM REV D EVM Bill of Materials

This appendix contains the TUSB8044AEVM REV D EVM BOM.

Table 2. TUSB8044A QFN Lab EVM Bill Of Materials: Texas Instruments, CCI and ICP

Item	Qty	Reference	Part	Manufacturer	Part Number	Pkg	Description
1	1	C5	1uF	Murata	GRM219R61A105KA01D	805	1µF ±10% 10V Ceramic Capacitor X5R 0805 (2012 Metric)
2	1	C3	1uF	Samsung	CL05B105KQ5NQNC	402	CAP CER 1UF 6.3V 10% X7R 0402
3	5	C39,C47,C49,C57,C59	0.001uF	TDK	C1005X7R1H102K	402	CAP CER 1000PF 50V X7R 10% 0402
4	9	C6,C9,C12,C15,C19,C22,C25,C28,C32,	0.001uF	TDK	C0603X7R1E102K030BA	201	CAP CER 1000PF 25V 10% X7R 0201
5	9	C7,C10,C13,C16,C20,C23,C26,C29,C33	0.01uF	Yageo	CC0201KRX7R7BB103	201	CAP CER 10000PF 16V 10% X7R 0201
6	18	C4,C38,C40,C41,C46,C48,C50,C51,C56,C58,C66,C69,C72,C75,C77,C78,C80,C81	0.1uF	Yageo	CC0402KRX5R6BB104	402	CAP CERAMIC .1UF 10V X5R 0402
7	19	C8,C11,C14,C17,C21,C24,C27,C30,C34,C36,C37,C42,C43,C44,C45,C52,C53,C54,C55	0.1uF	TDK	C0603X5R0J104M	201	CAP CER .10UF 6.3V X5R 0201
8	2	C1,C2	18pF	AVX	04025A180JAT2A	402	CAP CERM 18PF 5% 50V NP0 0402
9	9	C18,C31,C35,C61,C67,C68,C73,C74,C82	10uF	Murata Electronics	GRM31CR61C106KA88L	1206	CAPACITOR CERM 10UF 16V 10% SMD
10	4	C70,C71,C76,C79	150uF	Kemet	T495D157K010ATE100 (Tantalum)	7343	CAP TANT 150UF 10V 10% LOESR SMD
11	0	R10,R32,R42,R43,R44,R45	NOPOP			402	
12	6	D1,D4,D5,D6,D7,D8	LED Green 0805	Lite On	LTST-C171GKT	805	LED GREEN CLEAR THIN 0805 SMD
13	0	D2,D3	LED Green 0805 - NOPOP	Lite On	LTST-C171GKT	805	LED GREEN CLEAR THIN 0805 SMD
14	5	FB1,FB3,FB4,FB5,FB6	220 @ 100MHZ Ferrite Bead	Murata	BLM18PG221SN1D	603	FERRITE CHIP 220 OHM 1400MA 0603
15	2	SW1,SW2	8-POS 50-MIL SMT	C&K Components	SD08H0SBR		SWITCH DIP SPST SEALED 8POS SMD
16	1	J1	USB3_TYPEB_CONNECTOR	Amphenol	GSB321131HR	9_RA_TH_B	CONN RCPT USB 3.0 TYPE B R/A 9PS
17	4	J2,J3,J4,J5	USB3_TYPEA_CONNECTOR	Amphenol	GSB311131HR	9_RA_TH_A	CONN RCPT USB 3.0 TYPE A R/A 9PS
18	1	J6	2.1mm x 5.5mm DC Power Jack	CUI Inc.	PJ-202AH	2.1mm x 5.5mm	CONN PWR JACK 2.1X5.5MM HIGH CUR
19	6	R1,R15,R17,R18,R19,R20	1M	Rohm Semiconductor	MCR01MZPJ105	402	RES 1.0M OHM 1/16W 5% 0402 SMD
20	1	R2	90.9K 1%	Rohm Semiconductor	MCR01MZPF9092	402	RES 90.9K OHM 1/16W 1% 0402 SMD
21	4	R26,R27,R29,R36	10K	Rohm Semiconductor	MCR01MZPJ103	402	RES 10K OHM 1/16W 5% 0402 SMD
22	1	R3	10K 1%	Rohm Semiconductor	MCR01MZPF1002	402	RES 10K OHM 1/16W 1% 0402 SMD
23	4	R6,R7,R8,R9	4.7K	Rohm Semiconductor	MCR01MZPJ472	402	RES 4.7K OHM 1/16W 5% 0402 SMD

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Table 2. TUSB8044A QFN Lab EVM Bill Of Materials: Texas Instruments, CCI and ICP (continued)

Item	Qty	Reference	Part	Manufacturer	Part Number	Pkg	Description
24	15	R4,R5,R11,R12,R13,R14,R22,R23,R24,R25,R38,R39,R46, R47, R48	1K	Rohm Semiconductor	MCR01MZPJ102	402	RES 1.0K OHM 1/16W 5% 0402 SMD
25	8	R16,R28,R30,R31,R35,R37,	330	Rohm Semiconductor	MCR01MZPJ331	402	RES 330 OHM 1/16W 5% 0402 SMD
		R40,R41					
26	1	R33	1.87K	Vishay / Dale	CRCW04021K87FKED	402	RES 1.87K OHM 1/16W 1% 0402 SMD
27	1	R34	4.99K	Vishay / Dale	CRCW04024K99FKED	402	RES 4.99K OHM 1/16W 1% 0402 SMD
28	1	R21	9.53K 1%	Rohm Semiconductor	MCR01MRTF9531	402	RES 9.53K OHM 1/16W 1% 0402 SMD
29	1	U1	TUSB8044A - USB 3.0 Hub	Texas Instruments	TUSB8044AEVM	64QFN	
30	1	U2	AT24C04 I^2C EEPROM	Assmann WSW Components	A 08-LC-TR	8DIP	CONN IC DIP SOCKET 8POS TIN
31	4	U7,U8,U9,U10	TPS2001C	Texas Instruments	TPS2001CDGN	8DGN	IC PWR SW USB 2.87A 1CH 8MSOP
32	1	U4	TPS7A4533 - 3.3V Voltage Regulator	Texas Instruments	TPS7A4533KTT	DDPAK-5	IC REG LDO 3.3V 1.5A 5-DDPAK
33	1	U6	TPS74801RGW - 1.1V Voltage Regulator	Texas Instruments	TPS74801RGW	20VQFN	IC REG LDO ADJ 1.5A 20VQFN
34	1	Y1	ECS-24MHZ Crystal	ECS	ECS-240-20-30B-TR	5.0mm x 3.2mm	CRYSTAL 24.000 MHZ 20PF SMD
35	4		PCB Standoff	Keystone Electronics	2203		HEX STANDOFF 4-40 ALUMINUM 1/2"
36	4		Screw	Keystone Electronics	9900		MACHINE SCREW PAN PHILLIPS 4-40
37	1	FB2	0 ohm	Yageo	RC0603JR-070RL	603	RES 0.0 OHM 1/10W 0603 SMD
38	0	JP6	Conn 2x5 shroud - NO POP	3M	2510-6003UB	HDR5X2 M 0.1" TH	
39	6	J7,J8,J9,J10,J11,J12	Header 1x2	3M	961102-6404-AR	HDR2X1 M 0.1" TH	CONN HEADER VERT SGL 2POS GOLD
40	1	J13	Header 3PIN	3M	961102-6404-AR	HDR2X1 M 0.1" TH	CONN HEADER VERT SGL 2POS GOLD
41	1	SW3	Power Switch - L101011MS02Q	C&K Components	L101011MS02Q	SPST	
42	0	GND1, GND2	NOPOP				
43	1	LB1	sticker	3M	695-WHITE-2"X36YD		add text: TUSB8044AEVM INT077-001 REV A
44	6	Shunt	Shunt	3M	969102-0000-DA		Place shunts on: J7,J8,J9,J10,J11,J12
45	1	PCB BOARDS	TUSB8044AEVM		INT077-001		TUSB8044AEVM PCBBOARD

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TUSB8044AEVM REV D EVM Schematics

Figure 2 through Figure 4 the TUSB8044AEVM REV D EVM schematics.

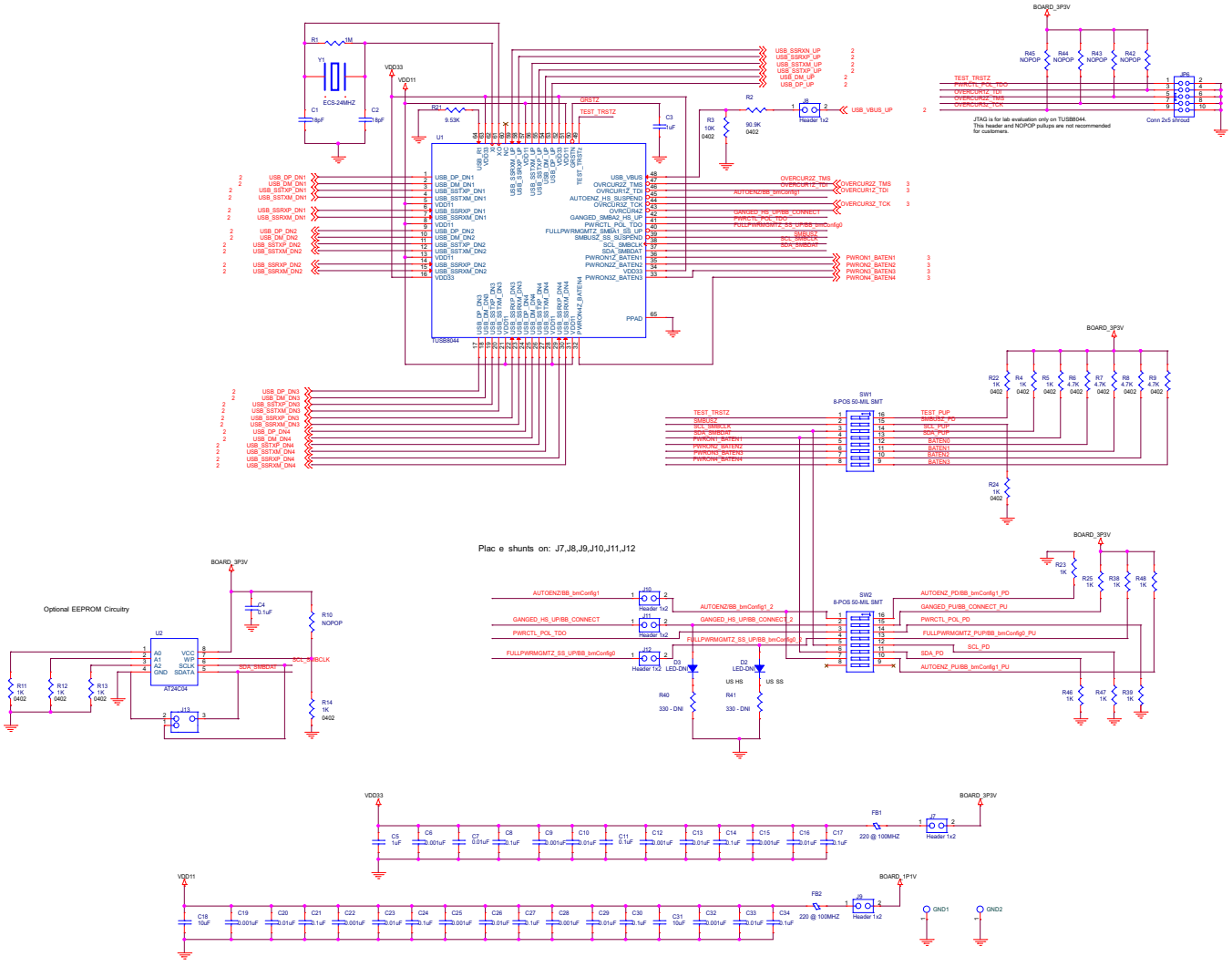

Figure 2. TUSB8044AEVM REV D EVM Top Layer Layout

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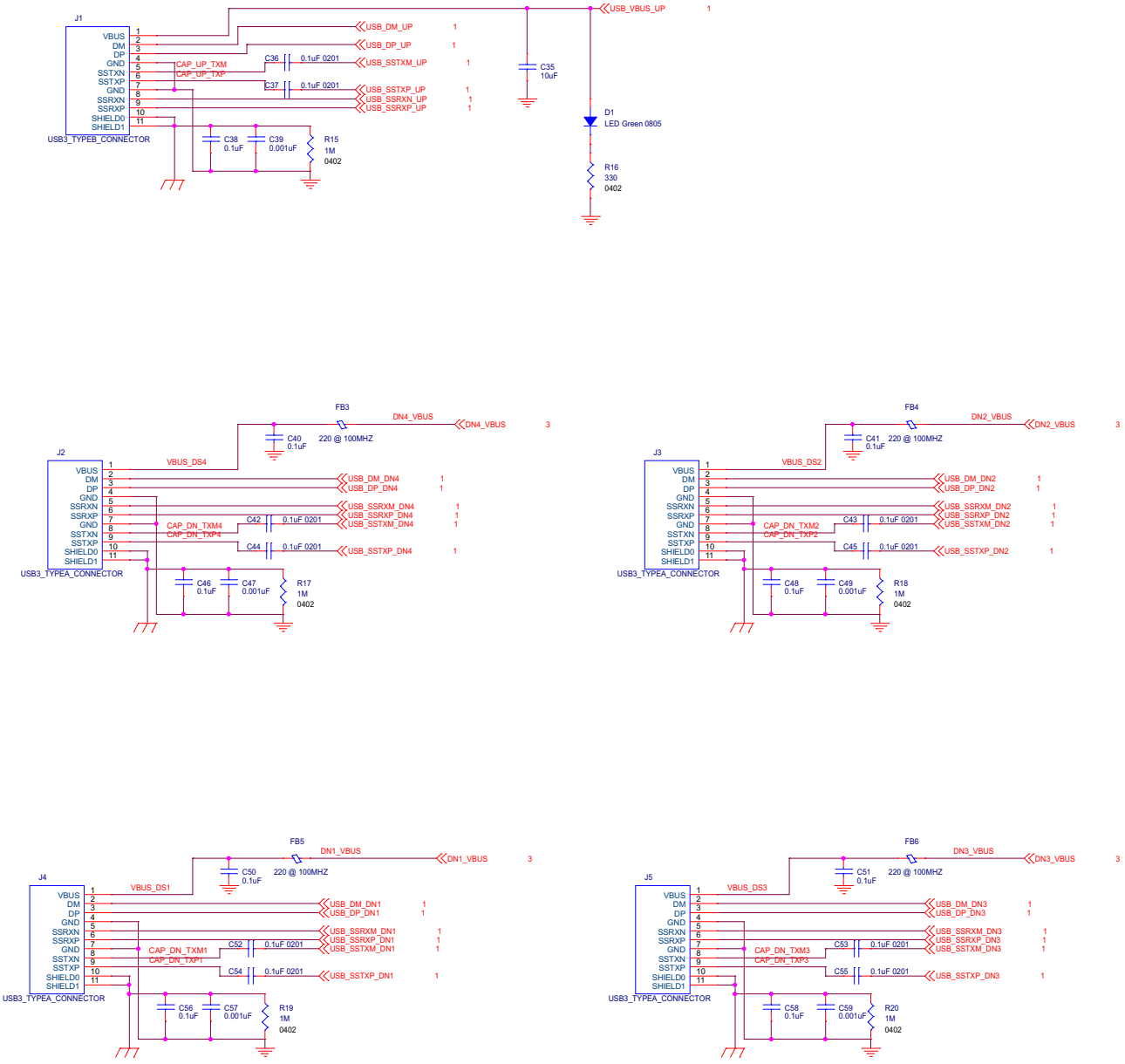

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Figure 3. USB Port Connections

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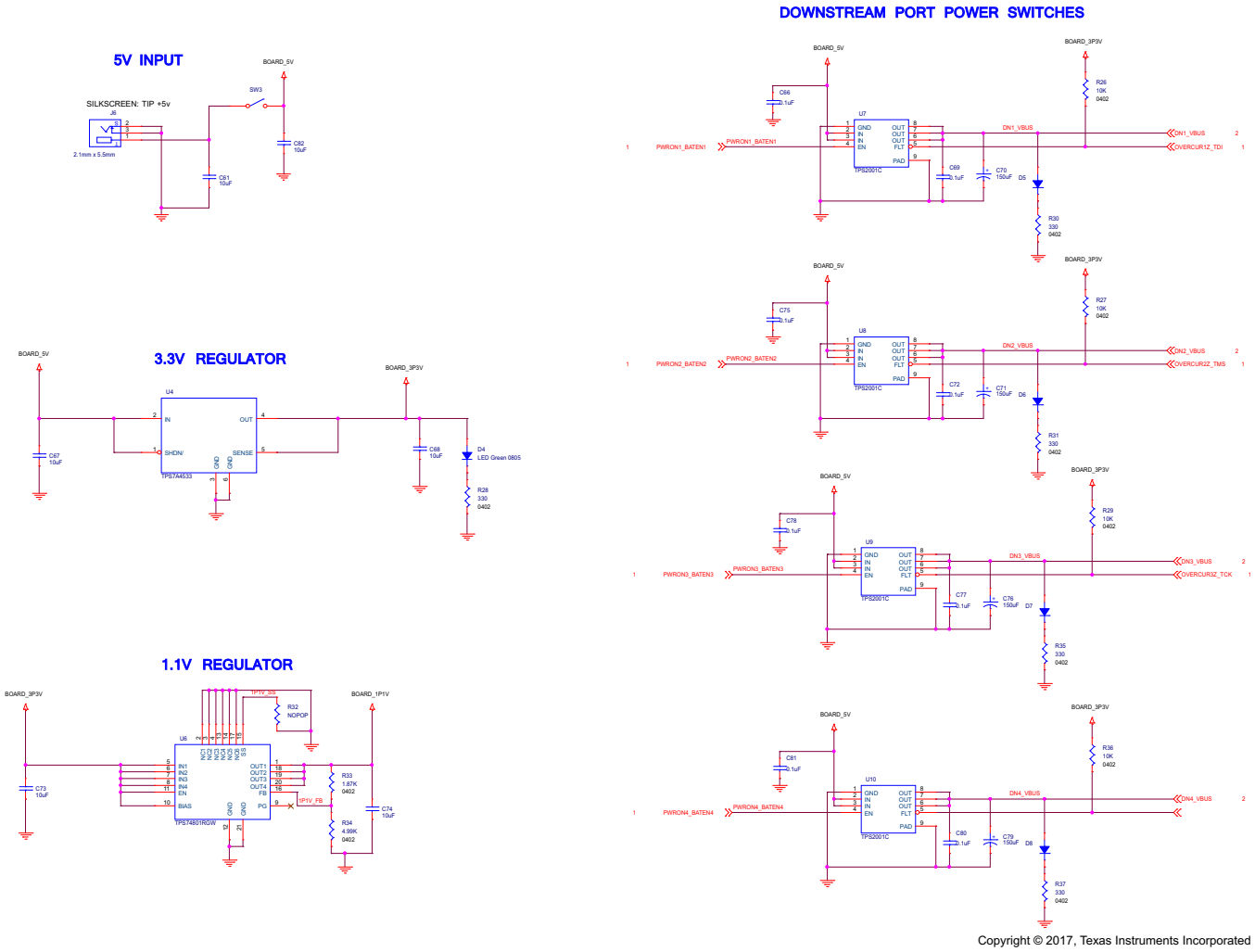

Figure 4. Power

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