Programmer's Guide

DS160PR810 Programming Guide

ABSTRACT

This document is a programming reference for the DS160PR810 Octal-Channel PCI-Express Gen-4 Linear Redriver. This document contains detailed information related to the DS160PR810 advanced configuration options. The intended audience includes software engineers working on system diagnostics and control software.

TI recommends that the reader be familiar with the DS160PR810 data sheet. This document and all other collateral data related to the DS160PR810 redriver (application notes, models, and more) are available to download from the TI website. Alternatively, contact your local Texas Instruments field sales representative.

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1 Access Methods

There are two ways the designer can access the DS160PR810. The methods are:

- Register control through the Serial Management Bus (SMBus)
- Automatic configuration through an external EEPROM

1.1 Register Programming Through SMBus

The DS160PR810 internal registers can be accessed through standard SMBus protocol. The DS160PR810 features two banks of channels, Bank 0 (Channels 0- 3) and Bank 1 (Channels 4-7), each featuring a separate register set and requiring a unique SMBus secondary address. The SMBus secondary address pairs (one for each channel bank) are determined at power up based on the configuration of the EQ0_0 / ADDR1 and EQ1_0 / ADDR0 pins. The pin state is read on power up, after the internal power-on reset signal is deasserted.

The EQ0_0 / ADDR1 and EQ1_0 / ADDR0 pins along with the MODE, GAIN0, GAIN1, EQ0_1, EQ1_1, and RX_DET pins are 4-level input pins that are used to control the configuration of the device. These 4-level inputs use a resistor divider to help set the four valid levels as shown in Table 1-1.

Table 1-1. DS160PR810 4-Level Control Pin Settings

Pin Level	Pin Setting
L0	1 kΩ to GND
L1	13 kΩ to GND
L2	59 kΩ to GND
L3	Float

There are 16 unique SMBus secondary address pairs (one address for each channel bank) that can be assigned to the device by placing external resistor straps on the EQ0_0 / ADDR1 and EQ1_0 / ADDR0 pins as shown in Table 1-2. When multiple DS160PR810 devices are on the same SMBus interface bus, each channel bank of each device must be configured with a unique SMBus secondary address pair.

Table 1-2. DS160PR810SMBus Address Map

ADDR1 Pin Level	ADDR0 Pin Level	Bank 0: Channels 0-3: 7-Bit Address [HEX]	Bank 1: Channels 4-7: 7-Bit Address [HEX]
L0	L0	0x18	0x19
L0	L1	0x1A	0x1B
L0	L2	0x1C	0x1D
L0	L3	0x1E	0x1F
L1	L0	0x20	0x21
L1	L1	0x22	0x23
L1	L2	0x24	0x25
L1	L3	0x26	0x27
L2	L0	0x28	0x29
L2	L1	0x2A	0x2B
L2	L2	0x2C	0x2D
L2	L3	0x2E	0x2F
L3	L0	0x30	0x31
L3	L1	0x32	0x33
L3	L2	0x34	0x35
L3	L3	0x36	0x37

1.2 Device Configuration Through External EEPROM

The DS160PR810 can automatically read its initial configuration from the EEPROM at power up. Detailed information on EEPROM hex file generation for this device is provided in the *Understanding EEPROM Programming for DS160PR810 PCI-Express 4.0 Linear Redriver* application report.

2 Register Map Overview

The DS160PR810 has two types of registers:

- **Share Registers** – These registers can be accessed at any time and are used for device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers** – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.

Both Share and Channel registers of a single channel bank are contained within a single register page as shown in Table 2-1.

Table 2-1. Register Map Overview

Address Range	Channel Bank 0 Access	Channel Bank 1 Access
0x00 - 0x03	Channel 0 registers	Channel 4 registers
0x20 - 0x23	Channel 1 registers	Channel 5 registers
0x40 - 0x43	Channel 2 registers	Channel 6 registers
0x60 - 0x63	Channel 3 registers	Channel 7 registers
0x80 - 0x83	Broadcast write channel bank 0 registers, read channel 0 registers	Broadcast write channel bank 1 registers, read channel 4 registers
0xA0 - 0xA3	Broadcast write channel 0-1 registers, read channel 0 registers	Broadcast write channel 4-5 registers, read channel 4 registers
0xC0 - 0xC3	Broadcast write channel 2-3 registers, read channel 2 registers	Broadcast write channel 6-7 registers, read channel 6 registers
0xE2 - 0xE3, 0xF0 - 0xF1	Bank 0 Share registers	Bank 1 Share registers

3 Example Programming Sequences

The DS160PR810 is highly programmable and customizable for multiple applications. The following sections provide guidance for programming the DS160PR810 for common applications.

The following information is provided in each sequence:

- **Step**: Many sequences contain several steps. The order in which actions are to be taken is indicated by the step number.
- **Register Set**: Actions are intended for either the Shared or Channel register of either Bank 0 or Bank 1. Since each channel bank has its own SMBus address, no explicit channel bank selection is necessary.
- **Operation**: Read or Write. If it is a Read operation, a register value or write mask is not associated.
- **Register Address**: Select the register to write to.
- **Register Value**: Value to write to register address.
- **Write Mask**: Unless the write mask is 0xFF, perform all writes as a read/modify/write operation. Modify only the bits identified by the mask.

3.1 Set CTLE Gain Level

The DS160PR810 requires manual CTLE tuning. The CTLE gain level can be changed by modifying the value of each CTLE stage (EQ1 and EQ2) or by bypassing the EQ1 stage. The CTLE level can be set individually for each channel or broadcast to all channels. Table 3-1 shows an example sequence for setting the CTLE gain level to 5.0 dB at 8 GHz (CTLE Index 2) on the Bank 0 channels and to 7.0 dB (CTLE Index 4) on the Bank 1 channels using individual writes to each channel. Use register values provided in Table 3-3 to set the CTLE gain level to any other available value.

Table 3-1. Sequence to Set CTLE Level on Each Channel Individually

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Bank 0: Channel 0	Write	0x01	0x08	0x3F	Set CTLE to Index 2 on Channel 0.
2	Bank 0: Channel 1	Write	0x21	0x08	0x3F	Set CTLE to Index 2 on Channel 1.
3	Bank 0: Channel 2	Write	0x41	0x08	0x3F	Set CTLE to Index 2 on Channel 2.
4	Bank 0: Channel 3	Write	0x61	0x08	0x3F	Set CTLE to Index 2 on Channel 3.
5	Bank 1: Channel 4	Write	0x01	0x11	0x3F	Set CTLE to Index 4 on Channel 4.
6	Bank 1: Channel 5	Write	0x21	0x11	0x3F	Set CTLE to Index 4 on Channel 5.
7	Bank 1: Channel 6	Write	0x41	0x11	0x3F	Set CTLE to Index 4 on Channel 6.
8	Bank 1: Channel 7	Write	0x61	0x11	0x3F	Set CTLE to Index 4 on Channel 7.

Assuming 0x18 and 0x19 are the SMBus addresses for the Channel Banks 0 and 1 respectively, the following is the XML batch script of the sequence in Table 3-1:

```
<i2c_write addr="0x18" count="0" radix"16">01 08</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">21 08</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">41 08</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">61 08</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">01 11</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">21 11</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">41 11</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">61 11</i2c_write>
```

Table 3-2 shows an example sequence to set the CTLE gain level to 5.0 dB at 8 GHz (CTLE Index 2) on Bank 0 channels and to 7.0 dB (CTLE Index 4) on Bank 1 channels using a broadcast write to each channel bank.

Table 3-2. Sequence to Broadcast CTLE Level to All Channels

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Bank 0: Channels 0-3	Write	0x81	0x08	0x3F	Set EQ to Index 2 on Channels 0-3.
2	Bank 1: Channels 4-7	Write	0x81	0x11	0x3F	Set EQ to Index 4 on Channels 4-7.

Assuming 0x18 and 0x19 are the SMBus addresses for the Channel Banks 0 and 1 respectively, the following is the XML batch script of the sequence in Table 3-2:

```
<i2c_write addr="0x18" count="0" radix"16">81 08</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">81 11</i2c_write>
```

Table 3-3 gives a CTLE Control Register value as a function of CTLE Index (0 - 15). Example CTLE Control Register addresses are given in Table 3-1 and Table 3-2.

Table 3-3. CTLE Control Register Value as a Function of CTLE Index

CTLE Index	CTLE Gain at 4 GHz (dB)	CTLE Gain at 8 GHz (dB)	CTLE Control Register Value [HEX]
0	0.0	-0.2	0x40
1	1.5	4.5	0x43
2	2.0	5.5	0x08
3	2.5	6.5	0x0A
4	2.7	7.0	0x11
5	3.0	8.0	0x12
6	4.0	9.0	0x13
7	5.0	10.0	0x1A
8	6.0	11.0	0x1B
9	7.0	12.0	0x23
10	7.5	13.0	0x2B
11	8.0	13.5	0x2C
12	8.5	15.0	0x2D
13	9.5	16.5	0x35
14	10.0	17.0	0x36
15	11.0	18.0	0x3F

3.2 Reset RX Detect State Machine

The RX Detect State Machine may be manually reset for all channels.

Table 3-4. Sequence to Reset RX Detect State Machine

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Bank 0: Channels 0-3	Write	0x89	0x04	0x04	Set RX Detect Reset bit to: 1 (Reset RX Detect State Machine)
2	Bank 1: Channels 4-7	Write	0x89	0x00	0x04	Set RX Detect Reset bit to: 0 (Clear set bit)

Assuming 0x18 and 0x19 are the I2C / SMBus addresses for the Channel Banks 0 and 1 respectively, the following is the XML batch script of the sequence in Table 3-4 to reset the RX Detect state machine on all channels:

```
<i2c_write addr="0x18" count="0" radix"16">89 04</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">89 04</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">09 00</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">09 00</i2c_write>
```

3.3 Set CTLE DC Gain Level

The CTLE DC Gain value may be set individually for each channel or broadcast to all channels.

Table 3-5. Sequence to Broadcast DC Gain Level to All Channels

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Bank 0: Channels 0-3	Write	0x82	0x00	0x04	Set DC Gain on Bank 0 channels to: 0 dB (Default).
				0x04	0x04	Set DC Gain on Bank 0 channels to: 3.5 dB.
2	Bank 1: Channels 4-7	Write	0x82	0x00	0x04	Set DC Gain on Bank 1 channels to: 0 dB (Default).
				0x04	0x04	Set DC Gain on Bank 1 channels to: 3.5 dB.

Assuming 0x18 and 0x19 are the I2C/SMBus addresses for the Channel Banks 0 and 1 respectively, the following is the XML batch script of the sequence in Table 3-5 to broadcast DC Gain to 3.5 dB:

```
<i2c_write addr="0x18" count="0" radix"16">82 04</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">82 04</i2c_write>
```

3.4 Set VOD Level

The DS160PR810 driver differential output voltage can be modified, if needed.

Table 3-6. Sequence to Broadcast VOD Level to All Channels

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Bank 0: Channels 0-3	Write	0x82	0x00	0x03	Set VOD on Bank 0 channels to: -6 dB
				0x01	0x03	Set VOD on Bank 0 channels to: -3.5 dB
				0x10	0x03	Set VOD on Bank 0 channels to: -1.6 dB
				0x11	0x03	Set VOD on Bank 0 channels to: 0 dB (Default)
2	Bank 1: Channels 4-7	Write	0x82	0x00	0x03	Set VOD on Bank 1 channels to: -6 dB
				0x01	0x03	Set VOD on Bank 1 channels to: -3.5 dB
				0x10	0x03	Set VOD on Bank 1 channels to: -1.6 dB
				0x11	0x03	Set VOD on Bank 1 channels to: 0 dB (Default)

Assuming 0x18 and 0x19 are the I2C/SMBus addresses for the Channel Banks 0 and 1 respectively, the following is the XML batch script of the sequence in Table 3-6 to broadcast set VOD to -3.5 dB:

```
<i2c_write addr="0x18" count="0" radix"16">82 01</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">82 01</i2c_write>
```

4 SHARE Registers

Table 4-1 lists the SHARE registers. All register offset addresses not listed in Table 4-1 should be considered as reserved locations and the register contents should not be modified.

Table 4-1. SHARE Registers

Offset	Acronym	Register Name	Section
0xE2	General	General Control Register	Go
0xE3	EE_Status	EEPROM Status Register	Go
0xF0	DEVICE_ID0	Device ID0 Register	Go
0xF1	DEVICE_ID1	Device ID1 Register	Go

Complex bit access types are encoded to fit into small table cells. Table 4-2 shows the codes that are used for access types in this section.

Table 4-2. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read only access
Write Type		
R/W/SC	R/W/SC	Read / Write access, Self-Clearing
Reset or Default Value		
-n		Value after reset or the default value

4.1 General Register (Offset = 0xE2) [reset = 0x0]

General is shown in Table 4-3.

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Table 4-3. General Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	rst_i2c_regs	R/W/SC	0x0	Device Reset Control: Reset all I^2C registers to default values (self-clearing).
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	frc_eeprm_rd	R/W/SC	0x0	Override MODE and READ_EN_N status to force manual EEPROM Configuration Load.

4.2 EE_Status Register (Offset = 0xE3) [reset = 0x0]

EE_Status is shown in Table 4-4.

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Table 4-4. EE_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	eecfg_cmplt	R	0x0	EEPROM load complete.
6	eecfg_fail	R	0x0	EEPROM load failed.
5	eecfg_atmpt_1	R	0x0	Number of attempts made to load EEPROM image.
4	eecfg_atmpt_0	R	0x0	see MSB
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

4.3 DEVICE_ID0 Register (Offset = 0xF0) [reset = X]

DEVICE_ID0 is shown in Table 4-5.

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Table 4-5. DEVICE_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	device_id0_3	R	X	Device ID0 [3:1]: 011
2	device_id0_2	R	X	see MSB
1	device_id0_1	R	X	see MSB
0	RESERVED	R	X	Reserved

4.4 DEVICE_ID1 Register (Offset = 0xF1) [reset = 0x27]

DEVICE_ID1 is shown in Table 4-6.

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Table 4-6. DEVICE_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	device_id1_7	R	0x0	Device ID1: 0010 0111
6	device_id1_6	R	0x0	See MSB
5	device_id1_5	R	0x1	See MSB
4	device_id1_4	R	0x0	See MSB
3	device_id1_3	R	0x0	See MSB
2	device_id1_2	R	0x1	See MSB
1	device_id1_1	R	0x1	See MSB
0	device_id1_0	R	0x1	See MSB

5 CHANNEL Registers

Table 5-1 lists the CHANNEL registers. All register offset addresses not listed in Table 5-1 should be considered as reserved locations and the register contents should not be modified.

Note that the register offset is provided for the channel 0 or channel 4 registers (channel bank 0 or channel bank 1). For the channel 1, 2, and 3 registers on the channel bank 0 (or the channels 5, 6, and 7 on the channel bank 1), add 0x20, 0x40, or 0x60 respectively to the provided offset.

Table 5-1. CHANNEL Registers

Offset	Acronym	Register Name	Section
0x0	RX_DET_STS	Receiver Detect Status Register	Go
0x1	EQ_CTRL	Equalizer Control Register	Go
0x2	GAIN_CTRL	DC Gain and VOD Control Register	Go
0x3	RX_DET_CTRL1	Receiver Detect Control Register 1	Go
0x9	RX_DET_CTRL2	Receiver Detect Control Register 2	Go

Complex bit access types are encoded to fit into small table cells. Table 5-2 shows the codes that are used for access types in this section.

Table 5-2. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read only access.
Write Type		
R/W	R/W	Read / Write access.
Reset or Default Value		
-n		Value after reset or the default value.

5.1 RX_DET_STS Register (Offset = 0x0) [reset = 0x0]

RX_DET_STS is shown in Table 5-3.

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Table 5-3. RX_DET_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	rx_det_comp_p	R	0x0	Rx Detect Positive Polarity Status: 0: Not detected 1: Detected The value is latched.
6	rx_det_comp_n	R	0x0	Rx Detect Negative Polarity Status: 0: Not detected 1: Detected The value is latched.
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

5.2 EQ_CTRL Register (Offset = 0x1) [reset = 0x9]

EQ_CTRL is shown in Table 5-4.

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Table 5-4. EQ_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	eq_en_bypass	R/W	0x0	Enable CTLE Stage 1 Bypass: 0: Bypass disabled 1: Bypass enabled
5	eq_bst1_2	R/W	0x0	CTLE Boost Stage 1 Control.
4	eq_bst1_1	R/W	0x0	See MSB
3	eq_bst1_0	R/W	0x1	See MSB
2	eq_bst2_2	R/W	0x0	CTLE Boost Stage 2 Control.
1	eq_bst2_1	R/W	0x0	See MSB
0	eq_bst2_0	R/W	0x1	See MSB

5.3 GAIN_CTRL Register (Offset = 0x2) [reset = 0x3]

GAIN_CTRL is shown in Table 5-5.

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Table 5-5. GAIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	eq_hi_gain	R/W	0x0	Set CTLE DC Gain: 0: 0 dB (Recommended) 1: 3.5 dB
1	drv_sel_vod_1	R/W	0x1	TX VOD Select: 00: - 6 dB 01: -3.5 dB 10: -1.6 dB 11: 0 dB (Recommended)
0	drv_sel_vod_0	R/W	0x1	See MSB

5.4 RX_DET_CTRL1 Register (Offset = 0x3) [reset = 0x0]

RX_DET_CTRL1 is shown in Table 5-6.

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Table 5-6. RX_DET_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	mr_rx_det_man	R/W	0x0	Manual override of rx_detect.
1	en_rx_det_count	R/W	0x0	Enable RX detect valid counter.
0	sel_rx_det_count	R/W	0x0	Select valid detect count before enable: 0: 2x consecutive valid detections 1: 3x consecutive valid detections

5.5 RX_DET_CTRL2 Register (Offset = 0x9) [reset = 0x0]

RX_DET_CTRL2 is shown in Table 5-7.

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Table 5-7. RX_DET_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	mr_rx_det_rst	R/W	0x0	RX Detect Reset
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

6 References

1. *DS160PR810 Octal-Channel PCI-Express 4.0 Linear Redriver* data sheet
2. *Understanding EEPROM Programming for DS160PR810 PCI-Express 4.0 Linear Redriver* application report

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2023	*	Initial Release

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