Functional Safety Information

REF34-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for REF34-Q1 (DBV-6, DBV-5, DGK-8 packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

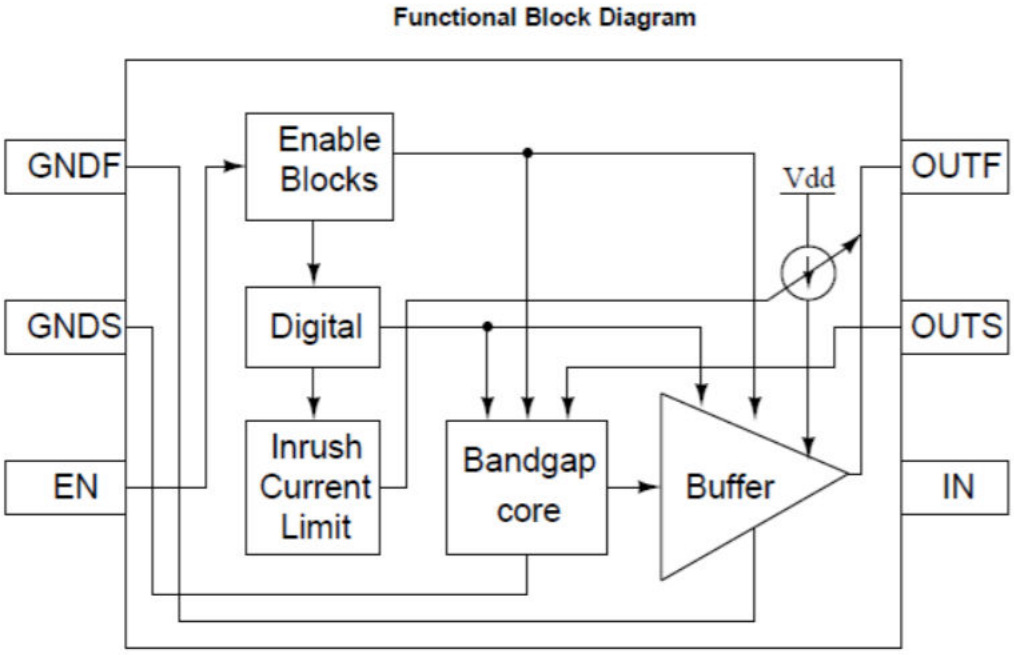

Figure 1-1. Functional Block Diagram

REF34-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DBV-6 Package

This section provides Functional Safety Failure In Time (FIT) rates for DBV-6 package of REF34-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	5
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 120.0 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	Digital, Analog, Mixed	25 FIT	55 C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DBV-5 Package

This section provides Functional Safety Failure In Time (FIT) rates for the DBV-5 package of REF34-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	5
Package FIT Rate	2

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 120 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 DGK-8 Package

This section provides Functional Safety Failure In Time (FIT) rates for the DGK package of REF34-Q1 based on two different industry-wide used reliability standards:

- Table 2-5provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	10
Die FIT Rate	6
Package FIT Rate	4

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 120 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for REF34-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTPUT open or HIZ	40%
OUTPUT to GND	10%
OUTPUT out of spec voltage or timing	40%
OUTPUT stuck on	10%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the REF34-Q1 (DBV-6, DBV-5 and DGK-8 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2, Table 4-6 and Table 4-10)
- Pin open-circuited (seeTable 4-3, Table 4-7 and Table 4-11)
- Pin short-circuited to an adjacent pin (see Table 4-4, Table 4-8 and Table 4-12)
- Pin short-circuited to supply (see Table 4-5, Table 4-9 and Table 4-13)

Table 4-2 through Table 4-13 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- 10uF capacitor connected to Vout
- 1uF capacitor connected to Vin

4.1 DBV-6 Package

Figure 4-1 shows the REF34-Q1 pin diagram for the DBV-6 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the REF34-Q1 data sheet.

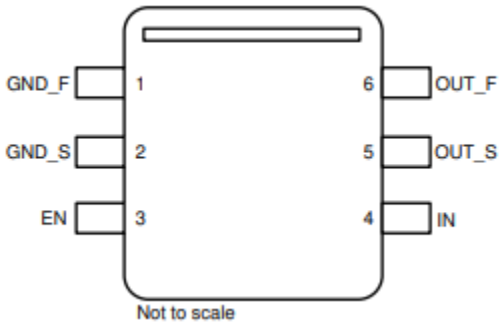

Figure 4-1. Pin Diagram (DBV-6) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND_F	1	No effect	D
GND_S	2	No effect	D
ENABLE	3	Disables device, no output voltage, high leakage	B
IN	4	No output voltage, high leakage	B
OUT_S	5	No output voltage	B
OUT_F	6	No output voltage	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND_F	1	No output voltage	B
GND_S	2	No output voltage	B
ENABLE	3	Disables device, no output voltage	B
IN	4	Output is not regulated	C
OUT_S	5	Output is not regulated	C
OUT_F	6	Output is not regulated	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND_F	1	GND_S	No effect	D
GND_S	2	ENABLE	Disables device, no output voltage, high leakage	B
ENABLE	3	IN	No effect	D
IN	4	OUT_S	Output is not regulated, high leakage	B
OUT_S	5	OUT_F	No effect	D
OUT_F	6	GND_F	No output voltage	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND_F	1	No outpout voltage, high leakage	B
GND_S	2	No output voltage, high leakage	B
ENABLE	3	No effect	D
IN	4	No effect	D
OUT_S	5	Output is not regulated, high leakage	B
OUT_F	6	Output is not regulated, high leakage	B

4.2 DBV-5 Package

Figure 4-2 shows the REF34-Q1 pin diagram for the DBV-5 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the REF34-Q1 data sheet.

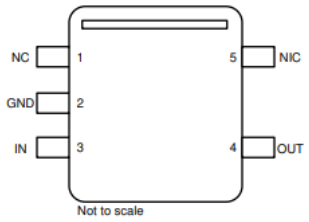

Figure 4-2. Pin Diagram (DBV-5 Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	No effect	D
GND	2	No effect	D
IN	3	No output voltage, high leakage	B
OUT	4	No output voltage	B
NC	5	No effect	D

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	No effect	D
GND	2	No output voltage	D
IN	3	Output is not regulated	C
OUT	4	Output is not regulated	C
NC	5	No effect	D

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	GND	No effect	D
GND	2	IN	Disables device, no output, high leakage	B
IN	3	OUT	Output not regulated, high leakage	B
OUT	4	NC	No effect	D
NC	5	NC	No effect	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	No effect	D
GND	2	No output voltage, high leakage	B
IN	3	No effect	D
OUT	4	Output is not regulated	C
NC	5	No effect	D

4.3 DGK-8 Package

Figure 4-2 shows the REF34-Q1 pin diagram for the DGK-8 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the REF34-Q1 data sheet.

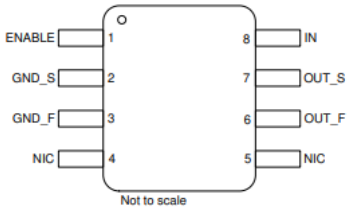

Figure 4-3. Pin Diagram (DGK-8 Package)

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND_F	1	No effect	D
GND_S	2	No effect	D
ENABLE	3	Disables device, no output voltage, high leakage	B
NC	4	No effect	D
NC	5	No effect	D
IN	6	No output voltage, high leakage	B
OUT_S	7	No output voltage	B
OUT_F	8	No output voltage	B

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND_F	1	No output voltage	B
GND_S	2	No output voltage	B
ENABLE	3	Disables device, no output voltage	B
NC	4	No effect	D
NC	5	No effect	D
IN	6	Output is not regulated	C
OUT_S	7	Output is not regulated	C
OUT_F	8	Output is not regulated	C

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND_F	1	GND_S	No effect	D
GND_S	2	ENABLE	Disables device, no output voltage, high leakage	B
ENABLE	3	NC	No effect	D
NC	4	NC	No effect	D
NC	5	IN	No effect	D
IN	6	OUT_S	Output is not regulated, high leakage	B
OUT_S	7	OUT_F	No effect	D
OUT_F	8	GND_F	No output voltage	B

Table 4-13. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND_F	1	No outpout voltage, high leakage	B
GND_S	2	No output voltage, high leakage	B
ENABLE	3	No effect	D
NC	4	No effect	D
NC	5	No effect	D
IN	6	No effect	D
OUT_S	7	Output is not regulated, high leakage	B
OUT_F	8	Output is not regulated, high leakage	B

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