LM5143-Q1 EVM User's Guide

With an input operating voltage as low as 3.5 V and up to 100 V as specified in Table 1, the LM5140/1/3/6-Q1 family of automotive synchronous buck controllers from TI provides flexibility, scalability, and optimized solution size for a range of applications. These controllers enable DC/DC solutions with high density, low EMI, and increased flexibility. All controllers are rated for a maximum operating junction temperature of 150°C and have AEC-Q100 grade 1 qualification.

Table 1. Automotive Synchronous Buck DC/DC Controller Family

DC/DC CONTROLLER	SINGLE or DUAL	V_{IN} RANGE	CONTROL METHOD	GATE DRIVE VOLTAGE	SYNC OUTPUT	PROGRAMMABLE DITHER
LM5140-Q1	Dual	3.8 V to 65 V	Peak current mode	5 V	180° phase shift	N/A
LM5141-Q1	Single	3.8 V to 65 V	Peak current mode	5 V	N/A	Yes
LM25141-Q1	Single	3.8 V to 42 V	Peak current mode	5 V	N/A	Yes
LM5143-Q1	Dual	3.5 V to 65 V	Peak current mode	5 V	90° phase shift	Yes
LM5146-Q1	Single	5.5 V to 100 V	Voltage mode	7.5 V	180° phase shift	N/A

The LM5143-Q1EVM-2100 evaluation module (EVM) is a dual-channel synchronous buck DC/DC regulator that employs synchronous rectification to achieve high conversion efficiency in a small footprint. It operates over a wide input voltage range of 5.5 V to 36 V, providing regulated outputs of 5 V and 3.3 V. The output voltages have better than 1% setpoint accuracy and are adjustable by modifying the feedback resistor values, permitting the user to customize the output voltage from 2.5 V to 8 V as needed.

The module design uses the LM5143-Q1 synchronous buck controller with the following features:

- Wide input voltage (wide V_{IN}) range of 3.5 V to 65 V
- Wide duty cycle range with low $t_{ON(min)}$ and $t_{OFF(min)}$
- Ultra-low shutdown and no-load standby quiescent currents
- Multi-phase capability
- Peak current-mode control loop architecture
- Integrated, high-current MOSFET gate drivers
- Cycle-by-cycle overcurrent protection with programmable hiccup
- Optional spread spectrum modulation for lower EMI
- Functional-safety capable

The free-running switching frequency of the EVM is 2.1 MHz and is synchronizable to a higher or lower frequency if required. Moreover, a synchronization output signal (SYNCOUT) 90° phase-shifted relative to the internal clock is available for master-slave configurations. VCC and gate drive UVLO protects the regulator at low input voltage conditions, and EN pins for each channel support application-specific power-up and power-down requirements.

The LM5143-Q1 is available in a 40-pin VQFNP package with 6-mm × 6-mm footprint to enable DC/DC solutions with high density and low component count. See the *LM5143-Q1 3.5-V to 65-V Dual Synchronous Buck DC/DC Controller* data sheet for more information. Use the LM5143-Q1 with WEBENCH® Power Designer to create a custom regulator design. To optimize component selection and examine predicted efficiency performance across line and load ranges, download the *LM5143-Q1 Quickstart Calculator*.

Contents

List of Figures

List of Tables

Trademarks

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1 High Density EVM Description

The LM5143-Q1EVM-2100 high-density EVM is designed to use a regulated or non-regulated high-voltage input rail ranging from 5.5 V to 36 V to produce tightly-regulated output voltages of 5 V and 3.3 V at load currents up to 7 A. Alternatively, as shown in Figure 2, a two-phase, 15-A single-output regulator is configured by changing the MODE, SS1/2, and COMP1/2 switch configurations, and tying the outputs together. This wide V_{IN} range DC/DC solution offers outsized voltage rating and operating margin to withstand supply rail voltage transients.

The free-running switching frequency is 2.1 MHz and is synchronizable to an external clock signal at a higher or lower frequency. The power-train passive components selected for this EVM, including buck inductors and ceramic input and output capacitors, are automotive AEC-Q200 rated and are available from multiple component vendors.

1.1 Typical Applications

- High-current automotive electronic systems using 2-,3-, and 4-phase implementations
- Dual outputs for ADAS and body electronics
- Infotainment systems and instrument clusters
- Automotive HEV/EV powertrain systems

1.2 Features and Electrical Performance

- Tightly-regulated output voltages of 5 V and 3.3 V with better than ±1% setpoint accuracy
- Wide input voltage operating range of 5.5 V to 36 V
- Single- and dual-output configurations
  - Dual outputs of 3.3 V and 5 V rated at 7 A each
  - Single output, two-phase solution provides 15 A
- Switching frequency of 2.1 MHz externally synchronizable up or down by 20%
- Ultra-high power conversion efficiency across wide load current ranges
  - Full-load efficiency of 90.25% at V_{IN} = 12 V (dual outputs of 5 V and 3.3 V at 7 A)
  - Full-load efficiency of 91.5% at V_{IN} = 12 V (single output of 5 V at 15 A)
- 25-µA controller standby current at V_{IN} = 12 V with channel 2 disabled
- Input π-stage EMI filter with electrolytic capacitor for parallel damping
  - Differential-mode and common-mode filter stages
  - Meets CISPR 25 and UNECE Reg 10 EMI standards
- Peak current-mode control architecture provides fast line and load transient response
  - Integrated slope compensation adaptive with switching frequency
  - Forced PWM (FPWM) or diode emulation mode (DEM) operation
- Integrated high-side and low-side power MOSFET gate drivers
  - 3.25-A and 4.25-A sink/source gate drive current capability
  - Independent source and sink gate driver pins for adjustable switch (SW) voltage slew rate
  - 14-ns adaptive dead-time control reduces power dissipation and MOSFET temperature rise
- Overcurrent protection (OCP) with shunt or inductor DCR current sensing
- Monotonic prebias output voltage start-up
- User-adjustable soft-start time set to 3 ms by 100-nF capacitors connected between SS1/SS2 and AGND
  - Option for output voltage tracking using master track signal connected to SS1 or SS2
- SYNCOUT signal 90° out-of-phase with internal clock
- Power Good indicators for each channel with 100-kΩ pullup resistors to VCC
- Selectable forced-PWM (FPWM) or diode emulation (DEM) modes using the MODE pin
- Fully assembled, tested, and proven PCB layout with 100-mm × 75-mm total footprint

2 EVM Characteristics

Table 2. Electrical Performance Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage range, V_{IN}	Operating		5.5	12	36	V
Input current, no load, I_{IN-NL}	I_{OUT1} = I_{OUT2} = 0 A, MODE tied to AGND	V_{IN} = 12 V		50		µA
		V_{IN} = 24 V		50		
		V_{IN} = 36 V		50		
Input current, disabled, I_{IN-OFF}	V_{EN1} = V_{EN2} = 0 V	V_{IN} = 12 V		4		µA
OUTPUT CHARACTERISTICS						
Output voltage, V_{OUT1} (1)	FB1 tied to VDDA		3.27	3.3	3.33	V
Output voltage, V_{OUT2} (1)	FB2 tied to AGND		4.95	5.0	5.05	
Output current, $I_{OUT1/2}$	V_{IN} = 5.5 V to 36 V, Airflow = 100 LFM (2)		0		7	A
Output voltage regulation, $\Delta V_{OUT1/2}$	Load regulation	$I_{OUT1/2}$ = 0 A to 7 A		0.5%		
	Line regulation	V_{IN} = 5.5 V to 36 V		0.5%		
Output voltage ripple, $V_{OUT1/2-AC}$	V_{IN} = 12 V, I_{OUT1} = I_{OUT2} = 7 A			10		mVrms
Output overcurrent protection, I_{OCP}	V_{IN} = 12 V			9		A
Soft-start time, t_{SS}	C_{SS1} = C_{SS2} = 100 nF			3		ms
Hiccup time, t_{RES}	C_{RES} = 220 nF			13		ms
SYSTEM CHARACTERISTICS						
Switching frequency, F_{SW-nom}	V_{IN} = 12 V			2.1		MHz
Half-load efficiency, η_{HALF} (1)	I_{OUT1} = I_{OUT2} = 3.5 A	V_{IN} = 8 V		91.5%		
		V_{IN} = 12 V		90.5%		
		V_{IN} = 18 V		87%		
Full load efficiency, η_{FULL}	I_{OUT1} = I_{OUT2} = 7 A	V_{IN} = 8 V		89.5%		
		V_{IN} = 12 V		90.2%		
		V_{IN} = 18 V		88.2%		
LM5143-Q1 junction temperature, T_J			–40		150	ºC

(1) The default output voltages of this EVM are 3.3 V and 5 V. Efficiency and other performance metrics can change based on operating input voltage, load currents, externally-connected output capacitors, and other parameters.

(2) The recommended airflow when operating at input voltages greater than 18 V is 100 LFM.

3 Application Circuit Diagram

Figure 1 shows the schematic of an LM5143-Q1-based synchronous buck regulator (EMI filter stage not shown). Soft start (SS), restart (RES), and dither (DITH) components are shown that are configurable as required by the specific application.

As shown in Figure 2, a two-phase, single-output regulator is implemented by typing the outputs together, connecting COMP1 to COMP2, SS1 to SS2, MODE to VDDA, and FB2 to AGND.

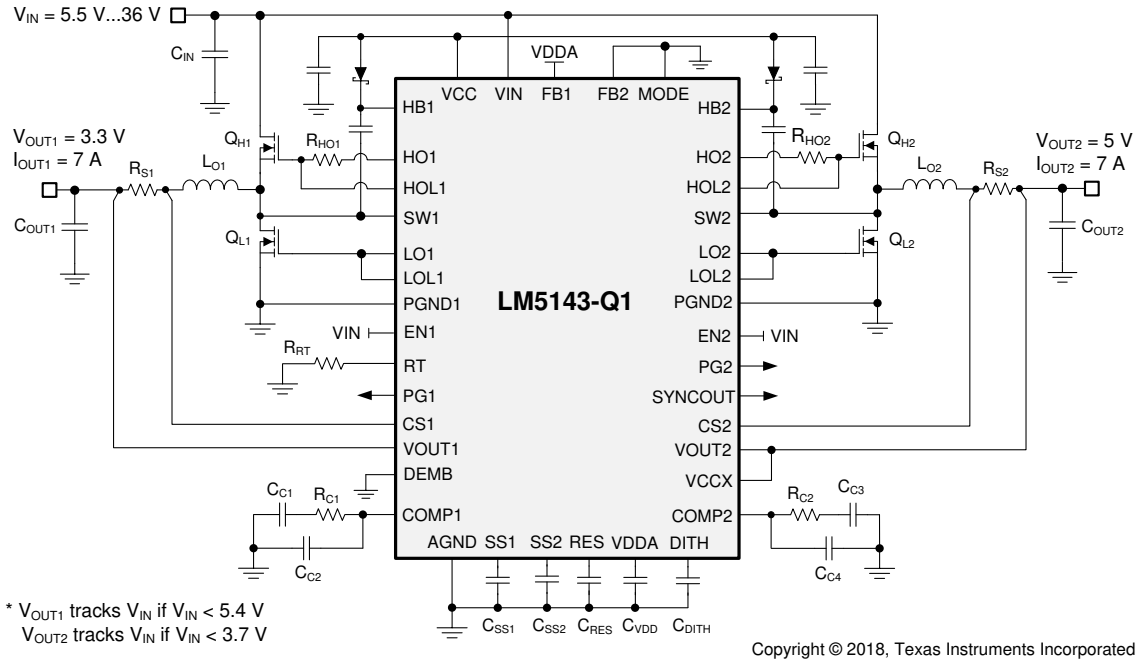


Figure 1. LM5143-Q1 Dual Synchronous Buck Regulator Simplified Schematic

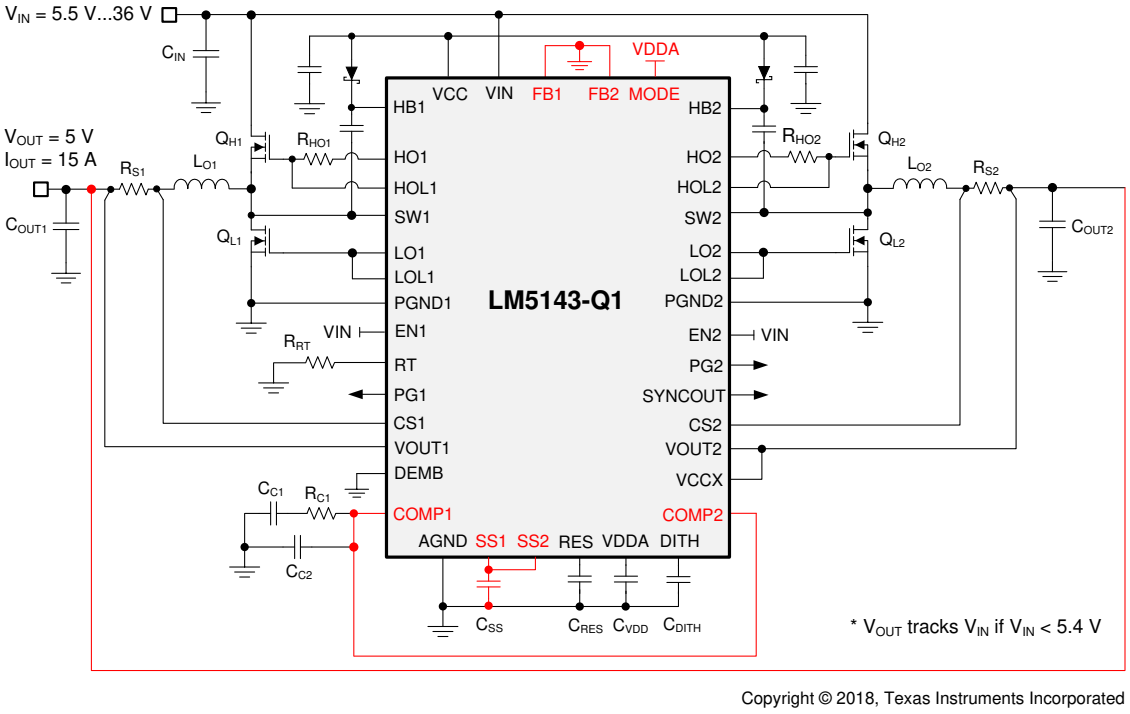


Figure 2. LM5143-Q1 Single-Output, Two-Phase Synchronous Buck Regulator Simplified Schematic

4 EVM Photo

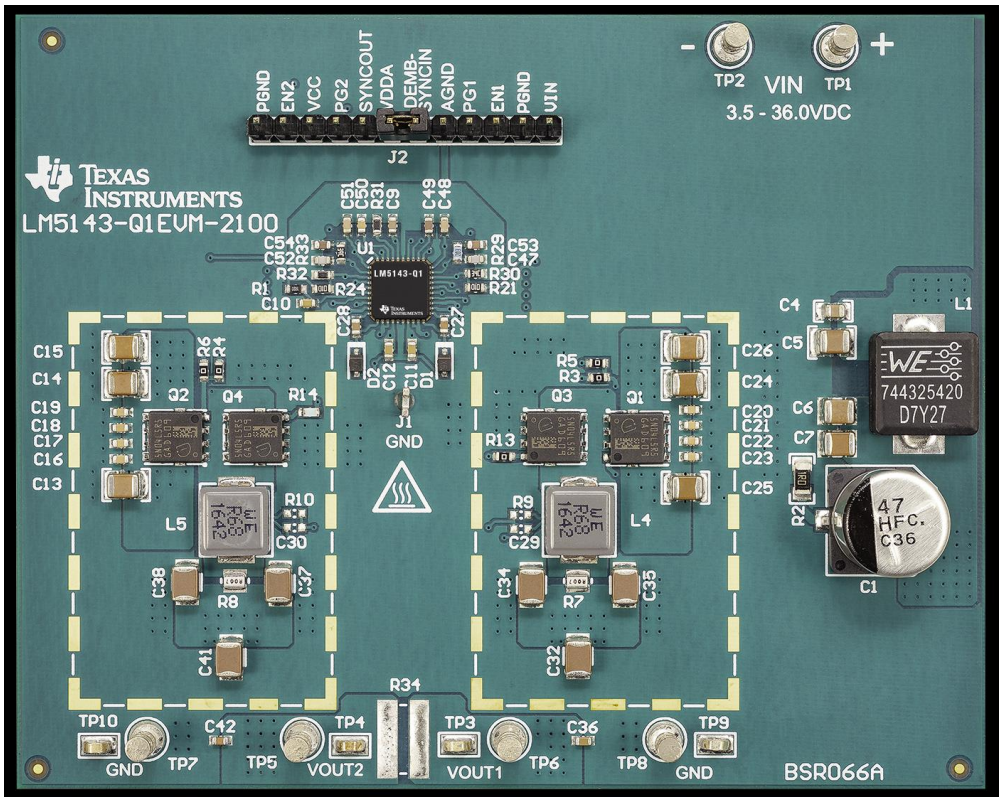


Figure 3. LM5143-Q1 EVM, 100 mm × 75 mm

CAUTION

Caution Hot surface.
Contact may cause burns.
Do not touch.

5 Test Setup and Procedure

5.1 EVM Connections

Referencing the EVM connections described in Table 3, the recommended test setup to evaluate the LM5143-Q1EVM-2100 is shown in Figure 4. Working at an ESD-protected workstation, make sure that any wrist straps, boot straps, or mats are connected and referencing the user to earth ground before handling the EVM.

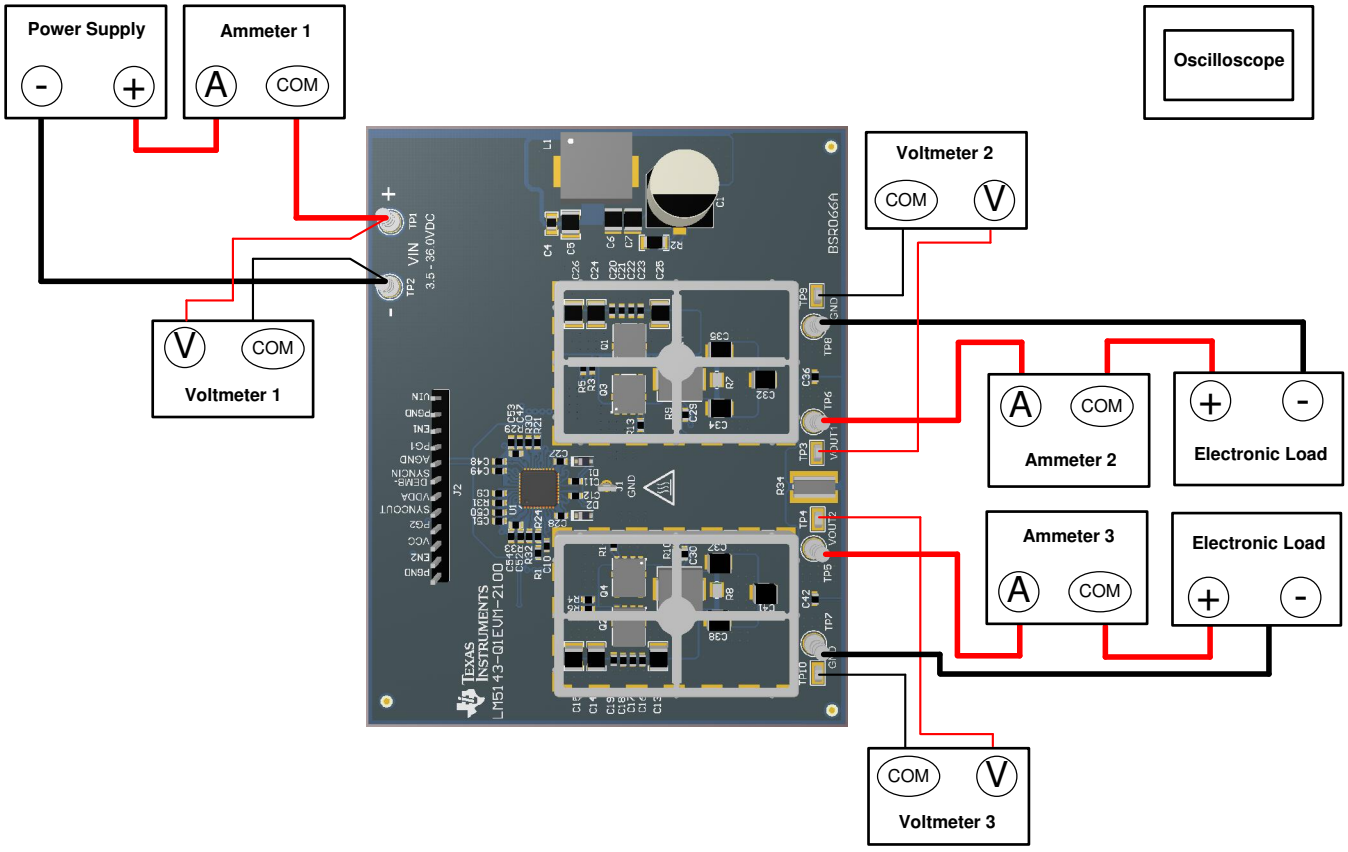


Figure 4. EVM Test Setup

CAUTION

Refer to the LM5143-Q1 data sheet, LM5143-Q1 Quickstart Calculator and WEBENCH® Power Designer for additional guidance pertaining to component selection and controller operation.

Table 3. EVM Power Connections

LABEL	DESCRIPTION
VIN+	Positive input voltage power and sense connection
VIN-	Negative input voltage and output voltage power and sense connection
VOUT1	Channel 1 positive output voltage power and sense connection
VOUT2	Channel 2 positive output voltage power and sense connection
GND	Negative output voltage power and sense connection

Table 4. EVM Signal Connections

LABEL	DESCRIPTION
VCC	Bias supply connection for the gate drivers
VDDA	Bias supply connection for the analog circuits
DEMB/SYNCIN	Synchronization input
SYNCOUT	Synchronization output
PG1, PG2	Power Good indicators
SS1, SS2	Soft-start/tracking signal inputs
EN1, EN2	ENABLE inputs – tie to GND to disable the respective channel
PGND	Power GND connection
AGND	Analog GND connection

5.2 Test Equipment

Voltage Source: Use an input voltage source capable of supplying 0–36-V and 12 A.

Multimeters:

- **Voltmeter 1:** Input voltage at VIN+ to VIN–. Set voltmeter to an input impedance of 100 MΩ.
- **Voltmeter 2:** Output voltage at VOUT1 to GND. Set voltmeter to an input impedance of 100 MΩ.
- **Voltmeter 3:** Output voltage at VOUT2 to GND. Set voltmeter to an input impedance of 100 MΩ.
- **Ammeter 1:** Input current. Set ammeter to 1-second aperture time.
- **Ammeter 2:** Output current for channel 1. Set ammeter to 1-second aperture time.
- **Ammeter 2:** Output current for channel 2. Set ammeter to 1-second aperture time.

Electronic Load: The load must be an electronic constant-resistance (CR) or constant-current (CC) mode load capable of 0 Adc to 10 Adc at 12 V. For a no-load input current measurement, disconnect the electronic load as it may draw a small residual current.

Oscilloscope: With the scope set to 20-MHz bandwidth and AC coupling, measure the output voltage ripple directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the ground barrel of the probe through the ground lead to the negative terminal of the capacitor. TI does not recommend using a long-leaded ground connection because this can induce additional noise given a large ground loop. To measure other waveforms, adjust the oscilloscope as needed.

Safety: Always use caution when touching any circuits that may be live or energized.

5.3 Recommended Test Setup

5.3.1 Input Connections

- Prior to connecting the DC input source, set the current limit of the input supply to 0.1 A maximum. Ensure the input source is initially set to 0 V and connected to the VIN+ and VIN– connection points as shown in Figure 4. An additional input bulk capacitor is recommended to provide damping if long input lines are used.
- Connect voltmeter 1 at VIN+ and VIN– connection points to measure the input voltage.
- Connect ammeter 1 to measure the input current and set to at least 1-second aperture time.

5.3.2 Output Connections

- Connect electronic loads to VOUT1 and VOUT2 connections. Set the loads to constant-resistance mode or constant-current mode at 0 A before applying input voltage.
- Connect voltmeter 2 at VOUT1 and GND connections to measure the output voltage of channel 1.
- Connect voltmeter 3 at VOUT2 and GND connections to measure the output voltage of channel 2.
- Connect ammeter 2 and ammeter 3 to measure the output currents.

5.4 Test Procedure

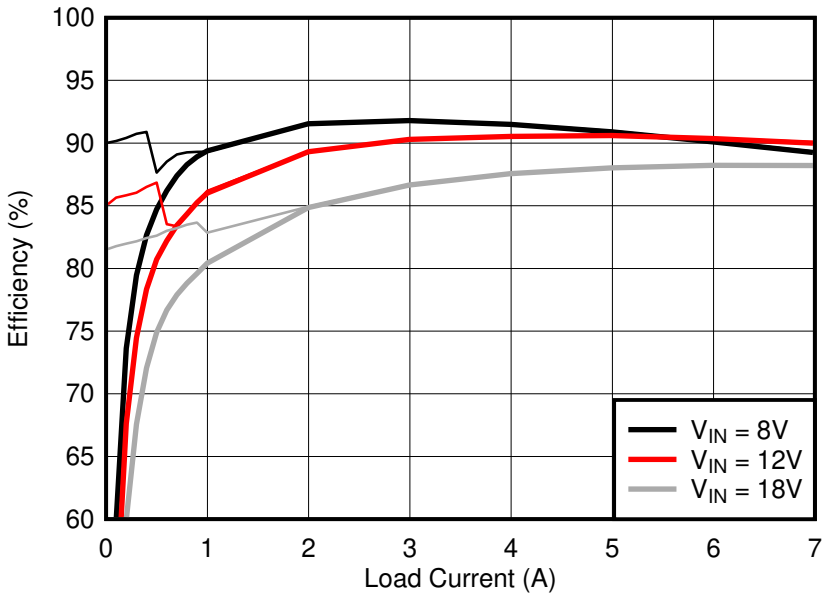
5.4.1 Line and Load Regulation, Efficiency

- Set up the EVM as described above.
- Set load to constant resistance or constant current mode and to sink 0 A.
- Increase input source from 0 V to 12 V; use voltmeter 1 to measure the input voltage.
- Increase the current limit of the input supply to 12 A.
- Using voltmeter 2 to measure the output voltage, V_{OUT1}, vary the load current from 0 A to 7 A DC; V_{OUT1} must remain within the load regulation specification.
- Using voltmeter 3 to measure the output voltage, V_{OUT2}, vary the load current from 0 A to 7 A DC; V_{OUT2} should remain within the load regulation specification.
- Set the load currents to 3.5 A (50% rated load) and vary the input source voltage from 5.5 V to 36 V; V_{OUT1} and V_{OUT2} must remain within the line regulation specification.
- Decrease load to 0 A. Decrease input source voltage to 0 V.

6 Test Data and Performance Curves

Figure 5 through Figure 24 present typical performance curves for the LM5143-Q1EVM-2100. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements.

6.1 Conversion Efficiency



The curves with higher efficiency at light load correspond to when diode emulation is enabled (DEMB tied to AGND).

Figure 5. Dual-Channel Efficiency, V_{IN} = 12 V, V_{OUT1} = 3.3 V, V_{OUT2} = 5 V

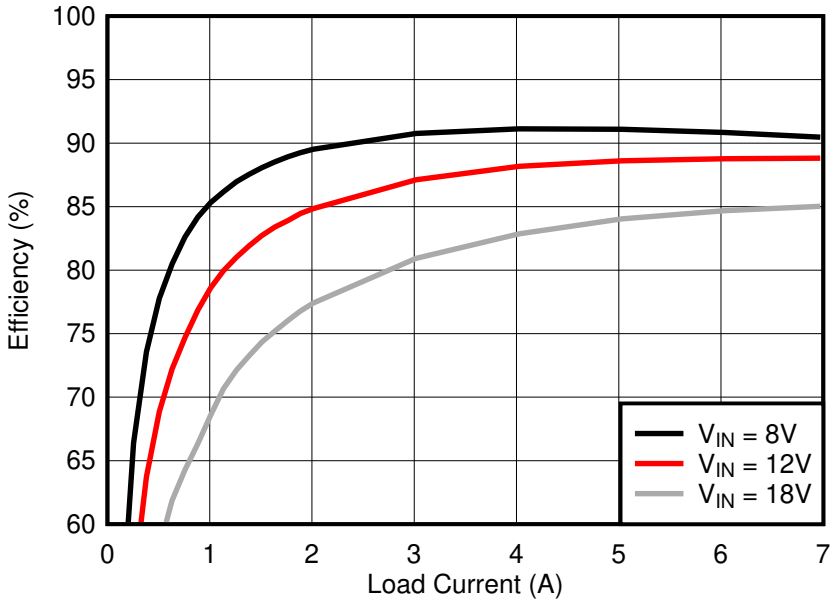


Figure 6. Ch1 Efficiency, V_{IN} = 12 V, V_{OUT1} = 3.3 V, FPWM, Channel 2 OFF

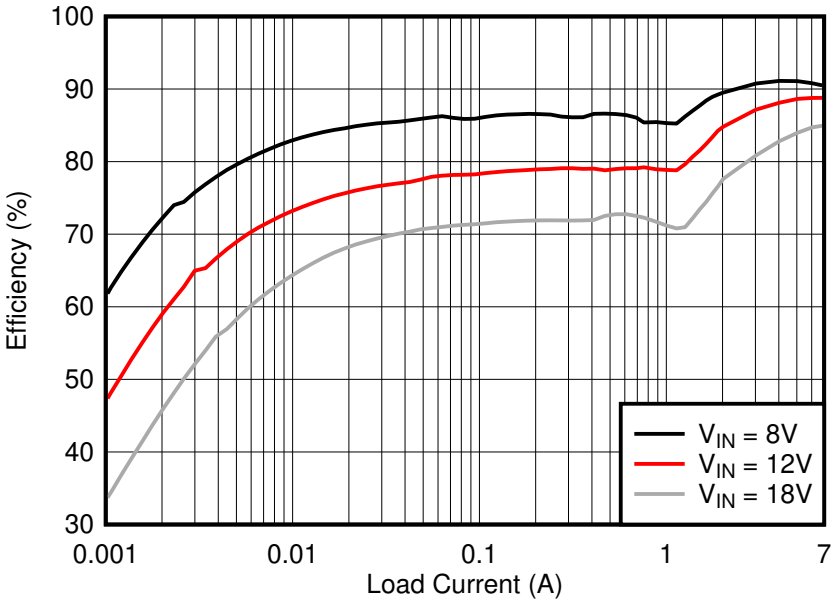


Figure 7. Ch1 Efficiency, V_{IN} = 12 V, V_{OUT1} = 3.3 V, Diode Emulation, Channel 2 OFF (Log Scale)

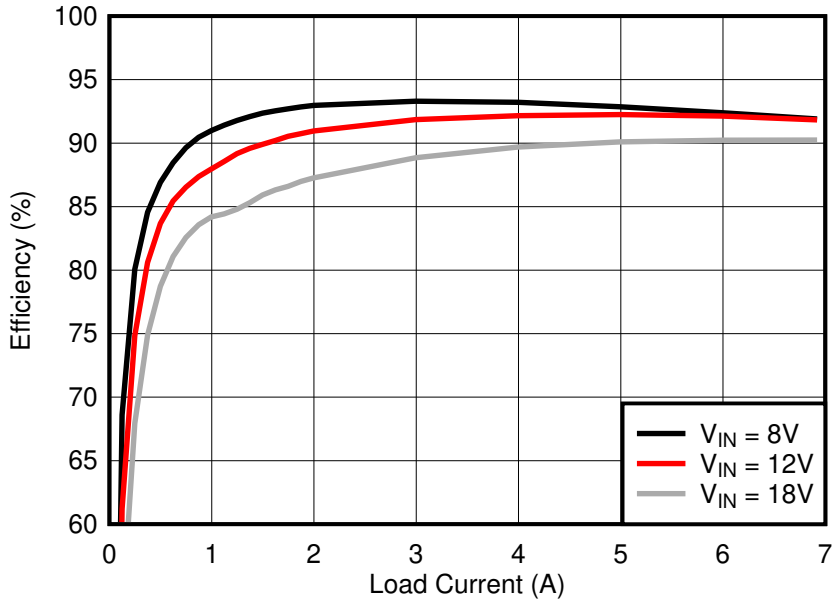


Figure 8. Ch2 Efficiency, V_{IN} = 12 V, V_{OUT2} = 5 V, FPWM, Channel 1 OFF

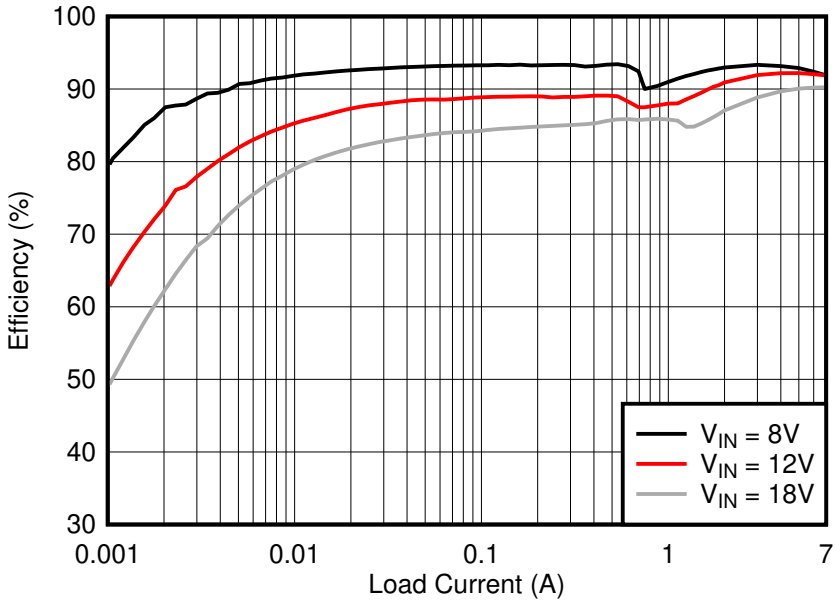
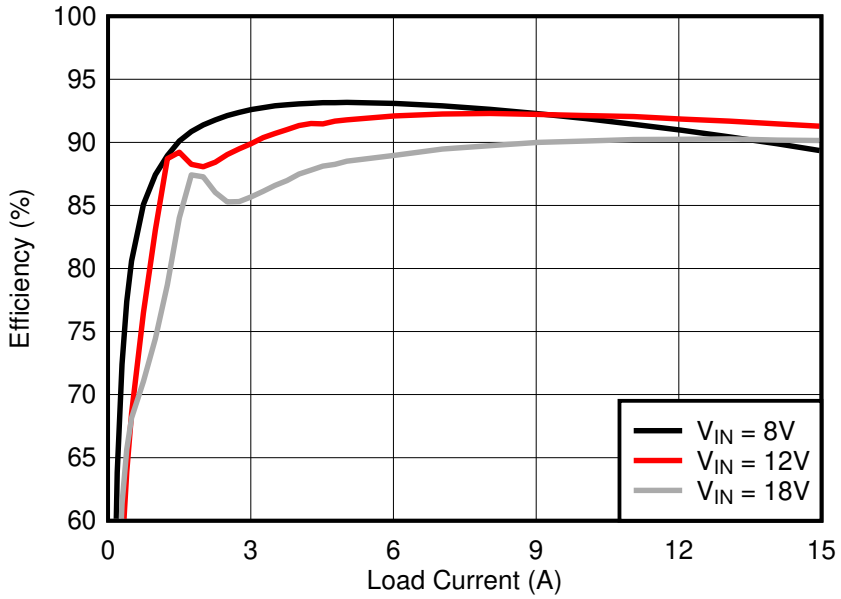


Figure 9. Ch2 Efficiency, V_{IN} = 12 V, V_{OUT2} = 5 V, Diode Emulation, Channel 1 OFF (Log Scale)



Implement a two-phase circuit by connecting the outputs together and changing the switch positions to connect SS1 to SS2, COMP1 to COMP2, and MODE to VDDA. Also tie FB2 to AGND.

Figure 10. Two-Phase Regulator Efficiency, V_{OUT} = 5 V, FPWM

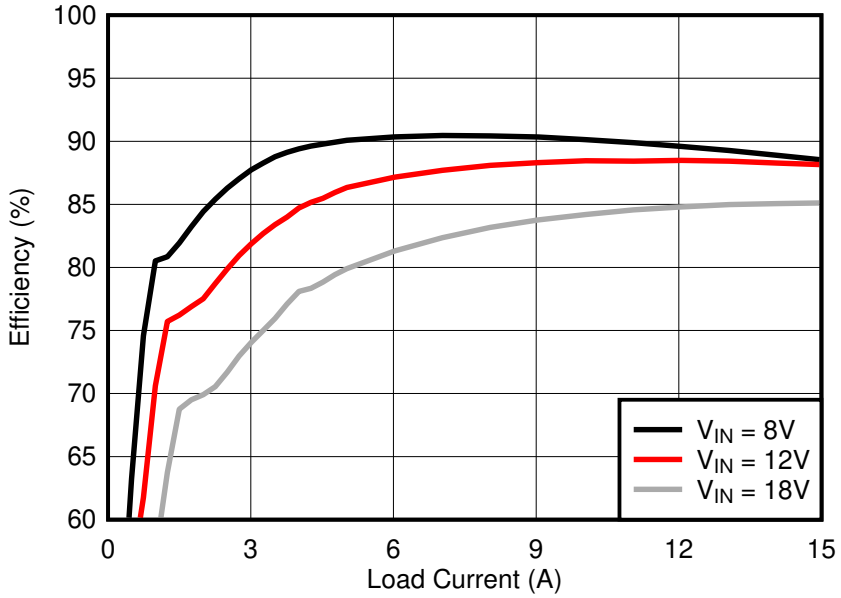


Figure 11. Two-Phase Regulator Efficiency, V_{OUT} = 3.3 V, FPWM

6.2 Operating Waveforms

6.2.1 Switching

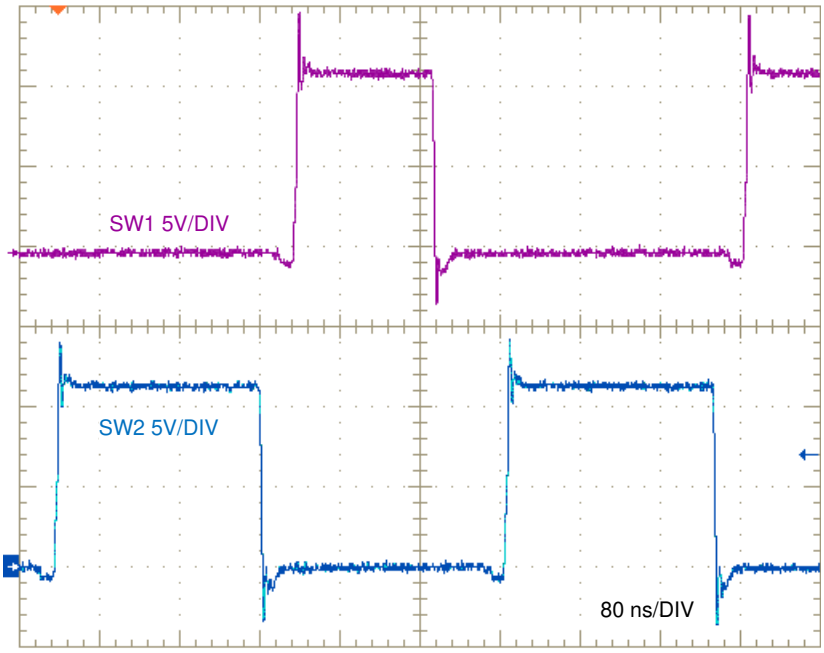


Figure 12. SW Node Voltages, V_{IN} = 12 V, I_{OUT1} = I_{OUT2} = 7 A

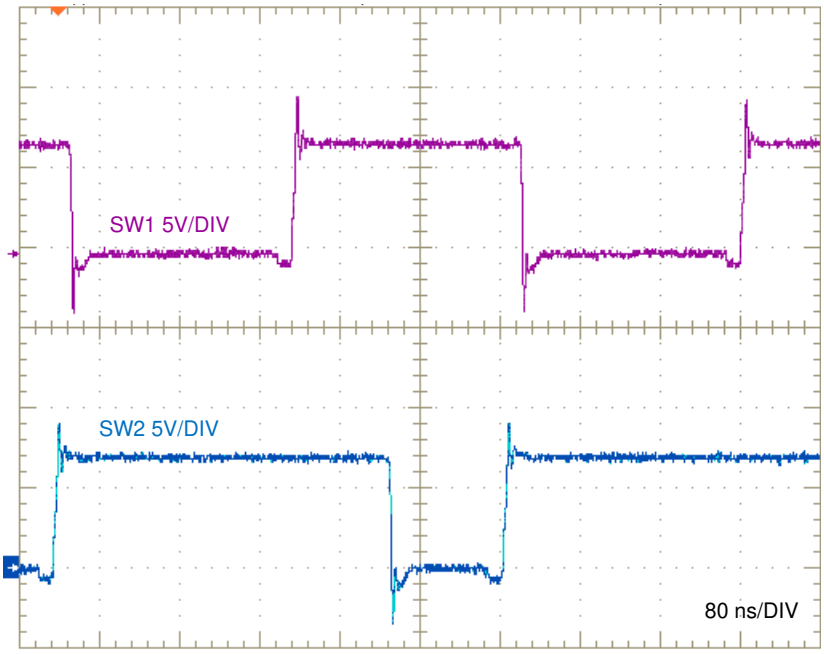


Figure 13. SW Node Voltages, V_{IN} = 8 V, I_{OUT1} = I_{OUT2} = 7 A

6.2.2 Load Transient Response

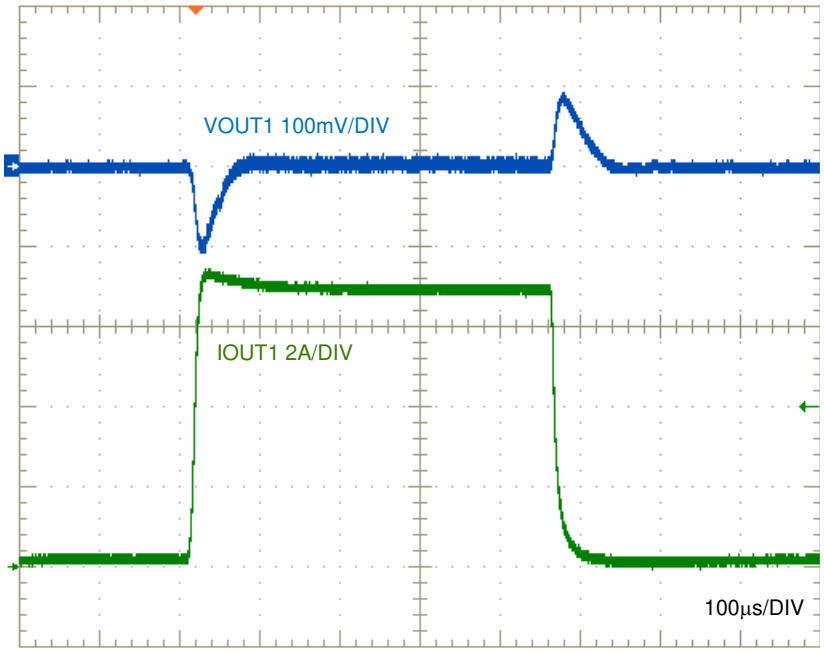


Figure 14. Ch1 (3.3 V) Load Transient Response, V_{IN} = 12 V, FPWM, 0 A to 7 A at 1 A/µs

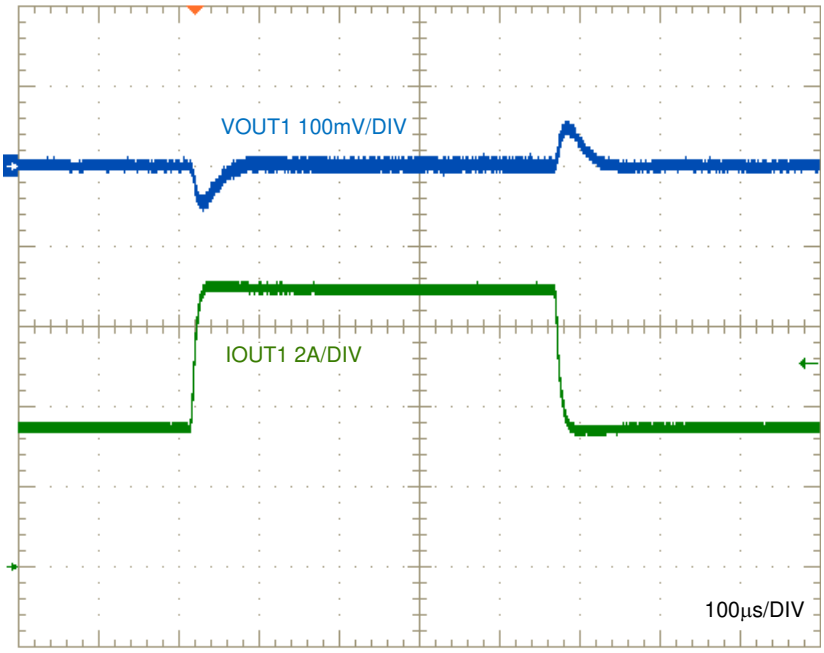


Figure 15. Ch1 (3.3 V) Load Transient Response, V_{IN} = 12 V, FPWM, 3.5 A to 7 A at 1 A/µs

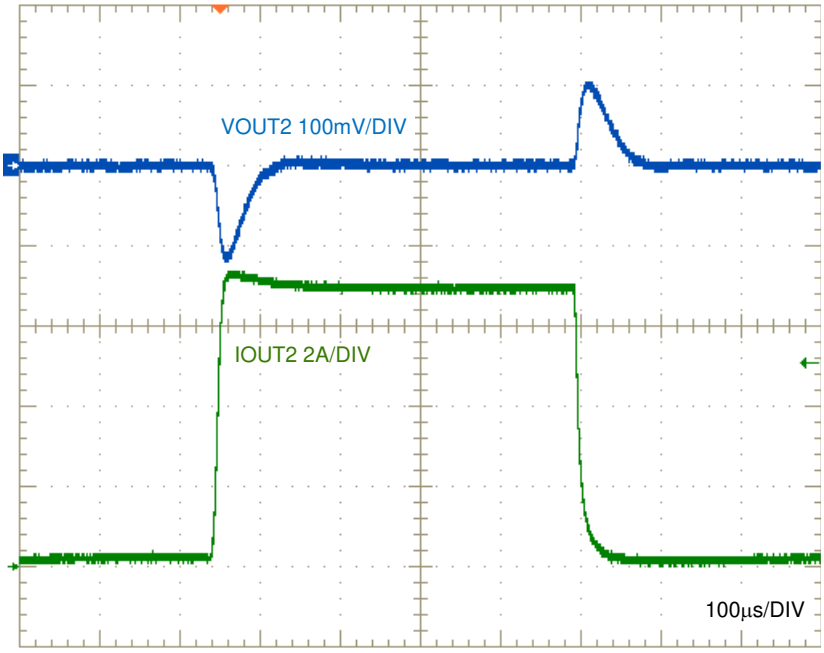


Figure 16. Ch2 (5 V) Load Transient Response, V_{IN} = 12 V, FPWM, 0 A to 7 A at 1 A/µs

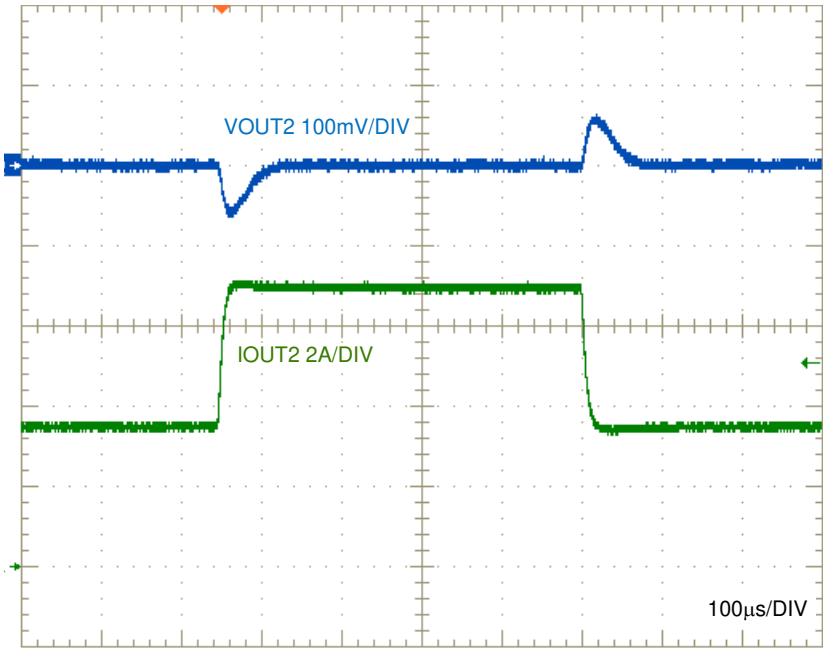


Figure 17. Ch2 (5 V) Load Transient Response, V_{IN} = 12 V, FPWM, 3.5 A to 7 A at 1 A/µs

6.2.3 Line Transient Response

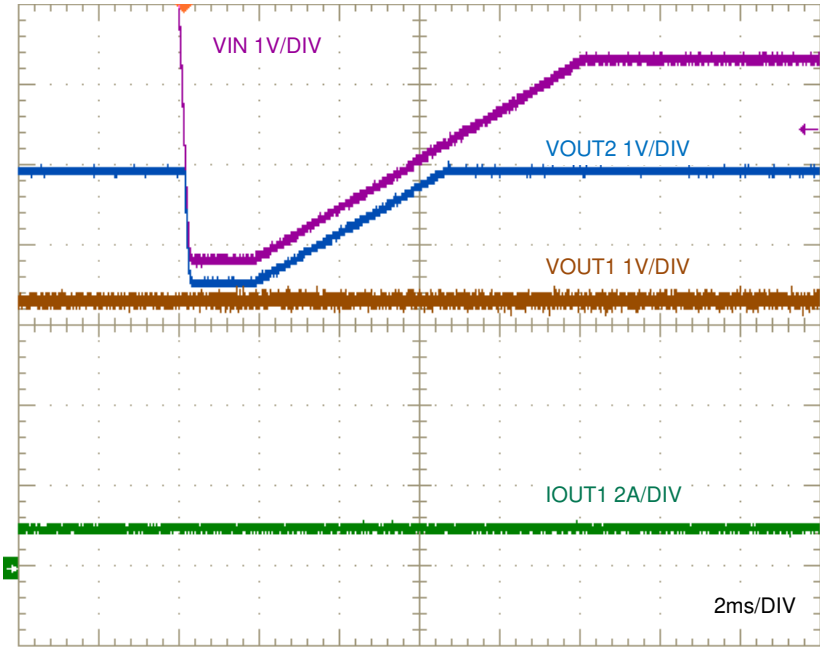


Figure 18. Cold-crank Response to V_{IN} = 3.8 V, I_{OUT1} = I_{OUT2} = 1 A

6.2.4 Startup/Shutdown With ENABLE ON/OFF

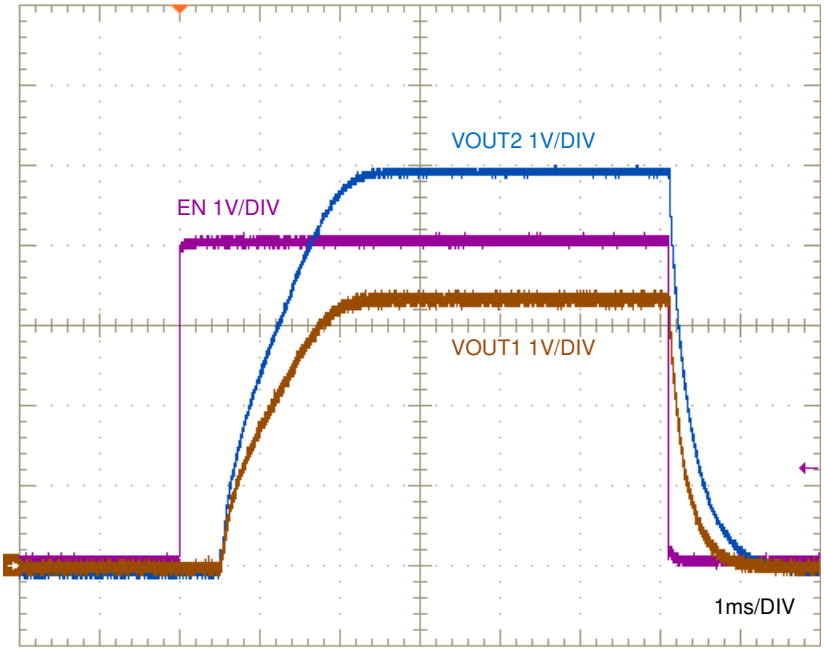


Figure 19. ENABLE ON and OFF, V_{IN} = 12 V, I_{OUT1} = I_{OUT2} = 7 A Resistive, C_{SS1} = C_{SS2} = 68 nF

6.2.5 Startup/Shutdown with EN1 and EN2 Tied to VIN

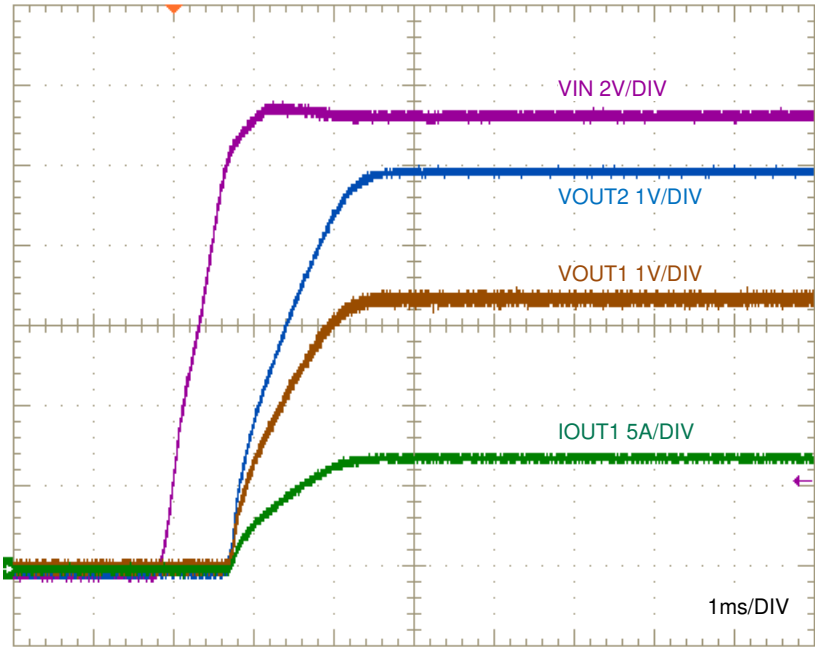


Figure 20. Startup, V_{IN} = 12 V, I_{OUT1} = I_{OUT2} = 7 A Resistive, C_{SS1} = C_{SS2} = 68 nF

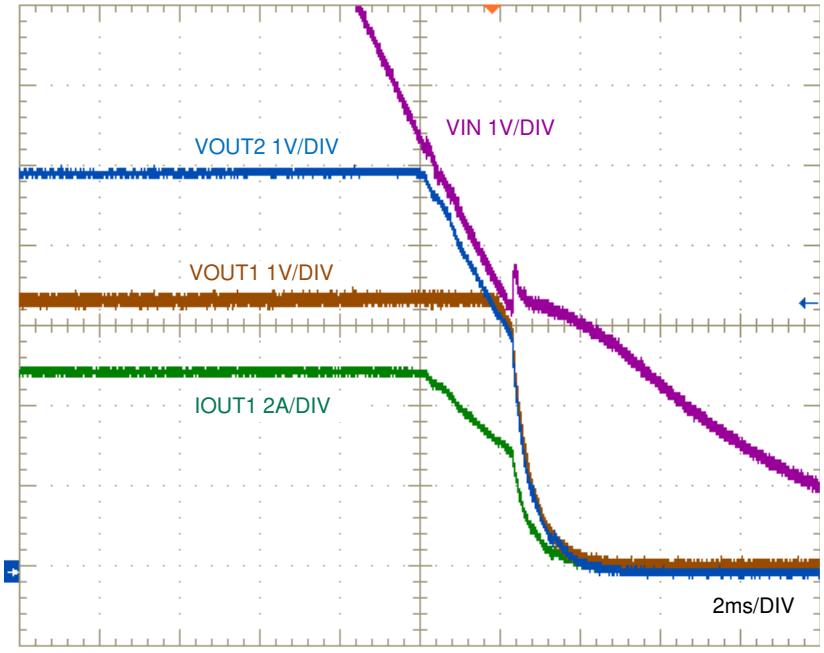


Figure 21. Shutdown, V_{IN} = 12 V, I_{OUT1} = I_{OUT2} = 7 A Resistive

6.3 Bode Plots

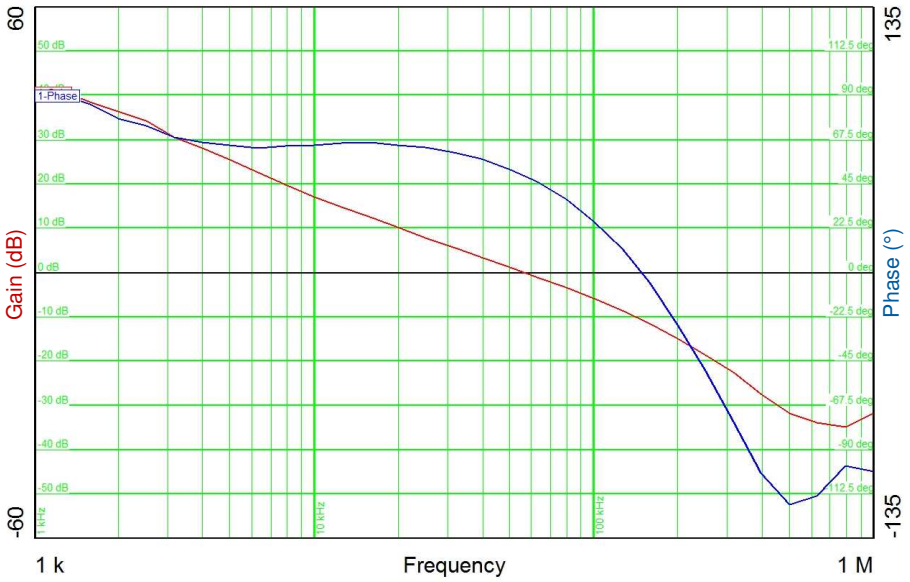


Figure 22. Bode Plot, V_{IN} = 12 V, V_{OUT1} = 3.3 V, I_{OUT1} = 7 A Resistive

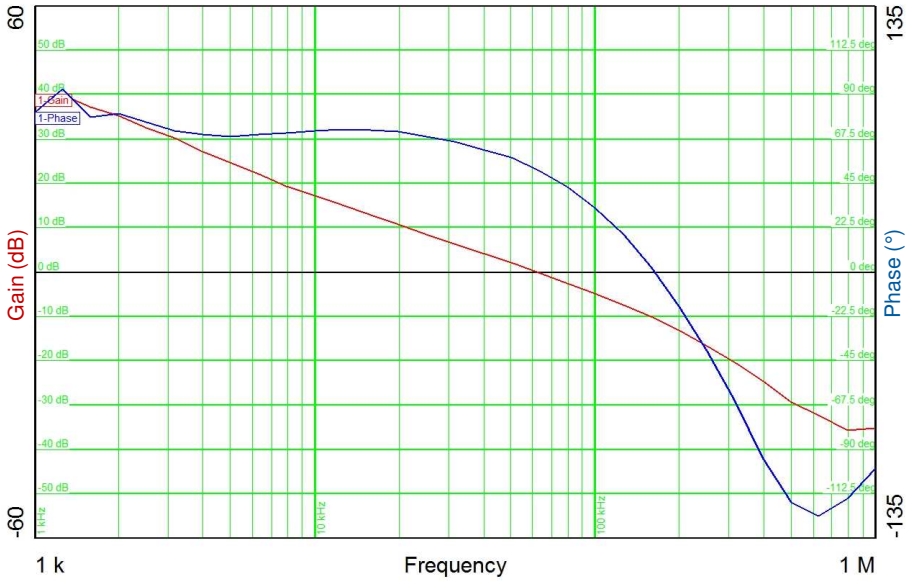


Figure 23. Bode Plot, V_{IN} = 12 V, V_{OUT2} = 5 V, I_{OUT2} = 7 A Resistive

6.4 Thermal Performance

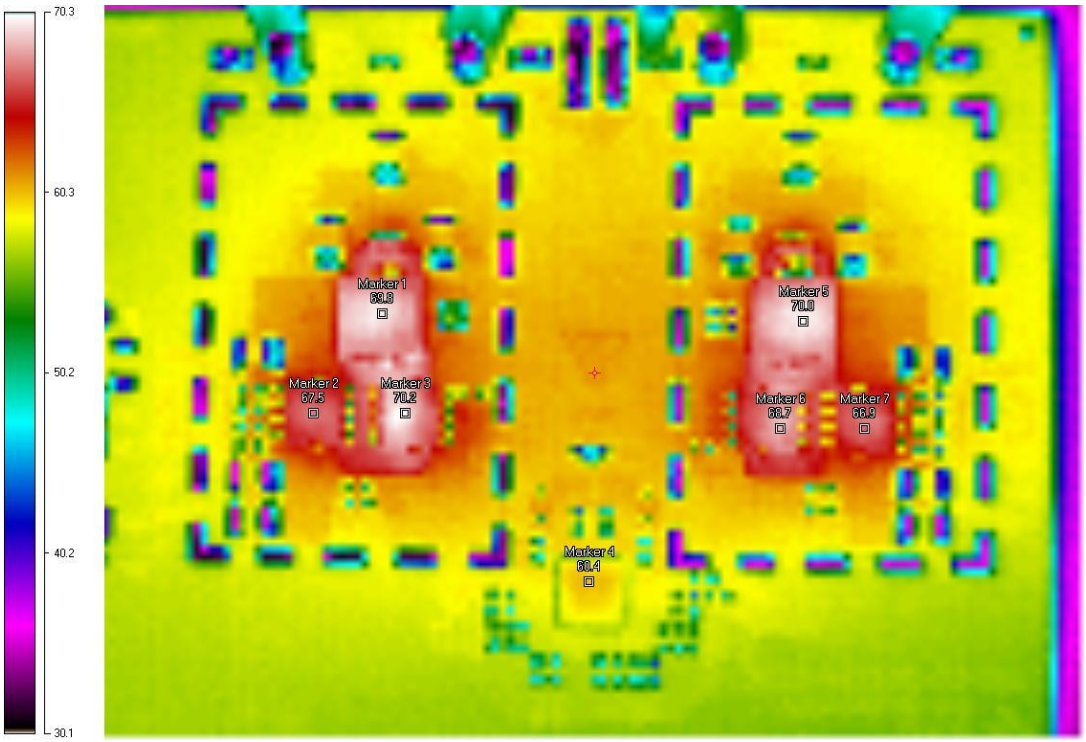


Figure 24. Thermal Performance, V_{IN} = 12 V, I_{OUT1} = I_{OUT2} = 7 A, Free Convection Airflow

6.5 CISPR 25 EMI Performance

Figure 25 presents the EMI performance of the LM5143-Q1 EVM at 13.5-V input and shields installed. Conducted emissions are measured over a frequency range of 150 kHz to 108 MHz using a 5-µH LISN according to the CISPR 25 specification. CISPR 25 class 5 peak and average limit lines are denoted in red. The yellow and blue spectra are measured using peak and average detection, respectively.

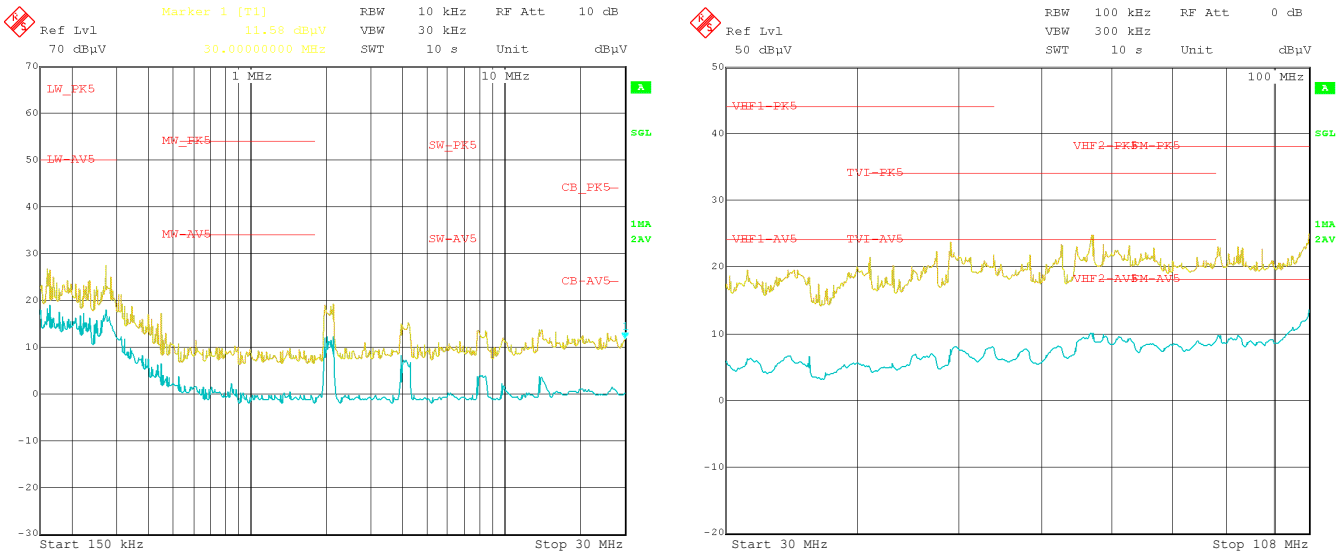


Figure 25. CISPR 25 Class 5 Conducted Emissions Plot, 150 kHz to 30 MHz, V_{IN} = 13.5 V, I_{OUT1} = I_{OUT2} = 7 A Resistive, (a) 150 kHz to 30 MHz, (b) 30 MHz to 108 MHz

7 EVM Documentation

7.1 Schematic

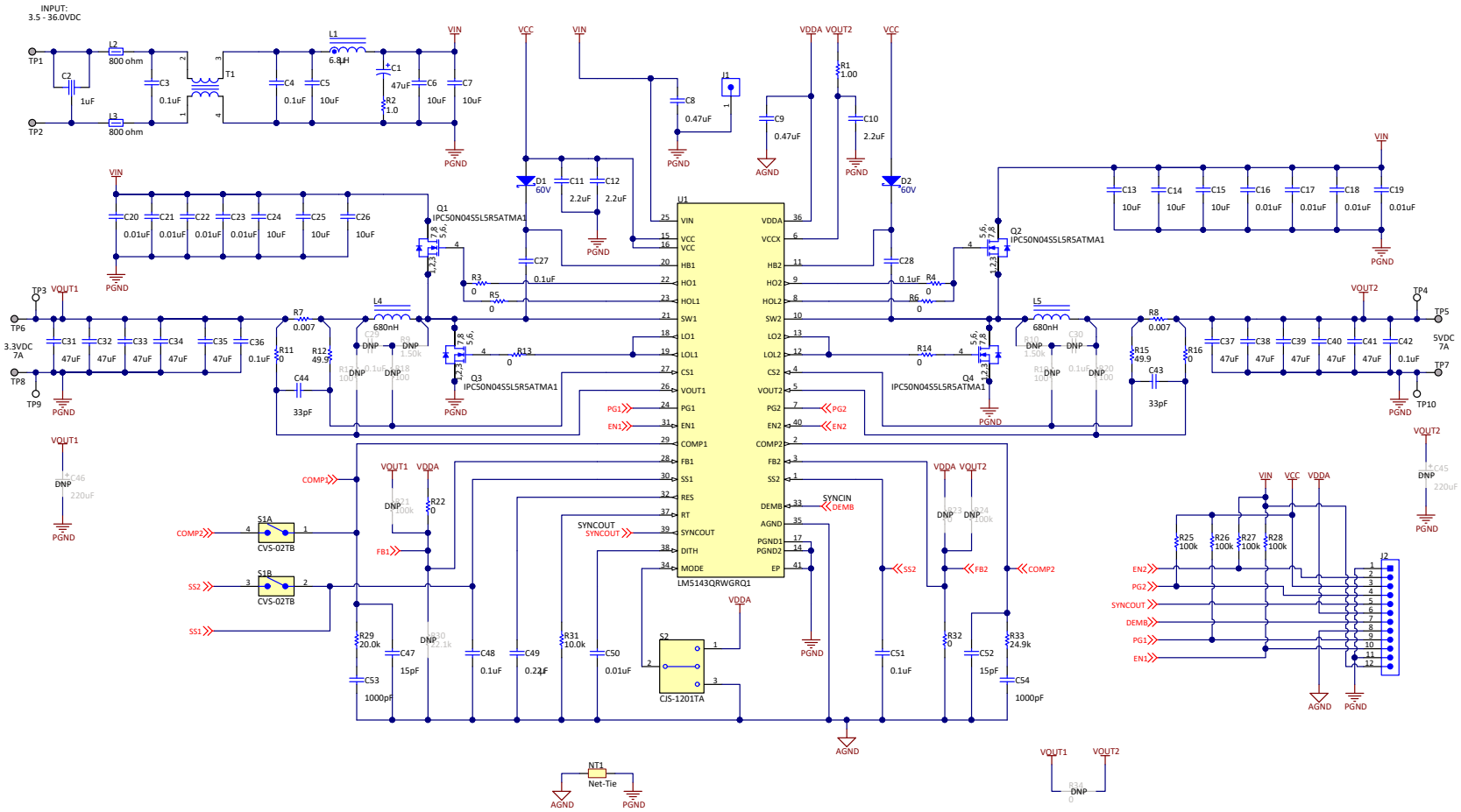


Figure 26. EVM Schematic

7.2 Bill of Materials

Table 5. Bill of Materials

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	C1	Capacitor, Aluminum, 47 µF, 50 V	EEE-FC1H470P	Panasonic
1	C2	Capacitor, Ceramic, 0.1 µF, 100 V, X7R, 1206	YFF31AH2A105M	TDK
2	C3, C4	Capacitor, Ceramic, 0.1 µF, 100 V, X7R, 0603	C0805C104K1RACTU	Kemet
9	C5, C6, C7, C13, C14, C15, C24, C25, C26	Capacitor, Ceramic, 10 µF, 50 V, X7R, 1210, AEC-Q200	UMJ325KB7106KMHT	Taiyo Yuden
			CNA6P1X7R1H106K250AE	TDK
		Capacitor, Ceramic, 10 µF, 50 V, X7R, 1206, AEC-Q200	CGA5L1X7R1H106K160AC	TDK
1	C8	Capacitor, Ceramic, 0.47 µF, 100 V, X7R, 0805	Std	Std
1	C9	Capacitor, Ceramic, 0.47 µF, 16 V, X7R, 0805	Std	Std
3	C10, C11, C12	Capacitor, Ceramic, 2.2 µF, 10 V, X7R, 0603	Std	Std
9	C16, C17, C18, C19, C20, C21, C22, C23, C50	Capacitor, Ceramic, 10 nF, 100 V, X7R, 0603	GRM188R72A103KA01D	Murata
3	C27, C28, C42	Capacitor, Ceramic, 0.1 µF, 25 V, X7R, 0603	Std	Std
10	C31, C32, C33, C34, C35, C37, C38, C39, C40, C41	Capacitor, Ceramic, 47 µF, 6.3 V, X7R, 1210, AEC-Q200	CGA6P1X7S0J476M250AC	TDK
			JMK325B7476KMHTR	Taiyo Yuden
			GCM32ER70J476KE19L	Murata
1	C36	Capacitor, Ceramic, 2.2 µF, 16 V, X7R, 0603	EMK107BB7225MA-T	Taiyo Yuden
2	C43, C44	Capacitor, Ceramic, 33 pF, 100 V, C0G, 5%, 0603	Std	Std
2	C47, C52	Capacitor, Ceramic, 15 pF, 50 V, C0G, 5%, 0603	Std	Std
2	C48, C51	Capacitor, Ceramic, 100 nF, 25 V, X7R, 10%, 0603	Std	Std
1	C49	Capacitor, Ceramic, 220 nF, 16 V, X7R, 0603	Std	Std
2	C53, C54	Capacitor, Ceramic, 1 nF, 50 V, X7R, 10%, 0603	Std	Std
0	C45, C46	Capacitor, Tant Polymer, 220 µF, 10 V, 7343, 25 mΩ ESR, AEC-Q200	T598D227M010ATE025	Kemet
2	D1, D2	Schottky Diode, 60 V, 1 A, SOD-323	PMEG6010CEJ	Nexperia
0	H1, H2	Surface Mount Shield, 38.1 × 25.4 mm, Height 6 mm	BMI-S-205-F	Laird
0	H7, H8	Shield Cover, 38.56 × 25.86 mm	BMI-S-205-C	Laird
1	J1	Test Point Slotted, 0.118", TH	1040	Keystone
1	J2	Header, 2.54 mm, 12×1, Au, TH	PBC12SABN	Sullins
1	L1	Inductor, 4.2 µH, 7.1 mΩ typ, 14A Isat, 4.7 mm typ, AEC-Q200	744325420	Würth Electronik
		Inductor, 4.7 µH, 8.3 mΩ typ, 15.7 A Isat, 5.2 mm typ, AEC-Q200	VCHA105D-4R7MS6	Cyntec
		Inductor, 4.7 µH, 9.2 mΩ typ, 15.7 A Isat, 6.5 mm max, AEC-Q200	SPM10065VT-4R7M-D	TDK
2	L2, L3	Ferrite Bead, 800 Ω at 100 MHz, 8 A, 2220	HR2220V801R-10	Laird
2	L4, L5	Inductor, 0.68 µH, 4.8 mΩ typ, 25 A, 2.8 mm typ, AEC-Q200	744373460068	Würth Electronik
		Inductor, 0.68 µH, 4.5 mΩ typ, 22 A, 2.8 mm typ, AEC-Q200	VCMV063T-R68MN2T[3]	Cyntec
		Inductor, 0.68 µH, 7.4 mΩ typ, 12.2 A, 3 mm max, AEC-Q200	SPM5030VT-R68M-D	TDK
4	Q1, Q2, Q3, Q4	MOSFET, N-Channel, 40 V, 5.7 mΩ, AEC-Q101	IPC50N04S5L5R5	Infineon
1	R1	Resistor, Chip, 1 Ω, 1/10W, 1%, 0603	Std	Std
1	R2	Resistor, Chip, 1 Ω, 1/4W, 5%, 1206	Std	Std
10	R3, R4, R5, R6, R11, R13, R14, R16, R22, R32	Resistor, Chip, 0 Ω, 1/10W, 1%, 0603	Std	Std
2	R7, R8	Resistor, Chip, 7 mΩ, 1W, 1%, 0508, AEC-Q200	KRL2012M-R007-F-T1	Susumu
2	R12, R15	Resistor, Chip, 49.9 Ω, 1/10W, 1%, 0603	Std	Std
4	R25, R26, R27, R28	Resistor, Chip, 100 kΩ, 1/16W, 1%, 0603	Std	Std
1	R29	Resistor, Chip, 20 kΩ, 1/10W, 1%, 0603	Std	Std
1	R31	Resistor, Chip, 10 kΩ, 1/10W, 1%, 0603	Std	Std
1	R32	Resistor, Chip, 13.7 kΩ, 1/10W, 1%, 0603	Std	Std
1	R33	Resistor, Chip, 24.9 kΩ, 1/10W, 1%, 0603	Std	Std
0	R34	Resistor, Chip, 0 Ω, 2 W, 1%, 1225	RCL12250000Z0EG	Vishay
1	S1	DIP Switch, SPST, 2Pos, Slide, SMT	CVS-02TB	Copal Electronics
1	S2	Slide SW, SPDT 0.1 A 50VDC	CJS-1201TA	Copal Electronics

Table 5. Bill of Materials (continued)

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	T1	Common-mode Choke, 700 Ω at 100 MHz, 6 mΩ, 8 A, AEC-Q200	ACM12V-701-2PL-TL00	TDK
6	TP1, TP2, TP5, TP6, TP7, TP8	Terminal, Turret, TH, Triple	1598-2	Keystone
4	TP3, TP4, TP9, TP10	Test Point, Miniature, SMT	5015	Keystone
1	U1	IC, LM5143-Q1, 65-V Dual Synchronous Buck Controller, VQFN-40	LM5143QRGWRQ1	TI
1	PCB1	PCB, FR4, 6 layer, 2 oz, 100 mm x 75 mm	PCB	–

7.3 PCB Layout

Figure 27 through Figure 34 show the design of the LM5143-Q1 EVM using a 6-layer PCB with 2-oz copper thickness. The EVM is essentially a single-sided design except for certain input filtering and small-signal components located on the bottom side.

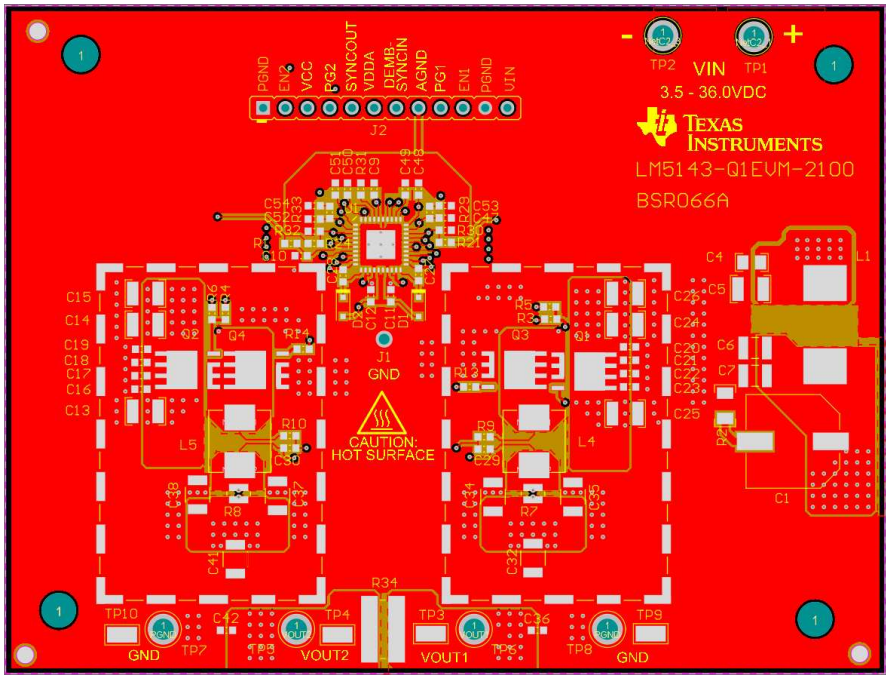


Figure 27. Top Copper (Top View)

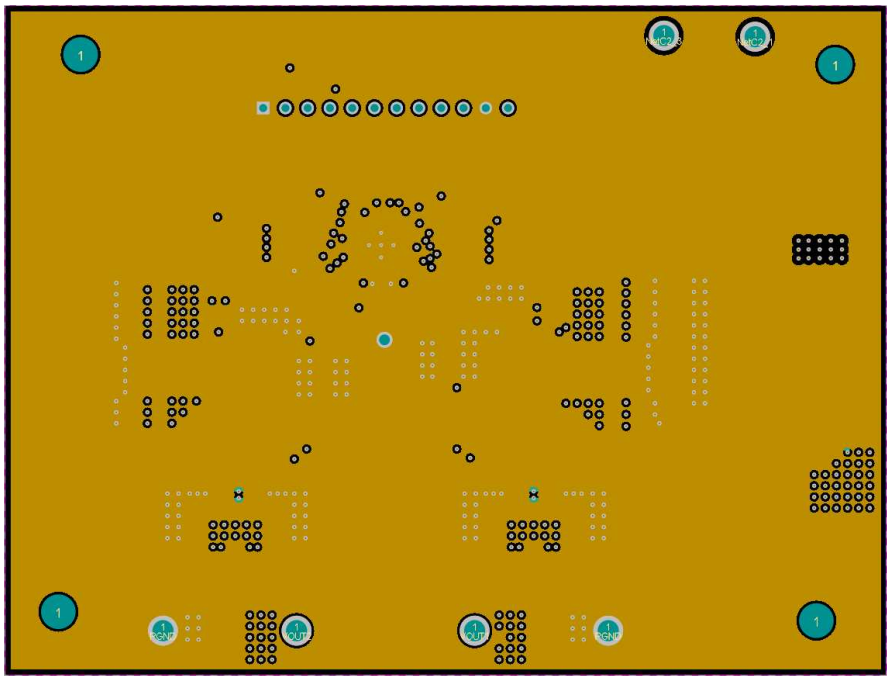


Figure 28. Layer 2 Copper (Top View)

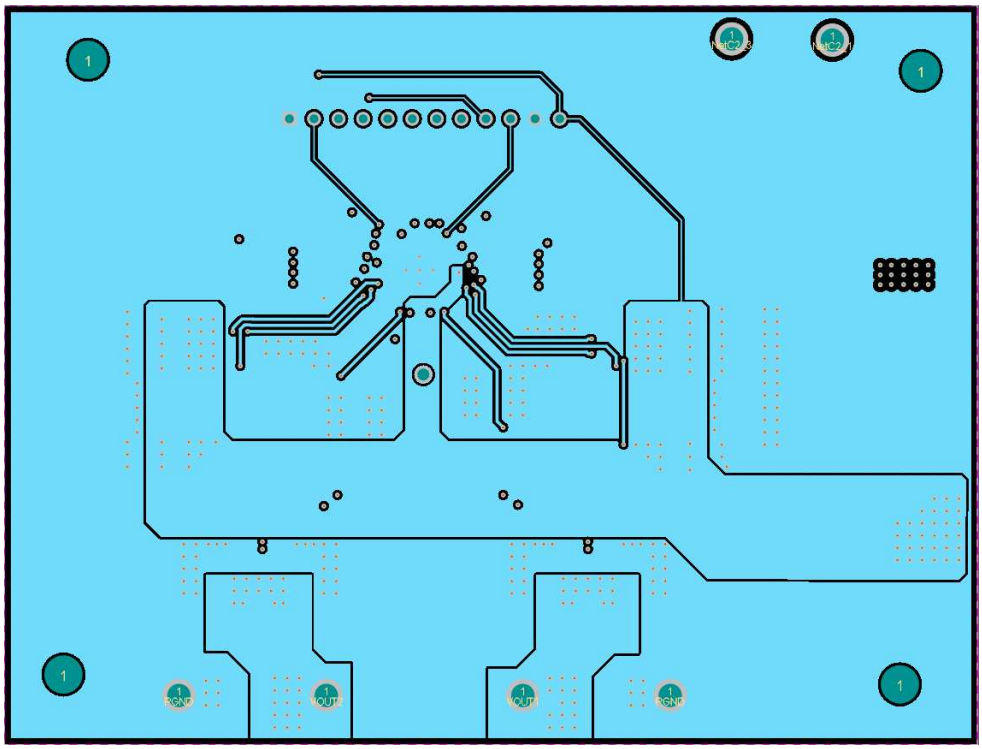


Figure 29. Layer 3 Copper (Top View)

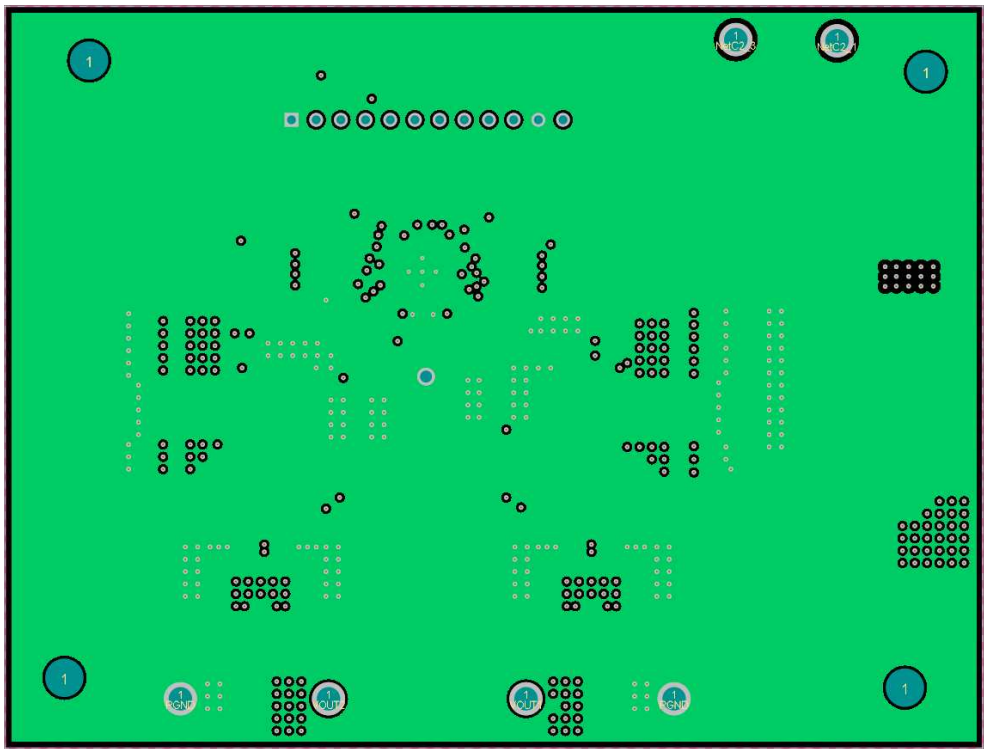


Figure 30. Layer 4 Copper (Top View)

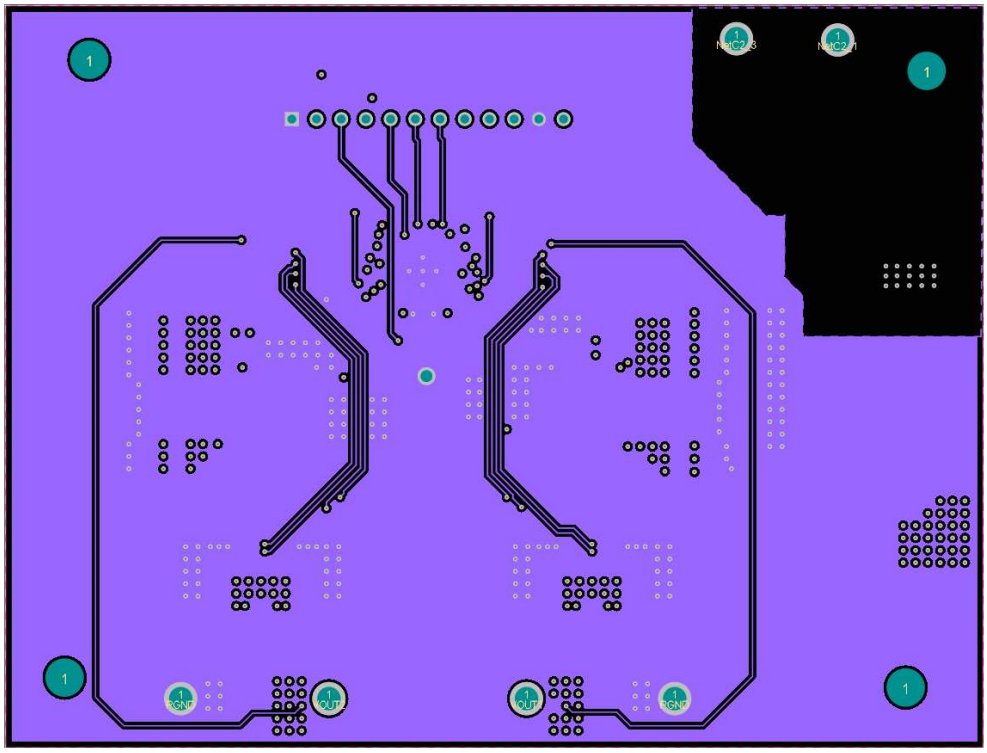


Figure 31. Layer 5 Copper (Top View)

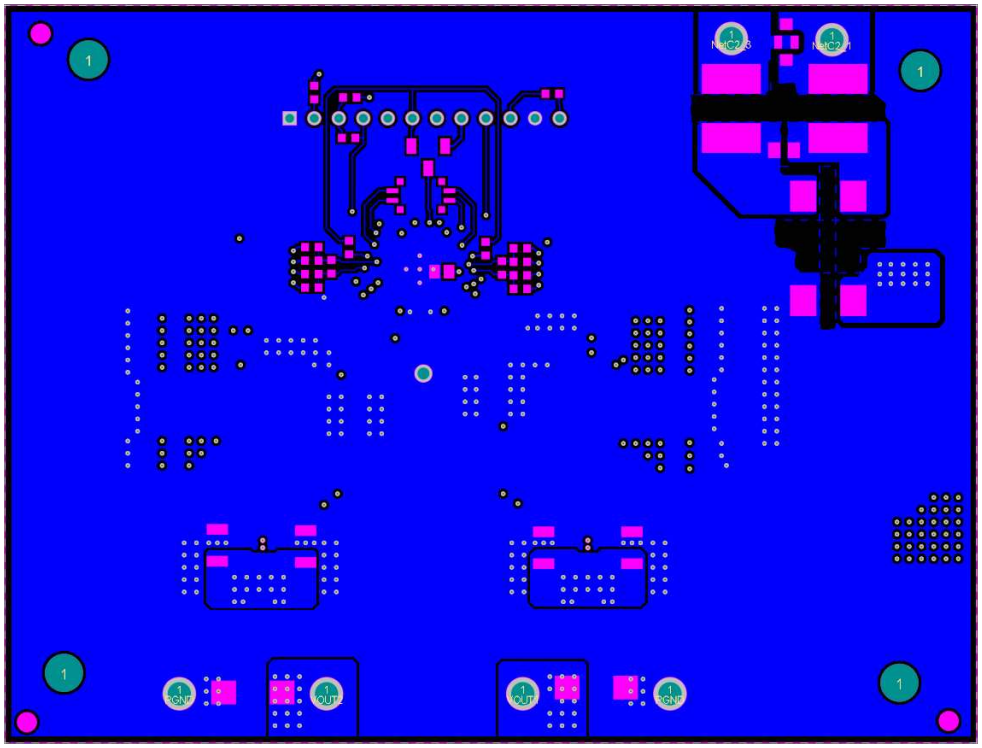


Figure 32. Bottom Copper (Top View)

7.4 Component Drawings

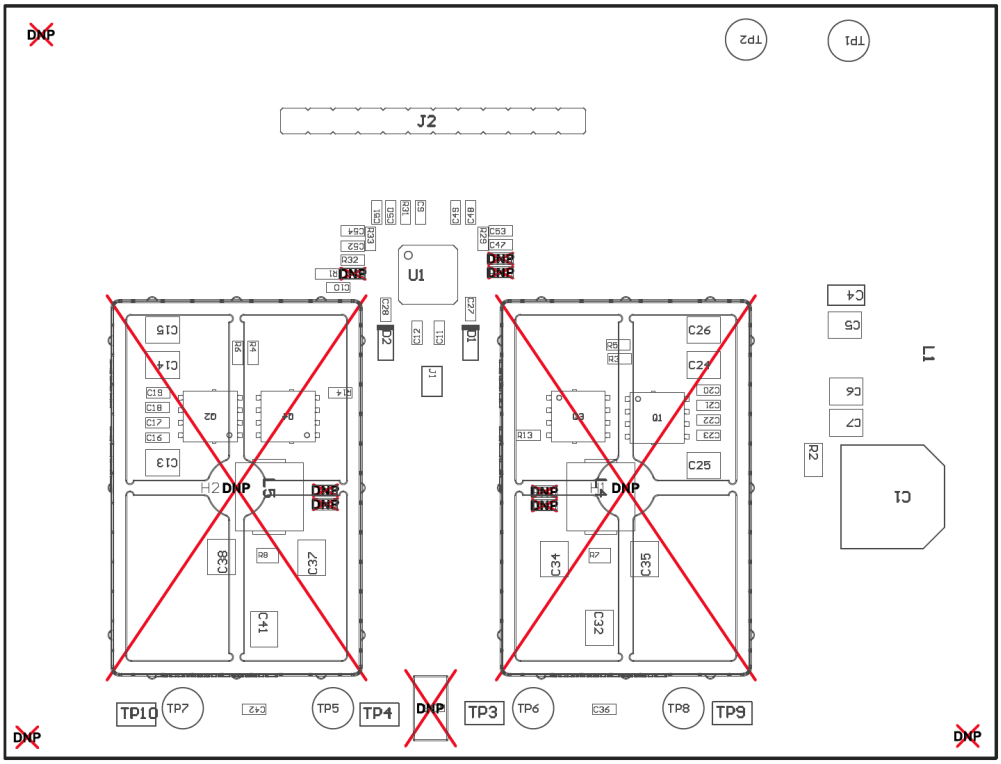


Figure 33. Top Component Drawing

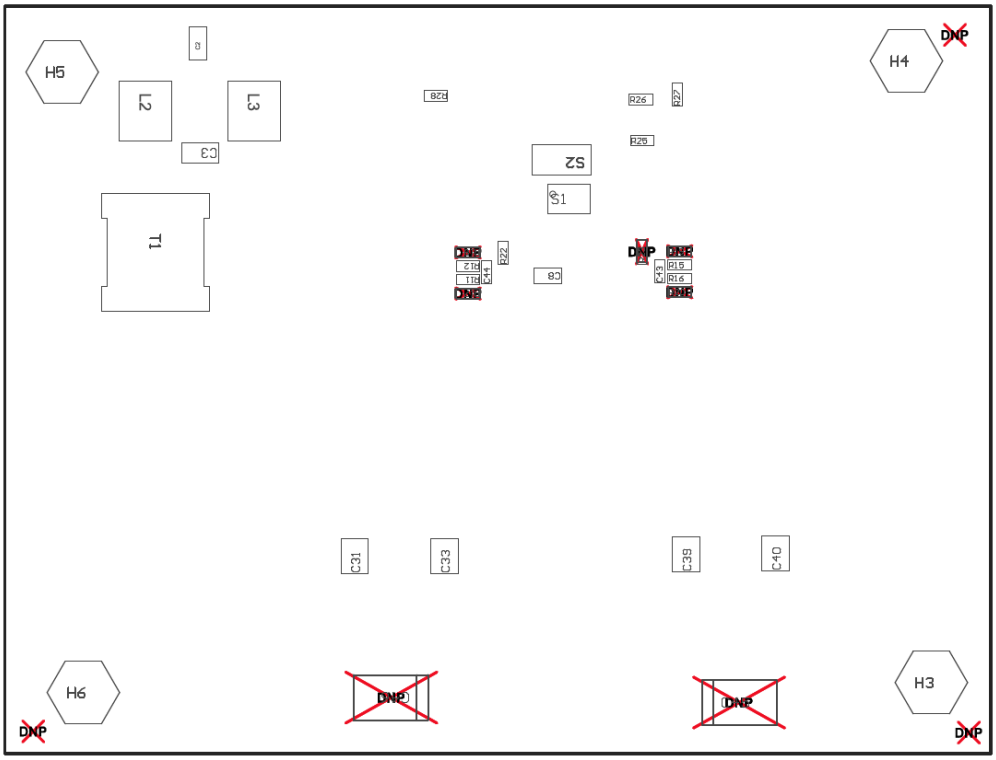


Figure 34. Bottom Component Drawing

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

For development support see the following:

- For TI's reference design library, visit TI Designs
- For TI's WEBENCH Design Environments, visit the WEBENCH® Design Center
- LM5143-Q1 DC/DC Controller Quickstart Calculator and PSPICE simulation models

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- *LM5143-Q1 Data Sheet* (SNVSB29)
- *LM5143-Q1 4-Phase Buck Regulator Design* (SNVA870)
- *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout* (SNVA803)
- *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics* (SLYT682)
- *AN-2162 Simple Success with Conducted EMI from DC-DC Converters* (SNVA489)
- White Papers:
  - *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications* (SLYY104)
  - *An Overview of Conducted EMI Specifications for Power Supplies* (SLYY136)
  - *An Overview of Radiated EMI Specifications for Power Supplies* (SLYY142)

8.2.1.1 PCB Layout Resources

- *AN-1149 Layout Guidelines for Switching Power Supplies* (SNVA021)
- *AN-1229 Simple Switcher PCB Layout Guidelines* (SNVA054)
- *Constructing Your Power Supply – Layout Considerations* (SLUP230)
- *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x* (SNVA721)
- Power House Blogs:
  - *High-Density PCB Layout of DC-DC Converters*

8.2.1.2 Thermal Design Resources

- *AN-2020 Thermal Design by Insight, Not Hindsight* (SNVA419)
- *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* (SNVA183)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Thermal Design Made Simple with LM43603 and LM43602* (SNVA719)
- *PowerPAD Thermally Enhanced Package* (SLMA002)
- *PowerPAD Made Easy* (SLMA004)
- *Using New Thermal Metrics* (SBVA025)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (April 2019) to B Revision **Page**

- Added *Table 1* 1
- Added low I_Q and multi-phase capability feature bullets in the Introduction 1
- Updated *Section 8* 28

Changes from Original (October 2018) to A Revision **Page**

- Added SW node voltage waveform. 14
- Added EMI results 20
- Changed input capacitor C2 in schematic and BOM. 21

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