TMS320C64x DSP Host Port Interface (HPI) Performance

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ABSTRACT

This application report describes the number of CPU cycles required to perform a given host port interface (HPI) data transfer based on a variety of permutations of burst length, CPU speed, EMIF speed, etc.

The HPI provides direct connectivity between a host processor and a CPU's memory space via a 32/16-bit parallel port. The HPI throughput between a host processor and the TMS320C64x™ DSP is a function of the transaction type (read or write, with or without auto-increment,) memory access time, and the DSP's hardware configuration.

This document provides data sheets of possible TMS320C64x hardware configurations, and their effects on HPI throughput performance; more specifically, transfer latency, the number of CPU cycles required to transfer *n* words of data, and overall throughput given *n* word bursts.

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1 Design Problem

How do various hardware permutations affect the host port interface (HPI) throughput on TMS320C64x digital signal processors?

2 Solution

The HPI provides a host processor with direct connectivity to the CPU's memory space and memory-mapped peripherals through an asynchronous parallel port. The HPIC, the HPIA, and the HPID registers are used to perform host access. The HPIC is the HPI control register, used to set configuration bits and initialize the interface; the HPIA is the HPI address register which contains the address of the memory where the current access occurs; and the HPID is the HPI data register which contains information from the data bus. Normally, the host access sequence is: initialize the HPIC register, initialize the HPIA register, and write/read from the HPID register. Various hardware configurations influence the performance of a HPI transfer in different ways. The configurations under examination include:

- CPU speed
- HPI speed
- HPI width
- Transfer source/destination
- EMIF speed
- EMIF width
- Burst length
- Transfer type

Where transfer types are:

- Read with auto-increment address mode
- Read with fixed address mode
- Write with auto-increment address mode
- Write with fixed address mode

When operating in fixed-address mode, the address register is not updated between transfers. In auto-increment address mode, the address register is incremented between transfers, allowing the host to asynchronously burst data across the HPI. A HPI burst transfer terminates with a host access to either the HPIA or HPIC.

A note concerning HPI speed: Despite the fact that the HPI is an asynchronous interface, HPI measurements are evaluated at different HPI clock speeds. During a transaction without wait states, HSTROBE_ acts as a clock. Therefore, HPI speed actually refers to the HSTROBE_ frequency when data is being transferred without wait states.

3 Measurement Assumptions

In the cases presented here, the TMS320C64x DSP is in the idle mode. The DMA controller is dedicated to the HPI, since the only requests to the DMA are the ones from the HPI. Unless otherwise stated, the EMIF is connected to SDRAM. All measurements are approximate, and were taken with ideal system traffic. The actual throughput for specific applications will vary.

4 Latency

Transaction latency is the amount of time from when the host starts a transaction to when the target is ready to transfer the first data item. To improve performance, the HPI uses an internal read/write buffer to prefetch data before performing the transaction. While the host is prefetching data, it must insert host wait states by deasserting $\overline{\text{HRDY}}$. The final latency of a transaction is the time required to initialize the HPIA, and prefetch data. You do not need to initialize the HPIC since it only needs to be done once, and is not required before all transfers.

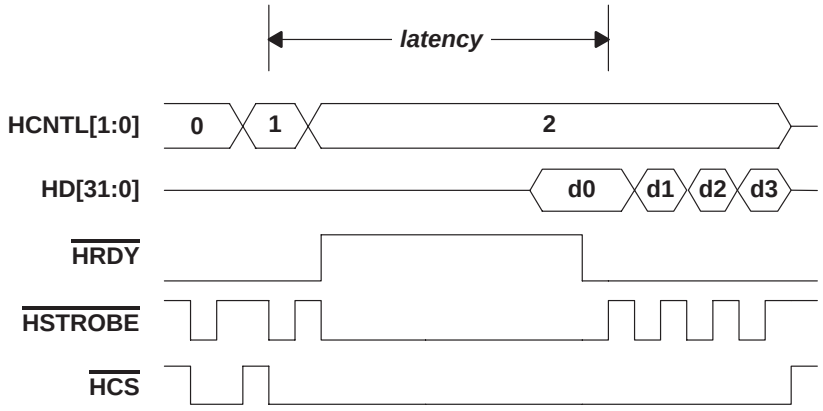

Figure 1. Auto-Increment Read Latency Timing Diagram

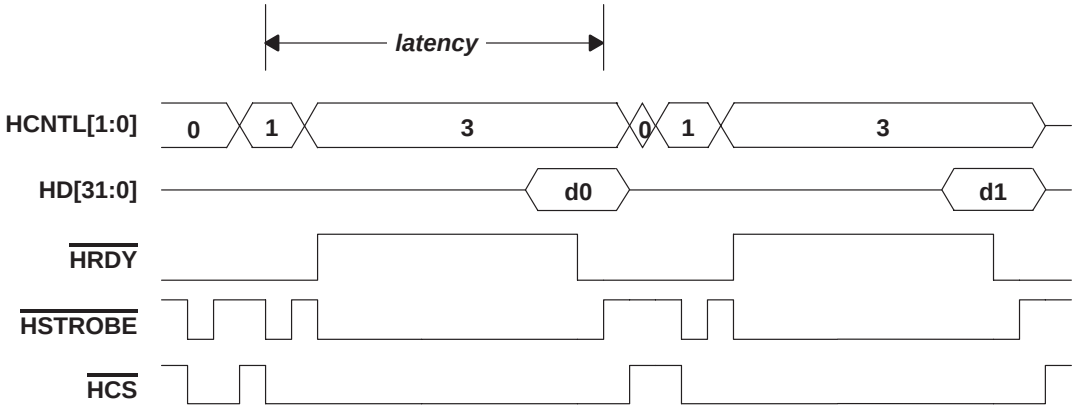

Figure 2. Fixed Read Latency Timing Diagram

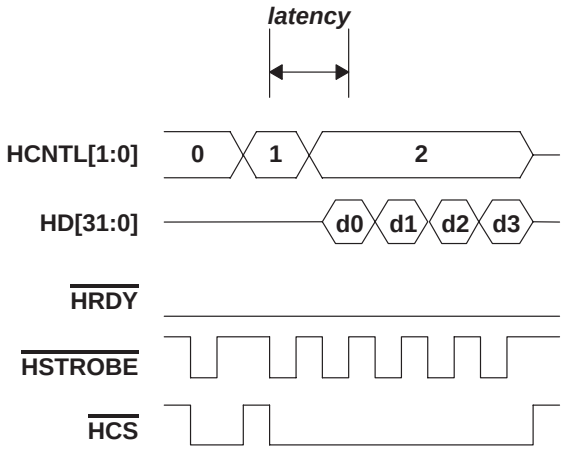

Figure 3. Auto-Increment Write Latency Timing Diagram

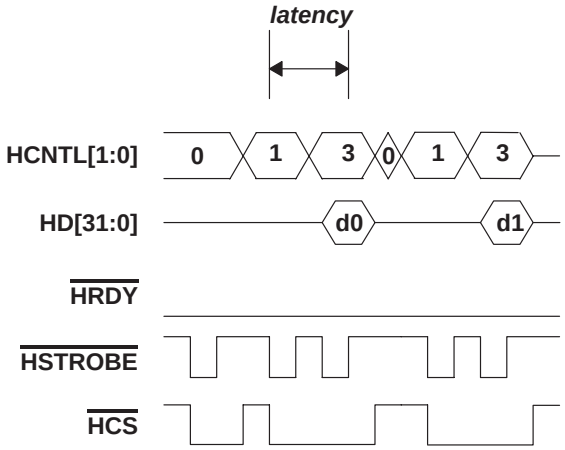

Figure 4. Fixed Write Latency Timing Diagram

5 Number of CPU Cycles Required to Transfer *n* Words of Data

Before a host transfers data through the HPI bus, it must prefetch data into either its read-ahead or write buffers. The host may then burst data across the HPI bus. As the data in the buffer deplete, the device must simultaneously prefetch more data while continually transferring information. If the time required to prefetch data exceeds the time to transfer data, the buffer will eventually completely empty and the host must insert a wait state by deasserting $\overline{\text{HRDY}}$. Once more data is available in the buffer, the host may reassert $\overline{\text{HRDY}}$ and continue the transaction.

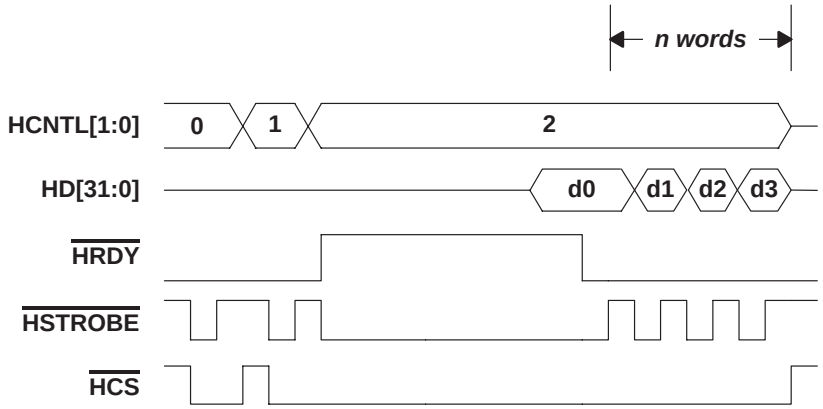

Figure 5. Number of CPU Cycles to Auto-Increment Read *n* Words Timing Diagram

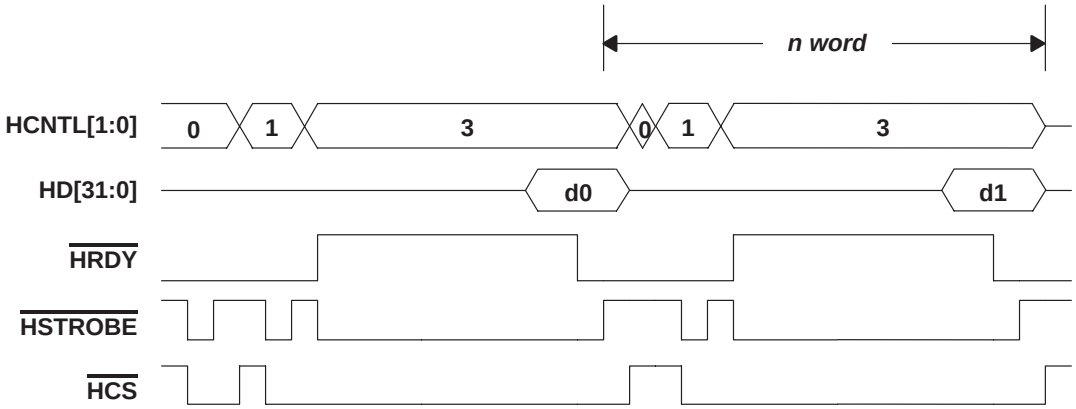

Figure 6. Number of CPU Cycles to Fixed Read *n* Words Timing Diagram

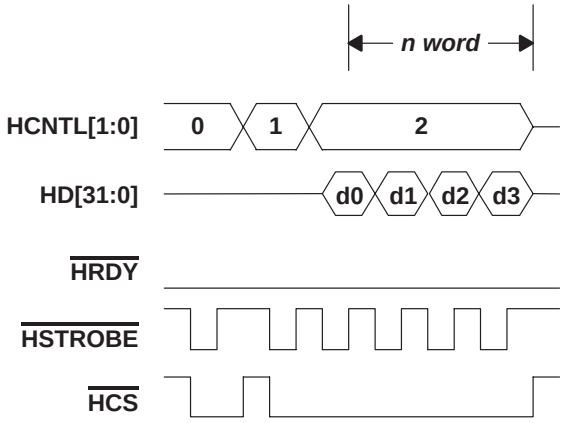

Figure 7. Number of CPU Cycles to Auto-Increment Write *n* Words Timing Diagram

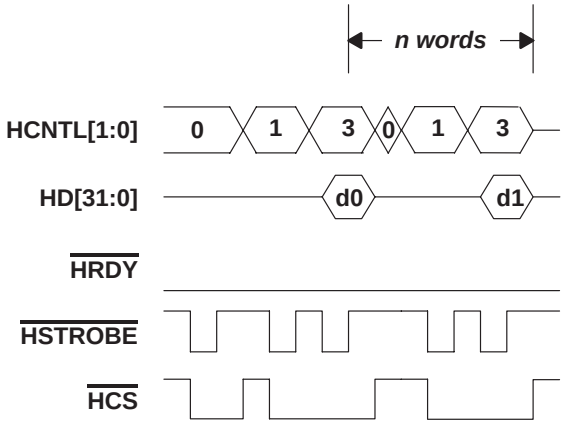

Figure 8. Number of CPU Cycles to Fixed Write *n* Words Timing Diagram

6 Total Throughput

The total throughput is defined as the amount of data transferred per unit time. Total HPI throughput is measured from the start of the transaction until the last data item has been transferred. The equation for calculating total throughput is:

$$TotalThroughput = \frac{(\#words)(4)}{(cpuclk)(latency + xfer)} \text{ [bytes/s]}$$

Where:

#words is the number of words of data transferred

cpuclk is the CPU clock period

latency is the number of cycles between when the master starts the transaction to when the target is ready to transfer the first data item

xfer is the number of cycles required to transfer *n* words of data

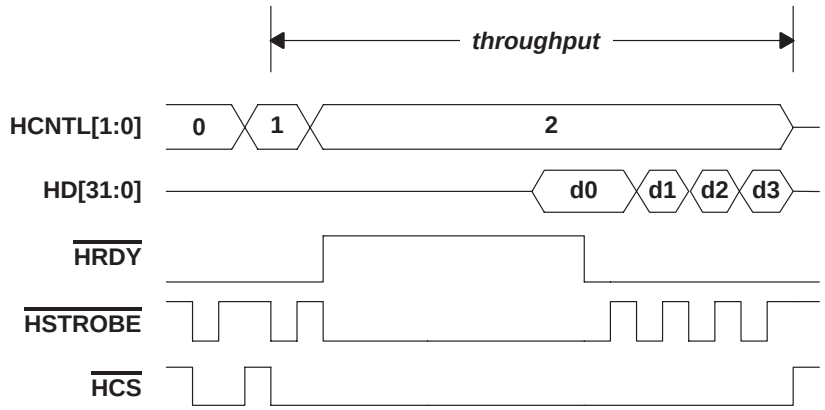

Figure 9. Auto-Increment Read Throughput Timing Diagram

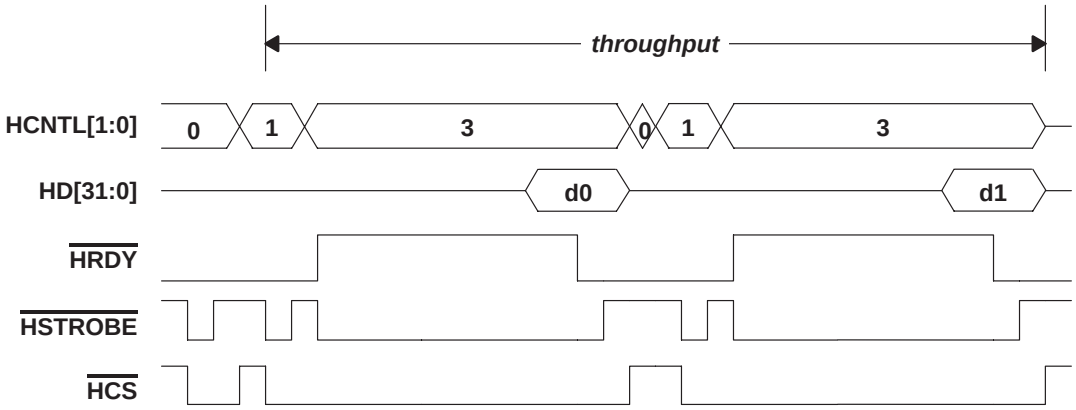

Figure 10. Fixed-Read Throughput Timing Diagram

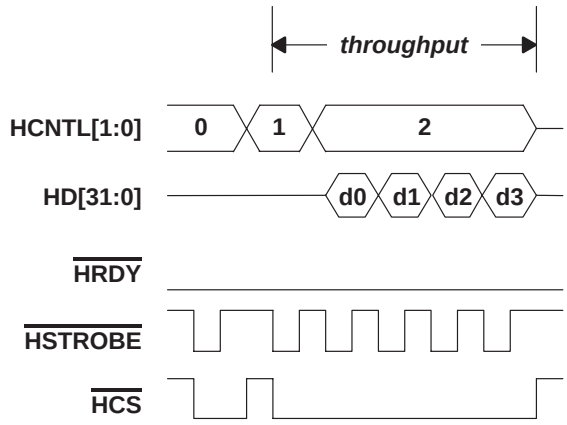

Figure 11. Auto-Increment Write Throughput Timing Diagram

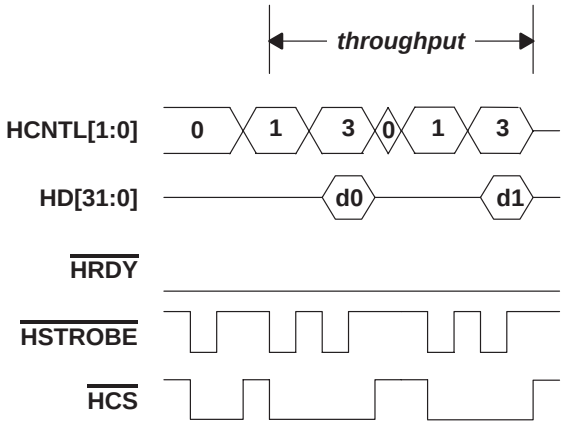

Figure 12. Fixed-Write Throughput Timing Diagram

7 Measurement Results

Table 1. HPI Benchmarks

CPU	Transfer Type	SRC/DST	HPI	HPI Width	Burst Length	EMIF	Latency	Xfer	Throughput (MB/s)
500	Auto-increment Write	L2 256k	45	32	8		17	83	160.0
					512		17	6136	166.4
				16	8		28	172	80.0
					512		28	22885	44.7
			25	32	8		30	150	88.9
					512		30	10226	99.8
				16	8		50	310	44.4
					512		50	20467	49.9
		EMIFA (SDRAM)	45	32	8	133	17	83	160.0
						100	17	83	160.0
					512	133	17	6635	154.0
						100	17	6634	154.0
				16	8	133	28	172	80.0
						100	28	172	80.0
					512	133	28	11439	89.3
						100	28	11369	89.8
			25	32	8	133	30	150	88.9
						100	30	150	88.9
					512	133	30	10227	99.8
						100	30	10226	99.8
				16	8	133	50	310	44.4
						100	50	310	44.4
					512	133	50	20466	49.9
						100	50	20466	49.9

NOTES: 1. Latency is measured in number of CPU cycles.
2. Xfer stands for the number of CPU cycles required to transfer n words of data.
3. HPI represents the HPI's STROBE_frequency in MHz.

Table 1. HPI Benchmarks (Continued)

CPU	Transfer Type	SRC/DST	HPI	HPI Width	Burst Length	EMIF	Latency	Xfer	Throughput (MB/s)
500	Auto-increment Read	L2 256k	45	32	8		101	83	87.0
					512		101	6032	167.0
				16	8		112	172	56.4
					512		112	5865	171.3
			25	32	8		113	150	60.8
					512		113	10185	99.4
				16	8		133	310	36.1
					512		133	20425	49.8
		EMIFA (SDRAM)	45	32	8	133	139	83	71.8
						100	157	83	66.6
					512	133	139	6899	145.5
						100	158	7437	134.8
				16	8	133	146	172	50.2
						100	168	172	47.0
					512	133	146	11522	87.8
						100	168	11512	87.7
			25	32	8	133	157	150	52.1
						100	171	150	49.8
					512	133	156	10184	99.0
						100	171	10198	98.8
				16	8	133	177	310	32.9
						100	191	310	31.9
					512	133	177	20424	49.7
						100	191	20425	49.7

NOTES: 1. Latency is measured in number of CPU cycles.
2. Xfer stands for the number of CPU cycles required to transfer n words of data.
3. HPI represents the HPI's STROBE_frequency in MHz.

Table 1. HPI Benchmarks (Continued)

CPU	Transfer Type	SRC/DST	HPI	HPI Width	Burst Length	EMIF	Latency	Xfer	Throughput (MB/s)
500	Fixed-Write	L2 256k	45	32	8		17	219	67.8
				16	8		28	386	38.7
			25	32	8		30	395	37.6
				16	8		50	695	21.5
		EMIFA (SDRAM)	45	32	8	133	17	219	67.8
						100	17	219	67.8
				16	8	133	28	386	38.7
						100	28	386	38.7
			25	32	8	133	30	395	37.6
						100	30	395	37.6
				16	8	133	50	695	21.5
						100	50	695	21.5
	Fixed-Read	L2 256k	45	32	8		103	807	17.6
				16			112	977	14.7
			25	32			113	977	14.7
				16			133	1277	11.3
		EMIFA (SDRAM)	45	32	8	133	114	901	15.8
						100	123	965	14.7
				16		133	124	1077	13.3
						100	137	1135	12.6
			25	32		133	127	1088	13.2
						100	138	1150	12.4
				16		133	150	1382	10.4
						100	157	1450	10.0

NOTES: 1. Latency is measured in number of CPU cycles.
2. Xfer stands for the number of CPU cycles required to transfer n words of data.
3. HPI represents the HPI's STROBE_frequency in MHz.

Table 1. HPI Benchmarks (Continued)

CPU	Transfer Type	SRC/DST	HPI	HPI Width	Burst Length	EMIF	Latency	Xfer	Throughput (MB/s)
600	Auto-increment Write	L2 256k	45	32	8		20	100	160.0
					512		20	6971	175.8
				16	8		33	207	80.0
					512		33	27351	44.9
			25	32	8		36	180	88.9
		L2 256k	25	32	512		36	12272	99.8
				16	8		60	372	44.4
					512		60	24560	49.9
		EMIFA (SDRAM)	45	32	8	133	20	100	160.0
						100	20	100	160.0
					512	133	20	7132	171.8
						100	20	7131	171.8
				16	8	133	33	207	80.0
						100	33	207	80.0
					512	133	33	13672	89.7
						100	33	13643	89.8
			25	32	8	133	36	180	88.9
						100	36	180	88.9
					512	133	36	12272	99.8
						100	36	12272	99.8
				16	8	133	60	372	44.4
						100	60	372	44.4
					512	133	60	24560	49.9
						100	60	24560	49.9

NOTES: 1. Latency is measured in number of CPU cycles.
2. Xfer stands for the number of CPU cycles required to transfer n words of data.
3. HPI represents the HPI's STROBE_frequency in MHz.

Table 1. HPI Benchmarks (Continued)

CPU	Transfer Type	SRC/DST	HPI	HPI Width	Burst Length	EMIF	Latency	Xfer	Throughput (MB/s)
600	Auto-increment Read	L2 256k	45	32	8		104	100	94.3
					512		104	6984	173.4
				16	8		117	207	59.3
					512		117	6951	173.9
			25	32	8		119	180	64.3
					512		119	12209	99.7
				16	8		143	372	37.3
					512		143	24496	49.9
		EMIFA (SDRAM)	45	32	8	133	151	100	76.6
						100	171	100	70.9
					512	133	151	7496	160.7
						100	172	8143	147.8
				16	8	133	160	207	52.4
						100	186	207	48.9
					512	133	160	13740	88.4
						100	185	13728	88.3
			25	32	8	133	167	180	55.3
						100	193	180	51.5
					512	133	165	12207	99.3
						100	193	12223	99.0
				16	8	133	190	372	34.2
						100	215	372	32.7
					512	133	190	24495	49.8
						100	215	24496	49.7

NOTES: 1. Latency is measured in number of CPU cycles.
2. Xfer stands for the number of CPU cycles required to transfer n words of data.
3. HPI represents the HPI's STROBE_frequency in MHz.

Table 1. HPI Benchmarks (Continued)

CPU	Transfer Type	SRC/DST	HPI	HPI Width	Burst Length	EMIF	Latency	Xfer	Throughput (MB/s)
600	Fixed-Write	L2 256k	45	32	8		20	263	67.8
				16			33	463	38.7
			25	32	8		36	474	37.6
				16			60	834	21.5
		EMIFA (SDRAM)	45	32	8	133	20	263	67.8
						100	20	263	67.8
				16	8	133	33	463	38.7
						100	33	463	38.7
			25	32	8	133	36	474	37.6
						100	36	474	37.6
				16	8	133	60	834	21.5
						100	60	834	21.5
	Fixed-Read	L2 256k	45	32	8		106	850	20.1
				16			117	1051	16.4
			25	32	8		119	1054	16.4
				16			143	1413	12.3
		EMIFA (SDRAM)	45	32	8	133	123	974	17.5
						100	133	1059	16.1
				16	8	133	134	1179	14.6
						100	149	1263	13.6
			25	32	8	133	136	1191	14.5
						100	153	1298	13.2
				16	8	133	163	1553	11.2
						100	178	1657	10.5

NOTES: 1. Latency is measured in number of CPU cycles.
2. Xfer stands for the number of CPU cycles required to transfer n words of data.
3. HPI represents the HPI's STROBE_frequency in MHz.

Table 1. HPI Benchmarks (Continued)

CPU	Transfer Type	SRC/DST	HPI	HPI Width	Burst Length	EMIF	Latency	Xfer	Throughput (MB/s)
720	Auto-increment Write	L2 256k	45	32	8		24	120	160.0
					512		24	8186	179.6
				16	8		40	248	80.0
					512		40	32763	45.0
			25	32	8		43	216	88.9
					512		43	14726	99.8
				16	8		72	446	44.4
					512		72	29472	49.9
		EMIFA (SDRAM)	45	32	8	133	24	120	160.0
					512		24	8191	179.5
				16	8	133	40	248	80.0
					512		40	16384	89.8
			25	32	8	133	43	216	88.9
						100	43	216	88.9
					512	133	43	14726	99.8
						100	43	14726	99.8
				16	8	133	72	446	44.4
						100	72	446	44.4
					512	133	72	29472	49.9
						100	72	29472	49.9

NOTES: 1. Latency is measured in number of CPU cycles.
2. Xfer stands for the number of CPU cycles required to transfer n words of data.
3. HPI represents the HPI's STROBE_frequency in MHz.

Table 1. HPI Benchmarks (Continued)

CPU	Transfer Type	SRC/DST	HPI	HPI Width	Burst Length	EMIF	Latency	Xfer	Throughput (MB/s)
720	Auto-increment Read	L2 256k	45	32	8		108	120	101.3
					512		107	8213	177.2
				16	8		124	248	62.0
					512		123	8246	176.2
			25	32	8		125	216	67.5
					512		125	14650	99.8
				16	8		155	446	38.3
					512		155	29396	49.9
		EMIFA (SDRAM)	45	32	8	133	169	120	79.7
					512		169	8677	166.7
				16	8	133	182	248	53.6
					512		182	16467	88.6
			25	32	8	133	174	216	59.1
						100	222	216	52.6
					512	133	172	14648	99.5
						100	222	14667	99.0
				16	8	133	201	446	35.6
						100	244	446	33.4
					512	133	201	29394	49.8
						100	244	29395	49.8

NOTES: 1. Latency is measured in number of CPU cycles.
2. Xfer stands for the number of CPU cycles required to transfer n words of data.
3. HPI represents the HPI's STROBE_frequency in MHz.

Table 1. HPI Benchmarks (Continued)

CPU	Transfer Type	SRC/DST	HPI	HPI Width	Burst Length	EMIF	Latency	Xfer	Throughput (MB/s)
720	Fixed-Write	L2 256k	45	32	8		24	316	67.8
				16			40	556	38.7
			25	32	8		43	569	37.6
				16			72	1001	21.5
		EMIFA (SDRAM)	45	32	8	133	24	316	67.8
				16			40	556	38.7
			25	32	8	133	43	569	37.6
						100	43	569	37.6
				16	8	133	72	1001	21.5
						100	72	1001	21.5
	Fixed-Read	L2 256k	45	32	8		109	901	22.8
				16			123	1141	18.2
			25	32	8		126	1146	18.1
				16			154	1576	13.3
		EMIFA (SDRAM)	45	32	8	133	133	1007	20.2
				16			150	1256	16.4
			25	32	8	133	149	1315	15.7
						100	171	1476	14.0
				16	8	133	177	1758	11.9
						100	210	1905	10.9

NOTES: 1. Latency is measured in number of CPU cycles.
2. Xfer stands for the number of CPU cycles required to transfer n words of data.
3. HPI represents the HPI's STROBE_frequency in MHz.

8 References

1. *TMS320C6000 Peripherals Reference Guide* (SPRU190)
2. Shanley, Tom and Don Anderson. *PCI System Architecture, 4th Edition.* Mindshare Inc. 1999.
3. *TMS320C6201/6701 DSP Host Port Interface (HPI) Performance* (SPRA449)

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