Application Note

ADC Input Circuit Evaluation for C2000 Real-Time MCUs (using PSPICE-FOR-TI)

TEXAS INSTRUMENTS

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ABSTRACT

The analog-to-digital converter (ADC) is a key module used to sense feedback and monitoring signals in a real-time control application. However, without careful design and evaluation of the circuits driving the ADC input, significant sample-and-hold circuit (S+H) settling errors can occur, resulting in poor performance of the ADC sensing and thus the system. This application report will identify the resources that can be used to understand ADC input settling and design appropriate ADC driving circuits as well as how to evaluate these resources in the specific context of TMS320F2837xD, TMS320F2837xS, TMS320F2838xD, TMS320F2838xS, TMS320F2807x, TMS320F28004x, TMS320F28002x, TMS320F28003x, TMS320F280013x, and the TMS320F280015x series microcontrollers.

Project collateral and source code discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/spracy9. This application report uses the PSpice for TI design and simulation tool. ADC Input Circuit Evaluation for C2000 MCUs (TINA-TI) covers the same content but uses the TINA-TI SPICE-based analog simulation program instead.

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1 Introduction

When designing a system utilizing C2000 real-time MCUs, evaluating the input circuits that are driving the ADC for proper settling is a necessary step. Inadequate settling can lead to a variety of sampling issues, most commonly signal distortion and memory cross-talk. This application report explores the methodology presented in the eight-part video series on ADC input settling by TI Precision Labs: TI Precision Labs - SAR ADC Input Driver Design in the specific context of the ADCs on C2000 real-time MCUs.

1.1 Mechanism of ADC Input Settling

To convert a sensed analog voltage to a digital conversion result, the ADC first must accurately capture the applied input voltage into its sample-and-hold circuit (S+H). As shown in Figure 1-1, this entails charging the internal ADC S+H capacitor (C_h) to within some acceptable tolerance (typically 0.5 LSBs) of the applied voltage within the configured acquisition window time (also referred to as the S+H time).
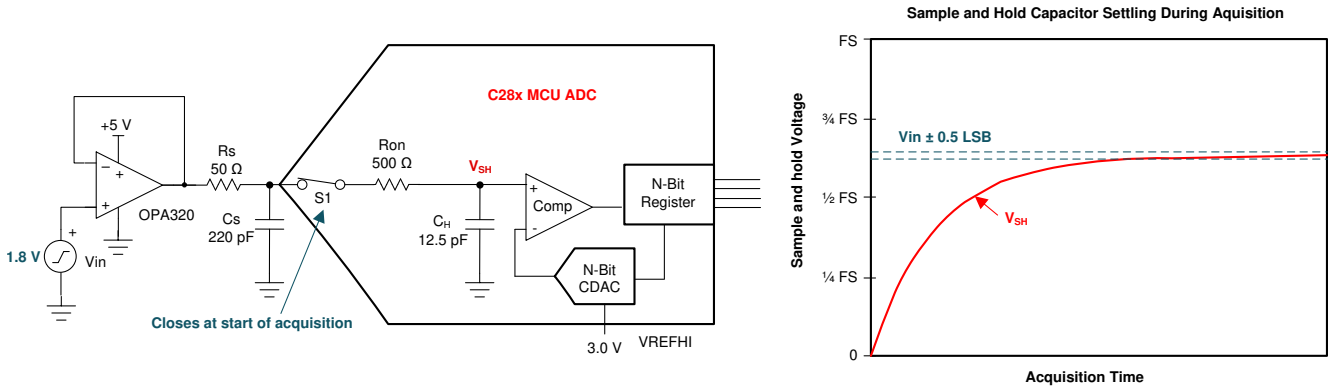
Figure 1-1. Settling of the ADC S+H Capacitor

Quickly charging C_h to the applied voltage is complicated by the finite bandwidth and settling time of the external ADC driver circuit and by the settling time of the internal ADC S+H circuit. In Figure 1-1, the driver is shown as an op-amp (OPA320), which has a finite bandwidth, and the driver circuit also has intentionally placed source resistance (R_s) and intentionally placed source capacitance (Cs) which have a finite settling time determined by their RC time constant. Note that other circuit topologies are possible for driving the ADC, and these circuits may have additional components that need to be modeled to ensure appropriate settling time. These components could include unintentional parasitics such as the output impedance of a sensor or the effective source resistance of a voltage divider. Figure 1-1 also shows that the ADC has an internal parasitic switch resistance (R_{on}). This, along with C_h, provides an additional RC time constant that limits settling speed.

1.2 Symptoms of Inadequate Settling

Once a voltage has been captured into the S+H capacitor, the ADC translates this voltage into a digital conversion result during the conversion phase. The CPU can then use this result to control or monitor the system. However, if the captured voltage does not accurately represent the applied voltage due to settling error, the final conversion result causes errors even if the ADC conversion process is perfect.

These settling errors manifests differently depending on whether the ADC is sampling the same channel repeatedly or scanning through multiple channels in a sequence. The settling errors also manifest differently depending on the starting voltage on the S+H capacitor at the beginning of the acquisition phase. Some ADC architectural implementations have a starting S+H voltage close to the previously sampled voltage while other architectures usually start the acquisition phase with a discharged S+H capacitor.

1.2.1 Distortion

In the case where the ADC is repeatedly sampling the same signal, settling error typically manifests as distortion of the input signal. In architectures where the S+H voltage starts near the previously sampled voltage, slow moving portions of the input signal settles better than fast moving portions. An architecture where sequential samples begin their settling from the voltage sampled and held in the previous conversion is illustrated in Figure 1-2.
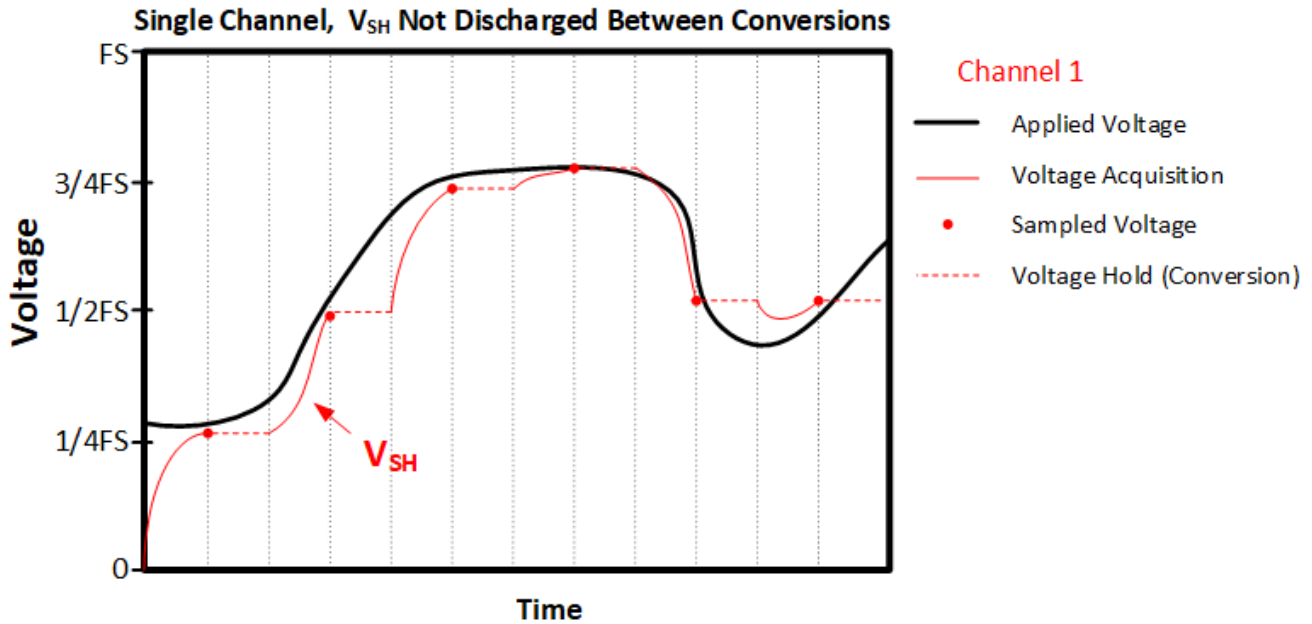
Figure 1-2. Sequence of Samples With C_H Retained Between Conversions

In architectures where the S+H capacitor starts each acquisition phase discharged, higher input voltages have worse settling, resulting in distorted scaling of the signal. An architecture where sequential samples always begin their settling from near zero-scale is illustrated in Figure 1-3.
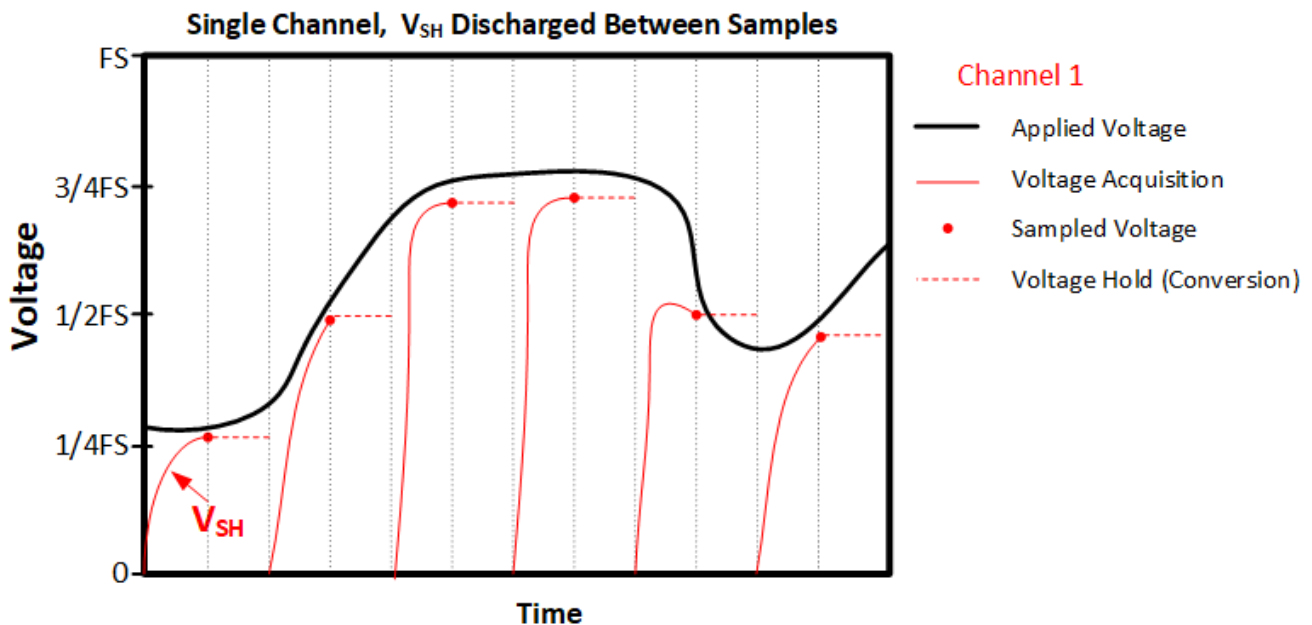
Figure 1-3. Sequence of Samples With C_H Discharged Between Conversions

1.2.2 Memory Cross-Talk

In many C2000 real-time MCU applications, a typical use case is using the ADC input multiplexer to scan through multiple channels in a sequence. If a converted channel has inadequate settling, the channel may be pulled towards the voltage of the previous conversion in the sequence. This occurs because the S+H voltage starts near the previously converted voltage and then settles towards (but does not reach) the applied voltage. This tendency for the previous conversion result in a sequence of conversions to affect the current conversion is called memory cross-talk. Memory cross-talk can generally be completely mitigated via appropriate settling design.

A situation where a shared sample and hold must settle back-and-forth between two different multiplexed input signals is illustrated in Figure 1-4.
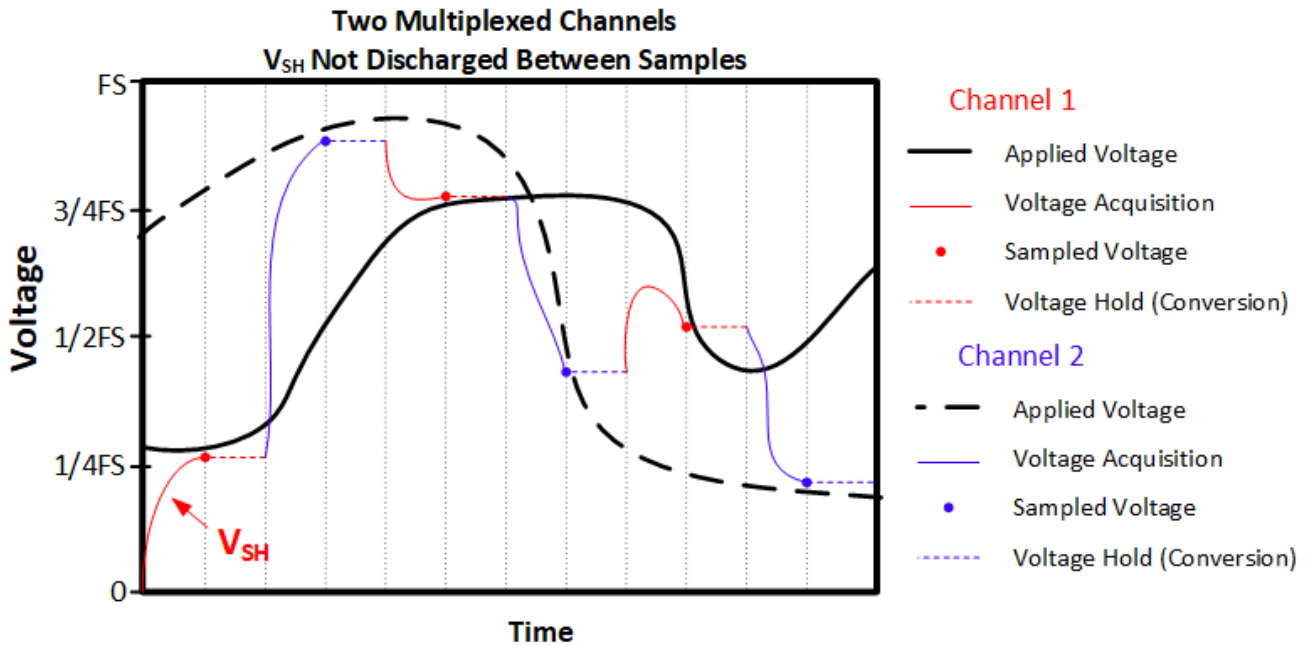
Figure 1-4. Sequence of Multiplexed Samples

Converter architectures that start with the S+H capacitor completely discharged generally do not experience significant memory cross-talk (but still experience input settling related distortion if the ADC driving circuits are not appropriate for the allocated acquisition time).

1.2.3 Accuracy

The errors introduced by inadequate input settling generally can not be calibrated out or reduced via oversampling and averaging. Therefore, applications that are concerned with absolute sampling accuracy also need to ensure proper ADC input settling even if the sensed input signal is low-frequency or even DC.

1.2.4 C2000 ADC Architecture

C2000 real-time MCU ADCs generally start with the S+H capacitor pre-charged to a voltage close to the previous conversion result. The exception to this is for ADCs that support differential signaling, but which are operating in single-ended mode. In this case, the S+H capacitor starts the discharge when the previous conversion was from an even numbered channel and the current channel is an odd numbered channel, or vice-versa. For example, the S+H capacitor starts the discharge if channel A4 is being sampled after A3 (or vice-versa), but start close to the previously converted voltage when sampling channel A4 after channel A2 or channel A1 after channel A3.

1.3 Resources

The following tools and materials are useful for ADC driver circuit design and evaluation for input settling.

1.3.1 TINA-TI SPICE-Based Analog Simulation Program

TI provides the TINA-TI application to TI customers to allow easy SPICE-based simulation of circuits utilizing TI products. Because this application report uses PSpice for TI instead of TINA-TI to evaluate circuit settling performance, it is not necessary to ensure TINA-TI is downloaded and installed before proceeding. However, the TINA-TI application and additional resources are still made available.

Link to Tool Folder: TINA-TI™

1.3.2 PSPICE for TI Design and Simulation Tool

TI provides the PSpice for TI application to TI customers to allow easy SPICE-based simulation of circuits utilizing TI products. This application report utilizes this program to evaluate circuit settling performance. Ensure this application is downloaded and installed before proceeding.

Link to Tool Folder: PSPICE® for TI

Link to PSpice for TI Training Series: Explore PSpice for TI

Link to TI E2E Support Forum: Welcome to TI E2E Design Support Forums

Link to Cadence PSpice for TI Forum: Welcome to PSpice Forum

1.3.3 TI Precision Labs - SAR ADC Input Driver Design Series

TI Precision Labs has provided an excellent eight-part video series that demonstrates how to design the input drivers for a SAR ADC. Reviewing this material will help to further understand the high-speed op-amp based signal conditioning design process and options.

Link to Video Training Series: TI Precision Labs - SAR ADC Input Driver Design

1.3.4 Analog Engineer's Calculator

The analog engineer's calculator tool provides a variety of very useful GUI-based calculation tabs to assist with common analog circuit design tasks. The high-speed op-amp design methodology takes advantage of the Data Converters ➜ ADC SAR Drive calculator.

Link to Tool Folder: Analog Engineer's Calculator

1.3.5 Related Application Reports

TI provides several application reports that pertain to the design and evaluation of ADC input circuits on C2000 real-time MCU devices. These application reports are listed along with brief descriptions.

Application Report Title	Schematic Capture and Simulation Tool	Purpose
ADC Input Circuit Evaluation for C2000 MCUs (TINA-TI)	TINA-TI	Describes how to design and evaluate a traditional high-speed ADC driving circuit. Input circuit includes an op-amp. Appropriate when sampling a high bandwidth signal near the maximum sample rate of the ADC.
ADC Input Circuit Evaluation for C2000 MCUs (PSpice for TI)	PSpice for TI	
Charge-Sharing Driving Circuits for C2000 ADCs (TINA-TI)	TINA-TI	Describes how to design and evaluate a charge-sharing ADC driving circuit. Input circuit may or may not include an op-amp. Appropriate when sampling a signal with a sufficiently low bandwidth and sample rate.
Charge-Sharing Driving Circuits for C2000 ADCs (PSpice for TI)	PSpice for TI	
Methods for Mitigating ADC Memory Cross-Talk	TINA-TI	Describes strategies to mitigate memory cross-talk error when the input circuit design does not achieve adequate settling. Applicable under special circumstances.

1.3.6 PSpice for TI ADC Input Models

This application report is bundled with pre-generated ADC input models for several families of devices. The families of devices are listed alongside the ADC input models associated with each family and a brief description of each ADC input model.

For C2000 devices that are not listed in Table 1-1, the input models below can still be used as long as the signal mode matches (use a single-ended model for single-ended ADC operation or use a differential model for differential ADC operation). The R_{on} and C_h values also need to be updated to match the values specified in the device-specific data manual.

Table 1-1. Series of Devices

Series of Devices	ADC Input Model	Description
TMS320F2807x	F2807x_Ext	F2807x ADC input model External reference of 3.0 V 12-bit resolution Single-ended input mode
TMS320F2837xD, TMS320F2837xS	F2837x_Ext_12BSE	F2837x ADC input model External reference of 3.0 V 12-bit resolution Single-ended input mode
	F2837x_Ext_16BDE	F2837x ADC input model External reference of 3.0 V 16-bit resolution Differential input mode
TMS320F2838xD, TMS320F2838xS	F2838x_Ext_12BSE	F2838x ADC input model External reference of 3.0 V 12-bit resolution Single-ended input mode
	F2838x_Ext_16BSE	F2838x ADC input model External reference of 3.0 V 16-bit resolution Single-ended input mode
	F2838x_Ext_16BDE	F2838x ADC input model External reference of 3.0 V 16-bit resolution Differential input mode
TMS320F28002x	F28002x_Ext	F28002x ADC input model External reference of 3.0 V 12-bit resolution Single-ended input mode
	F28002x_Int25	F28002x ADC input model External reference of 2.5 V 12-bit resolution Single-ended input mode
	F28002x_Int33	F28002x ADC input model External reference of 3.3 V 12-bit resolution Single-ended input mode
TMS320F28004x	F28004x_Ext	F28004x ADC input model External reference of 3.0 V 12-bit resolution Single-ended input mode
	F28004x_Int25	F28004x ADC input model Internal reference of 2.5 V 12-bit resolution Single-ended input mode
	F28004x_Int33	F28004x ADC input model Internal reference of 3.3 V 12-bit resolution Single-ended input mode

Table 1-1. Series of Devices (continued)

Series of Devices	ADC Input Model	Description
TMS320F28003x	F28003x_Ext	F28003x ADC input model External reference of 3.0 V 12-bit resolution Single-ended input mode
	F28003x_Int25	F28003x ADC input model Internal reference of 2.5 V 12-bit resolution Single-ended input mode
	F28003x_Int33	F28003x ADC input model Internal reference of 3.3 V 12-bit resolution Single-ended input mode
TMS320F280013x	F280013x_Ext	F280013x ADC input model External reference of 3.0 V 12-bit resolution Single-ended input mode
	F280013x_Int25	F280013x ADC input model Internal reference of 2.5 V 12-bit resolution Single-ended input mode
	F280013x_Int33	F280013x ADC input model Internal reference of 3.3 V 12-bit resolution Single-ended input mode
TMS320F280015x	F280015x_Ext	F280015x ADC input model External reference of 3.0 V 12-bit resolution Single-ended input mode
	F280015x_Int25	F280015x ADC input model Internal reference of 2.5 V 12-bit resolution Single-ended input mode
	F280015x_Int33	F280015x ADC input model Internal reference of 3.3 V 12-bit resolution Single-ended input mode

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CAUTION

While the ADC input models for multiple C2000 devices are bundled with this application report, input model component values should always first be verified with the device-specific data manual before proceeding. For more information, see Section 2.5.

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2 Input Settling Design Steps

The TI Precision Labs - SAR ADC Input Driver Design methodology to design an ideal ADC input driver can be broken into the steps shown below. Subsequent sections discuss how these steps can be applied to C2000 ADCs.

1. Select the ADC.
2. Find the minimum op-amp bandwidth and RC filter ranges.
3. Select an op-amp.
4. Verify the op-amp model.
5. Build the ADC input model.
6. Refine RC filter values via simulation.
7. Perform final simulations.

2.1 Select the ADC

It is assumed that you have already selected a C28x based microcontroller with one or more integrated ADC modules. The C28x product search can be used to select an MCU: C2000 real-time control MCU - Products and the C2000 peripheral guide enumerates the differences between peripherals on different devices (including the ADC): C2000 Real-Time Control MCU Peripherals Reference Guide.

Once a C2000 device has been selected, you should locate the following information in the device-specific data manual before proceeding.

Data Manual Information	Location	Comments
Minimum sample window duration	"ADC Operating Conditions" table in the "ADC Electrical Data and Timing" section	Some devices support multiple resolution modes and signaling modes; ensure that the parameter corresponds to the mode you intend to use.
ADC input model	"Input Model Parameters" table in the "ADC Input Model" section	Some devices support multiple resolution modes and signaling modes; ensure that the model corresponds to the mode you intend to use.
Specific parasitic capacitance for selected ADC pin	"Per-Channel Parasitic Capacitance" table in the "ADC Input Model" section	If channel assignment is not yet known, use the value for ADCIN15.
ADC timings	"ADC Timings" table in the "ADC Timing Diagrams" section	Some devices support multiple resolution modes and signaling modes; ensure that the timings correspond to the mode you intend to use. You will also need to know your intended CPU clock (SYSCLK) and ADC clock (ADCCLK) rate. If not yet known, use the maximum ADCCLK value given in the "ADC Operating Conditions" table along with the maximum SYSCLK for the device.

2.2 Find the Minimum Op-Amp Bandwidth and RC Filter Ranges

Once you have located the detailed ADC information in the device-specific data manual, you can use the Analog Engineer's Calculator to determine the minimum required driving op-amp bandwidth as well as the potential ranges of the external source resistor and external source capacitor to put on the ADC input.

Open the Analog Engineer's Calculator application and select the calculator Data Converters ➔ ADC SAR Drive calculator. This will give a calculator window similar to that shown in Figure 2-1.
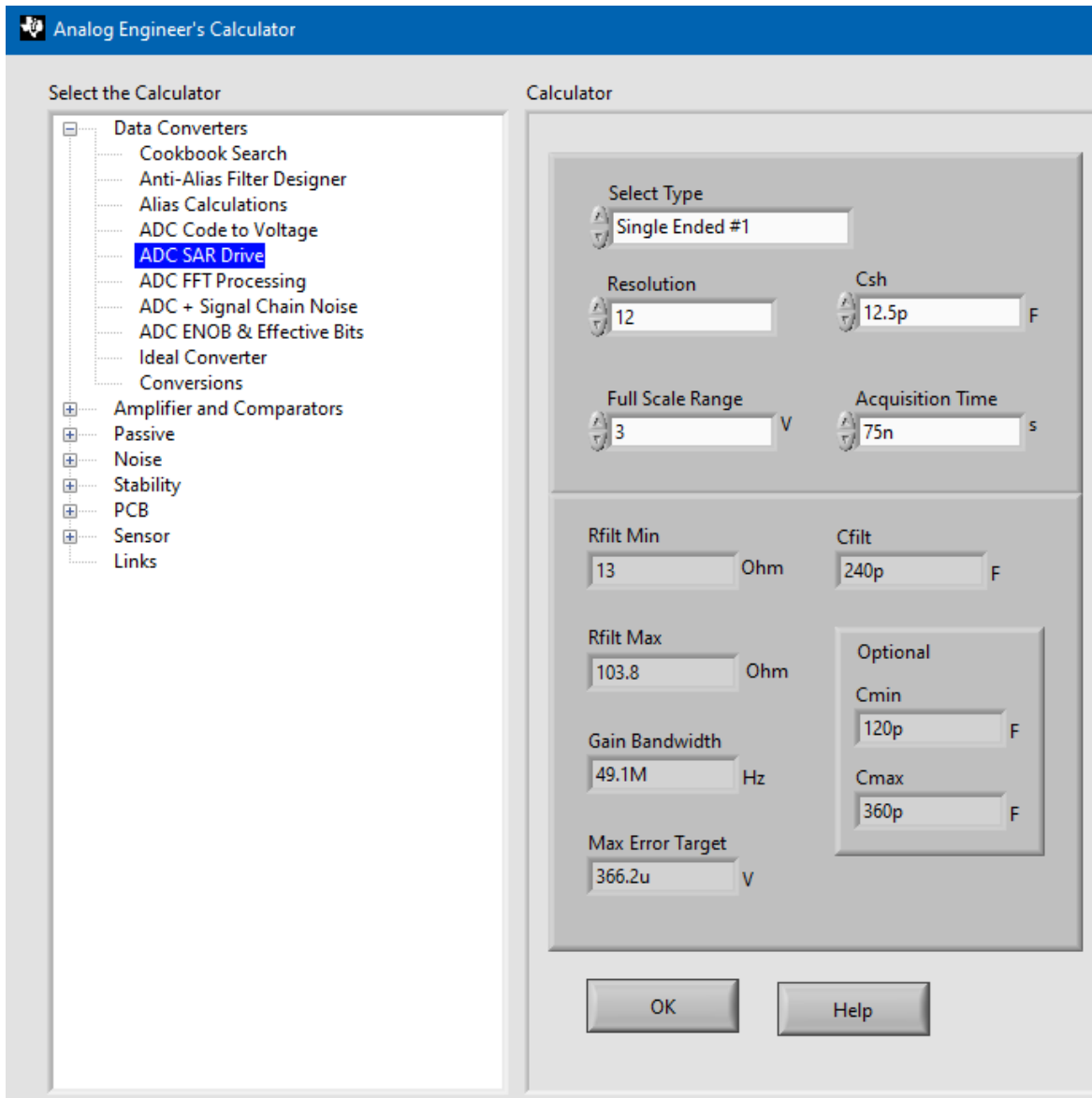
Figure 2-1. Screenshot of Analog Engineer's Calculator

Once the correct calculator is open, enter the input information.

2.2.1 Select Type

C2000 ADCs can be configured as either single-ended input mode or differential input mode depending on the particular device. The calculator allows several input mode types. Table 2-1 maps the C2000 input modes to calculator selection types.

Table 2-1. Calculator Input Type Map

C2000 Signal Mode	Calculator Input Type Selection
Single-ended	"Single Ended #1"
Differential	"Differential"

2.2.2 Resolution

Enter the resolution of the ADC mode to be used in bits. For C2000 ADCs, this is usually 12-bits or 16-bits.

Usually the actual resolution of the ADC will be selected. However, in cases where an ADC channel does not need to utilize the full resolution of the ADC, a lower value can be entered to relax the input settling design requirements.

For example:

Resolution = 12 bits, C_{sh} = 12.5 pF, Full-scale range = 3.0 V, Acquisition duration = 100 ns
- Full resolution of 12 bits requires minimum op-amp bandwidth of 37 MHz and settling to better than 0.366 mV
- Reduced resolution of 10 bits (approximately 0.1% settling) requires a minimum op-amp bandwidth of 28 MHz and settling to better than 1.465 mV

2.2.3 C_{sh}

Enter the value of the ADC S+H capacitor. This can be found as the parameter "C_h" in the *Input Model Parameters* table in the device-specific data manual. Different resolutions and reference modes may have different input model parameters, so ensure that the parameter is selected that corresponds to the intended ADC use mode.

2.2.4 Full-Scale Range

Enter the voltage corresponding to the full-scale range of the ADC. When using external reference mode, this corresponds to the voltage supplied on the VREFHI pin of the ADC, usually 2.5 V or 3.0 V. When using internal reference mode (on supported devices), this corresponds to the voltage range of the selected reference mode (2.5 V or 3.3 V).

2.2.5 Acquisition Time

Enter the target ADC acquisition window time. For the lowest ADC conversion latency (corresponding to the maximum ADC sample rate), select the minimum value of the parameter "Sample window duration" in the *ADC Operating Conditions* table in the device-specific data manual.

Selecting a target S+H time larger than the ADC minimum acquisition time can ease the input settling design requirements for the input driving op-amp.

For example:

Resolution = 12 bits, C_{sh} = 12.5 pF, Full-scale range = 3.0 V
- Acquisition time = 75 ns requires a driving op-amp with around 50 MHz of bandwidth
- Acquisition time = 150 ns requires a driving op-amp with around 25 MHz of bandwidth
- Acquisition time = 750 ns requires a driving op-amp with around 5 MHz of bandwidth

These decisions can be made on a per-channel basis since the C2000 ADC wrapper allows per-SoC configuration of the S+H time (by using the ACQPS setting in the SoC control register).

2.2.6 Outputs

Once all inputs have been provided to the calculator, record the outputs for later analysis

- R_{filt} and C_{filt} output ranges will be explored via PSpice for TI simulation in order to determine an optimal driver circuit
- The max error target output corresponds to 1/2 LSBs at the specified resolution. The final PSpice for TI simulation will be considered successful if the settling is within this bound.
- The gain bandwidth output will be used in the next step to select an appropriate op-amp. The selected op-amp should have a unity-gain bandwidth of this value or better for best settling performance.

2.2.7 Math Behind the Calculator

Additional information about analytically determining the required op-amp bandwidth and ranges of R_{filt} and C_{filt} can be found in the final TI Precision Labs video in the SAR ADC Input Driver Design series: Math Behind the R-C Component Selection.

2.3 Select an Op-Amp

An appropriate op-amp next needs to be selected for the ADC driver circuit. This op-amp needs to meet the minimum unity gain bandwidth reported by the Analog Engineer's calculator.

Additional instructions for selecting the op-amp are given in the TI Precision Labs video: Selecting and Verifying the Driver Amplifier.

> If selecting an op-amp to meet the specified requirements is proving difficult, remember that both the settling resolution and the target acquisition time can be relaxed (if the application requirements allow) to relax the driving op-amp requirements. These can both be adjusted on a per-channel basis to allow critical ADC inputs to have optimal performance while auxiliary ADC inputs can be allowed to have relaxed performance.

2.4 Verify the Op-Amp Model

Next, it is necessary to obtain the PSpice for TI model for the op-amp selected in the previous step.

The PSpice for TI model for the selected op-amp can be obtained using the PSpice Part Search tool. To launch the PSpice Part Search tool, go to Place ➜ PSpice Component... ➜ Search... using the menu in the upper left of the PSpice for TI schematic capture window. Alternatively, click the Launch PSpice Part Search button in the upper right of the PSpice for TI schematic capture window. The icon for this button looks like an integrated circuit with a magnifying glass. Enter the part name of the selected op-amp in the search bar of the PSpice Part Search tool to find the PSpice for TI model.

The TI Precision Labs video Selecting and Verifying the Driver Amplifier provides detailed instructions on how to verify the model against the information provided in the device-specific data manual. Specifically, the model must be verified against the "Open-Loop Gain and Phase vs Frequency" plot provided in the device-specific data manual as well as one or both of the "Open-Loop Output Impedance vs Frequency" and "Closed-Loop Output Impedance vs Frequency" plots provided in the device-specific data manual. To generate these plots, an AC simulation must be performed.

Note that performing an AC simulation in PSpice for TI requires the creation of an AC Sweep / Noise simulation profile. When performing an AC simulation in PSpice for TI, ensure that all AC sources have an AC magnitude of 1. The magnitude in decibels of an output variable can be measured using a dB Magnitude marker. Similarly, the phase in degrees of an output variable can be measured using a Phase marker. To place these markers, go to PSpice ➜ Markers ➜ Advanced using the menu in the upper left of the PSpice for TI schematic capture window. Measuring the magnitude in decibels and the phase in degrees of a trace expression more complex than a single output variable is only possible from the PSpice for TI simulation window. In the PSpice for TI simulation window, the magnitude in decibels of a trace expression can be measured using the DB() function, and the phase in degrees of a trace expression can be measured using the P() function.

2.5 Build the ADC Input Model

To simulate and refine the ADC input driver circuit in PSpice for TI, it is first necessary to build a PSpice for TI input model for the ADC. The TI Precision Labs video Building the SAR ADC Input Model outlines how to perform this process based on the information provided in the device-specific data manual for an ADC device. This application report is bundled with pre-generated ADC input models for TMS320F2837xD, TMS320F2837xS, TMS320F2838xD, TMS320F2838xS, TMS320F2807x, TMS320F28004x, and TMS320F28002x family devices, so manual creation of these models is not necessary.

The same TI Precision Labs video also outlines how to configure your TINA-TI simulation parameters to optimize your simulation results. However, this application report instead outlines how to configure your PSpice for TI simulation parameters to optimize your simulation results. To increase the numeric precision of bias point simulation results, go to PSpice ➔ Bias Points ➔ Preferences... and increase the Displayed Precision parameter. To optimize transient simulation results, open the transient simulation profile and decrease the maximum step size. To increase the numeric precision of simulation results in the PSpice for TI simulation window, go to Tools ➔ Options... ➔ Cursor Settings and increase the number of cursor digits.

This application report requires precision on the level of microvolts. For this reason, ensure that the Displayed Precision parameter and number of cursor digits are greater than or equal to 7. The maximum step size is configured on a simulation-by-simulation basis, but a maximum step size that is three to four orders of magnitude smaller than the simulation stop time is generally sufficient.

> **CAUTION**
>
> For additional guidance on how to further optimize your simulation results, please review the technical article Getting started in PSpice for TI, part 1: Optimize your simulation profile in 6 steps.
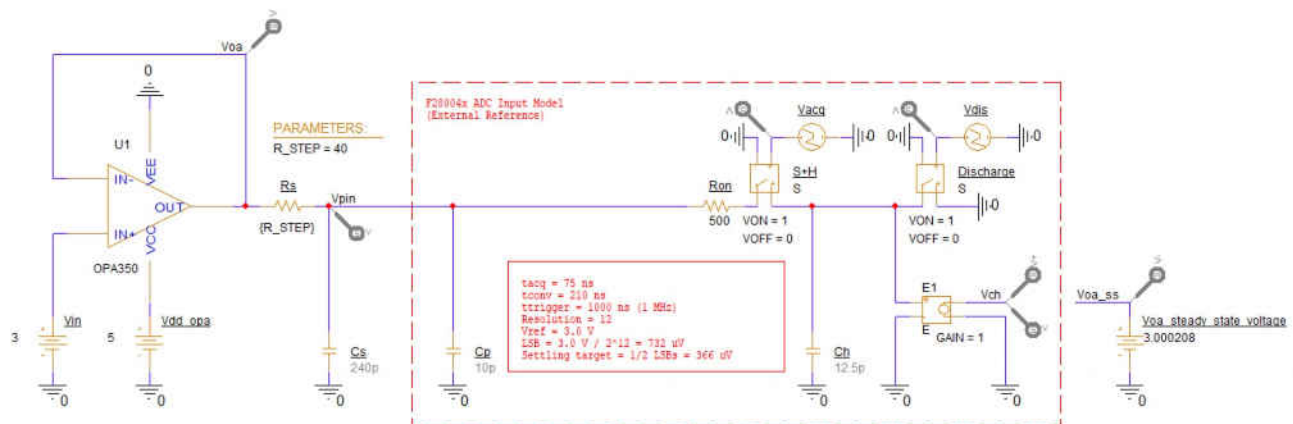

Figure 2-2. F28004x ADC Input Model

An example of one of the provided ADC input models can be seen in Figure 2-2. The following sections briefly describe the primary functions of each model component.

2.5.1 V_{in}

V_{in} is the applied voltage that will be used to charge the S+H capacitor. While any input can be simulated, applying the full-scale input voltage providing the worst-case DC settling conditions because the S+H capacitor always starts discharged in this model.

2.5.2 V_{oa}, V_{oa_SS}, and V_{error}

PSpice for TI op-amp models incorporate various non-idealities, which results in the DC steady state output of the op-amp at V_{oa} not exactly matching V_{in}. The steady state output at V_{oa} can be simulated and entered into V_{oa_ss} such that V_{error} is an accurate representation of only the input settling error.

2.5.3 R_s, C_s, and V_{cont}

R_s and C_s are the source resistance and source capacitance. These values correspond to R_{filt} and C_{filt} in the TI Precision Labs training terminology. R_s resistance is determined by the global parameter R_STEP. Using a global parameter allows parameter sweeping when there are two R_s resistors in the differential models.

2.5.4 C_h, R_{on}, and C_p

Component values for the ADC input model.

C_h, the S+H capacitor, corresponds to C_{sh} in the TI Precision Labs training terminology while R_{on}, the S+H switch on resistance, corresponds to R_{sh}.

C_p is the pin-specific input capacitance. This can be optionally added to the simulation to improve simulation accuracy. Adding the pin-specific input capacitance is particularly helpful for pins that are multiplexed with VDAC (alternate DAC voltage reference pin) that have a value of C_p, which is greater than 100 pF on most devices.

Pins that are multiplexed with the buffered DAC output on F2837x and F2807x devices have a parasitic 50 kΩ pull-down resistor present on these pins. It is recommended to add this resistor to the model (not shown in Figure 2-2) to better represent behavior of these pins.

CAUTION

While the ADC input models for multiple C2000 devices are bundled with this application report, input model component values should always first be verified with the device-specific data manual before proceeding. Values for C_h and R_{on} can be obtained from the *Input Model Parameters* table in the device-specific data manual while values for C_p can be obtained from the *Per-Channel Parasitic Capacitance* table. In any cases where the device-specific data manual values disagree with the values in this document or in the provided models, the device-specific data manual values should always be considered the correct values.

2.5.5 S+H Switch, Discharge Switch, t_{acq}, and t_{dis}

Switch "S+H" controls when the S+H capacitor, C_h, is being charged by the driving circuit. The timings for this switch are controlled by t_{acq}. Sample t_{acq} timing configurations for a 75 ns acquisition window are shown in Figure 2-3.

Switch "Discharge" controls when the S+H capacitor, C_h, is being reset by being discharged to ground. The timings for this switch are controlled by t_{dis}. Sample t_{dis} timing configurations for a 1 µs trigger period are shown in Figure 2-4.

When neither t_{acq} or t_{dis} are active, the value of the S+H capacitor is held at its final settled value.

Note that the timings are configured to emulate conversions triggered at a set 1 MHz frequency instead of back-to-back continuous conversions. This more closely emulates the typical C2000 ADC use case of being periodically triggered by the ePWM module. The triggering rate can be modified to match the actual application ePWM trigger rate by modifying the period of the t_{acq} and t_{dis} timing sources. Do, however, ensure that the trigger rate is slower than the total acquisition time plus ADC conversion time. The ADC conversion time can be found in the device-specific data manual table "ADC Timings".
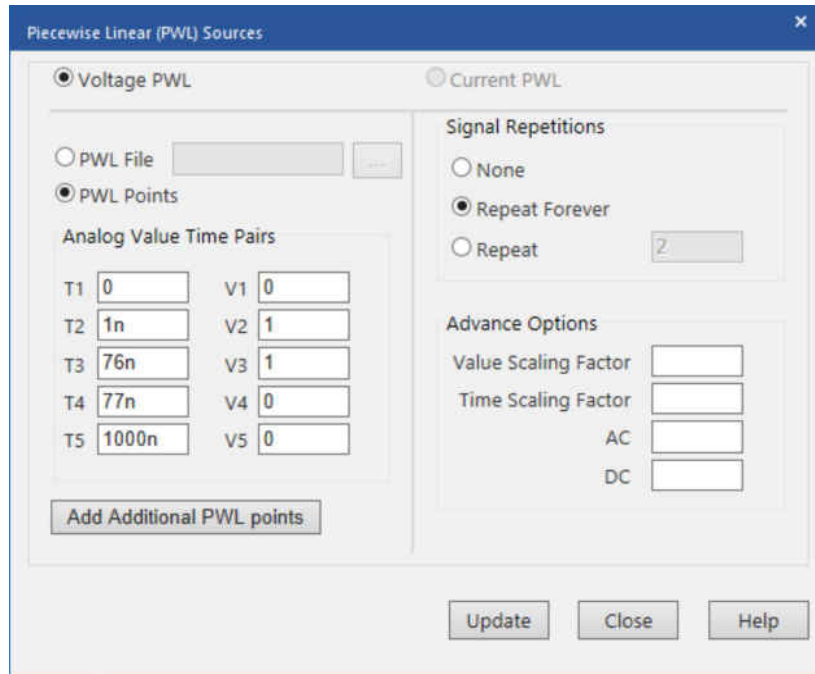

Figure 2-3. Example Timings for t_{acq} (Piecewise Linear)
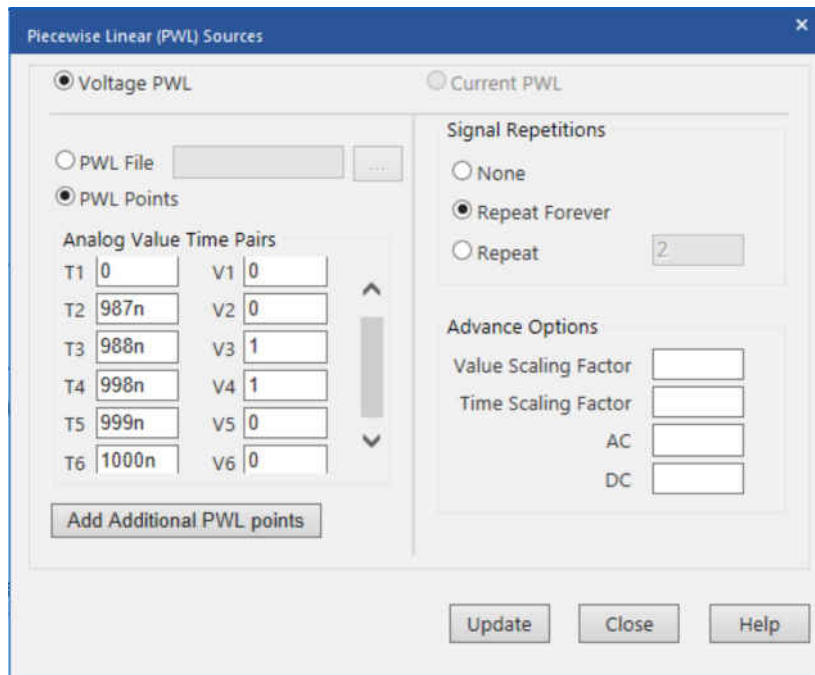

Figure 2-4. Example Timings for t_{dis} (Piecewise Linear)

2.6 Refine RC Filter Values Via Simulation

Once the ADC input model has been combined with the op-amp simulation model, simulation can be used to select the best values of R_s and C_s. In-depth instructions for performing the component refinement simulation can be found in the TI Precision Labs video Refine the Rfilt and Cfilt Values on ADC Drive. However, the input circuit design example in Section 3 follows alternative instructions that leverage the unique capabilities of PSpice for TI to select the best values of R_s and C_s.

Once optimal values of R_s and C_s have been determined, a final simulation should be performed using the closest available standard component values. This will establish the final settling error, which can be compared to the settling error target obtained from the Analog Engineer's Calculator.

If the settling error does not meet the target, additional iteration is required that entails evaluating a different op-amp, evaluating different R_s and C_s values, or relaxing the S+H time or settling resolution targets.

2.7 Perform Final Simulations

Additional simulations to verify the robustness of the design can also optionally be performed. These include:

- Simulate with a longer S+H duration to ensure that input is consistently settling
- Observe settling at the op-amp's output node. This node also settles to within 1/2 LSBs (or the selected settling target) at the end of the acquisition period
- Observe settling over multiple cycles
- Perform settling simulations with an AC input

Information on performing these simulations can be found in the TI Precision Labs video Final SAR ADC Drive Simulations. Note that while this video describes conceptually how to perform these simulations, the video does not provide explicit instructions on how to perform these simulations using PSpice for TI. Exploration of these simulations using PSpice for TI is beyond the scope of this application report.

2.8 Input Design Worksheet

Table 2-2 lists the required inputs needed to evaluate an ADC input driving circuit and provides a place to summarize the outputs. Completing this worksheet for each unique circuit in your real-time control application is recommended to ensure good settling performance. For some circuits, it may be desirable to use the alternate design methodology presented in the application report Charge-Sharing Driving Circuits for C2000 ADCs (using PSPICE-FOR-TI simulation tool). That report also provides a worksheet that can be evaluated using the alternate design methodology.

Table 2-2. ADC Input Settling Design Worksheet

Symbol	Description	Value	Comments
Vfs	Full scale voltage range		In external reference mode, this is the voltage supplied to the VREFHI pin (usually 3.0V or 2.5 V) In internal reference mode, this is the effective input range based on the selected reference mode (usually 3.3 V or 2.5 V)
N	Target settling resolution (bits)		Usually the same as the resolution of the ADC Lower resolution can be targeted to relax the input design requirements
V_{errmax}	Maximum error target		$V_{fs} / 2^{N+1}$ Obtain using Analog Engineer's Calculator: ADC SAR Drive
t_{sh}	S+H time		Enter target S+H time if known Longer S+H times will result in less stringent BW requirements for the driving op-amp. Can be solved for given a pre-determined op-amp selection or a pre-determined R_S and C_S
Ron	ADC switch resistance		Provided in the *Input Model Parameters* table in the device-specific data manual TI Precision Labs training refers to this as "R_{sh}"
C_h	ADC S+H capacitance		Provided in the *Input Model Parameters* table in the device-specific data manual TI Precision Labs training refers to this as "C_{sh}"
C_p	ADC pin parasitic capacitance		Provided in the *Per-Channel Parasitic Capacitance* table in the device-specific data manual
C_S (range)	Range of source capacitance		Obtain using Analog Engineer's Calculator: ADC SAR Drive. TI Precision Labs training refers to this as "C_{filt}"

Table 2-2. ADC Input Settling Design Worksheet (continued)

Symbol	Description	Value	Comments
R_S (range)	Range of source resistance		Obtain using Analog Engineer's Calculator: ADC SAR Drive. TI Precision Labs training refers to this as "R_{filt}"
BWOPA	ADC driver op-amp minimum bandwidth		Obtain using Analog Engineer's Calculator: ADC SAR Drive.
Op-amp	Selected Op-amp part number		Record selected op-amp here
V_{oa_ss}	Steady state op-amp output voltage		Generated from DC nodal analysis of the V_{oa} node Copy to V_{oa_ss} before proceeding with other simulations
C_S (final)	Final source capacitance		Final selected C_s from simulation. TI Precision Labs training refers to this as "C_{filt}"
R_S (final)	Final source resistance		Final selected R_S from simulation. TI Precision Labs training refers to this as "R_{filt}"
BW_{RsCs}	Filter bandwidth from C_S and R_S		$1 / (2\pi \cdot C_S \cdot R_S)$ **Note** For proper settling, the filter bandwidth will be necessarily higher than the ½ the sampling frequency, thus the combination of C_S and R_S generally will not function as an anti-aliasing filter.
V_{err}	Actual settling error		Ensure $V_{err} < V_{errmax}$ Othwerwise, additional iteration on selection of C_s , R_s , or the driving amplifier is needed.

3 Example Circuit Design

The following sections work through and discuss designing an example C2000 circuit for input settling.

3.1 Select the ADC

This example assumes an F280049 device in external reference mode (VREFHI = 3.0 V) using channel A0. Triggering occurs at 1 MHz. This ADC supports 12-bit single-ended sampling only.

From the *TMS320F28004x Microcontrollers Data Manual*, the following key values are obtained:

- Minimum sample window duration = 75 ns
- Ch = 12.5 pF
- Ron = 500 Ω
- Cp = 12.7 pF
- ADC conversion time = 210 ns (t_{eoc} in the *ADC Timings* table from the *TMS320F28004x Microcontrollers Data Manual*) = 21 SYSCLK cycles, SYSCLK = 100 MHz)

3.2 Find the Minimum Op-Amp Bandwidth and RC Filter Ranges

Figure 3-1 shows the inputs and outputs to the Analog Engineer's Calculator for this example. Note that the S+H duration is relaxed from the ADC minimum of 75 ns to 100 ns. From this, the following key values are obtained:

- C_s = 240 pF (120 pF to 360 pF range, if needed)
- R_s range = 17 Ω to 138 Ω
- Op-amp minimum bandwidth = 37 MHz
- Settling error target (1/2 LSBs) = 366 µV

In conjunction with the op-amp selection step, it was found that slightly relaxing the S+H duration reduced the required op-amp bandwidth from 50 MHz to 37 MHz. This allowed for an op-amp selection that better met the project constraints (OPA350) while still meeting the application requirements for sample latency.
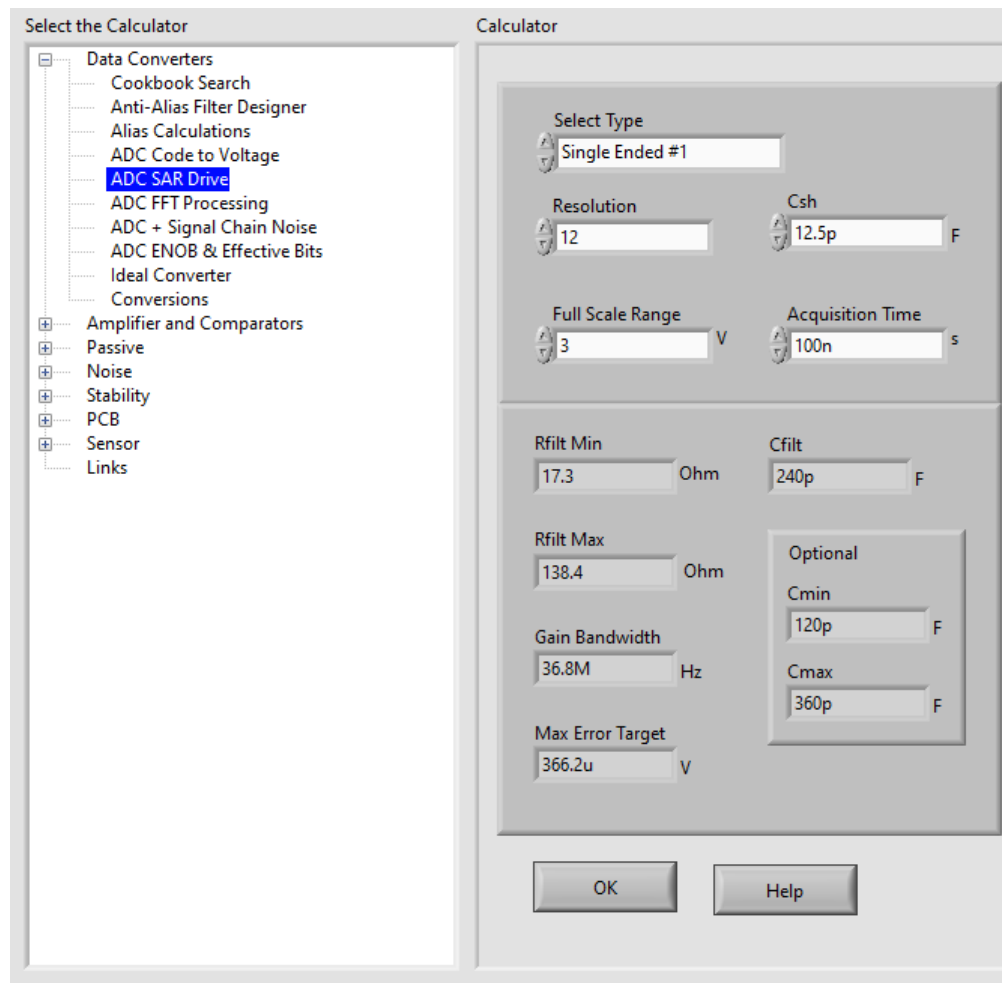
Figure 3-1. F280049 Example Analog Engineer's Calculator Output

3.3 Verify the Op-Amp Model

The latest OPA350 model was obtained using the PSpice Part Search tool.

3.4 Build the ADC Input Model

The OPA350 model was combined with the provided F28004x_Ext.opj ADC input model. In addition to setting the driving amplifier to OPA350, the following were performed on the PSpice for TI file to prepare for simulation:

• Op-amp power supplies set to an appropriate voltage (5.0 V and ground)
• V_{in} set to full-scale voltage (3.0 V)
• C_s and C_p initial value set to full-scale voltage (3.0 V)
• V_{oa_ss} set to the voltage obtained from DC nodal voltage analysis (demonstrated in the next section)
• T_{acq} and T_{dis} source period set to 1000 ns (1 MHz trigger frequency)
• T_{acq} source S+H time set to 100 ns
• C_p, R_{on}, and C_h values set based on values obtained from the device-specific data manual
• C_s set to the nominal value provided by calculator
• R_s set to a value in the calculator provided range (by setting R_STEP)

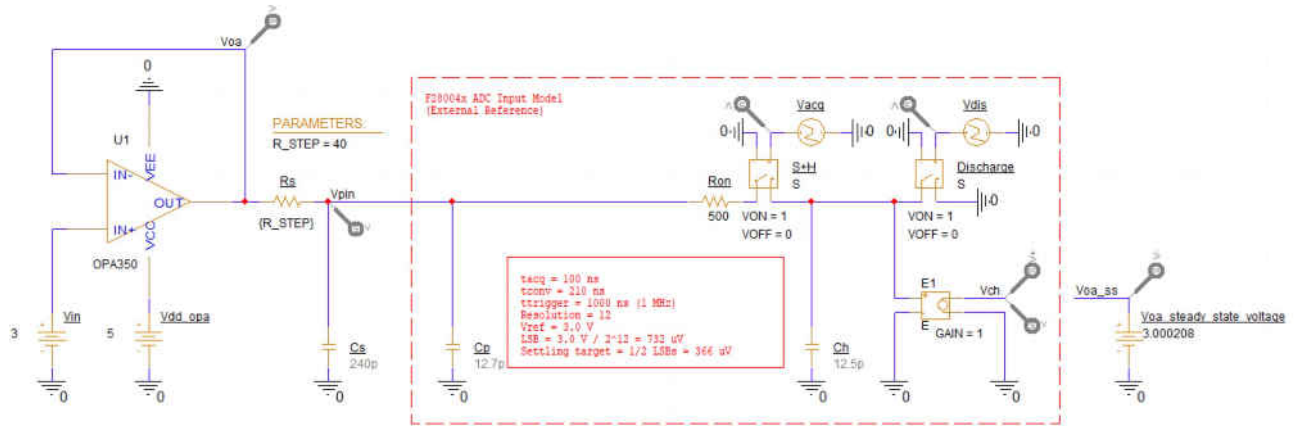The initial circuit is shown in Figure 3-2 and the timings for tacq and tdis are shown in Figure 3-3 and Figure 3-4.

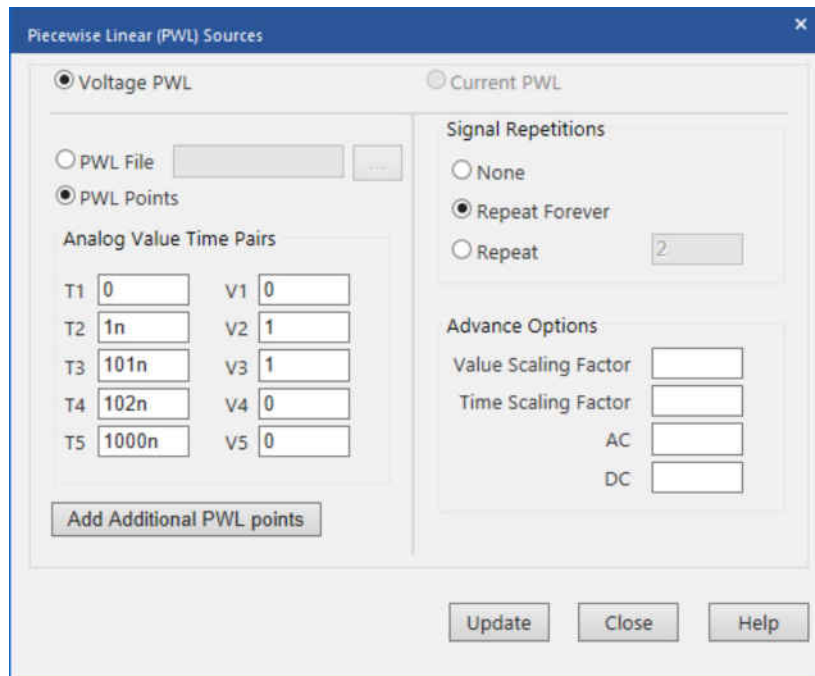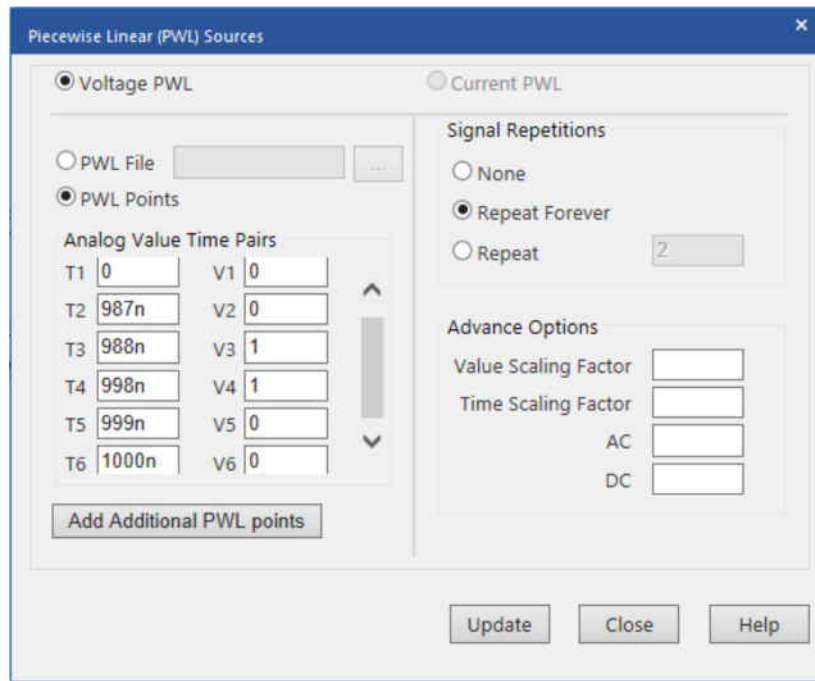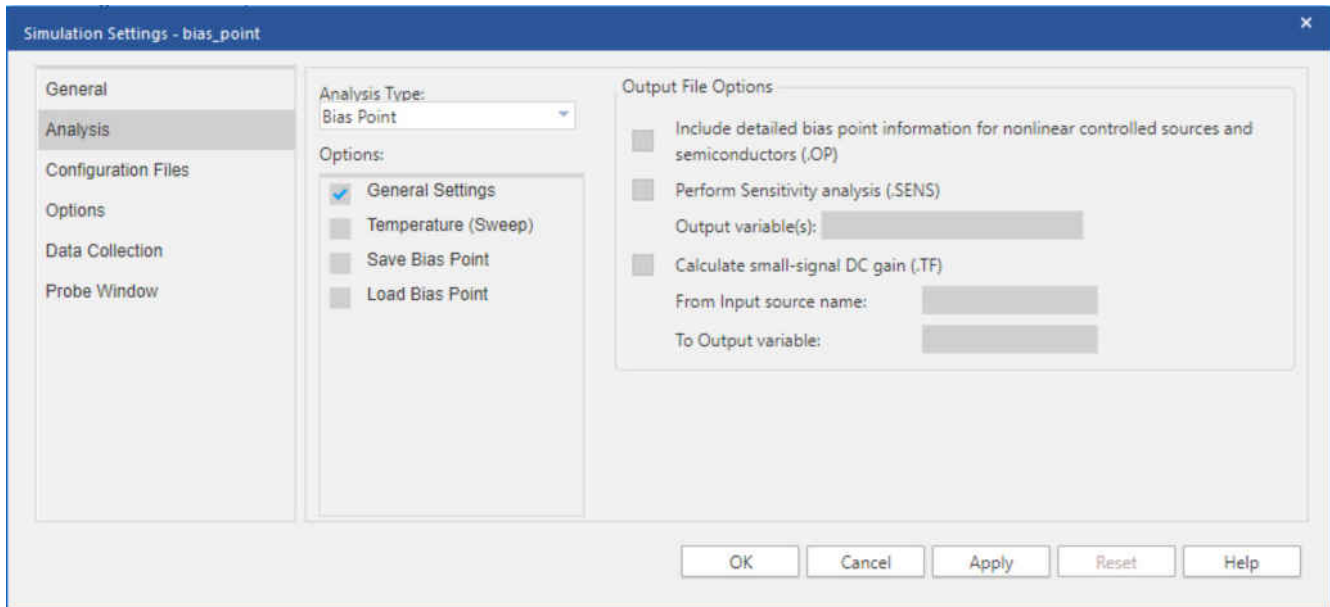**Figure 3-2. F280049 Example PSpice for TI Circuit**

Figure 3-3. F280049 Example T$_{acq}$ Source Timings

Figure 3-4. F280049 Example T$_{dis}$ Source Timings

3.5 Bias Point Analysis to Determine Voa_ss

To finalize the PSpice for TI input model, perform a bias point analysis to determine the steady-state output value for V_{oa} given the specific op-amp being evaluated. Performing a bias point analysis in PSpice for TI requires the creation of a Bias Point simulation profile. Once the simulation profile is created, go to PSpice ➔ Run to perform the analysis. Perform a bias point analysis using the simulation profile shown in Figure 3-5

Figure 3-5. F280049 Example Bias Point Analysis Simulation Profile

If the bias point analysis does not converge, then a transient analysis must be performed instead to determine the steady-state output value for V_{oa} given the specific op-amp being evaluated. For instructions on how to proceed, close the PSpice for TI simulation window and see Section 3.6. If the bias point analysis converges, close the PSpice for TI simulation window. Using the menu in the upper left of the PSpice for TI schematic capture window, go to PSpice ➜ Bias Points and enable bias voltage display. The bias voltages should appear as shown in Figure 3-6

Figure 3-6. F280049 Example Bias Point Analysis Results

The bias voltage of the node at the output of the specific op-amp being evaluated is the steady-state output value for V_{oa}. For OPA350 in this circuit, this procedure gives:

• V_{oa} = 3.000141 V

Copy this value to the V_{oa_ss} voltage source.

> **CAUTION**
>
> Ensure that the steady-state output value for V_{oa} is accurate to the microvolt (i.e., there are at least six digits following the decimal point). For guidance on how to optimize simulation results, see Section 2.5.

Because the steady-state output value for V_{oa} given the specific op-amp being evaluated is known, skip the next section, Section 3.6, and refer to Section 3.7 for instructions on how to proceed.

Note

The remainder of the application report assumes that the bias point analysis does not converge. If the bias point analysis does not converge, then any transient analysis must skip the initial bias point calculation. Thus, subsequent transient analyzed in this application report skip the initial bias point calculation. However, if the bias point analysis converges, then any transient analysis should not skip the initial bias point calculation. Thus, subsequent transient analysis should not skip the initial bias point calculation. For this reason, results obtained may vary from the results presented in this application report.

3.6 Transient Analysis to Determine V_{oa_ss}

To finalize the PSpice for TI input model, perform a transient analysis to determine the steady-state output value for V_{oa} given the specific op-amp being evaluated. Prior to the transient analysis, disconnect the left end of R_{on} from the circuit and attach that end to ground. Note that a voltage level marker is already attached to the output of the op-amp. The modified circuit is shown in Figure 3-7.
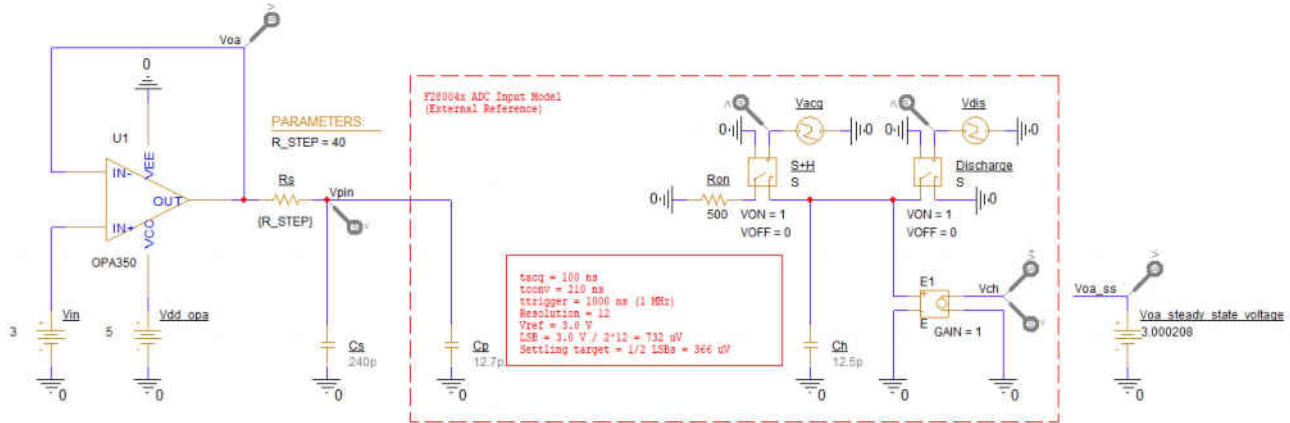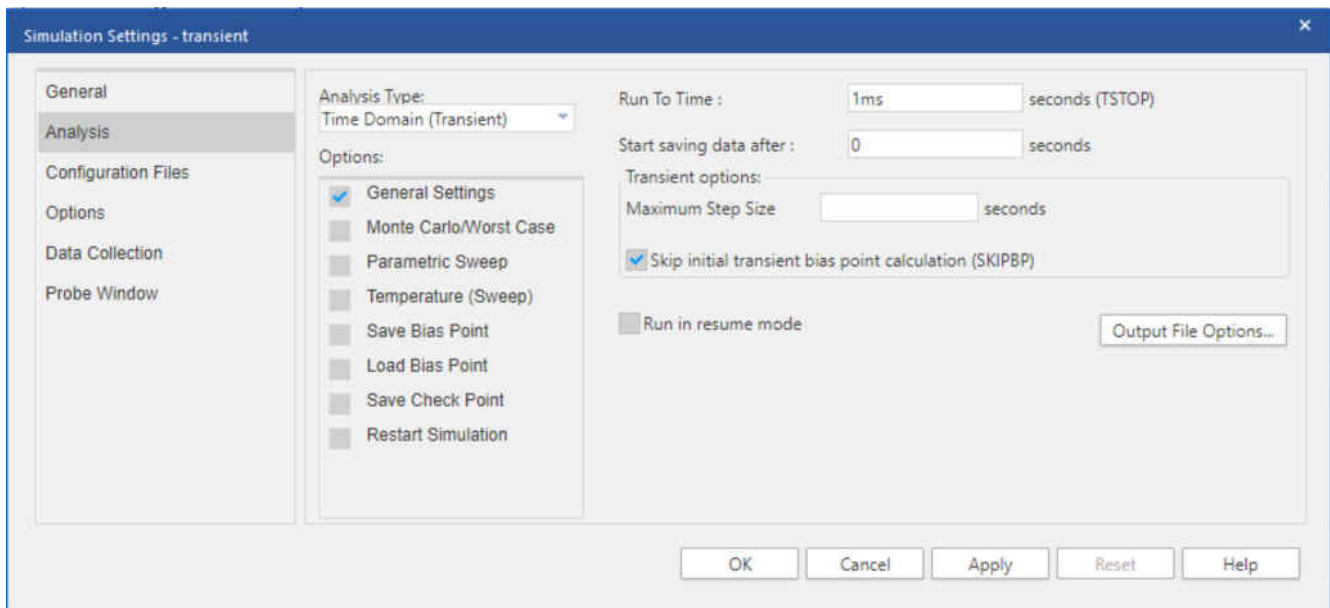

Figure 3-7. F280049 Example Modified PSpice for TI Circuit

Performing a transient analysis in PSpice for TI requires the creation of a Time Domain (Transient) simulation profile. Once the simulation profile is created, go to PSpice ➔ Run to perform the analysis. Perform a transient analysis using the simulation profile shown in Figure 3-8.

Figure 3-8. F280049 Example Transient Analysis Simulation Profile

Delete all outputs other than V_{oa} and set V_{oa} range to +2.95 V to +3.05 V. Alternatively, go to Window ➔ Display Control... using the menu in the upper left of the PSpice for TI simulation window to access a list of preset display configurations provided by TI. Restore the Steady-State Analysis display configuration. Note that these preset display configurations are only available in the PSpice for TI projects bundled with this application report. Then use a probe cursor to measure the steady-state output value for V_{oa} as shown in Figure 3-9.
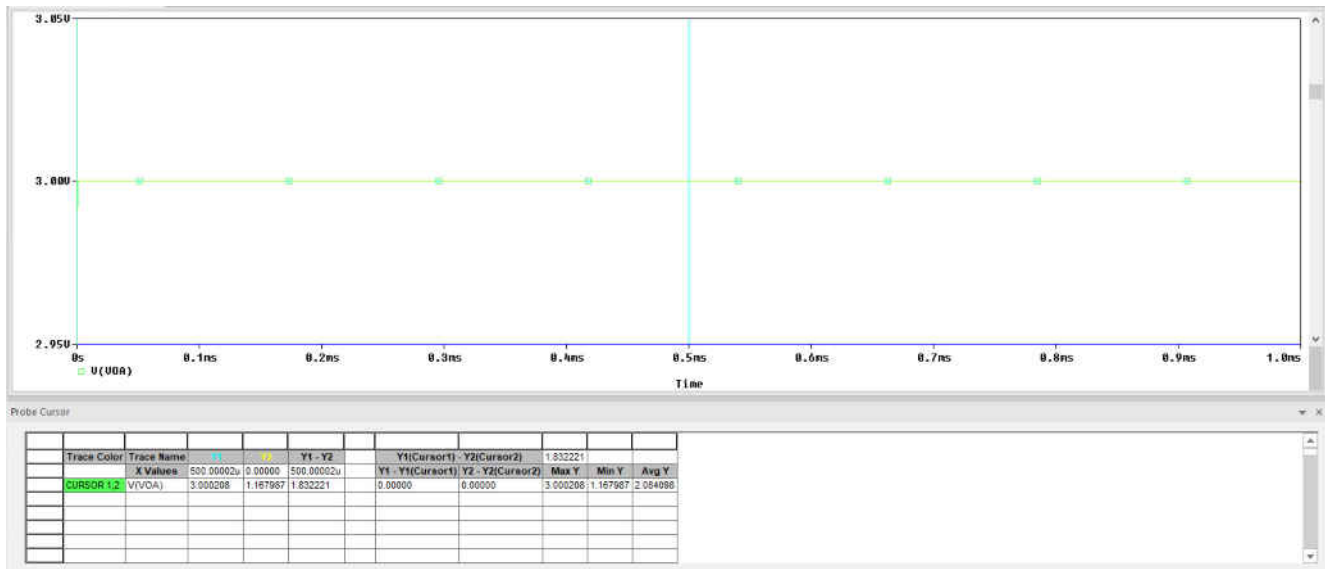
Figure 3-9. F280049 Example Transient Analysis Results

For OPA350 in this circuit, this procedure gives:

- V_{oa} = 3.000208 V

Copy this value to the V_{oa_ss} voltage source. Following the transient analysis, detach the left end of R_{on} from ground and reconnect that end to the circuit.

> **CAUTION**
>
> Ensure that the steady-state output value for V_{oa} is accurate to the microvolt (there are at least six digits following the decimal point). If necessary, review Section 2.5 for guidance on how to optimize simulation results.

Now that the steady-state output value for V_{oa} is given, the specific op-amp being evaluated is known. For instruction on how to proceed, see Section 3.7.

Note

Note that the remainder of the application report assumes that the bias point analysis does not converge. If the bias point analysis converges, then any transient analyses should not skip the initial bias point calculation. However, if the bias point analysis does not converge, then any transient analyses must skip the initial bias point calculation. Thus, subsequent transient analyses in this application report skip the initial bias point calculation.

3.7 Perform Initial Transient Analysis

Now that the circuit is setup for simulation, the first step is to run a basic transient analysis to ensure everything is functioning and to check the initial settling. Performing a transient analysis in PSpice for TI requires the creation of a Time Domain (Transient) simulation profile. Once the simulation profile is created, go to PSpice ➔ Run to perform the analysis.

The settling should be captured after allowing the circuit to stabilize for a couple sampling cycles, so a time period of 2.5 µs to 5.5 µs is selected as shown in Figure 3-10. This allows capture of the full 3rd and 4th sampling cycles (each cycle is 1 µs since the trigger frequency is 1 MHz). A maximum step size of 0.1 ns is chosen to produce sufficiently granular simulation results.
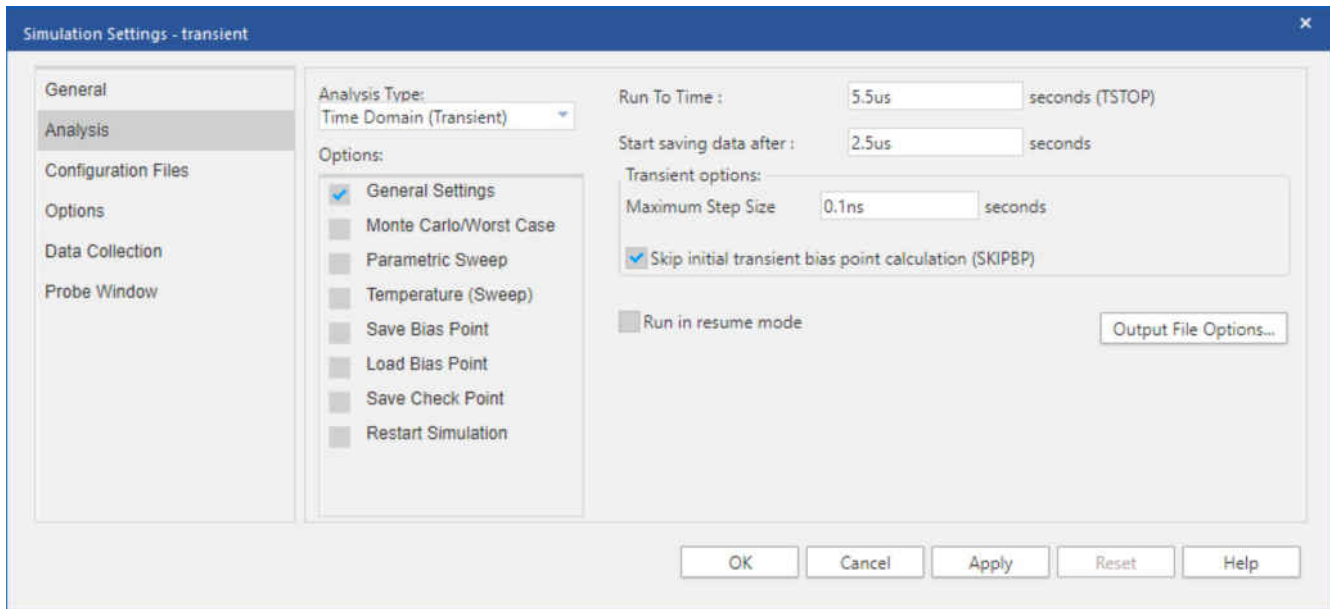
Figure 3-10. F280049 Example Transient Analysis Simulation Profile

After performing the analysis, separate the output waveforms onto different plots. Set V_{acq} range to 0 V to +1 V. Set V_{ch} range to 0 V to +4 V. Set V_{dis} range to 0 V to +1 V. Set V_{error} range to -10 mV to +10 mV. Set V_{oa} range to+2.9 V to +3.1 V. Finally, set V_{pin} range to+2.9 V to +3.1 V. Alternatively, go to Window ➔ Display Control... using the menu in the upper left of the PSpice for TI simulation window to access a list of preset display configurations provided by TI. Restore the Transient Results display configuration. Note that these preset display configurations are only available in the PSpice for TI projects bundled with this application report. Figure 3-11 shows the output waveforms from the transient simulation. From this output, it is clear that:

- Discharge and acquisition times are functioning as expected
- The transients on V_{oa} and V_{pin} are of reasonable magnitude (less than 100 mV, so the signal settling will be considered a small signal event)
- V_{error} is settling to about 69 µV, which is well within the error target of 366 µV
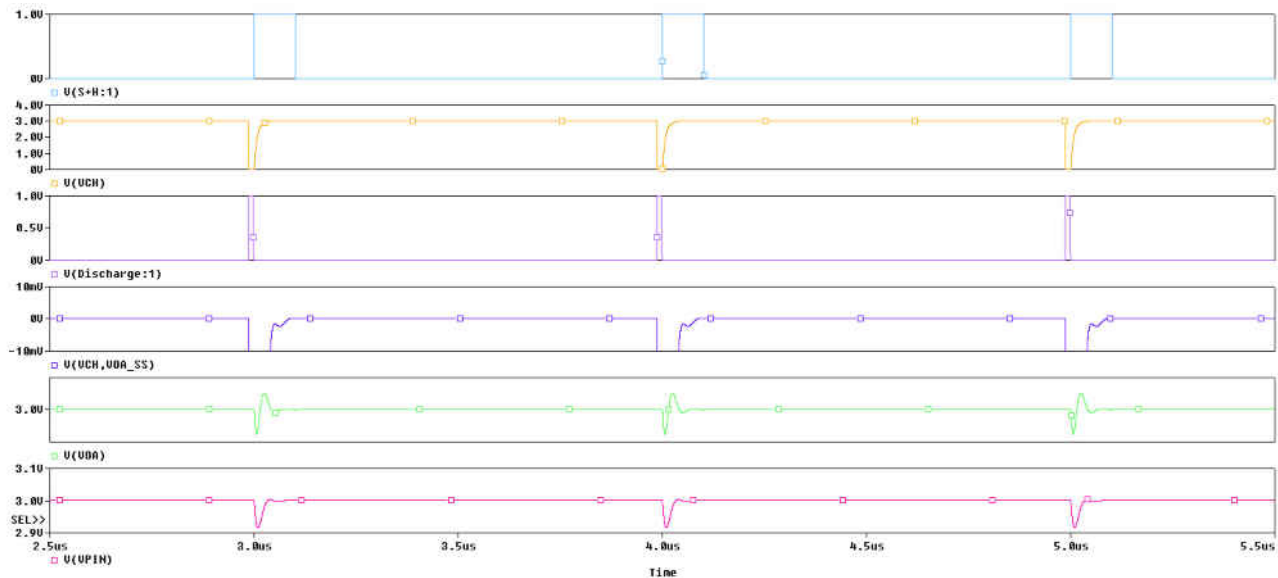
Figure 3-11. F280049 Example Initial Transient Results

3.8 Iterative Approach to Refine RC Filter Values

Now that the basic simulation has shown that the simulation is fundamentally working, sweeps can be performed to refine the R_s component selection.

To perform a sweep, open the transient simulation profile and enable the Parametric Sweep option. In the Parametric Sweep settings, choose the global parameter R_STEP as the sweep variable. Then choose a linear sweep type with a start value of 17 Ω, an end value of 138 Ω, and an increment of 10 Ω as shown in Figure 3-12.
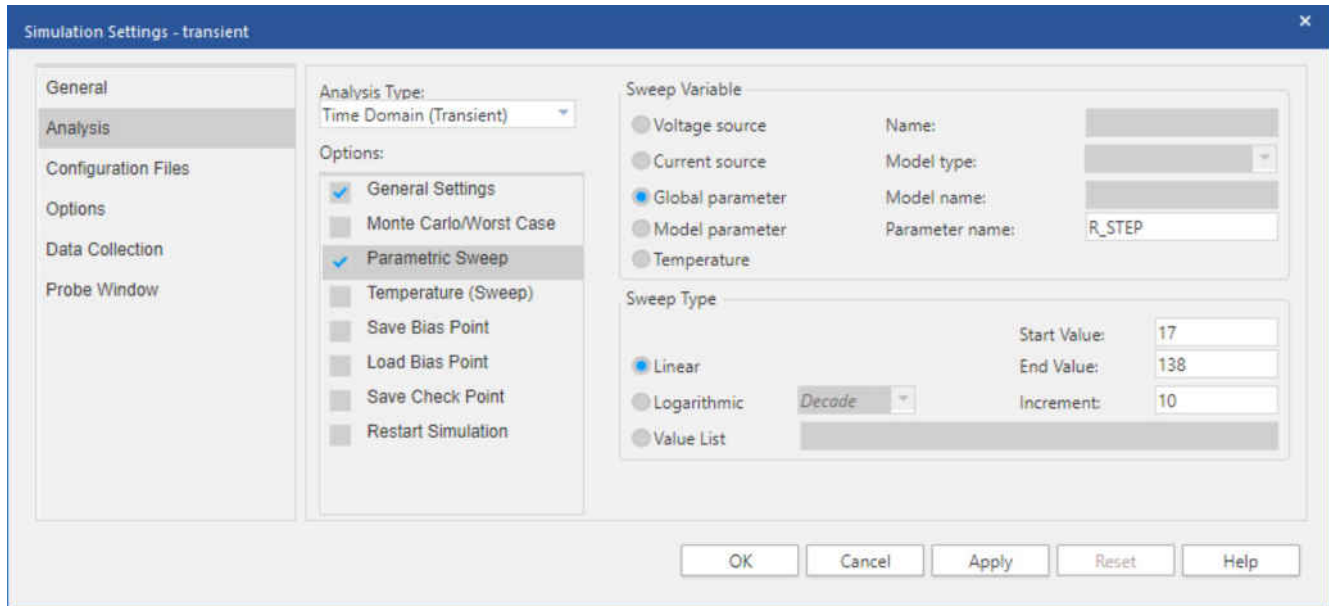
Figure 3-12. F280049 Example Parametric Sweep Settings

After performing the analysis, delete all outputs other than V_{error} and set V_{error} range to -30 mV to +30 mV. Additionally, limit the waveform to +2.95 µs to +3.15 µs to better observe the settling. Alternatively, go to Window ➔ Display Control... using the menu in the upper left of the PSpice for TI simulation window to access a list of preset display configurations provided by TI. Restore the Sweep Results display configuration. Note that these preset display configurations are only available in the PSpice for TI projects bundled with this application report. Figure 3-13 shows the output of the transient simulation with a sweep of R_s.

From this output, it can be concluded:

- Higher resistance values in the R_s range do not provide quick enough settling. For instance, 107 Ω only settles to 6.1 mV in the allocated S+H time while the settling target is 366 µV
- A good range for further investigation would be 20 Ω to 60 Ω. Determining the optimal value of R_s requires further analysis, which may include additional simulations
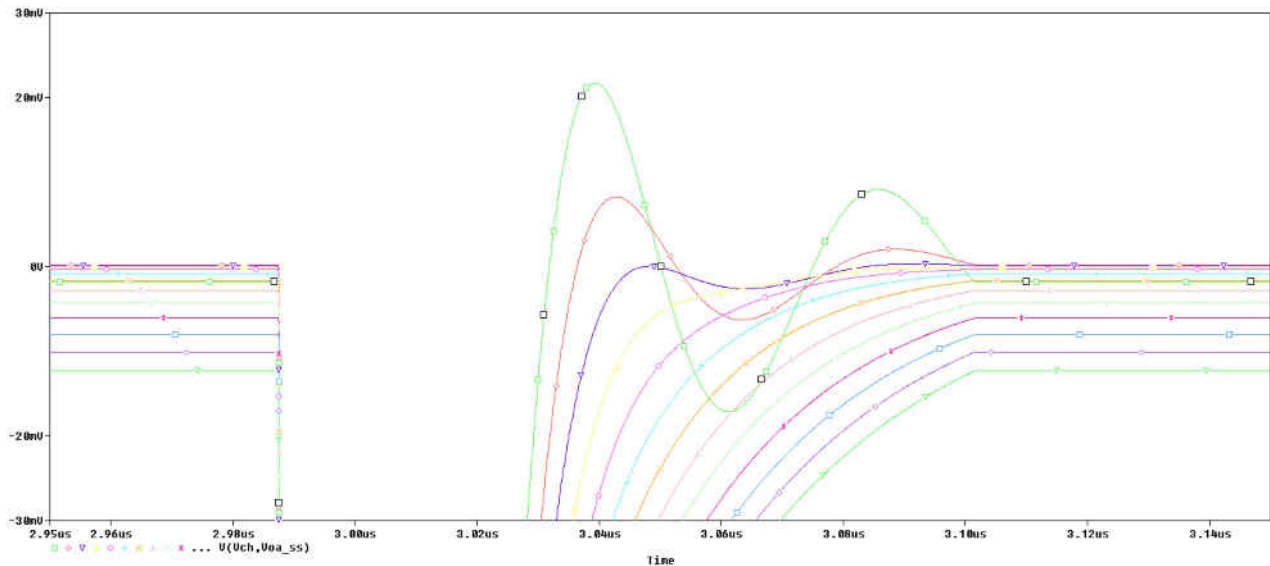
Figure 3-13. F280049 Example R$_s$ Initial Sweep Results

Based on the initial sweep results, it may already be possible to identify one or more values of R$_s$ that provide adequate settling. If desired, the R$_s$ component selection can be further refined by iteratively narrowing the linear sweep range. A value list sweep may also be performed to test values of R$_s$ that are not linearly spaced. An example simulation profile for a value list sweep is shown in Figure 3-14.
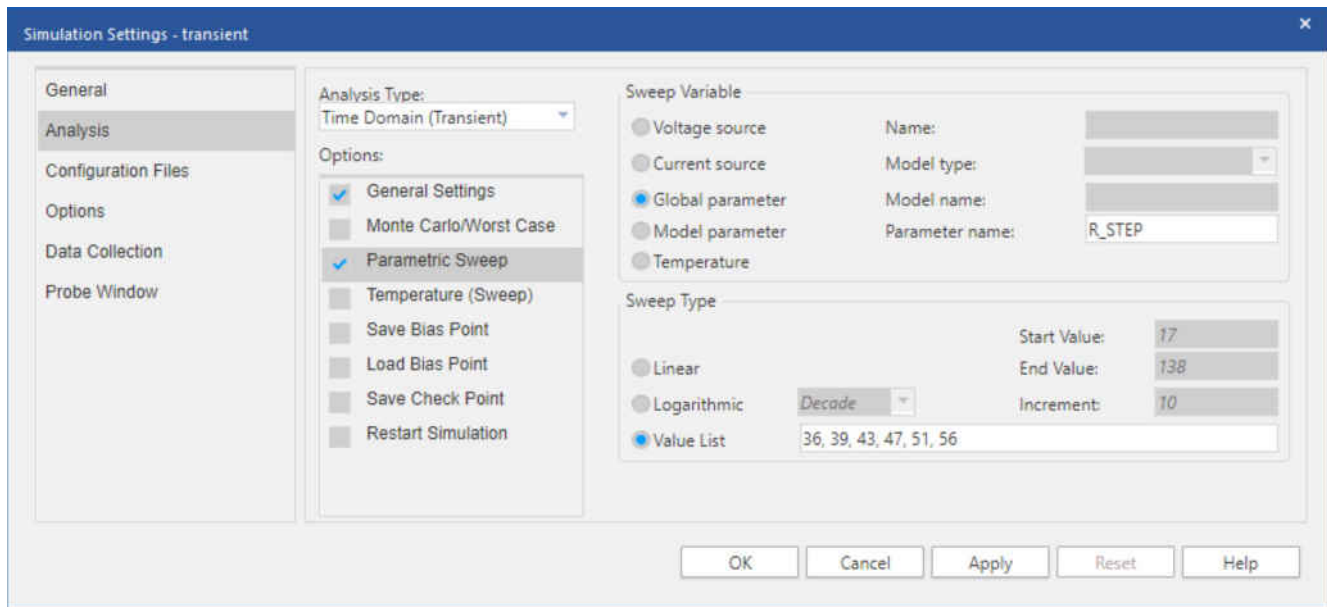

Figure 3-14. F280049 Example Parametric Sweep Settings

Thus, a final value of R$_s$ can be selected that provides adequate settling. With enough iterations, the final value of R$_s$ can be made optimal. However, Section 3.9 introduces an alternative method to better select the optimal value of R$_s$ using the Performance Analysis tool.

3.9 Perform Final Transient Analysis

As an alternative to the iterative approach presented in Section 3.8, the Performance Analysis tool can be used to better select the optimal value of R$_s$. By applying the Performance Analysis tool to the initial sweep results presented in Figure 3-12, it is possible to graph settling error as a function of the value of R$_s$. To launch the Performance Analysis tool, go to Trace ➜ Performance Analysis... using the menu in the upper left of the PSpice for TI simulation window. The Performance Analysis tool is shown in Figure 3-15.
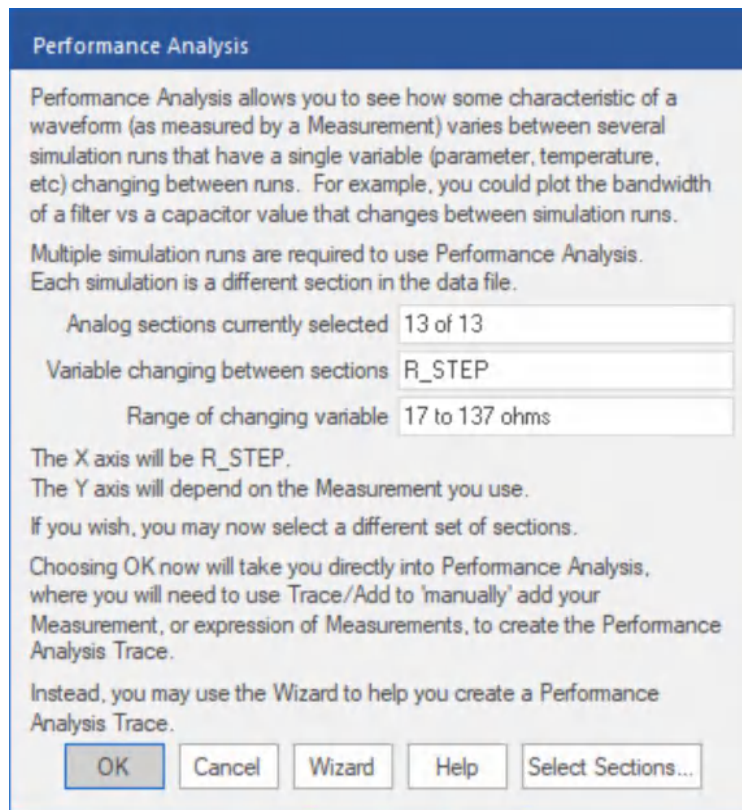
Figure 3-15. F280049 Example Performance Analysis

Use the Wizard to create a Performance Analysis Trace. When prompted to choose a measurement, select YatX as shown in Figure 3-16. When prompted to complete the measurement expression, enter V(Vch, Voa_ss) as the name of the trace to search and 3.12 µs as the X value at which to measure the Y value as shown in Figure 3-17. Note that this measurement expression measures the Y value of the V_{error} trace at 3.12 µs, which is just past the end of an acquisition window. Thus, this measurement expression measures the settling error.
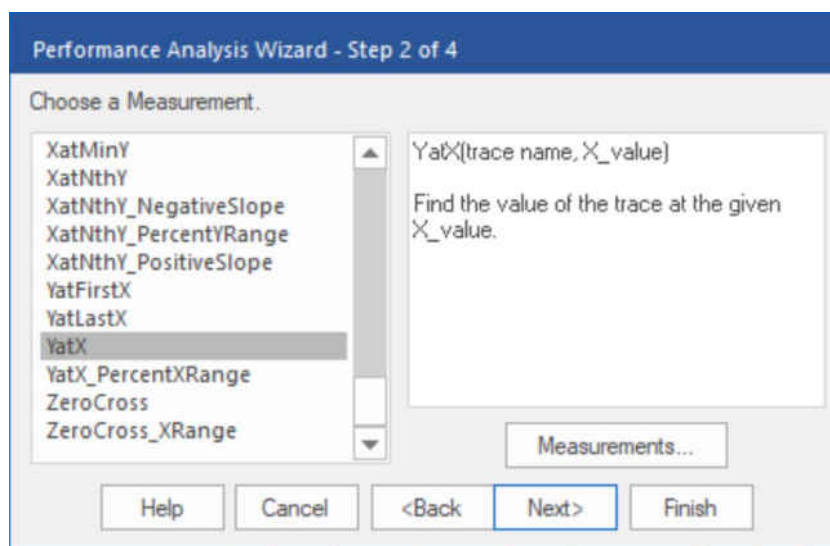
Figure 3-16. F280049 Example Performance Analysis Wizard - Step 2 of 4
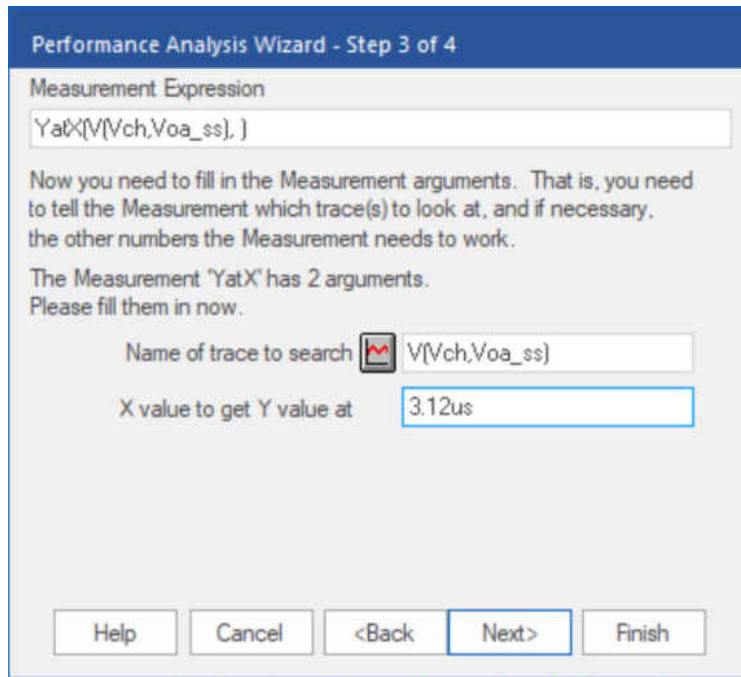
Figure 3-17. F280049 Example Performance Analysis Wizard - Step 3 of 4

When finished using the Wizard, a Performance Analysis Trace of settling error as a function of the value of R_s should appear as shown in Figure 3-18. Note that the settling error scale has been adjusted to show a range of -2 mV to +2 mV. The settling error scale can be further adjusted as desired by double-clicking on the vertical axis and modifying the Data Range.
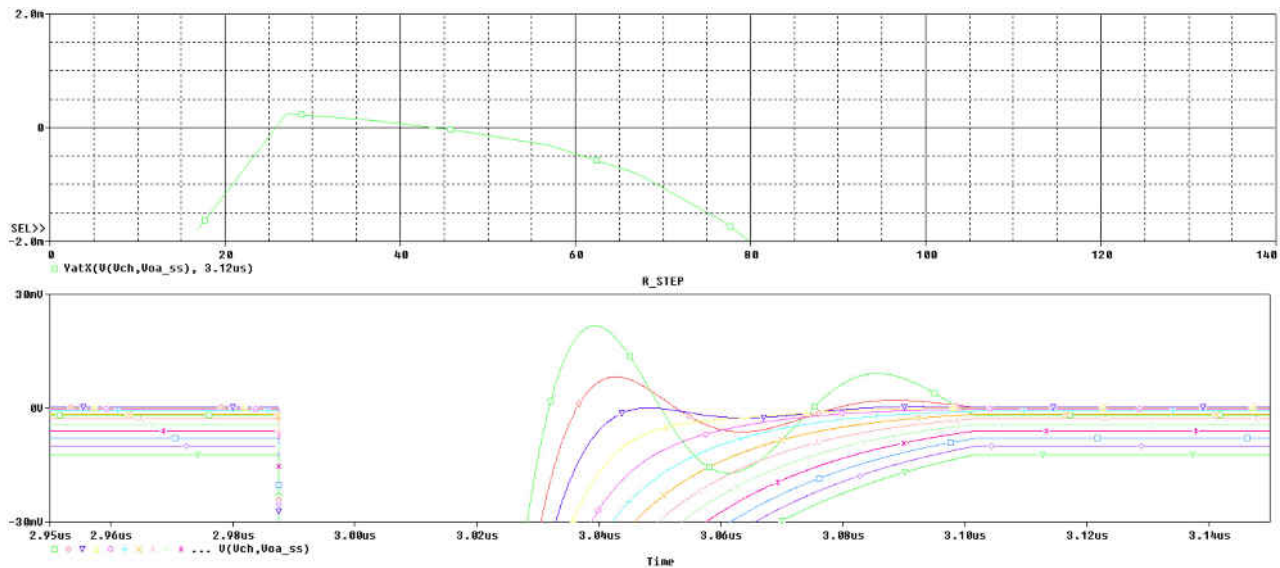

Figure 3-18. F280049 Example Performance Analysis Trace

Examining the Performance Analysis Trace shows that the settling error is approximately zero when the value of R_s is roughly 26 Ω and again when the value of R_s is roughly 44 Ω. However, Figure 3-12 shows that smaller values of R_s tend to result in greater oscillations of V_{error} than larger values of R_s. Greater oscillations of V_{error} are not ideal because small changes to the duration of the acquisition window can lead to large variations in settling error. Additionally, the slope of the Performance Analysis Trace at values of R_s near 26 Ω is steeper than the slope of the Performance Analysis Trace at values of R_s near 44 Ω. A steeper slope of the Performance Analysis Trace is not preferable because small variations in the value of R_s can lead to large changes in settling error. For this reason, values of R_s around 26 Ω are ignored in favor of values of R_s around 44 Ω.

Based on the Performance Analysis Trace, any value of R_s between 24 Ω and 56 Ω inclusive is expected to provide adequate settling. As a result, a final value of R_s can be selected from the set of standard resistor values in the range from 24 Ω to 56 Ω inclusive with a preference for standard resistor values near 44 Ω. The optimal value of R_s is the standard resistor value in this range that provides the least settling error. According to the Performance Analysis Trace, the 5% standard resistor value in this range that provides the least settling error is is 43 Ω. Thus, the final value of R_s is selected as the optimal value of 43 Ω.

3.10 Perform Final Transient Analysis

With the final R_s and C_s values determined, a final transient simulation without the Parametric Sweep option enabled can be performed to validate the component selections. After performing the simulation, separate the output waveforms onto different plots. Set V_{acq} range to 0 V to +1 V. Set V_{ch} range to 0 V to +4 V. Set V_{dis} range to 0 V to +1 V. Set V_{error} range to -10 mV to +10 mV. Set V_{oa} range to +2.9 V to +3.1 V. Finally, set V_{pin} range to +2.9 V to +3.1 V. Additionally, limit the waveform to +2.9 μs to +3.5 μs to better observe the output waveforms. Alternatively, go to Window ➔ Display Control... using the menu in the upper left of the PSpice for TI simulation window to access a list of preset display configurations provided by TI. Restore the Final Transient Results display configuration. Note that these preset display configurations are only available in the PSpice for TI projects bundled with this application report. Figure 3-19 shows the results of this final simulation. From these results, it appears that the settling crosses the settling target of 366 μV somewhere around 83 ns and the final settling at 100 ns is around 15 μV. The final application circuit should have excellent ADC input settling.
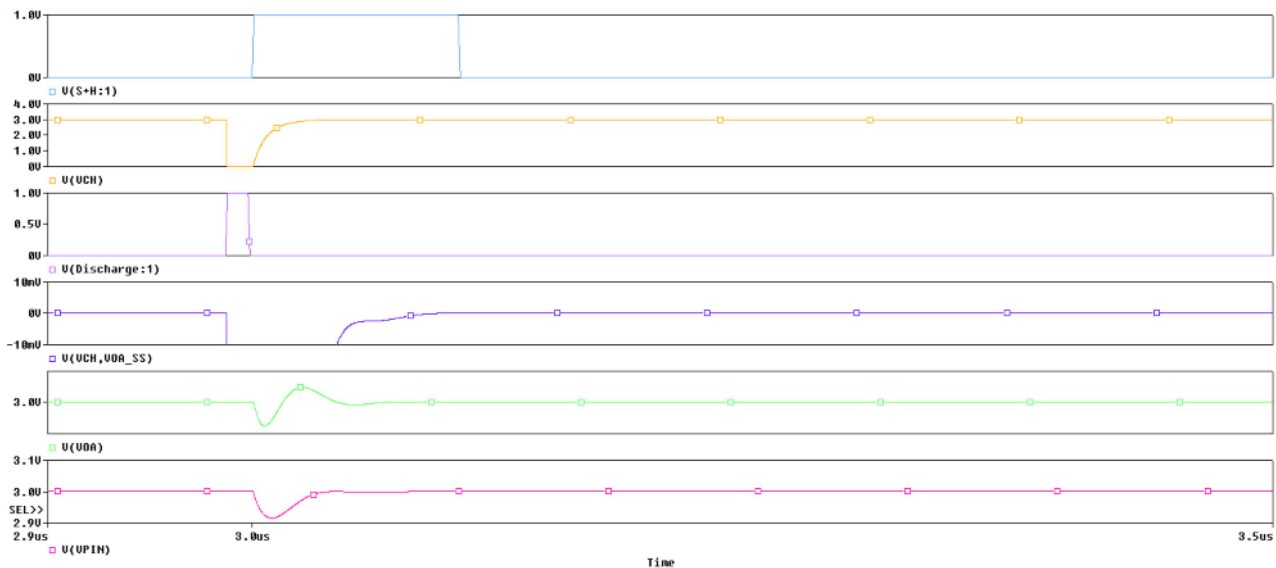
Figure 3-19. F280049 Example Final Transient Results

3.11 Further Refinement

Overall, it appears that this design has quite a bit of settling margin. If further optimization is desired, the designer could explore using an op-amp with slightly lower bandwidth. Alternatively, the simulation supports using a S+H window that is shorter than 100 ns, if desired.

Another area refinement is to resolve a circuit with intentionally higher R_s and C_s. As designed, the low-pass filter bandwidth of the R_s and C_s circuit is about 15 MHz, so this circuit provides some rejection of high-frequency noise. By intentionally increasing R_s and C_s, the filter bandwidth can be lowered, resulting in additional noise rejection. However, note that the R_s and C_s circuit can generally not provide a true anti-aliasing filter, as this would necessarily result in a settling time constant that would be much too large to allow proper settling. If a true anti-aliasing filter is needed, this should be built as a separate filter stage before the ADC drive stage.

> **CAUTION**
> Even if the simulations indicate that the input could settle faster than the minimum acquisition window specified in the device-specific data manual, do not select an acquisition window that violates the device-specific data manual minimum acquisition window time.

3.12 Further Simulations

As indicated in Section 2.7, once the final components are selected, it is possible to perform additional simulations to further validate the design. This design was validated over multiple cycles and with increased S+H duration (not shown). No issues were identified in these additional simulations.

3.13 Completed Worksheet

Table 3-1 shows the completed worksheet for the F280049 with OPA2350 example.

Table 3-1. ADC Input Settling Design Worksheet (F280049 Example)

Symbol	Description	Value	Comments
V_{fs}	Full scale voltage range	3.0 V	In external reference mode, this is the voltage supplied to the VREFHI pin (usually 3.0 V or 2.5 V) In internal reference mode, this is the effective input range based on the selected reference mode (usually 3.3 V or 2.5 V)
N	Target settling resolution (bits)	12 bits	Usually the same as the resolution of the ADC Lower resolution can be targeted to relax the input design requirements
V_{errmax}	Maximum error target	366 uV	$V_{fs} / 2^{N+1}$ Obtain using Analog Engineer's Calculator: ADC SAR Drive
t_{sh}	S+H time	100 ns	Enter target S+H time if known Longer S+H times will result in less stringent BW requirements for the driving op-amp. Can be solved for given a pre-determined op-amp selection or a pre-determined R_S and C_S
R_{on}	ADC switch resistance	500 Ω	Provided in the data manual table "Input Model Parameters" TI Precision Labs training refers to this as "R_{sh}"
C_h	ADC S+H capacitance	12.5 pF	Provided in the data manual table "Input Model Parameters" TI Precision Labs training refers to this as "C_{sh}"
C_p	ADC pin parasitic capacitance	12.7 pF	Provided in the data manual table "Per-Channel Parasitic Capacitance"
C_S (range)	Range of source capacitance	240 pF (120pF to 360pF)	Obtain using Analog Engineer's Calculator: ADC SAR Drive. TI Precision Labs training refers to this as "C_{filt}"
R_S (range)	Range of source resistance	17 to 138 Ω	Obtain using Analog Engineer's Calculator: ADC SAR Drive. TI Precision Labs training refers to this as "R_{filt}"
BW_{OPA}	ADC driver op-amp minimum bandwidth	37 MHz	Obtain using Analog Engineer's Calculator: ADC SAR Drive.
Op-amp	Selected Op-amp part number	OPA2350	Record selected op-amp here
V_{oa_ss}	Steady state op-amp output voltage	3.000014 V	Generated from DC nodal analysis of the V_{oa} node Copy to Voa_ss before proceeding with other simulations
C_S (final)	Final source capacitance	240 pF	Final selected C_S from simulation. TI Precision Labs training refers to this as "C_{filt}"
R_S (final)	Final source resistance	27 Ω	Final selected R_S from simulation. TI Precision Labs training refers to this as "R_{filt}"

Table 3-1. ADC Input Settling Design Worksheet (F280049 Example) (continued)

Symbol	Description	Value	Comments
BW$_{RsCs}$	Filter bandwidth from C$_S$ and R$_S$	2.5 MHz	$1 / (2\pi \cdot C_S \cdot R_S)$ **Note** For proper settling, the filter bandwidth will be necessarily higher than the ½ the sampling frequency, thus the combination of C$_S$ and R$_S$ generally will not function as an anti-aliasing filter.
Verr	Actual settling error	17 µV	Ensure V$_{err}$ < V$_{errmax}$ Othwerwise, additional iteration on selection of C$_S$, R$_S$, or the driving amplifier is needed

4 Working With Existing Circuits or Additional Constraints

The TI Precisions Labs design methodology explored in this report starts by assuming a S+H window is known and that the op-amp and R$_s$ and C$_s$ have not yet been determined. The following sections provide some guidance if one or more of these components has already been selected or otherwise needs to be constrained.

4.1 Existing Circuits

Fully determined input driving circuits can of course be simulated to check their settling using the provided ADC input models and simulation methodology.

Note that it is especially important to verify the performance over many sampling cycles for existing circuits that were not designed using the TI Precision Labs methodology. One common case where this is important is when the input was designed using a "charge-sharing" design methodology.

4.1.1 Brief Overview of Charge Sharing

Normally, as the size of C$_s$ increases, the settling time will also increase. It is generally not advantageous to make C$_s$ very large. However, if C$_s$ becomes sufficiently large, it can fully provide all the charge needed to drive C$_h$ to within the settling error target, regardless of the value of R$_s$.

The external source still needs to recharge C$_s$ through R$_s$ in the time between samples, otherwise each sample will slowly deplete the voltage on C$_s$. This results in a sample-rate limitation based on the magnitude of the R$_s$ resistance.

For 1/2 LSBs settling, the critical value of C$_s$ occurs at $C_s = 2^{(N+1)} \times C_h$.

4.1.2 Charge Sharing Example

In the example circuit in Figure 4-1, Cs has been set to approximately $2^{(N+1)} \times C_h$ and the sample trigger rate is set to 100 kHz.
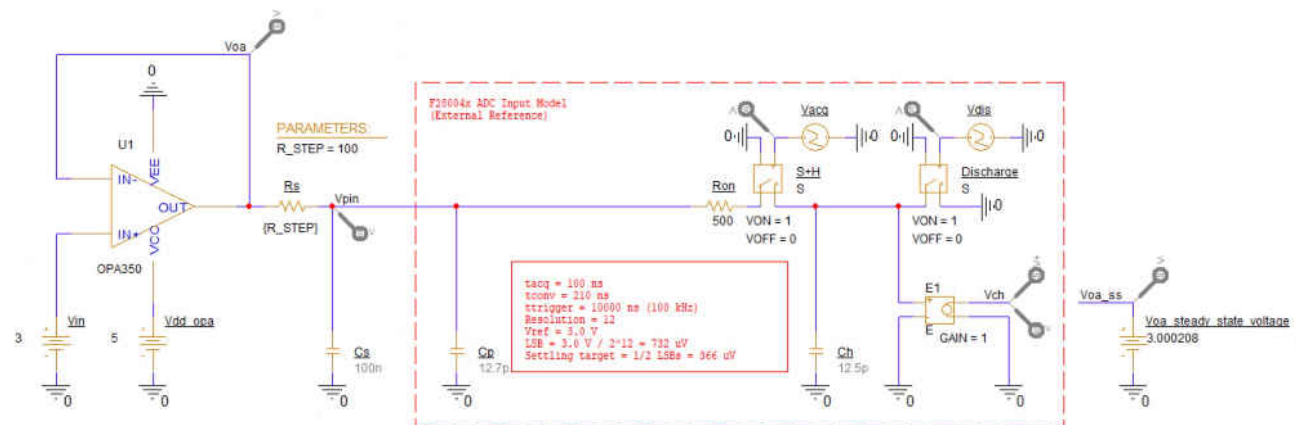

Figure 4-1. Example Circuit Utilizing Charge Sharing

Figure 4-2 shows the pin transient over many sampling cycles when R_s is 100 Ω. It can be seen that the voltage on the pin (which is the voltage directly on C_s) recovers to within 1/2 LSBs in the time between conversions. This will result in good ADC input settling using a very short S+H window as long as the sample-rate remains at or below 100 ksps.
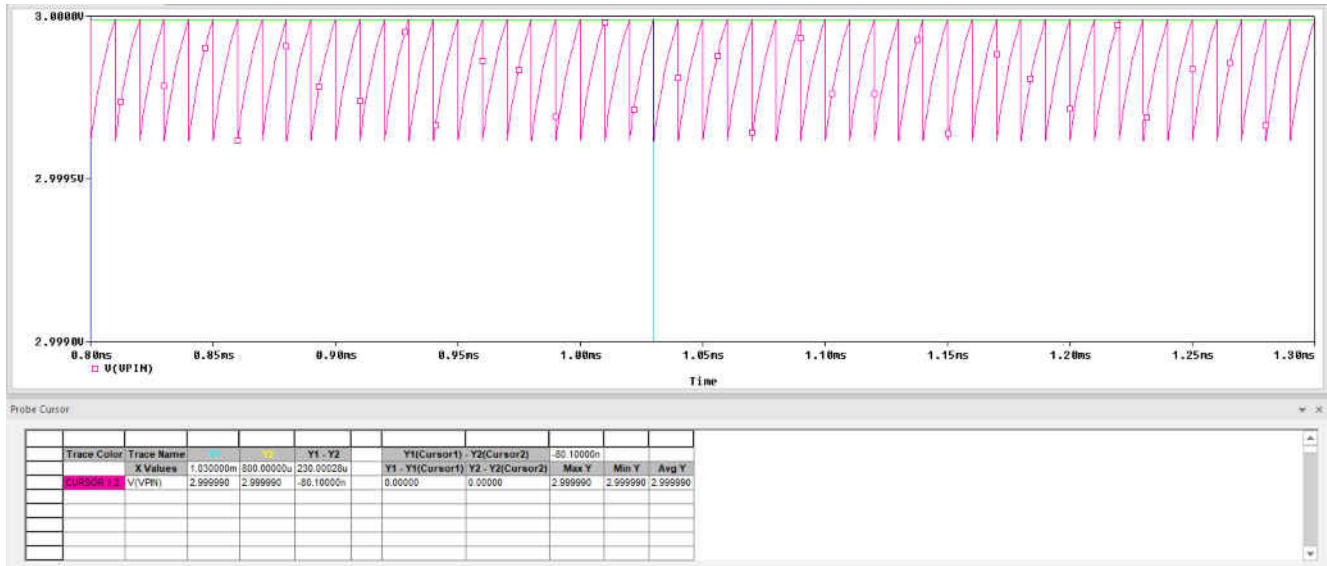
Figure 4-2. C_s Voltage With R_s = 100 Ω

Now consider the results in Figure 4-3. Rs has been set to 1k Ω. In this case, the voltage on C_s is slowly depleted sample-by-sample until an equilibrium is reached. At equilibrium, the pin voltage has an error of about 3.5 mV. Even though C_h will quickly match the C_s voltage during the S+H phase, the voltage on C_s has a significant error.
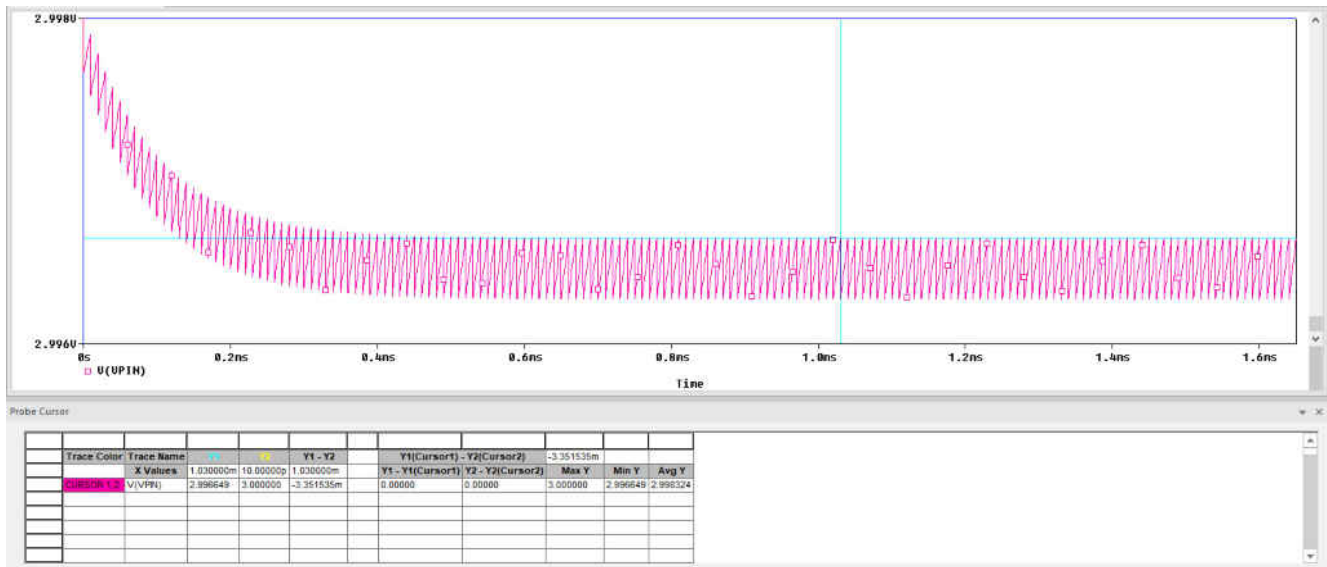
Figure 4-3. C_s Voltage With R_s = 1k Ω

To resolve this error, either R_s would need to be decreased or the sample rate would have to be reduced.

This example underscores the importance of simulating circuits with large C_s or R_s over many cycles.

4.1.3 Additional Resources for Charge Sharing

Further discussion of the charge-sharing design methodology is beyond the scope of this application report. However, *Charge-Sharing Driving Circuits for C2000 ADCs (using TINA-TI simulation tool)* and Charge-Sharing Driving Circuits for C2000 ADCs (using PSPICE-FOR-TI) present charge-sharing driving circuits in further detail. Note that these application reports cover the same content, but one uses the TINA-TI SPICE-based analog simulation program while the other uses the PSpice for TI design and simulation tool.

4.2 Pre-Selected Op-Amp

If the op-amp has already been selected for the input driver, the easiest method for proceeding with the design is to iterate the acquisition time setting in the Analog Engineer's Calculator until the necessary bandwidth matches the bandwidth of the pre-selected op-amp. The designer can then record the C_s and R_s component ranges and proceed with the design per the existing methodology (assuming that the predicted S+H meets the application's latency or sample rate requirements).

4.2.1 Pre-Selected Op-Amp Example

The designer wants to use OPA2320 as the driving op-amp for an ADC input (perhaps there is a spare channel from an OPA2320 performing another function on the PCB). OPA2320 has a bandwidth of 20 MHz and the ADC in question has a C_h value of 12.5 pF. By iterating the acqusition window input of the calculator, the solution shown in Figure 4-4 is found and thus a S+H window of 185 ns can be targeted.

Figure 4-4. Analog Engineer's Calculator Output for OPA2320

4.3 Pre-Selected R_s and C_s Values

If both external source components have been pre-selected, a target acquisition time can be determined by simulating the circuit with an ideal source or with an op-amp with very high bandwidth. This initial target acquisition time can then be used to provide some guidance in op-amp selection, and then design refinement can proceed as normal.

4.3.1 Analytical Solution for ADC Acquisition Time

A quick method for estimating the ADC S+H time given selections of R_s and C_s (along with the input model parameters from the device-specific data manual) is to use the formulas shown in Equation 1 and Equation 2:

$$T = \left(R_S + R_{on}\right)C_h + R_S\left(C_S + C_p\right)$$

$$k = \ln\left(\frac{2^N}{target\ settling\ error}\right) - \ln\left(\left(C_S + C_p\right)/C_h\right)$$

$$acquisition\ time = Tk$$

(1)

4.3.2 Example Analytical Solution for ADC Acquisition Time

- n = 12 bits
- R_{on} = 500 Ω
- C_h = 12.5 pF
- C_p = 12.7 pF
- Target settling error = 1/2 LSBs
- R_s = 180 Ω
- C_s = 150pF

$$T = \left(180\ \Omega + 500\ \Omega\right)12.5\ pF + 180\ \Omega\left(150\ pF + 12.7\ pF\right) = 37.8\ ns$$

$$k = \ln\left(\frac{4069\ LSBs}{0.5\ LSBs}\right) - \ln\left(\frac{\left(150\ pF + 12.7\ pF\right)}{12.5\ pF}\right) = 6.4\ time\ constants$$

$$acquisition\ time = 37.8\ ns \times 6.4 = 242\ ns$$

(2)

5 Summary

Input settling is an important design consideration for ADC driving circuits. Without proper evaluation, distortion and memory cross-talk errors could occur, resulting in degraded sensing performance and accuracy.

By using the excellent resources provided by in the TI Precision Labs - SAR ADC Input Driver Design video series, the Analog Engineer's Calculator, and the guidance in this application report, input settling can be systematically evaluated to ensure that ADC driving circuits have appropriate settling performance.

6 References

- TI Precision Labs - SAR ADC Input Driver Design
- Analog Engineer's Calculator
- TINA-TI
- PSPICE-FOR-TI
- Texas Instruments: *ADC Input Circuit Evaluation for C2000 MCUs (using TINA-TI simulation tool)*
- Texas Instruments: *Charge-Sharing Driving Circuits for C2000 ADCs (using TINA-TI simulation tool)*
- Texas Instruments: *Charge-Sharing Driving Circuits for C2000 ADCs (using PSPICE-FOR-TI)*
- Texas Instruments: *Methods for Mitigating ADC Memory Cross-Talk*
- Texas Instruments: *TMS320F28004x Microcontrollers Data Manual*

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