Application Note

Jacinto 7 Thermal Management Guide - Software Strategies

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ABSTRACT

This application report discusses the software strategies for TDA4VM/J721E/DRA829, DRA821 and other Jacinto 7 SoCs.

The relevant instructions are covered using the Linux SDK, the same concepts can be applied to other operating systems as well.

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Trademarks

1 Introduction

This application report is applicable for J7ES/TDA4VM and derivatives. Before reading further, it is important to highlight the difference between TDA4 Silicon Revision 1.1 and 1.0 with regard to thermal sensors:

It is recommended to use Silicon Revision 1.1 for further experiments, however if for some reason you need to use Silicon Revision 1.0, be aware of the Errata i2128 — "VTM: VTM Temperature Monitors (TEMPSENSORs) should Use a Software Trimming Method", details can be found in *J721E DRA829/TDA4VM Processors Silicon Revision 1.1/1.0*. Based on the silicon revisions the method employed to read on-die temperatures differ.

Note

For comparison, the Jacinto 6 devices such TDA2/DRA7 support thermal management from Linux with the (including Dynamic Voltage Frequency Scaling (DVFS)) through "cpufreq" feature. When SoC temperature goes beyond a programmable threshold the Linux thermal framework employs the registered cooling agents to control the heat. On Jacinto 6, the thermal framework employs "cpufreq" to reduce the OPP (lower voltage and frequency). Since J7 supports a single OPP, software can lower the frequency and keeping the voltage at the same level.

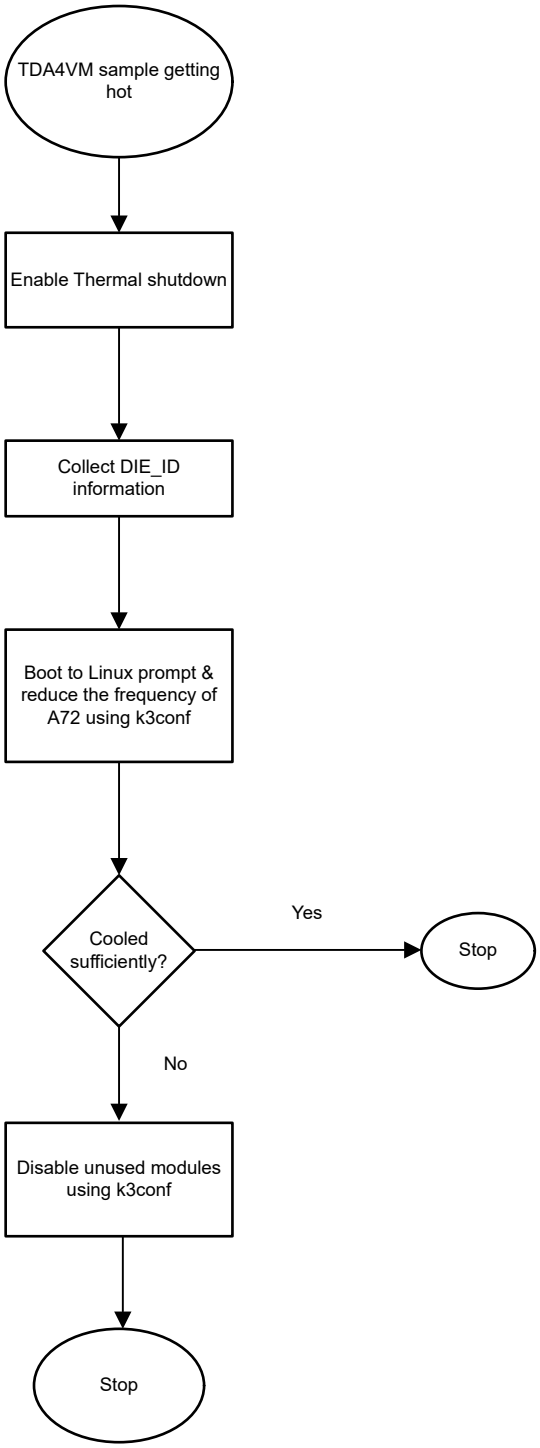

Figure 1-1. TDA4VM Cooling Strategies

Note

Customer needs to ensure that post A72 frequency reduction the system meets the expected use case performance. SDK tries to maximize performance and silicon entitlement. Customer needs to cut down unwanted resources by following the example. This in turn will help the thermal cause.

DIE ID is useful to get the device-specific details, this is used by TI for further analysis. This is one of the first bits of information that need to be collected. Use the following commands from Linux command line to read the DIE ID Registers:

```
echo `devmem2 0x43000020 w | tail -n1`
echo `devmem2 0x43000024 w | tail -n1`
echo `devmem2 0x43000028 w | tail -n1`
echo `devmem2 0x4300002c w | tail -n1`
```

Note

The same register read operation can be performed with CCS or Lauterbach.

Note

How to check if reboot happened because of Thermal Shutdown (TSHUT).

CTRLMMR_WKUP_RESET_SRC_STAT Register For Cold boot, the value of this register is 0x0 (1st fresh boot). In the event of TSHUT, then the next boot in Linux:

```
devmem2 0x43000050 w
Read at address  0x43000050 (0xffff86750050): 0x01000000
```

So bit24 is set corresponding to THERMAL_RST indicating the reset due to TSHUT.

2 Enabling Thermal Shutdown Mandatory Step

This kicks in at the very end when temperature is close to max thresholds of the SoC.

This needs one time register programming to be done. Below is the complete programming sequence that can be done from the Linux user space in absence of thermal driver:

1. WKUP_VTM_MISC_CTRL2[25-16] MAXT_OUTRG_ALERT_THR0 and WKUP_VTM_MISC_CTRL2[9-0] MAXT_OUTRG_ALERT_THR thresholds.

Note

Setting 0x305 (decimal 773) that maps to 125°C as the TSHUT alert threshold and 0x2e6 (decimal 742) which maps to 120°C. This is the default recommendation for TSHUT.

```
devmem2 0x42050010 w 0x2e60305
```


Table 5-1896. Temperature Translation Table

Parameter Type	Value								
Temperature [°C] (rounded)	-40	-25	0	25	50	75	100	125	150
Temperature [°C] (unrounded)	-40.03	-24.95	0.01	25.02	49.94	75.03	100.02	124.97	150.00
DATA_OUT Code	28	77	164	260	366	485	620	773	949

Table 5-1897 shows a table that gives coefficients of polynomial to calculate code or temperture. The equation to calculate code or temperature is:

$y = a4 \times x^4 + a3 \times x^3 + a2 \times x^2 + a1 \times x + a0$

Table 5-1897. Equation Method to Calculate Code or Temperature

Function	Unit	Coefficient				
		a4	a3	a2	a1	a0
Code = f(Temperature)	Decimal value of code	4.9847E-08	1.6972E-05	6.8759E-03	3.6509E+00	1.6407E+02
Temperature = f(Code)	°C	-9.2627E-12	6.0373E-08	-1.7058E-04	3.2512E-01	-4.9002E+01

Figure 2-1. Temperature Translation Table

The above table gives ADC code Vs Temperature in centigrade for few temperatures. In case other temperatures are needed, use Table 5-1897 equation to get the alert threshold values for a particular temperature.

For more information, see the *Temperature Translation* table in the *DRA829/TDA4VM/AM752x Technical Reference Manual*

Please use Silicon Revision 1.1 since Silicon Revision 1.0 has PVT sensor accuracy issue and the shutdown might happen at an offset of ± 20C.

2. WKUP_VTM_TMPSENS_CTRL_j[11] MAXT_OUTRG_EN = 1.

   Enable the individual sensors maxtemp_alert bit (Note: bit 4 (CONT) and bit 6 (CLRZ) are already set so keeping them set):

```
devmem2 0x42050300 w 0x850
devmem2 0x42050320 w 0x850
devmem2 0x42050340 w 0x850
devmem2 0x42050360 w 0x850
devmem2 0x42050380 w 0x850
```

3. WKUP_VTM_MISC_CTRL[0] ANYMAXT_OUTRG_ALERT_EN to 1.

   The global max temp alert generation bit to 1.

```
devmem2 0x4205000c w 0x1
```

3 Thermal Mitigation Strategies at a High Level

3.1 Strategy 1: Auditing the Power Domains That Contribute to the Highest Power Consumption

Key Power domains that contribute significantly are captured in Table 3-1. (These are the highest power consuming domains and they are not in any order).

Table 3-1. Power Domain Vs Module Mapping

Power Domain	Module
PD_MCU_R5FF0FSS	MCU_R5FSS
PD_C71X0	MMA & C71SS
PD_A72_CLUSTER0	A72SS
PD_A72_0	A72_CORE0
PD_A72_1	A72_CORE1
PD_GPUCOM	GPU
PD_CPUCORE	
PD_C66x_0	C66SS_0
PD_C66x_1	C66SS_0
PD_R5FSS_0	R5FSS_0
PD_R5SS_1	R5FSS_1
PD_DECODE	D5520MPx
PD_ENCODE	VXE384MP2
PD_DMPAC	DMPAC
PD_VPAC	VPAC

- A. *Shell script to get the status of the top power consuming power domains*

```
k3conf dump device > devdump
cat devdump | grep -E ' 202 | 203 | 124 | 140 |  4 | 16 | 140 | 141 | 243 | 244 | 48 | 290 | 144
| 153 | 249 '
```

A complete list of Device IDs can be looked up here:

Sample output:

```
root@j7-evm:~# ./high-power-pd.sh
| 4 | J721E_DEV_A72SS0 | DEVICE_STATE_ON |
| 16 | J721E_DEV_C71SS0_MMA | DEVICE_STATE_ON |
| 48 | J721E_DEV_DMPAC0 | DEVICE_STATE_OFF |
| 124 | J721E_DEV_GPU0 | DEVICE_STATE_ON |
| 140 | J721E_DEV_C66SS0 | DEVICE_STATE_ON |
| 141 | J721E_DEV_C66SS1 | DEVICE_STATE_ON |
| 144 | J721E_DEV_DECODER0 | DEVICE_STATE_OFF |
| 153 | J721E_DEV_ENCODER0 | DEVICE_STATE_OFF |
| 202 | J721E_DEV_A72SS0_CORE0 | DEVICE_STATE_ON |
| 203 | J721E_DEV_A72SS0_CORE1 | DEVICE_STATE_ON |
| 243 | J721E_DEV_R5FSS0 | DEVICE_STATE_ON |
| 244 | J721E_DEV_R5FSS1 | DEVICE_STATE_ON |
| 249 | J721E_DEV_MCU_R5FSS0 | DEVICE_STATE_ON |
| 290 | J721E_DEV_VPAC0 | DEVICE_STATE_OFF |
root@j7-evm:~#
```

- B. *Statically configuring the A72 core to start at 1 GHz*

```
Index: u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/mach-k3/j721e_init.c
===================================================================
--- u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33.orig/arch/arm/mach-k3/j721e_init.c
+++ u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/mach-k3/j721e_init.c
@@ -378,6 +378,10 @@ void board_init_f(ulong dummy)
     if (ret)
         panic("DRAM init failed: %d\n", ret);
 #endif
+#ifdef CONFIG_ARM64
+       int tmp;
+       tmp = set_a72_clk_frequency(1000000000);
+#endif
 }

 u32 spl_boot_mode(const u32 boot_device)
@@ -573,3 +577,26 @@ err_load:
     rproc_reset(2);
 }
 #endif
+
+#ifdef CONFIG_ARM64
+int set_a72_clk_frequency(u64 freq) {
+       struct ti_sci_handle *ti_sci;
+       struct ti_sci_clk_ops *clk_ops;
+       int ret = 0;
+
+       writel(0x80000001, 0x688040);
+       printf("The value of PLL8_SS_CTRL register 0x%x\n", readl(0x688040));
+       ti_sci = get_ti_sci_handle();
+       clk_ops = &ti_sci->ops.clk_ops;
+
+       ret = clk_ops->set_freq(ti_sci, 202, 2, 100000000, freq, 2000000000);
+       if (ret) {
+               printk("failed to set the frequency %d\n", ret);
+               return ret;
+       }
+
+       printk("Successfully set the clock frequency to %lld\n", freq);
+
+    return 0;
+}
+#endif
```

3.2 Strategy 2: Disable Loading of Remote Core Firmware

A simple way to disable remote cores (prevent from running) is by renaming their respective firmware:

```
sudo mv /media/$user/rootfs/lib/firmware/pdk-ipc/ipc_echo_test_c66xdsp_*_release_strip.xe66 /media/
$user/rootfs/lib/firmware/pdk-ipc/ipc_echo_test_c66xdsp_*_release_strip.xe66_bk
sync
reboot
```

To check if the above action has taken effect, run the k3conf commands, device 142 corresponds to DSP. A complete list of Device IDs can be looked up here:

```
root@j7-evm:~# k3conf dump device 142
142  J721E_DEV_C66SS0_CORE0 DEVICE_STATE_OFF

root@j7-evm:~# k3conf dump device 143
143 J721E_DEV_C66SS1_CORE0 DEVICE_STATE_OFF
```

3.3 Strategy 3: Disabling Modules on TDA4

This is a bit more involved due to multiple clients sending requests to the device manager to enable a particular module.

It could be R5 SPL, A72 SPL, A72 U-boot, Linux and remote core firmware. A careful audit of where the modules are enabled should be done. When we are using PSDKLA we need to remove the device tree nodes both from U-boot DTS and Linux Kernel DTS.

A careful audit of device manager debug logs is necessary to see if a module is explicitly turned on by any of the software entity.

DM built in with debug enabled can be used to get debug logs to analyze

3.3.1 Example: Disabling PCIe Instances on 7.3

Original state of PCIe instances on 7.3:

```
root@j7-evm:~# k3conf dump device 239
|-----------------------------------------------|
| Device ID | Device Name     | Device Status   |
|-----------------------------------------------|
|   239     | J721E_DEV_PCIE0 | DEVICE_STATE_ON |
|-----------------------------------------------|

root@j7-evm:~# k3conf dump device 240
|-----------------------------------------------|
| Device ID | Device Name     | Device Status   |
|-----------------------------------------------|
|   240     | J721E_DEV_PCIE1 | DEVICE_STATE_ON |
|-----------------------------------------------|

root@j7-evm:~# k3conf dump device 241
|-----------------------------------------------|
| Device ID | Device Name     | Device Status   |
|-----------------------------------------------|
|   241     | J721E_DEV_PCIE2 | DEVICE_STATE_ON |
|-----------------------------------------------|

root@j7-evm:~# k3conf dump device 242
|-----------------------------------------------|
| Device ID | Device Name     | Device Status   |
|-----------------------------------------------|
|   242     | J721E_DEV_PCIE3 | DEVICE_STATE_ON |
|-----------------------------------------------|
```

All of them are enabled in Linux. The Linux DTS patch needs to be disabled on all the PCIe instances:

```
diff --git a/arch/arm64/boot/dts/ti/k3-j721e-common-proc-board.dts b/arch/arm64/boot/dts/ti/k3-
j721e-common-proc-board.dts
index 0fee2285a..4744053f4 100644
--- a/arch/arm64/boot/dts/ti/k3-j721e-common-proc-board.dts
+++ b/arch/arm64/boot/dts/ti/k3-j721e-common-proc-board.dts
@@ -957,56 +957,6 @@
        };
 };

-&pcie0_rc {
-       reset-gpios = <&exp1 6 GPIO_ACTIVE_HIGH>;
-       phys = <&serdes0_pcie_link>;
-       phy-names = "pcie_phy";
-       num-lanes = <1>;
-};
-
-&pcie1_rc {
-       reset-gpios = <&exp1 2 GPIO_ACTIVE_HIGH>;
-       phys = <&serdes1_pcie_link>;
-       phy-names = "pcie_phy";
-       num-lanes = <2>;
-};
-
-&pcie2_rc {
-       reset-gpios = <&exp2 20 GPIO_ACTIVE_HIGH>;
-       phys = <&serdes2_pcie_link>;
-       phy-names = "pcie_phy";
-       num-lanes = <2>;
-};
-
-&pcie0_ep {
-       phys = <&serdes0_pcie_link>;
-       phy-names = "pcie_phy";
-       num-lanes = <1>;
-       status = "disabled";
-};
-
-&pcie1_ep {
-       phys = <&serdes1_pcie_link>;
-       phy-names = "pcie_phy";
-       num-lanes = <2>;
-       status = "disabled";
-};
-
-&pcie2_ep {
-       phys = <&serdes2_pcie_link>;
-       phy-names = "pcie_phy";
-       num-lanes = <2>;
-       status = "disabled";
-};
-
-&pcie3_rc {
-       status = "disabled";
-};
-
-&pcie3_ep {
-       status = "disabled";
-};
-
 &usb_serdes_mux {
        idle-states = <1>, <0>; /* USB0 to SERDES3, USB1 to SERDES1 */
 };
diff --git a/arch/arm64/boot/dts/ti/k3-j721e-main.dtsi b/arch/arm64/boot/dts/ti/k3-j721e-main.dtsi
index 2f756a048..11fea9d36 100644
--- a/arch/arm64/boot/dts/ti/k3-j721e-main.dtsi
+++ b/arch/arm64/boot/dts/ti/k3-j721e-main.dtsi
@@ -649,243 +649,6 @@
                };
        };

-       pcie0_rc: pcie@2900000 {
-               compatible = "ti,j721e-pcie-host";
-               reg = <0x00 0x02900000 0x00 0x1000>,
-                     <0x00 0x02907000 0x00 0x400>,
-                     <0x00 0x0d000000 0x00 0x00800000>,
-                     <0x00 0x10000000 0x00 0x00001000>;
-               reg-names = "intd_cfg", "user_cfg", "reg", "cfg";
```

```
-               ti,syscon-pcie-ctrl = <&pcie0_ctrl>;
-               max-link-speed = <3>;
-               num-lanes = <2>;
-               power-domains = <&k3_pds 239 TI_SCI_PD_EXCLUSIVE>;
-               clocks = <&k3_clks 239 1>;
-               clock-names = "fck";
-               #address-cells = <3>;
-               #size-cells = <2>;
-               bus-range = <0x0 0xf>;
-               cdns,max-outbound-regions = <32>;
-               cdns,no-bar-match-nbits = <64>;
-               vendor-id = /bits/ 16 <0x104c>;
-               device-id = /bits/ 16 <0xb00d>;
-               msi-map = <0x0 &gic_its 0x0 0x10000>;
-               dma-coherent;
-               ranges = <0x01000000 0x0 0x10001000  0x00 0x10001000  0x0 0x0010000>,
-                        <0x02000000 0x0 0x10011000  0x00 0x10011000  0x0 0x7fef000>;
-               #interrupt-cells = <1>;
-               interrupt-map-mask = <0 0 0 7>;
-               interrupt-map = <0 0 0 1 &pcie0_intc 0>, /* INT A */
-                               <0 0 0 2 &pcie0_intc 0>, /* INT B */
-                               <0 0 0 3 &pcie0_intc 0>, /* INT C */
-                               <0 0 0 4 &pcie0_intc 0>; /* INT D */
-
-               pcie0_intc: legacy-interrupt-controller {
-                       interrupt-controller;
-                       #interrupt-cells = <1>;
-                       interrupt-parent = <&gic500>;
-                       interrupts = <GIC_SPI 312 IRQ_TYPE_EDGE_RISING>;
-               };
-       };
-
-       pcie0_ep: pcie-ep@2900000 {
-               compatible = "ti,j721e-pcie-ep";
-               reg = <0x00 0x02900000 0x00 0x1000>,
-                     <0x00 0x02907000 0x00 0x400>,
-                     <0x00 0x0d000000 0x00 0x00800000>,
-                     <0x00 0x10000000 0x00 0x08000000>;
-               reg-names = "intd_cfg", "user_cfg", "reg", "mem";
-               ti,syscon-pcie-ctrl = <&pcie0_ctrl>;
-               max-link-speed = <3>;
-               num-lanes = <2>;
-               power-domains = <&k3_pds 239 TI_SCI_PD_EXCLUSIVE>;
-               clocks = <&k3_clks 239 1>;
-               clock-names = "fck";
-               cdns,max-outbound-regions = <32>;
-               max-functions = /bits/ 8 <6>;
-               max-virtual-functions = /bits/ 16 <4 4 4 4 0 0>;
-               dma-coherent;
-               #address-cells = <2>;
-               #size-cells = <2>;
-               ranges;
-       };
-
-       pcie1_rc: pcie@2910000 {
-               compatible = "ti,j721e-pcie-host";
-               reg = <0x00 0x02910000 0x00 0x1000>,
-                     <0x00 0x02917000 0x00 0x400>,
-                     <0x00 0x0d800000 0x00 0x00800000>,
-                     <0x00 0x18000000 0x00 0x00001000>;
-               reg-names = "intd_cfg", "user_cfg", "reg", "cfg";
-               ti,syscon-pcie-ctrl = <&pcie1_ctrl>;
-               max-link-speed = <3>;
-               num-lanes = <2>;
-               power-domains = <&k3_pds 240 TI_SCI_PD_EXCLUSIVE>;
-               clocks = <&k3_clks 240 1>;
-               clock-names = "fck";
-               #address-cells = <3>;
-               #size-cells = <2>;
-               bus-range = <0x0 0xf>;
-               cdns,max-outbound-regions = <32>;
-               cdns,no-bar-match-nbits = <64>;
-               vendor-id = /bits/ 16 <0x104c>;
-               device-id = /bits/ 16 <0xb00d>;
-               msi-map = <0x0 &gic_its 0x10000 0x10000>;
-               dma-coherent;
-               ranges = <0x01000000 0x0 0x18001000  0x00 0x18001000  0x0 0x0010000>,
-                        <0x02000000 0x0 0x18011000  0x00 0x18011000  0x0 0x7fef000>;
-               #interrupt-cells = <1>;
```

```
-               interrupt-map-mask = <0 0 0 7>;
-               interrupt-map = <0 0 0 1 &pcie1_intc 0>, /* INT A */
-                               <0 0 0 2 &pcie1_intc 0>, /* INT B */
-                               <0 0 0 3 &pcie1_intc 0>, /* INT C */
-                               <0 0 0 4 &pcie1_intc 0>; /* INT D */
-
-               pcie1_intc: legacy-interrupt-controller {
-                       interrupt-controller;
-                       #interrupt-cells = <2>;
-                       interrupt-parent = <&gic500>;
-                       interrupts = <GIC_SPI 324 IRQ_TYPE_EDGE_RISING>;
-               };
-       };
-
-       pcie1_ep: pcie-ep@2910000 {
-               compatible = "ti,j721e-pcie-ep";
-               reg = <0x00 0x02910000 0x00 0x1000>,
-                     <0x00 0x02917000 0x00 0x400>,
-                     <0x00 0x0d800000 0x00 0x00800000>,
-                     <0x00 0x18000000 0x00 0x08000000>;
-               reg-names = "intd_cfg", "user_cfg", "reg", "mem";
-               ti,syscon-pcie-ctrl = <&pcie1_ctrl>;
-               max-link-speed = <3>;
-               num-lanes = <2>;
-               power-domains = <&k3_pds 240 TI_SCI_PD_EXCLUSIVE>;
-               clocks = <&k3_clks 240 1>;
-               clock-names = "fck";
-               cdns,max-outbound-regions = <32>;
-               max-functions = /bits/ 8 <6>;
-               max-virtual-functions = /bits/ 16 <4 4 4 4 0 0>;
-               dma-coherent;
-       };
-
-       pcie2_rc: pcie@2920000 {
-               compatible = "ti,j721e-pcie-host";
-               reg = <0x00 0x02920000 0x00 0x1000>,
-                     <0x00 0x02927000 0x00 0x400>,
-                     <0x00 0x0e000000 0x00 0x00800000>,
-                     <0x44 0x00000000 0x00 0x00001000>;
-               reg-names = "intd_cfg", "user_cfg", "reg", "cfg";
-               ti,syscon-pcie-ctrl = <&pcie2_ctrl>;
-               max-link-speed = <3>;
-               num-lanes = <2>;
-               power-domains = <&k3_pds 241 TI_SCI_PD_EXCLUSIVE>;
-               clocks = <&k3_clks 241 1>;
-               clock-names = "fck";
-               #address-cells = <3>;
-               #size-cells = <2>;
-               bus-range = <0x0 0xf>;
-               cdns,max-outbound-regions = <32>;
-               cdns,no-bar-match-nbits = <64>;
-               vendor-id = /bits/ 16 <0x104c>;
-               device-id = /bits/ 16 <0xb00d>;
-               msi-map = <0x0 &gic_its 0x20000 0x10000>;
-               dma-coherent;
-               ranges = <0x01000000 0x00 0x00001000  0x44 0x00001000  0x0 0x0010000>,
-                        <0x02000000 0x00 0x00011000  0x44 0x00011000  0x0 0x7fef000>;
-               #interrupt-cells = <1>;
-               interrupt-map-mask = <0 0 0 7>;
-               interrupt-map = <0 0 0 1 &pcie2_intc 0>, /* INT A */
-                               <0 0 0 2 &pcie2_intc 0>, /* INT B */
-                               <0 0 0 3 &pcie2_intc 0>, /* INT C */
-                               <0 0 0 4 &pcie2_intc 0>; /* INT D */
-
-               pcie2_intc: legacy-interrupt-controller {
-                       interrupt-controller;
-                       #interrupt-cells = <2>;
-                       interrupt-parent = <&gic500>;
-                       interrupts = <GIC_SPI 336 IRQ_TYPE_EDGE_RISING>;
-               };
-       };
-
-       pcie2_ep: pcie-ep@2920000 {
-               compatible = "ti,j721e-pcie-ep";
-               reg = <0x00 0x02920000 0x00 0x1000>,
-                     <0x00 0x02927000 0x00 0x400>,
-                     <0x00 0x0e000000 0x00 0x00800000>,
-                     <0x44 0x00000000 0x00 0x08000000>;
-               reg-names = "intd_cfg", "user_cfg", "reg", "mem";
```

```
-               ti,syscon-pcie-ctrl = <&pcie2_ctrl>;
-               max-link-speed = <3>;
-               num-lanes = <2>;
-               power-domains = <&k3_pds 241 TI_SCI_PD_EXCLUSIVE>;
-               clocks = <&k3_clks 241 1>;
-               clock-names = "fck";
-               cdns,max-outbound-regions = <32>;
-               max-functions = /bits/ 8 <6>;
-               max-virtual-functions = /bits/ 16 <4 4 4 4 0 0>;
-               dma-coherent;
-       };
-
-       pcie3_rc: pcie@2930000 {
-               compatible = "ti,j721e-pcie-host";
-               reg = <0x00 0x02930000 0x00 0x1000>,
-                     <0x00 0x02937000 0x00 0x400>,
-                     <0x00 0x0e800000 0x00 0x00800000>,
-                     <0x44 0x10000000 0x00 0x00001000>;
-               reg-names = "intd_cfg", "user_cfg", "reg", "cfg";
-               ti,syscon-pcie-ctrl = <&pcie3_ctrl>;
-               max-link-speed = <3>;
-               num-lanes = <2>;
-               power-domains = <&k3_pds 242 TI_SCI_PD_EXCLUSIVE>;
-               clocks = <&k3_clks 242 1>;
-               clock-names = "fck";
-               #address-cells = <3>;
-               #size-cells = <2>;
-               bus-range = <0x0 0xf>;
-               cdns,max-outbound-regions = <32>;
-               cdns,no-bar-match-nbits = <64>;
-               vendor-id = /bits/ 16 <0x104c>;
-               device-id = /bits/ 16 <0xb00d>;
-               msi-map = <0x0 &gic_its 0x30000 0x10000>;
-               dma-coherent;
-               ranges = <0x01000000 0x00 0x00001000  0x44 0x10001000  0x0 0x0010000>,
-                        <0x02000000 0x00 0x00011000  0x44 0x10011000  0x0 0x7fef000>;
-               #interrupt-cells = <1>;
-               interrupt-map-mask = <0 0 0 7>;
-               interrupt-map = <0 0 0 1 &pcie3_intc 0>, /* INT A */
-                               <0 0 0 2 &pcie3_intc 0>, /* INT B */
-                               <0 0 0 3 &pcie3_intc 0>, /* INT C */
-                               <0 0 0 4 &pcie3_intc 0>; /* INT D */
-
-               pcie3_intc: legacy-interrupt-controller {
-                       interrupt-controller;
-                       #interrupt-cells = <2>;
-                       interrupt-parent = <&gic500>;
-                       interrupts = <GIC_SPI 348 IRQ_TYPE_EDGE_RISING>;
-               };
-       };
-
-       pcie3_ep: pcie-ep@2930000 {
-               compatible = "ti,j721e-pcie-ep";
-               reg = <0x00 0x02930000 0x00 0x1000>,
-                     <0x00 0x02937000 0x00 0x400>,
-                     <0x00 0x0e800000 0x00 0x00800000>,
-                     <0x44 0x10000000 0x00 0x08000000>;
-               reg-names = "intd_cfg", "user_cfg", "reg", "mem";
-               ti,syscon-pcie-ctrl = <&pcie3_ctrl>;
-               max-link-speed = <3>;
-               num-lanes = <2>;
-               power-domains = <&k3_pds 242 TI_SCI_PD_EXCLUSIVE>;
-               clocks = <&k3_clks 242 1>;
-               clock-names = "fck";
-               cdns,max-outbound-regions = <32>;
-               max-functions = /bits/ 8 <6>;
-               max-virtual-functions = /bits/ 16 <4 4 4 4 0 0>;
-               dma-coherent;
-               #address-cells = <2>;
-               #size-cells = <2>;
-       };
-
-       serdes_wiz4: wiz@5050000 {
-               compatible = "ti,j721e-wiz-10g";
```

After the above diff patch is applied on Linux dts, the dtb is recompiled and copied over to the SD Card:

To check if the above action has taken effect, run the k3conf commands:

```
k3conf dump device 'x'
```

replace x with the device ID to be checked.

Sample output for various PCIe devices:

```
root@j7-evm:~# k3conf dump device 239
 |-----------------------------------------------|
 | Device ID | Device Name     | Device Status    |
 |-----------------------------------------------|
 |   239     | J721E_DEV_PCIE0 | DEVICE_STATE_OFF |
 |-----------------------------------------------|

 root@j7-evm:~# k3conf dump device 240
 |-----------------------------------------------|
 | Device ID | Device Name     | Device Status    |
 |-----------------------------------------------|
 |   240     | J721E_DEV_PCIE1 | DEVICE_STATE_OFF |
 |-----------------------------------------------|

 root@j7-evm:~# k3conf dump device 241
 |-----------------------------------------------|
 | Device ID | Device Name     | Device Status    |
 |-----------------------------------------------|
 |   241     | J721E_DEV_PCIE2 | DEVICE_STATE_OFF |
 |-----------------------------------------------|

 root@j7-evm:~# k3conf dump device 242
 |-----------------------------------------------|
 | Device ID | Device Name     | Device Status    |
 |-----------------------------------------------|
 |   242     | J721E_DEV_PCIE3 | DEVICE_STATE_OFF |
 |-----------------------------------------------|
```

Modules that are enabled at u-boot need to be disabled at u-boot device tree. Sample patch for disabling modules at u-boot is here: .

```
From bc56b43cd2ebfd8423a815016d78d0f02cedc58d Mon Sep 17 00:00:00 2001
From: Keerthy <j-keerthy@ti.com>
Date: Thu, 21 Jan 2021 14:09:39 +0530
Subject: [PATCH] arm: dts: k3-j721e: Remove unused nodes

Remove unused nodes

Signed-off-by: Keerthy <j-keerthy@ti.com>
---
 .../k3-j721e-common-proc-board-u-boot.dtsi    |  10 --
 arch/arm/dts/k3-j721e-common-proc-board.dts   |  26 ----
 arch/arm/dts/k3-j721e-main.dtsi               | 132 ------------------
 .../arm/dts/k3-j721e-r5-common-proc-board.dts |  11 --
 arch/arm/dts/k3-j721e-tps65917-proc-board.dts |   8 --
 5 files changed, 187 deletions(-)

Index: u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/dts/k3-j721e-common-proc-board-u-
boot.dtsi
===================================================================
--- u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33.orig/arch/arm/dts/k3-j721e-common-proc-board-u-
boot.dtsi
+++ u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/dts/k3-j721e-common-proc-board-u-
boot.dtsi
@@ -146,16 +146,6 @@
     u-boot,dm-spl;
 };

-&usbss0 {
-    u-boot,dm-spl;
-    ti,usb2-only;
-};
-
-&usb0 {
-    dr_mode = "peripheral";
-    u-boot,dm-spl;
-};
-
```

```
 &mcu_cpsw {
     pinctrl-names = "default";
     pinctrl-0 = <&mcu_cpsw_pins_default &mcu_mdio_pins_default>;
Index: u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/dts/k3-j721e-common-proc-board.dts
===================================================================
--- u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33.orig/arch/arm/dts/k3-j721e-common-proc-
board.dts
+++ u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/dts/k3-j721e-common-proc-board.dts
@@ -19,8 +19,6 @@
         remoteproc1 = &mcu_r5fss0_core1;
         remoteproc2 = &main_r5fss0_core0;
         remoteproc3 = &main_r5fss0_core1;
-        remoteproc4 = &main_r5fss1_core0;
-        remoteproc5 = &main_r5fss1_core1;
         remoteproc6 = &c66_0;
         remoteproc7 = &c66_1;
         remoteproc8 = &c71_0;
@@ -216,30 +214,6 @@
     clock-frequency = <400000>;
 };

-&usbss0 {
-    pinctrl-names = "default";
-    pinctrl-0 = <&main_usbss0_pins_default>;
-    ti,vbus-divider;
-};
-
-&usb0 {
-    dr_mode = "otg";
-    maximum-speed = "super-speed";
-    phys = <&serdes3_usb_link>;
-    phy-names = "cdns3,usb3-phy";
-};
-
-&usbss1 {
-    pinctrl-names = "default";
-    pinctrl-0 = <&main_usbss1_pins_default>;
-    ti,usb2-only;
-};
-
-&usb1 {
-    dr_mode = "host";
-    maximum-speed = "high-speed";
-};
-
 &main_i2c0 {
     pinctrl-names = "default";
     pinctrl-0 = <&main_i2c0_pins_default>;
Index: u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/dts/k3-j721e-main.dtsi
===================================================================
--- u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33.orig/arch/arm/dts/k3-j721e-main.dtsi
+++ u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/dts/k3-j721e-main.dtsi
@@ -434,44 +434,6 @@
         };
     };

-    main_r5fss1: r5fss@5e00000 {
-        compatible = "ti,j721e-r5fss";
-        lockstep-mode = <0>;
-        #address-cells = <1>;
-        #size-cells = <1>;
-        ranges = <0x5e00000 0x00 0x5e00000 0x20000>,
-             <0x5f00000 0x00 0x5f00000 0x20000>;
-        power-domains = <&k3_pds 244 TI_SCI_PD_EXCLUSIVE>;
-
-        main_r5fss1_core0: r5f@5e00000 {
-            compatible = "ti,j721e-r5f";
-            reg = <0x5e00000 0x00008000>,
-                  <0x5e10000 0x00008000>;
-            reg-names = "atcm", "btcm";
-            ti,sci = <&dmsc>;
-            ti,sci-dev-id = <247>;
-            ti,sci-proc-ids = <0x08 0xFF>;
-            resets = <&k3_reset 247 1>;
-            atcm-enable = <1>;
-            btcm-enable = <1>;
-            loczrama = <1>;
-        };
-
```

```
-        main_r5fss1_core1: r5f@5f00000 {
-            compatible = "ti,j721e-r5f";
-            reg = <0x5f00000 0x00008000>,
-                  <0x5f10000 0x00008000>;
-            reg-names = "atcm", "btcm";
-            ti,sci = <&dmsc>;
-            ti,sci-dev-id = <248>;
-            ti,sci-proc-ids = <0x09 0xFF>;
-            resets = <&k3_reset 248 1>;
-            atcm-enable = <1>;
-            btcm-enable = <1>;
-            loczrama = <1>;
-        };
-    };
-
     c66_0: dsp@4d80800000 {
         compatible = "ti,j721e-c66-dsp";
         reg = <0x4d 0x80800000 0x00 0x00048000>,
@@ -507,100 +469,6 @@
         resets = <&k3_reset 15 1>;
     };

-    usbss0: cdns_usb@4104000 {
-        compatible = "ti,j721e-usb";
-        reg = <0x00 0x4104000 0x00 0x100>;
-        dma-coherent;
-        power-domains = <&k3_pds 288 TI_SCI_PD_EXCLUSIVE>;
-        clocks = <&k3_clks 288 15>, <&k3_clks 288 3>;
-        clock-names = "usb2_refclk", "lpm_clk";
-        assigned-clocks = <&k3_clks 288 15>;    /* USB2_REFCLK */
-        assigned-clock-parents = <&k3_clks 288 16>; /* HFOSC0 */
-        #address-cells = <2>;
-        #size-cells = <2>;
-        ranges;
-
-        phy@4108000 {
-            compatible = "ti,j721e-usb2-phy";
-            reg = <0x00 0x4108000 0x00 0x400>;
-        };
-
-        usb0: usb@6000000 {
-            compatible = "cdns,usb3";
-            reg = <0x00 0x6000000 0x00 0x10000>,
-                  <0x00 0x6010000 0x00 0x10000>,
-                  <0x00 0x6020000 0x00 0x10000>;
-            reg-names = "otg", "xhci", "dev";
-            interrupts = <GIC_SPI 96 IRQ_TYPE_LEVEL_HIGH>,    /* irq.0 */
-                         <GIC_SPI 102 IRQ_TYPE_LEVEL_HIGH>,    /* irq.6 */
-                         <GIC_SPI 120 IRQ_TYPE_LEVEL_HIGH>;    /* otgirq.0 */
-            interrupt-names = "host",
-                              "peripheral",
-                              "otg";
-            maximum-speed = "super-speed";
-            dr_mode = "otg";
-        };
-    };
-
-    usbss1: cdns_usb@4114000 {
-        compatible = "ti,j721e-usb";
-        reg = <0x00 0x4114000 0x00 0x100>;
-        dma-coherent;
-        power-domains = <&k3_pds 289 TI_SCI_PD_EXCLUSIVE>;
-        clocks = <&k3_clks 289 15>, <&k3_clks 289 3>;
-        clock-names = "usb2_refclk", "lpm_clk";
-        assigned-clocks = <&k3_clks 289 15>;    /* USB2_REFCLK */
-        assigned-clock-parents = <&k3_clks 289 16>; /* HFOSC0 */
-        #address-cells = <2>;
-        #size-cells = <2>;
-        ranges;
-
-        phy@4118000 {
-            compatible = "ti,j721e-usb2-phy";
-            reg = <0x00 0x4118000 0x00 0x400>;
-        };
-
-        usb1: usb@6400000 {
-            compatible = "cdns,usb3";
-            reg = <0x00 0x6400000 0x00 0x10000>,
-                  <0x00 0x6410000 0x00 0x10000>,
```

```
-                 <0x00 0x6420000 0x00 0x10000>;
-             reg-names = "otg", "xhci", "dev";
-             interrupts = <GIC_SPI 104 IRQ_TYPE_LEVEL_HIGH>,    /* irq.0 */
-                      <GIC_SPI 110 IRQ_TYPE_LEVEL_HIGH>,    /* irq.6 */
-                      <GIC_SPI 121 IRQ_TYPE_LEVEL_HIGH>;    /* otgirq.0 */
-             interrupt-names = "host",
-                       "peripheral",
-                       "otg";
-             maximum-speed = "super-speed";
-             dr_mode = "otg";
-         };
-     };
-
-     ufs_wrapper: ufs-wrapper@4e80000 {
-         compatible = "ti,j721e-ufs";
-         reg = <0x0 0x4e80000 0x0 0x100>;
-         power-domains = <&k3_pds 277 TI_SCI_PD_EXCLUSIVE>;
-         clocks = <&k3_clks 277 1>;
-         assigned-clocks = <&k3_clks 277 1>;
-         assigned-clock-parents = <&k3_clks 277 4>;
-         ranges;
-         #address-cells = <2>;
-         #size-cells = <2>;
-
-         ufs@4e84000 {
-             compatible = "cdns,ufshc-m31-16nm", "jedec,ufs-2.0";
-             reg = <0x0 0x4e84000 0x0 0x10000>;
-             interrupts = <GIC_SPI 17 IRQ_TYPE_LEVEL_HIGH>;
-             freq-table-hz = <0 0>, <0 0>;
-             clocks = <&k3_clks 277 0>, <&k3_clks 277 1>;
-             clock-names = "core_clk", "phy_clk";
-             assigned-clocks = <&k3_clks 277 1>;
-             assigned-clock-parents = <&k3_clks 277 4>;
-             dma-coherent;
-         };
-     };
-
      main_i2c0: i2c@2000000 {
          compatible = "ti,j721e-i2c", "ti,omap4-i2c";
          reg = <0x0 0x2000000 0x0 0x100>;
Index: u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/dts/k3-j721e-r5-common-proc-
board.dts
===================================================================
--- u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33.orig/arch/arm/dts/k3-j721e-r5-common-proc-
board.dts
+++ u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/dts/k3-j721e-r5-common-proc-board.dts
@@ -480,17 +480,6 @@
      u-boot,dm-spl;
  };

-&usbss0 {
-     /delete-property/ power-domains;
-     /delete-property/ assigned-clocks;
-     /delete-property/ assigned-clock-parents;
-     clocks = <&clk_19_2mhz>;
-     clock-names = "usb2_refclk";
-     pinctrl-names = "default";
-     pinctrl-0 = <&main_usbss0_pins_default>;
-     ti,vbus-divider;
-};
-
  &main_i2c0 {
      pinctrl-names = "default";
      pinctrl-0 = <&main_i2c0_pins_default>;
Index: u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/dts/k3-j721e-tps65917-proc-
board.dts
===================================================================
--- u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33.orig/arch/arm/dts/k3-j721e-tps65917-proc-
board.dts
+++ u-boot-2020.01+gitAUTOINC+2781231a33-g2781231a33/arch/arm/dts/k3-j721e-tps65917-proc-board.dts
@@ -118,11 +118,3 @@
  &main_sdhci1 {
      vqmmc-supply = <&ldo1_reg>;
  };
-
-&usbss0 {
-     /delete-property/ ti,usb2-only;
-};
-
```

```
-&usb0 {
-     dr_mode = "host";
-};
```

Some modules cannot be disabled using k3conf.

Example: **LPSC_PER_AUDIO** domain cannot be disabled using k3conf.

139	J721E_DEV_AASRC0
174	J721E_DEV_MCASP0
175	J721E_DEV_MCASP1

3.4 Strategy 4: Dynamic Frequency Scaling (DFS)

A simple Linux user space script that can be used to scale A72 frequency dynamically based on temperature polling. This requires additional Linux driver/DTS patches. For more information, go the E2E FAQ at this link: https://e2e.ti.com/support/processors/f/791/t/1060764.

```
 #!/bin/bash

threshold=80000
safe=79000
interval=1
ht=false
devmem2 0x688040 w 0x80000001

while :
do

t0=`cat /sys/class/thermal/thermal_zone0/temp`
t1=`cat /sys/class/thermal/thermal_zone1/temp`
t2=`cat /sys/class/thermal/thermal_zone2/temp`
t3=`cat /sys/class/thermal/thermal_zone3/temp`
t4=`cat /sys/class/thermal/thermal_zone4/temp`
echo $t0 $t1 $t2 $t3 $t4

if [ $t0 -gt $threshold ] || [ $t1 -gt $threshold ] || [ $t2 -gt $threshold ] || [ $t3 -gt
$threshold ] || [ $t4 -gt $threshold ];
then
    if [ "$ht" = false ];
    then
        echo "on die sensor temperature is higher than $threshold so reducing frequency of A72 to
1GHz"
        k3conf set clock 202  2 1000000000
        ht=true
    fi
else
    if [ "$ht" = true ] && [ $t0 -lt $safe ] && [ $t1 -lt $safe ] &&  [ $t2 -lt $safe ] && [ $t3
-lt $safe ] && [ $t4 -lt $safe ];
    then
        echo "All are under safe temp so pushing back A72 frequency to 2GHz"
        k3conf set clock 202  2 2000000000
        ht=false
    fi
fi

sleep $interval
done
```

Parameters:

- threshold=80000
- safe=79000
- interval=1

Threshold and Safe temperatures are in milli-degree centigrade, they can be adjusted accordingly. The script checks whether or not any of the 5 thermal zones are above 80°C. It also check whether or not the condition holds, then reduces A72 frequency to 1 GHz as a thermal mitigation strategy and keeps it at 1GHz until the SoC cools below 79°C, after which it re-enables the 2GHz(Top frequency).

Other method one can employ is the VTM temperature alert feature demonstrated in the RTOS SDK, CSL folder:

pdk*/packages/ti/csl/example/vtm/vtm_pvt_sensor_temp_alert/vtm_sensor_temp_alert.c

This example demonstrates how to set thermal alerts. One can implement mitigation actions upon receipt of temperature alert interrupts.

For example: Change to A72 or other core's frequency using ti_sci calls.

3.5 Strategy 5: How to Reduce Frequency of Other Cores

To set the C7x clock frequency to 500 MHz, device ID for C7x = 16 and CLK_ID = 1 use the following command on the Linux command line:

```
root@j7-evm:~# k3conf set clock 16 1 500000000

|-------------------------------------------------------------------------------------------|
| Device ID | Clock ID | Clock Name | Status | Clock Frequency |
|-------------------------------------------------------------------------------------------|
| 16 | 0 | DEV_C71SS0_MMA_PLL_CTRL_CLK | CLK_STATE_READY | 500000000 |
| 16 | 1 | DEV_C71SS0_MMA_MMA_CLK | CLK_STATE_READY | 500000000 |
```

To reduce the R5F clock frequency from 1GHZ to 500 MHz, device ID for MAIN_R5FSS0_CORE0 = 245 and CLK_ID = 0 use the following command on the Linux command line:

```
root@j7-evm:~# k3conf set clock 245 0 500000000
|-------------------------------------------------------------------------------------------------|
| Device ID | Clock ID | Clock Name | Status | Clock Frequency |
|-------------------------------------------------------------------------------------------------|
| 245 | 0 | DEV_R5FSS0_CORE0_CPU_CLK | CLK_STATE_READY | 500000000 |
| 245 | 1 | DEV_R5FSS0_CORE0_INTERFACE_CLK | CLK_STATE_READY | 500000000 |
| 245 | 2 | DEV_R5FSS0_CORE0_INTERFACE_PHASE | CLK_STATE_READY | 500000000 |
```

4 References

- Texas Instruments: *J721E DRA829/TDA4VM Processors Silicon Revision 1.1/1.0 Errata*
- Texas Instruments: *DRA829/TDA4VM/AM752x Technical Reference Manual*

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