

- SH01 - TITLE PAGE
- SH02 - NOTES
- SH03 - SoC MEM VIP CAM DIS SYS
- SH04 - SoC CNTVY
- SH05 - SoC DDR
- SH06 - SoC ANA PWR
- SH07 - SoC DIG PWR
- SH08 - DDR3 MEMORY BANK 1
- SH09 - MUX A/C QSPI/EMMC/GPMX
- SH10 - MUX B VOUT3/GPMC
- SH11 - MUX E VIN2
- SH12 - MUX H/J/K/L MCASP/VIN6A
- SH13 - MEM SPI/NAND/NOR
- SH14 - MEM eMMC/SD CARD
- SH15 - USB VBUS/CONNECTORS
- SH16 - USB-UART/JTAG
- SH17 - AIC3106
- SH18 - SERDES CLK/PCIe/MLB CONN
- SH19 - LCD/HDMI CONNECTORS
- SH20 - FPD LINK
- SH21 - CAMERA IF
- SH22 - I2C EXP/ EEPROM/TEMP
- SH23 - COM8
- SH24 - ETHERNET PORT0
- SH25 - ETHERNET PORT1
- SH26 - CAN/EXP CONNECTORS
- SH27 - POWER LM5140
- SH28 - PMIC
- SH29 - POWER MONITOR 1
- SH30 - DARA AND AUTOMATION

REVISION STATUS OF SHEETS

REV															
SH														DWN	DATE
														J.A.C.	02/05/2016
REV	C	C	A	A1	A	C	C	C2	C	C2				CHK	DATE
														T.W.K.	02/05/2016
SH	21	22	23	24	25	26	27	28	29	30				ENGR	DATE
														J.A.C.	02/05/2016
REV	A	A	A	b	A	A	A	A	A	A				ENGR-MGR	DATE
														J.A.C.	02/05/2016
SH	11	12	13	14	15	16	17	18	19	20				QA	DATE
														C.M.D.	02/05/2016
REV	D	D	D	D	D	D	D	B	A	A	NEXT ASSY	USED ON		MFG	DATE
														J.A.C.	02/05/2016
SH	1	2	3	4	5	6	7	8	9	10	APPLICATION			PLSE	DATE
														J.A.C.	02/05/2016

TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: TITLE PAGE

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Date: Friday, September 08, 2017 Sheet 1 of 30

ECN Number	518200-E002			
Date Requested	10/20/2016			
Requester	Robert E.			
Approvals	Tony C.			
Assembly Number	518200-0001			
Current Assembly Rev	B			
New Assembly Rev	C			
Date Implemented	10/24/2016			
Implementation notes				EEPROM will bump to Rev A.2
				ASSY, PWB, LOGIC Rev B TO C
DR13				Add silkscreen for JP1 Pin 1 - CANH Pin 2 - CANL
DR14				NA
DR15				SHEET 2: Change CDCEL925, U114 power rail to VPO_L3_1V8
				SHEET 28: U43 From 104715-0001R-TI to 104715-0002R-TI Create new part # 104715-0002R-TI for updated OTP
				U42 From 104714-0135R-TI to 104714-0136R-TI Create new part # 104714-0136R-TI for updated OTP
				Sheet 29 Change C528 From 102963-0101R 10uF To 104448-0220R 2.2uF
DR16				Update J6 Entry symbol to v.44
DR17				Remove the Lead Free and replace with RoHS Exempt
DR18				SHEET 21 Add EVM_12V to P10 pins 1,3 Add CSI2_GPIO_PWMA to pin 6 Add CSI2_GPIO_PWMB to pin 8
				SHEET 26 Add R564, R565 R0201-NOPOP Map H_MMC3_D4 to EHRPWM3A Map H_MMC3_D5 to EHRPWM3B
DR19				SHEET 3: Change VPP to LDO at 2V vs FET Delete Q6 Add U133 - 104954-0001R Add R562 - 102145-3163R, 31.6k 1% Add R563 - 102145-4703R, 47K 1%
DR20				EEPROM will bump to Rev A.2
DR21				SHEET 27: Add bleed circuit for 3v3 rail Add Q6 - 102437-0001R Add Q6 - 102159-0001R Add R826 - 100688-3650R Add R827 - 101370-1003R

REV C1: ADD ERRATA SHEET 31

REV C2:
UPDATE LP87xx PART NUMBERS FOR CORRECT OTP.
UPDATE AUTOMATION POWER CONTROL NOTE

REV D:
UPDATE SOC SYMBOL TO v1.2
R562 From 102145-3163R to 102145-2323R (31.6K to 23.2K for 1.8V instead of 2.0V on VPP)
INCORPORATE ERRATA FOR GPIO6_16/GPIO6_14 SIGNAL SWAP
UPDATE SD CARD FOOTPRINT FOR NON-EOL PART

TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: NOTES

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9,10 H_GPMC_A0
10 H_GPMC_A1
10 H_GPMC_A2
10 H_GPMC_A3
10 H_GPMC_A4
10 H_GPMC_A5
10 H_GPMC_A6
10 H_GPMC_A7
10 H_GPMC_A8
10 H_GPMC_A9
10 H_GPMC_A10
10 H_GPMC_A11
10 H_GPMC_A12
9 H_GPMC_A13
9 H_GPMC_A14
9 H_GPMC_A15
9 H_GPMC_A16
9 H_GPMC_A17
9 H_GPMC_A18

9 H_GPMC_A19
9 H_GPMC_A20
9 H_GPMC_A21
9 H_GPMC_A22
9 H_GPMC_A23
9 H_GPMC_A24
9 H_GPMC_A25
9 H_GPMC_A26
9 H_GPMC_A27
9 H_GPMC_A28

10 H_GPMC_AD0
10 H_GPMC_AD1
10 H_GPMC_AD2
10 H_GPMC_AD3
10 H_GPMC_AD4
10 H_GPMC_AD5
10 H_GPMC_AD6
10 H_GPMC_AD7
10 H_GPMC_AD8
10 H_GPMC_AD9
10 H_GPMC_AD10
10 H_GPMC_AD11
10 H_GPMC_AD12
10 H_GPMC_AD13
10 H_GPMC_AD14
10 H_GPMC_AD15

9 H_GPMC_ADVn_ALE
9 H_GPMC_BEN0
9 H_GPMC_BEN1
13 H_GPMC_OEN_REn
13 H_GPMC_WEn
9 H_GPMC_WAIT0
13 H_GPMC_CS0
9 H_GPMC_CS2
10 H_GPMC_CS3
9 H_GPMC_CLK

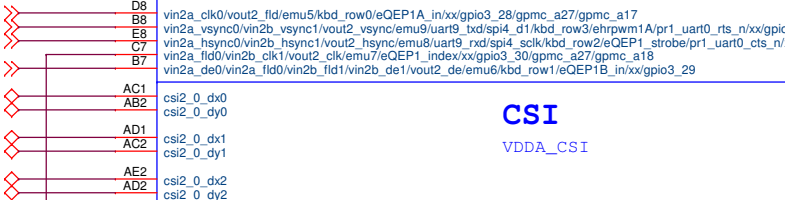
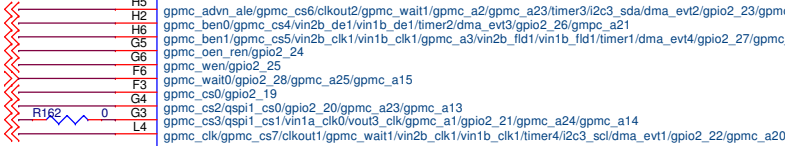
14 H_MMCI0_CMD
14 H_MMCI0_D0
14 H_MMCI0_D1
14 H_MMCI0_D2
14 H_MMCI0_D3
14 H_MMCI0_SDCD
3,18 H_MMCI0_SDWP

26 H_MMCI3_CMD
26 H_MMCI3_D0
26 H_MMCI3_D1
26 H_MMCI3_D2
26 H_MMCI3_D3
26 H_MMCI3_D4
26 H_MMCI3_D5
26 H_MMCI3_D6
26 H_MMCI3_D7
3,26 H_GPIO6_10
3,26 H_GPIO6_11

11 H_VIN2_D23
11 H_VIN2_D22
11 H_VIN2_D21
11 H_VIN2_D20
11 H_VIN2_D19
11 H_VIN2_D18
11 H_VIN2_D17
11 H_VIN2_D16
11 H_VIN2_D15
11 H_VIN2_D14
11 H_VIN2_D13
11 H_VIN2_D12
11 H_VIN2_D11
11 H_VIN2_D10
11 H_VIN2_D9
11 H_VIN2_D8
11 H_VIN2_D7
11 H_VIN2_D6
11 H_VIN2_D5
11 H_VIN2_D4
11 H_VIN2_D3
11 H_VIN2_D2
11 H_VIN2_D1
11 H_VIN2_D0

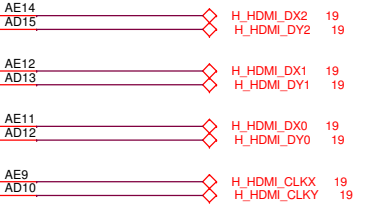
11 H_VIN2_CLK
11 H_VIN2_VSYN
11 H_VIN2_HSYN
11 H_VIN2_DE
21 H_CS12_DX0
21 H_CS12_DY0
21 H_CS12_DX1
21 H_CS12_DY1
21 H_CS12_DX2
21 H_CS12_DY2

3,26 H_GPIO6_10
3,26 H_GPIO6_11
3,12 H_GPIO6_14
3,12 H_GPIO6_15
3,24 H_GPIO6_16
3,18 H_MMCI0_SDWP
3 H_WKUP_0
4,19 H_DCAN1_RX



DRA71x / DRA79x / TDA2E-17 / AM570x
Data Manual: SPRS960A_July2016
Package: CBD, 17x17mm, 538 PBGA, 0.65mm Pitch
PCB Footprint: J6Entry_DRA71x_ZDN_v4
SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

HDMI
VDDA_HDMI



GPMC/GPIO
VDDSHV10

GPIO
VDDSHV3

GPMC/MMC2
VDDSHV11

SYSTEM

GPMC/GPIO
VDDSHV10

CLOCKING
VDDA_OSC

MEMORY-Nonvolatile

MMC1
VDDSHV8

MMC3/GPIO
VDDSHV7

CONTROL
VDDSHV3

Video Inputs

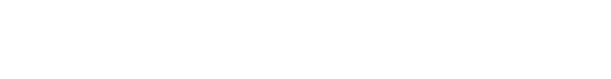
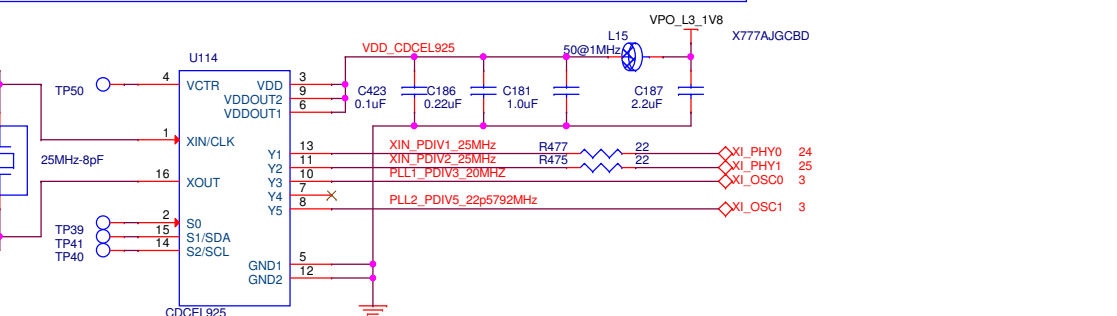
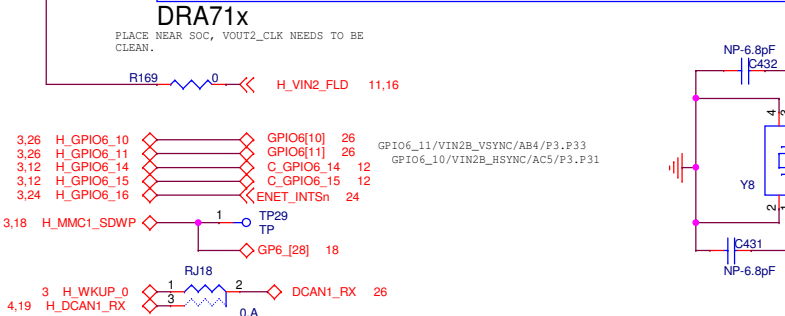
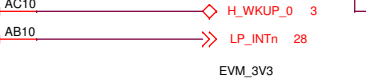
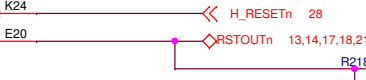
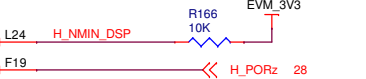
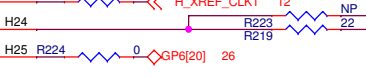
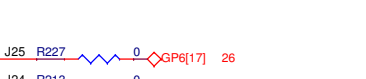
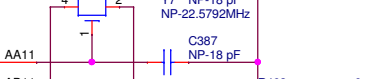
I2C
VDDSHV3

VIN2
VDDSHV1

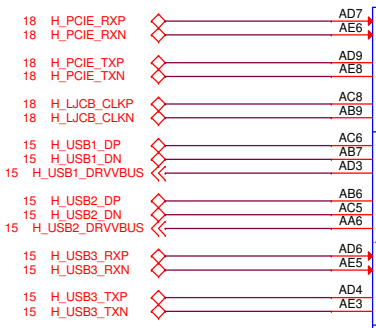
Debug
VDDSHV3

CSI
VDDA_CSI

Si Test



TEXAS INSTRUMENTS INCORPORATED			
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PCIE
VDDA_PCIE

USB
VDDA33V_USB

VDDA_USB

DRA71x / DRA79x / TDA2E-17 / AM570x
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SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

MCASP
VDDSHV3

CONNECTIVITY

ETHERNET
VDDSHV9

VDDSHV3

VDDSHV3

VDDSHV3

VDDSHV7

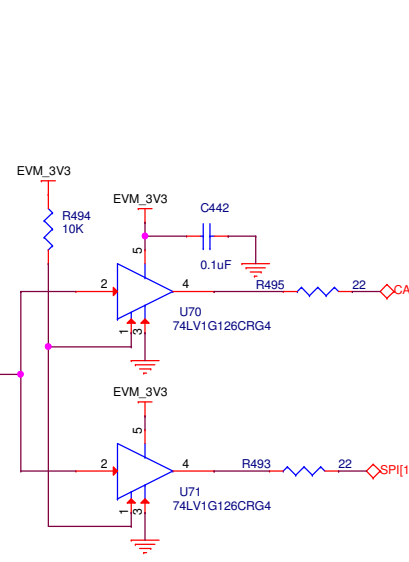
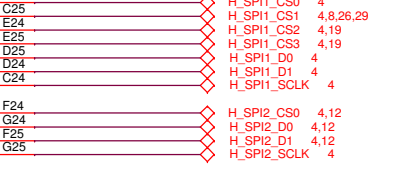
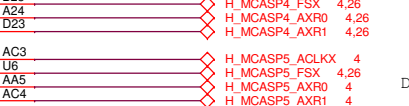
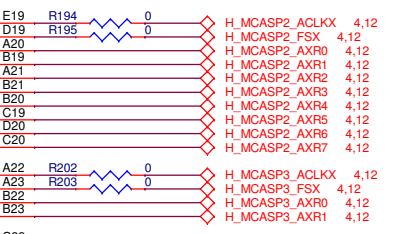
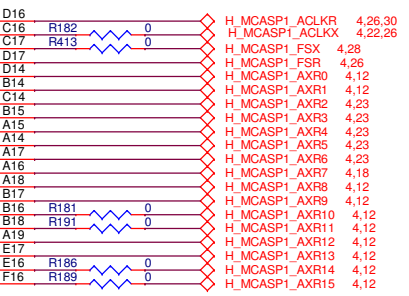
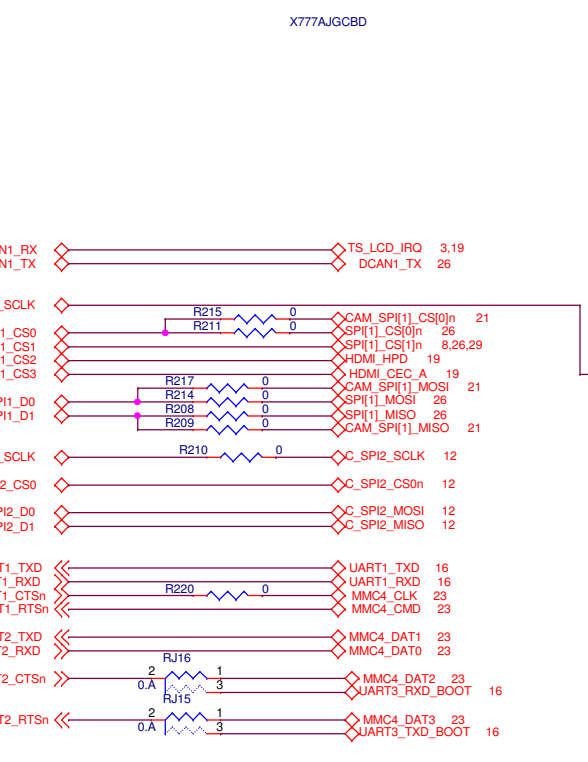
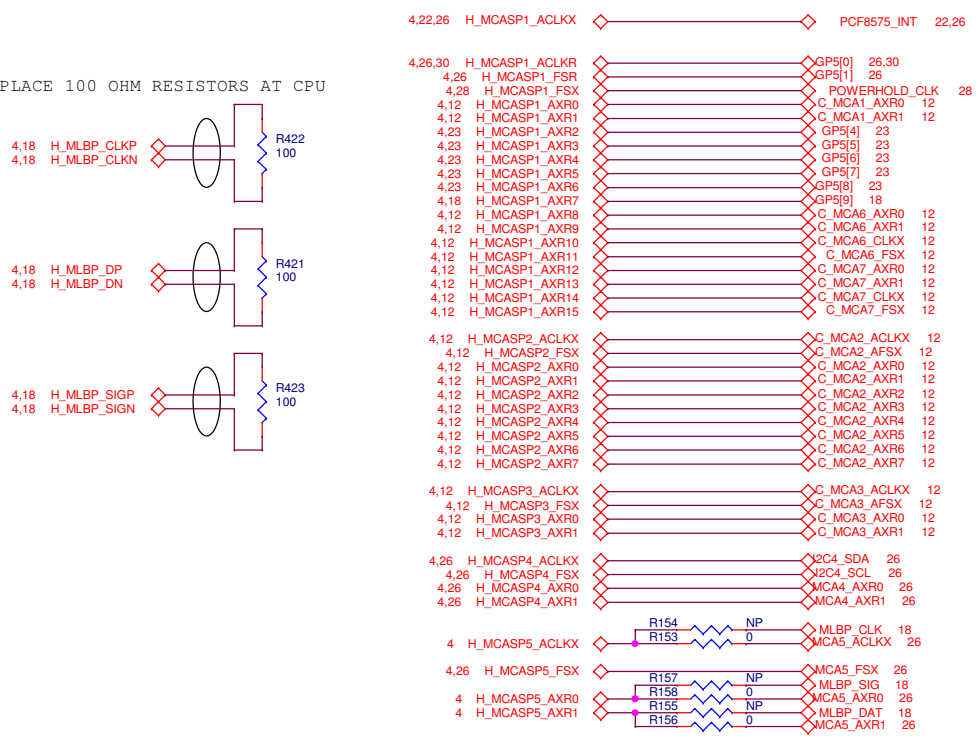
MLBP
VDDSHV3

SPI
VDDSHV3

UART
VDDSHV4

DCAN
VDDSHV3

DRA71x



TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"			
Page Contents: SoC CNTVY			
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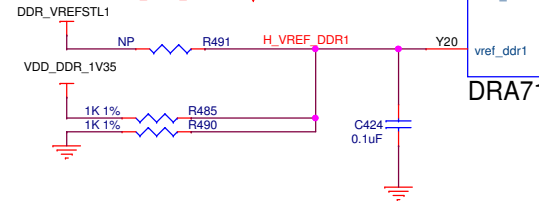


**DRA71x / DRA79x /
TDA2E-17 / AM570x**

Data Manual: SPRS960A_July2016
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 PCB Footprint: J6Entry_DRA71x_ZDN_v4
 SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

**MEMORY-
Volatile, DDR3
EMIF1**

VDDS_DDR1



DRA71x X777AJCGBD

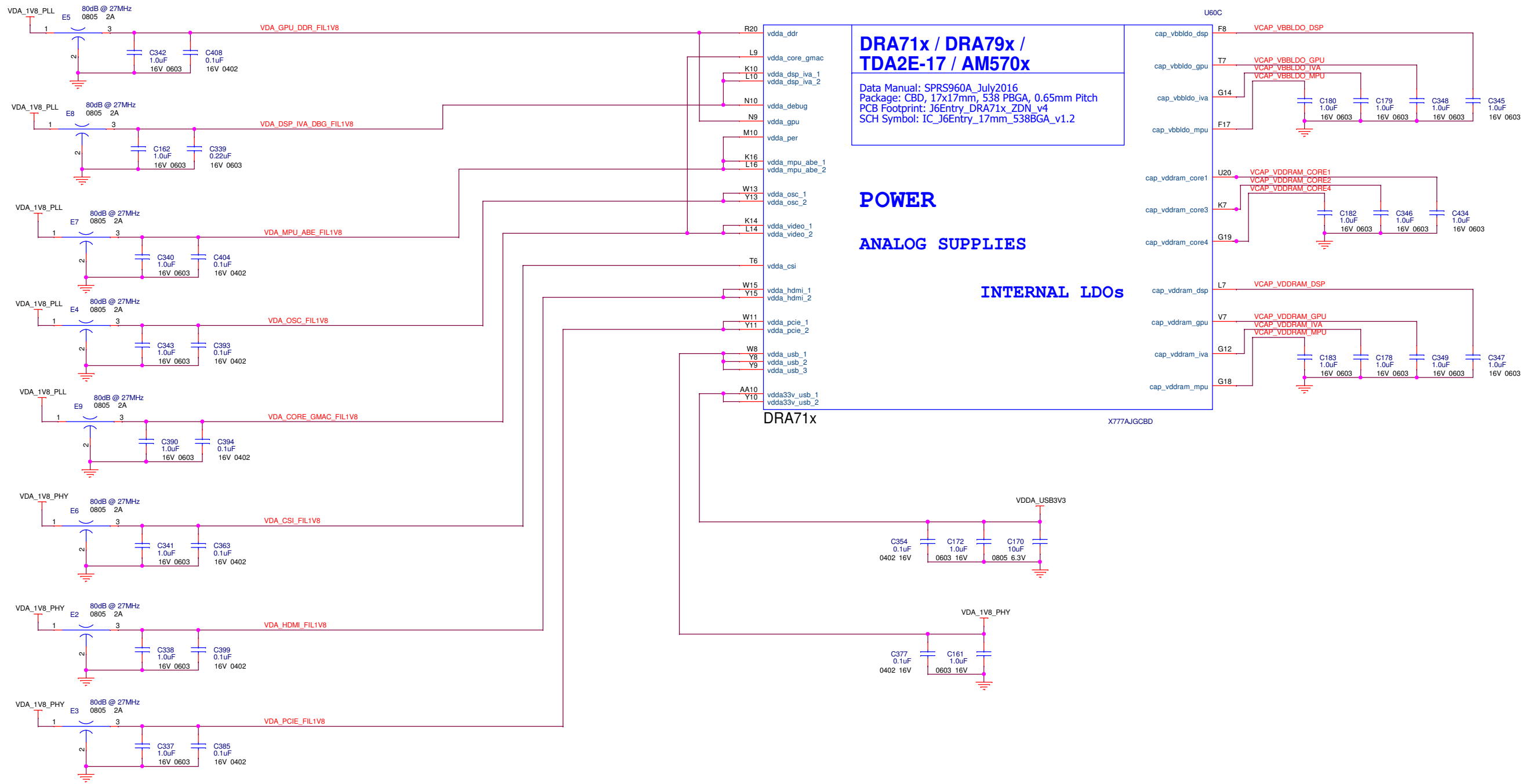
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

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DRA71x / DRA79x / TDA2E-17 / AM570x

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 SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

POWER

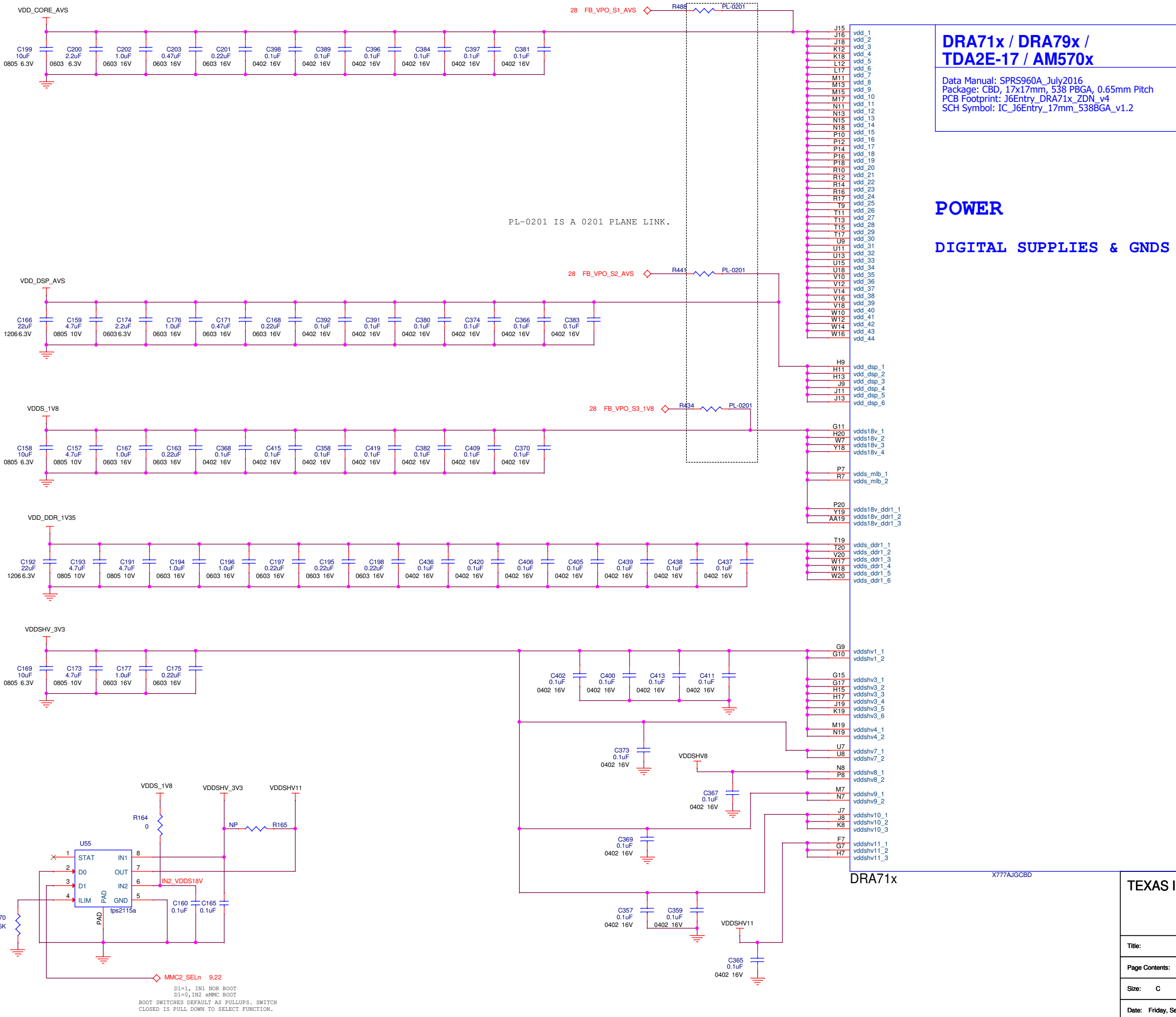
ANALOG SUPPLIES

INTERNAL LDOs

TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"		
Page Contents: SoC ANA PWR		
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Route the feedback connections as 4-8mil trace widths for remote sensing voltages only (not current carrying) and connected as close as possible to SoC power balls or Dcaps located very close to power ball (point of load).



DRA71x / DRA79x / TDA2E-17 / AM570x

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SCH Symbol: IC_J6Entry_17mm_538BGA_v1.2

POWER DIGITAL SUPPLIES & GNDS

- J15 vdd_1
- J16 vdd_2
- J18 vdd_3
- K12 vdd_4
- K18 vdd_5
- L12 vdd_6
- L17 vdd_7
- M11 vdd_8
- M13 vdd_9
- M15 vdd_10
- M17 vdd_11
- N11 vdd_12
- N13 vdd_13
- N15 vdd_14
- N18 vdd_15
- P10 vdd_16
- P12 vdd_17
- P14 vdd_18
- P16 vdd_19
- P18 vdd_20
- R10 vdd_21
- R12 vdd_22
- R14 vdd_23
- R16 vdd_24
- R17 vdd_25
- T19 vdd_26
- T11 vdd_27
- T13 vdd_28
- T15 vdd_29
- T17 vdd_30
- U9 vdd_31
- U11 vdd_32
- U13 vdd_33
- U15 vdd_34
- U18 vdd_35
- V10 vdd_36
- V12 vdd_37
- V14 vdd_38
- V16 vdd_39
- V18 vdd_40
- W10 vdd_41
- W12 vdd_42
- W14 vdd_43
- W16 vdd_44
- H9 vdd_dsp_1
- H11 vdd_dsp_2
- H13 vdd_dsp_3
- J9 vdd_dsp_4
- J11 vdd_dsp_5
- J13 vdd_dsp_6
- G11 vdds18v_1
- H20 vdds18v_2
- W7 vdds18v_3
- Y18 vdds18v_4
- P7 vdds_mib_1
- R7 vdds_mib_2
- P20 vdds18v_ddr1_1
- Y19 vdds18v_ddr1_2
- AA19 vdds18v_ddr1_3
- T19 vdds_ddr1_1
- T20 vdds_ddr1_2
- V20 vdds_ddr1_3
- W17 vdds_ddr1_4
- W18 vdds_ddr1_5
- W20 vdds_ddr1_6
- G9 vddshv1_1
- G10 vddshv1_2
- G15 vddshv3_1
- G17 vddshv3_2
- H15 vddshv3_3
- H17 vddshv3_4
- J19 vddshv3_5
- K19 vddshv3_6
- M19 vddshv4_1
- N19 vddshv4_2
- U7 vddshv7_1
- U8 vddshv7_2
- N8 vddshv8_1
- P8 vddshv8_2
- M7 vddshv9_1
- N7 vddshv9_2
- J7 vddshv10_1
- J8 vddshv10_2
- K8 vddshv10_3
- F7 vddshv11_1
- G7 vddshv11_2
- H7 vddshv11_3

- A1 vss_1
- A25 vss_2
- G8 vss_3
- G13 vss_4
- G16 vss_5
- H8 vss_6
- H10 vss_7
- H12 vss_8
- H14 vss_9
- H16 vss_10
- H18 vss_11
- H19 vss_12
- J10 vss_13
- J12 vss_14
- J14 vss_15
- J17 vss_16
- K9 vss_17
- K11 vss_18
- K13 vss_19
- K15 vss_20
- K17 vss_21
- L8 vss_22
- L11 vss_23
- L13 vss_24
- L15 vss_25
- L18 vss_26
- AA13 vss_27
- M8 vss_28
- M9 vss_29
- M12 vss_30
- M14 vss_31
- M16 vss_32
- M18 vss_33
- M20 vss_34
- N12 vss_35
- N14 vss_36
- N16 vss_37
- N17 vss_38
- N20 vss_39
- P9 vss_40
- P11 vss_41
- P13 vss_42
- P15 vss_43
- P17 vss_44
- P19 vss_45
- R8 vss_46
- R9 vss_47
- R11 vss_48
- R13 vss_49
- R15 vss_50
- R18 vss_51
- R19 vss_52
- T8 vss_53
- T10 vss_54
- T12 vss_55
- T14 vss_56
- T16 vss_57
- T18 vss_58
- U10 vss_59
- U12 vss_60
- U14 vss_61
- U16 vss_62
- U17 vss_63
- U19 vss_64
- V8 vss_65
- V9 vss_66
- V11 vss_67
- V13 vss_68
- V15 vss_69
- V17 vss_70
- V19 vss_71
- W9 vss_72
- W19 vss_73
- Y7 vss_74
- Y14 vss_75
- Y16 vss_76
- Y17 vss_77
- AA7 vss_78
- AA8 vss_79
- AA9 vss_80
- AB8 vss_81
- AC13 vss_82
- AE1 vss_83
- AE15 vss_84
- AE25 vss_85
- AA15 vss_86

DRA71x X777AJGCB

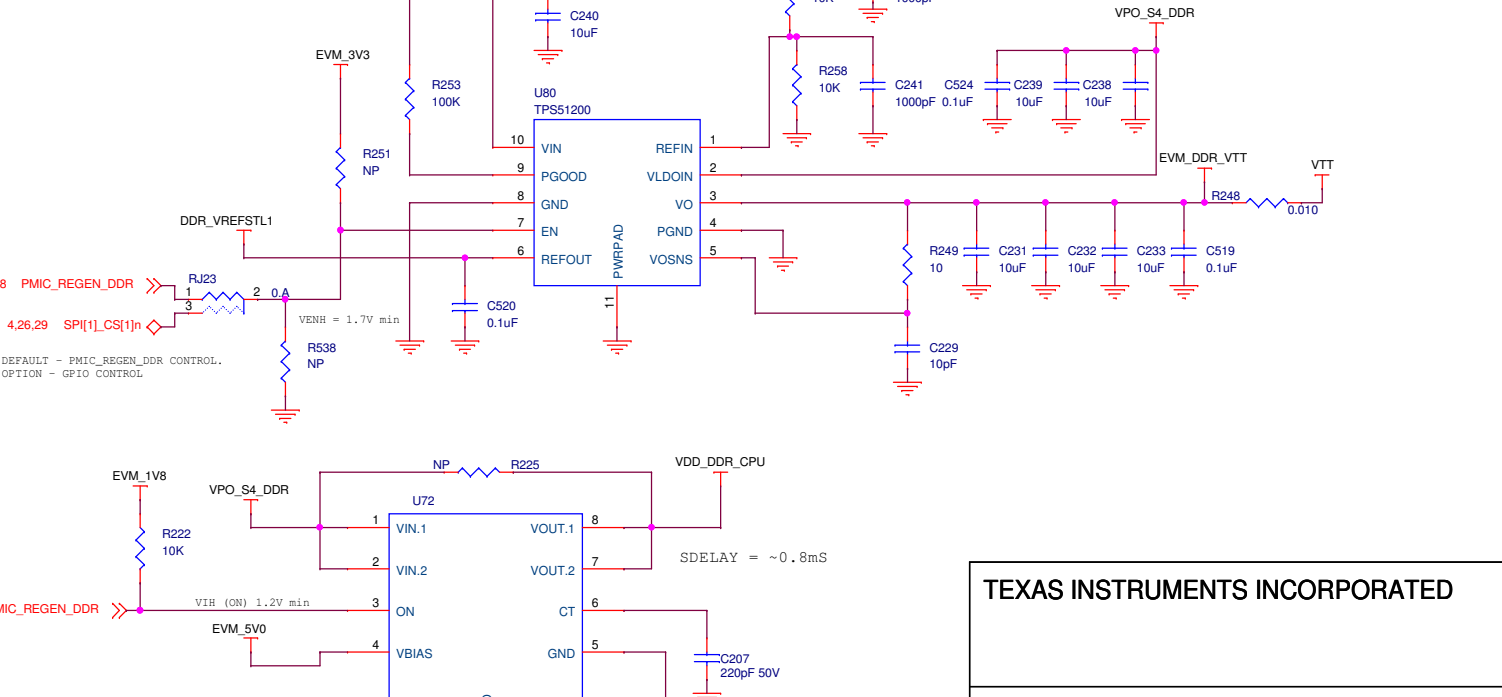
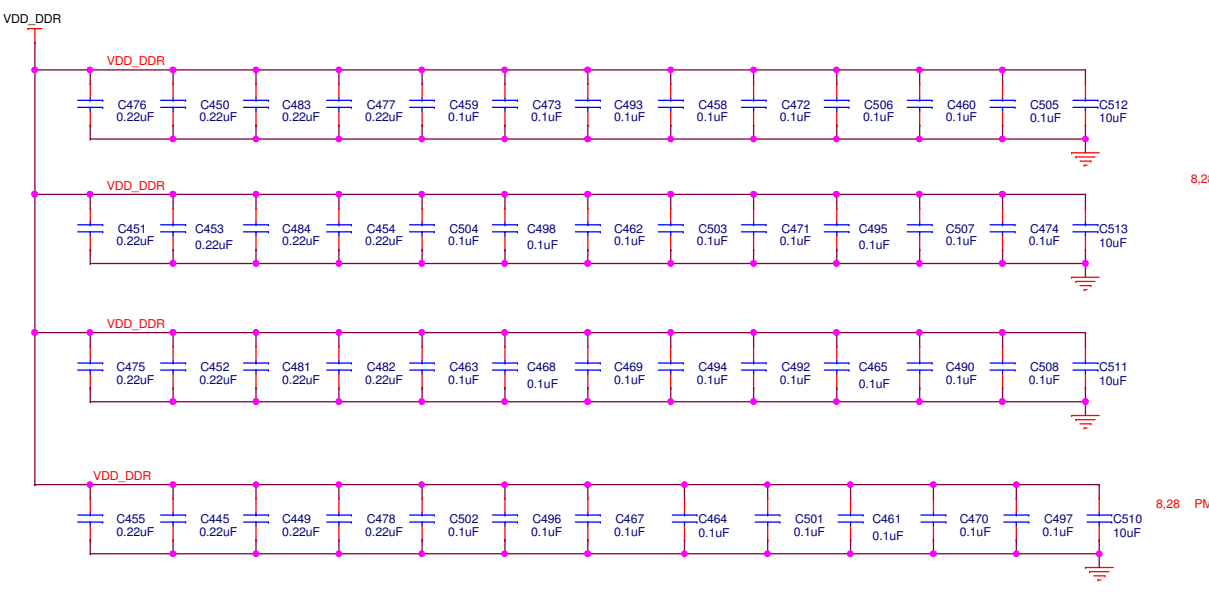
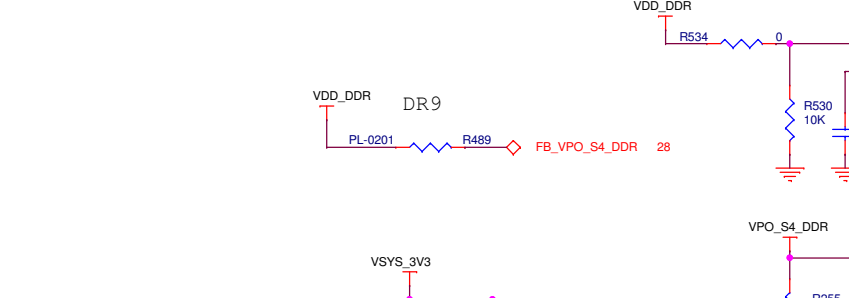
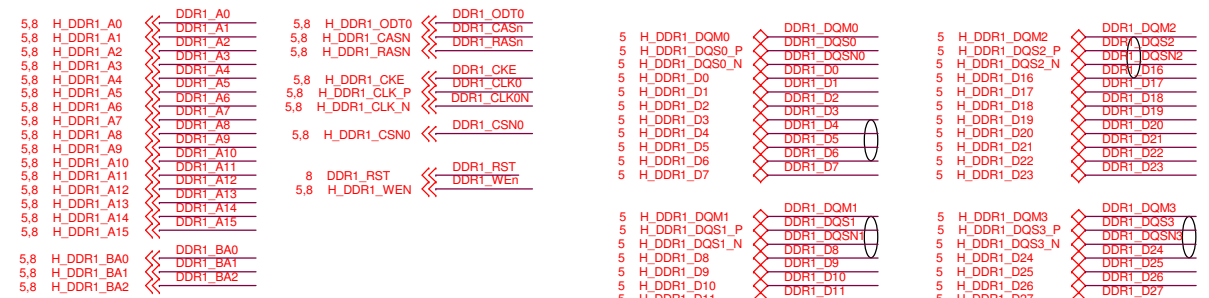
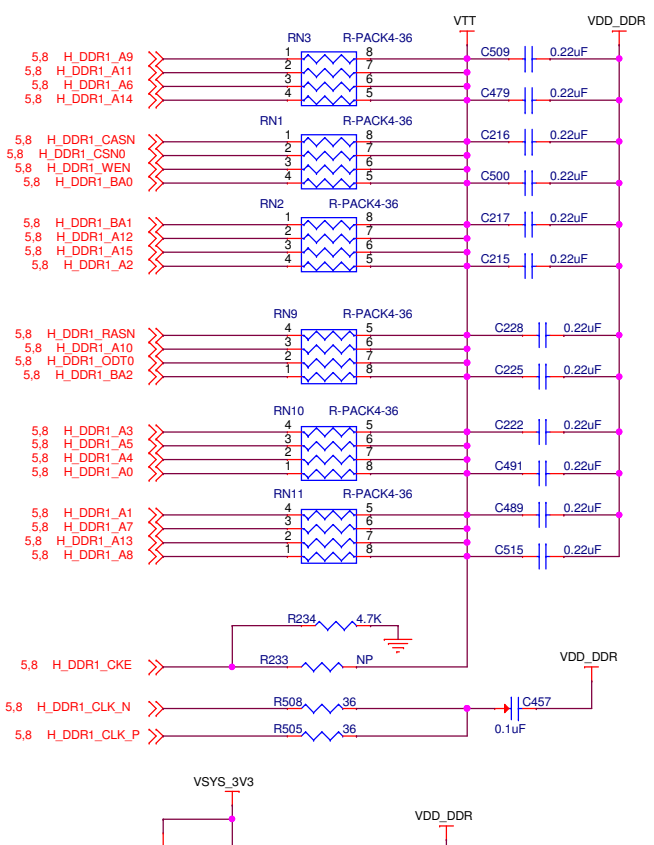
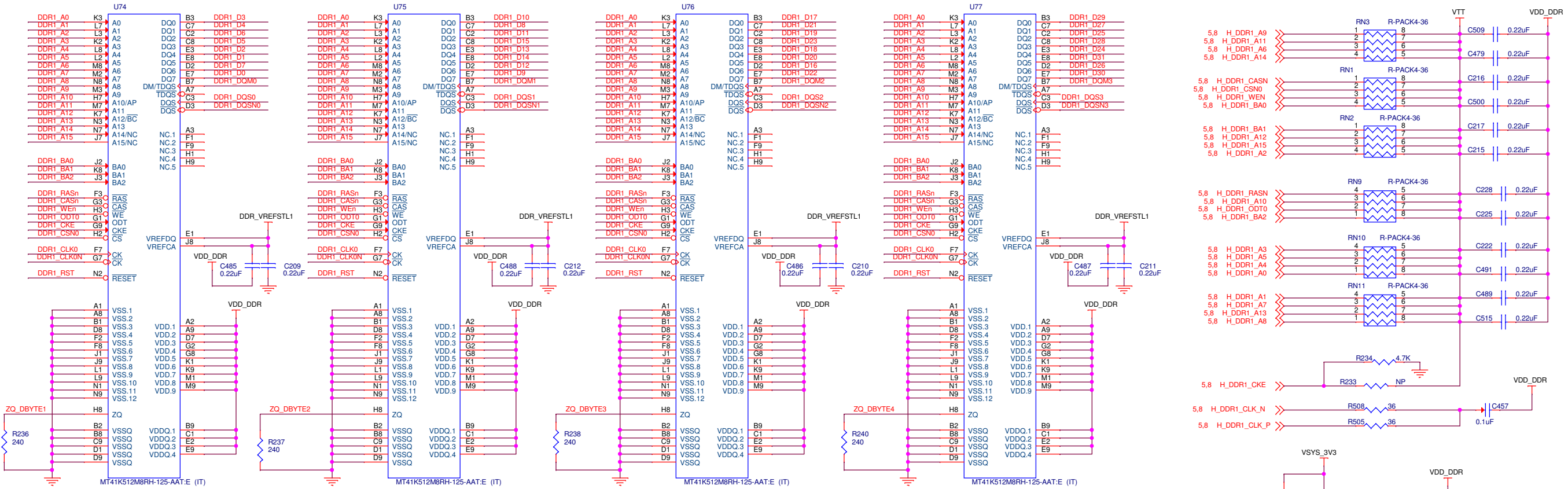
TEXAS INSTRUMENTS INCORPORATED

Title: *DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board*

Page Contents: SoC DIG PWR

Size: C	DOC NO: 518202	REV: D
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Date: Friday, September 08, 2017	Sheet 7 of 30
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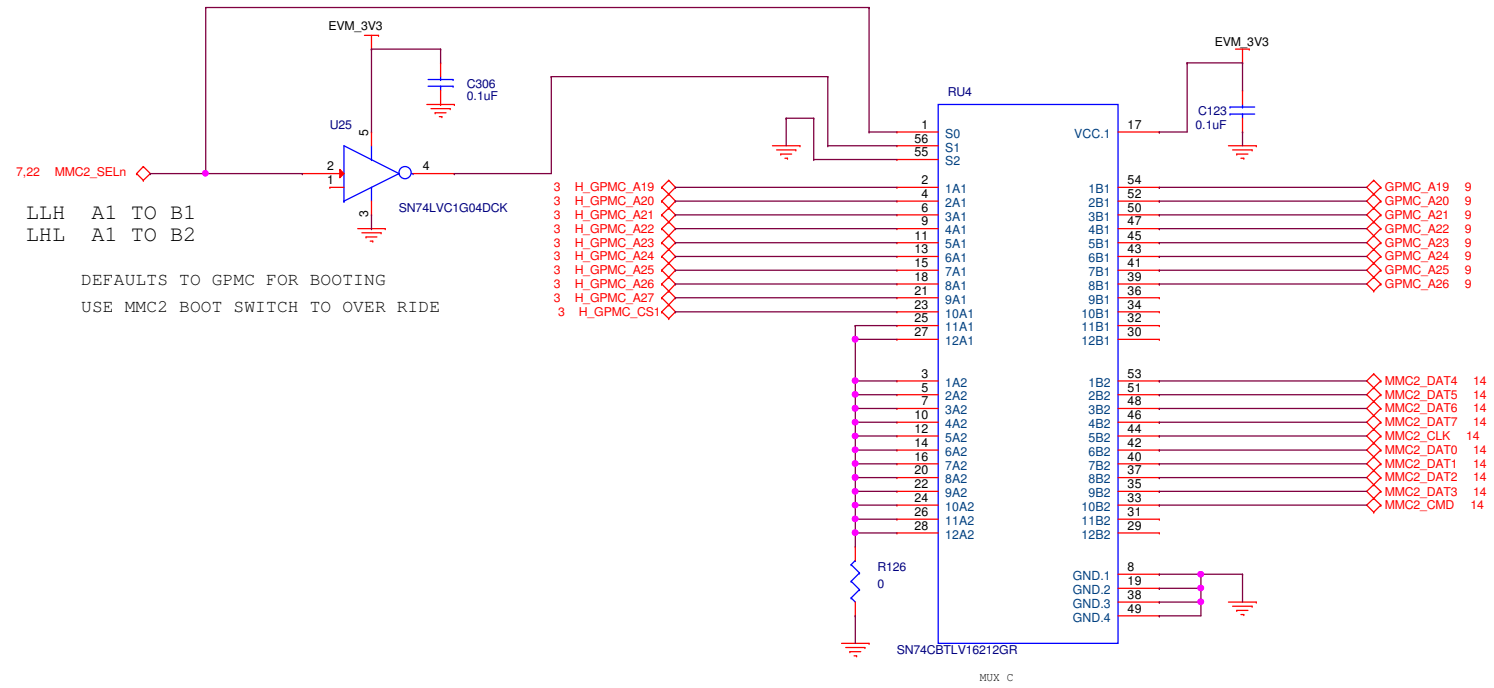
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: DDR3 MEMORY BANK 1

Size: C DOC NO: 518202 REV: B

Date: Friday, September 08, 2017 Sheet 8 of 30



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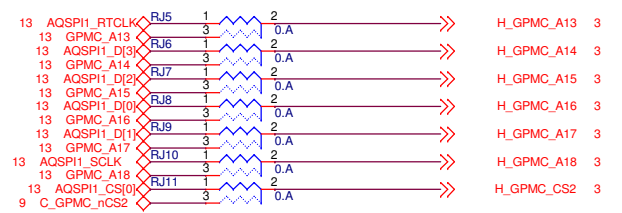
gpmc_a[19] mmc2_dat[4]
gpmc_a[20] mmc2_dat[5]
gpmc_a[21] mmc2_dat[6]
gpmc_a[22] mmc2_dat[7]
gpmc_a[23] mmc2_clk[7]
gpmc_a[24] mmc2_dat[0]
gpmc_a[25] mmc2_dat[1]
gpmc_a[26] mmc2_dat[2]
gpmc_a[27] mmc2_dat[3]
gpmc_cs[1] mmc2_cmd

```

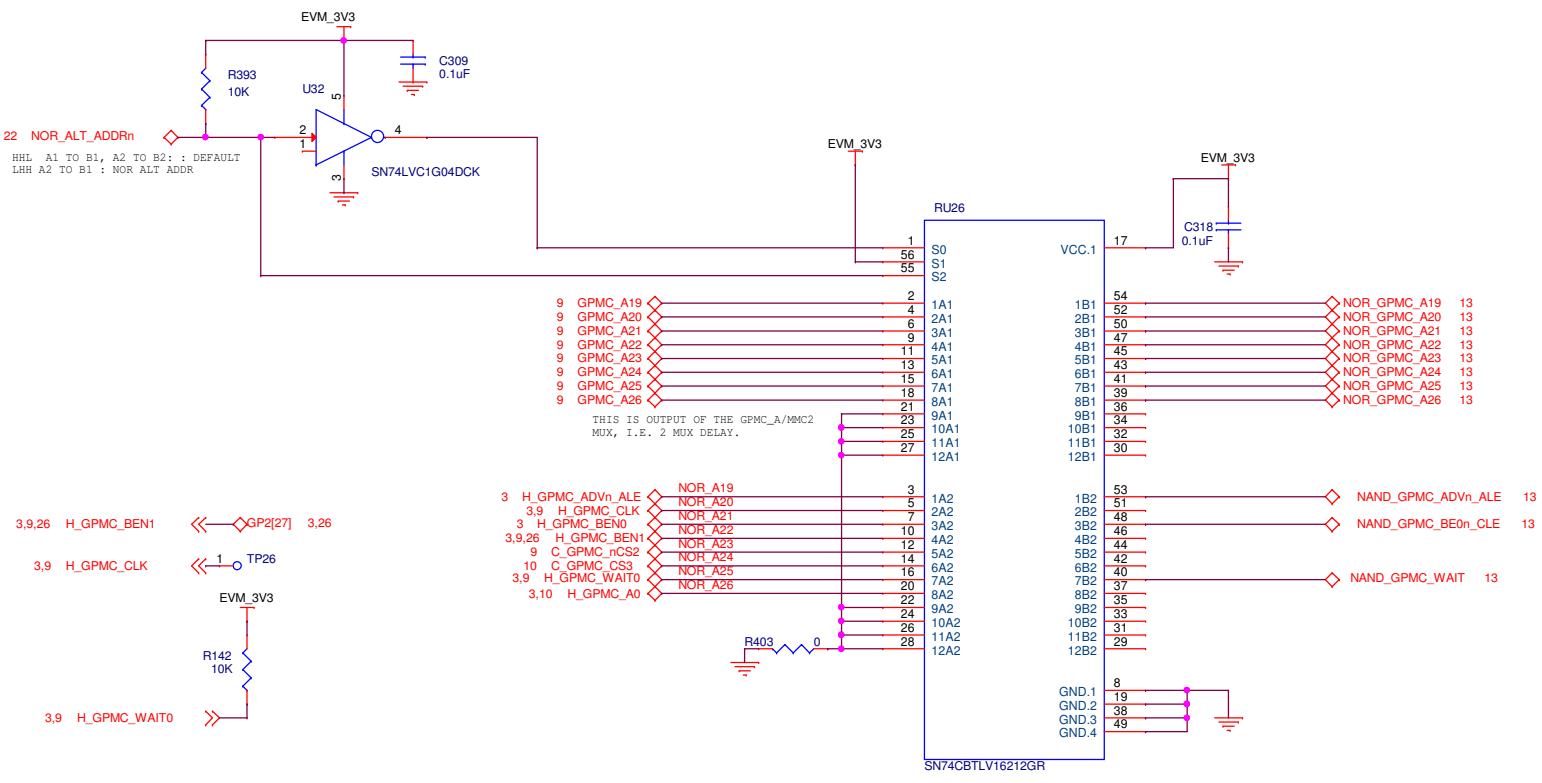
7,22 MMC2_SELn

LLH A1 TO B1
LHL A1 TO B2

DEFAULTS TO GPMC FOR BOOTING
USE MMC2 BOOT SWITCH TO OVER RIDE



AQSPI PATH IS THE FAST PATH WITH MAX TRACE LENGTH OF 2.75 INCHES.



22 NOR_ALT_ADDRn

HHL A1 TO B1, A2 TO B2 : DEFAULT
LHH A2 TO B1 : NOR ALT ADDR

3,9,26 H_GPMC_BEN1 <<< GP2[27] 3,26

3,9 H_GPMC_CLK <<< 1 TP26

3,9 H_GPMC_WAIT0 <<< EVM_3V3

THIS IS OUTPUT OF THE GPMC_A/MMC2 MUX, I.E. 2 MUX DELAY.

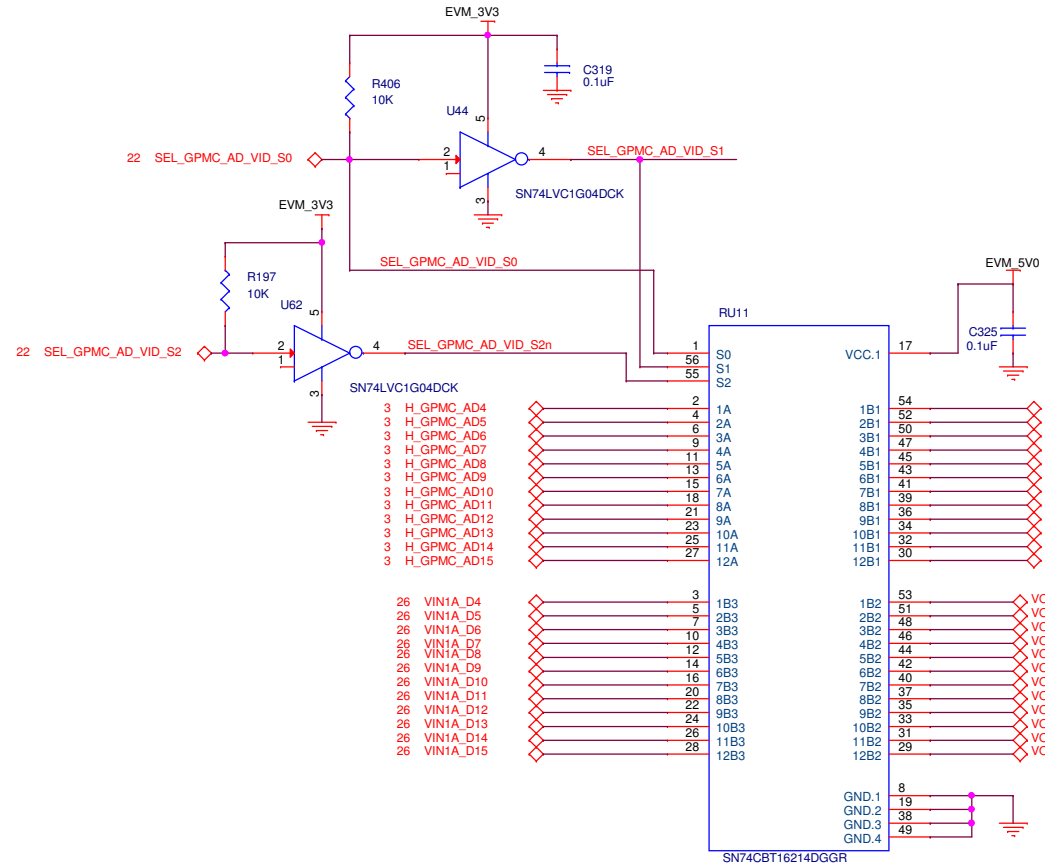
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

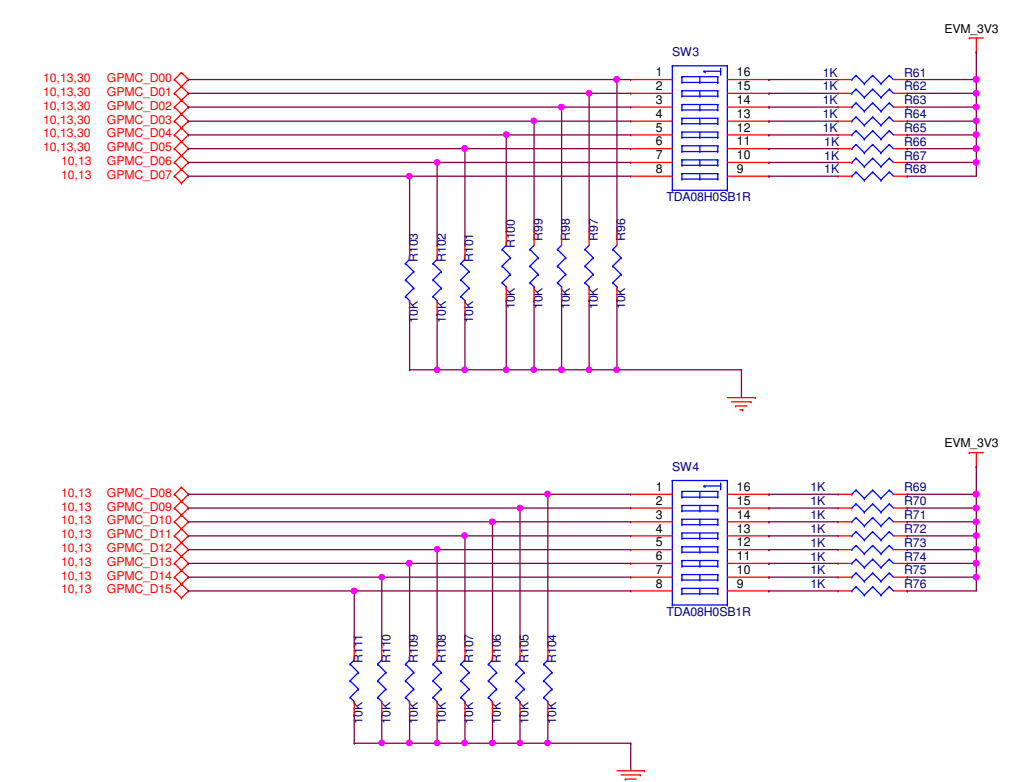
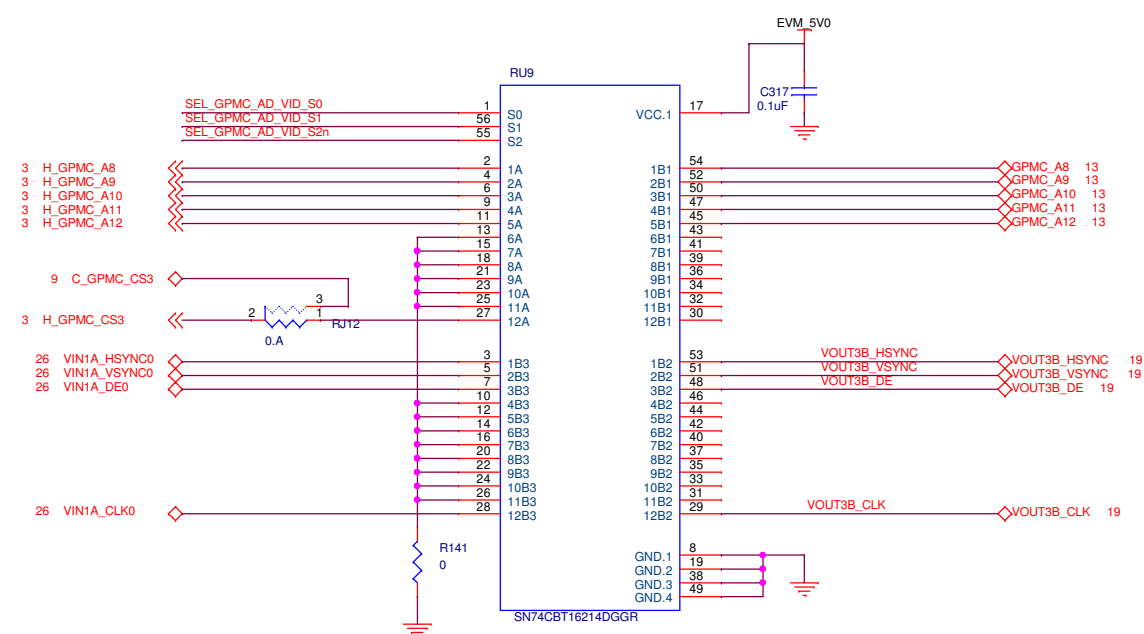
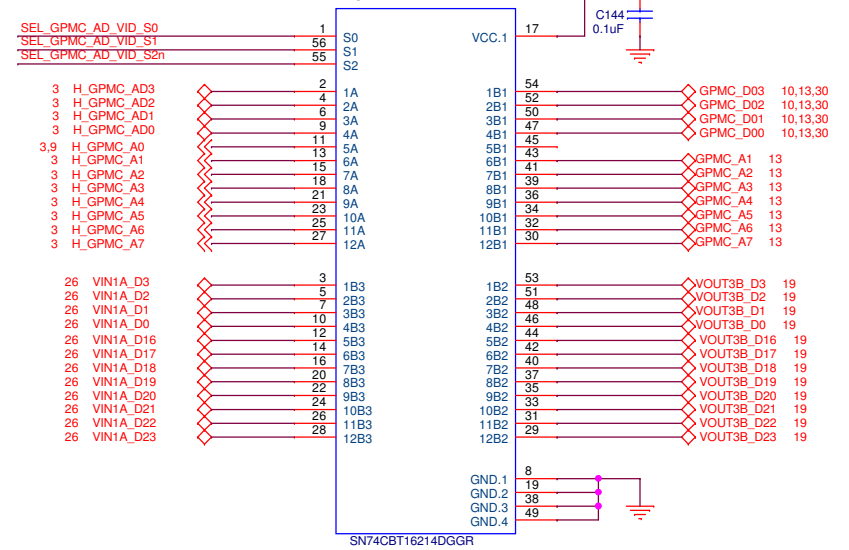
Page Contents: MUX A/C QSPI/EMMC/GPMC

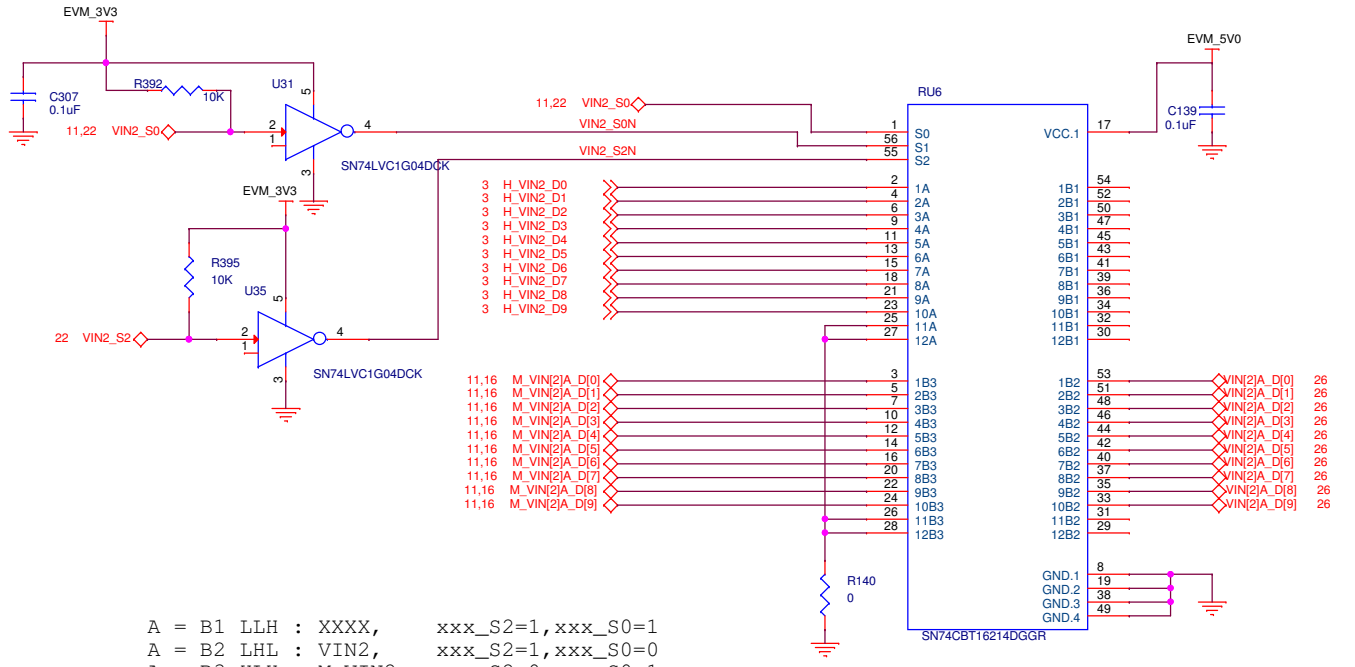
Size: C DOC NO: 518202 REV: A

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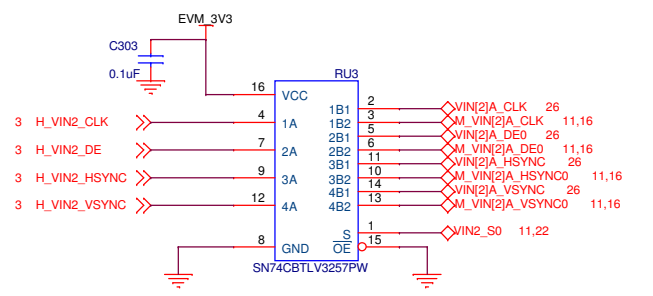


DEFAULTS TO GPMC FOR BOOTING
 A = B1 LLH : GPMC, xxx_S2=1, xxx_S0=1
 A = B2 LHL : VOUT, xxx_S2=1, xxx_S0=0
 A = B3 HLH : VIN, xxx_S2=0, xxx_S0=1

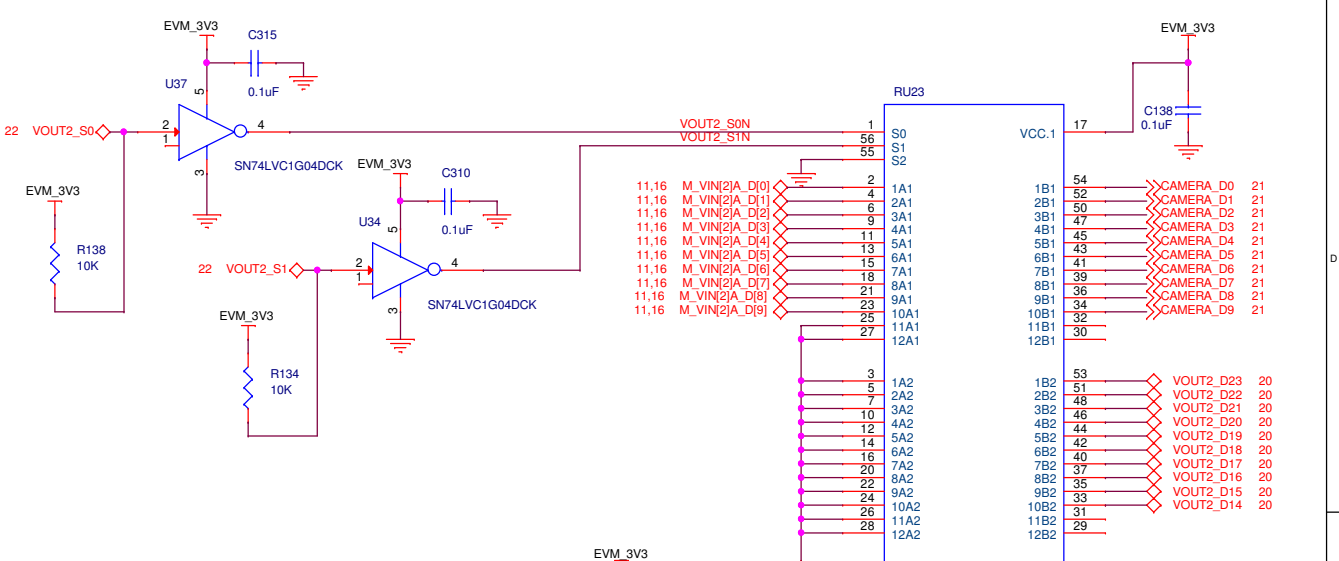
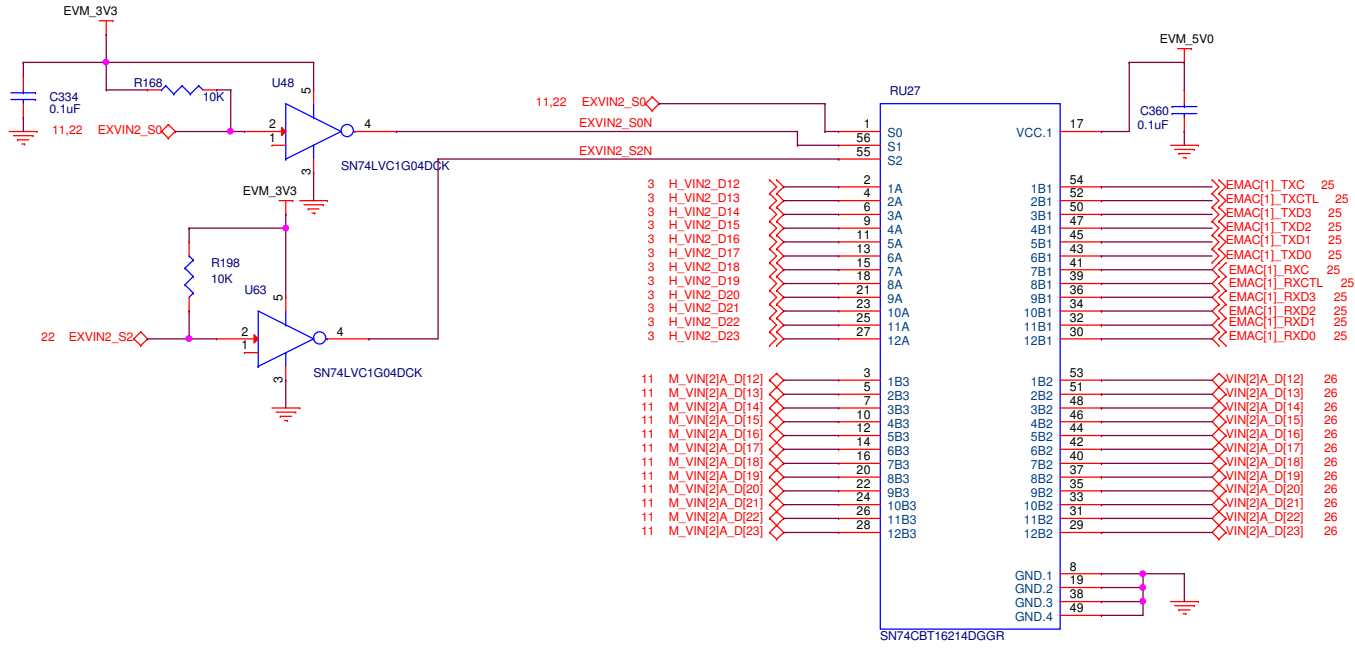
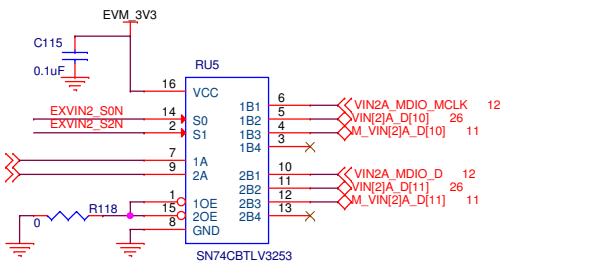




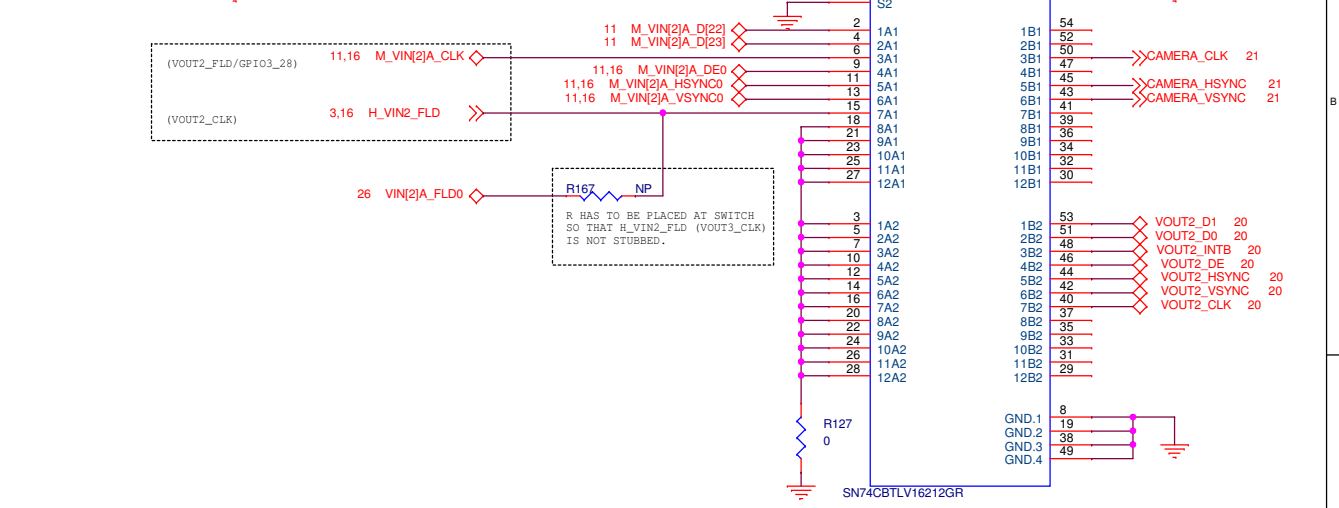
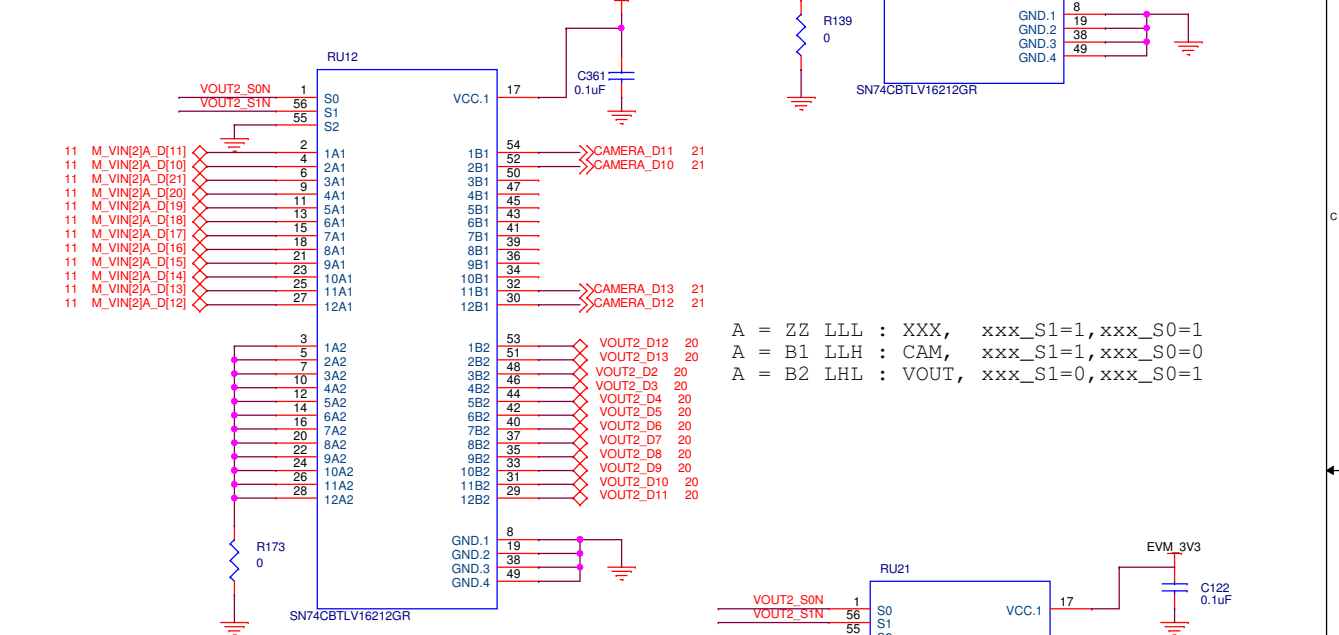
A = B1 LLH : XXXX, xxx_S2=1, xxx_S0=1
 A = B2 LHL : VIN2, xxx_S2=1, xxx_S0=0
 A = B3 HLH : M_VIN2, xxx_S2=0, xxx_S0=1



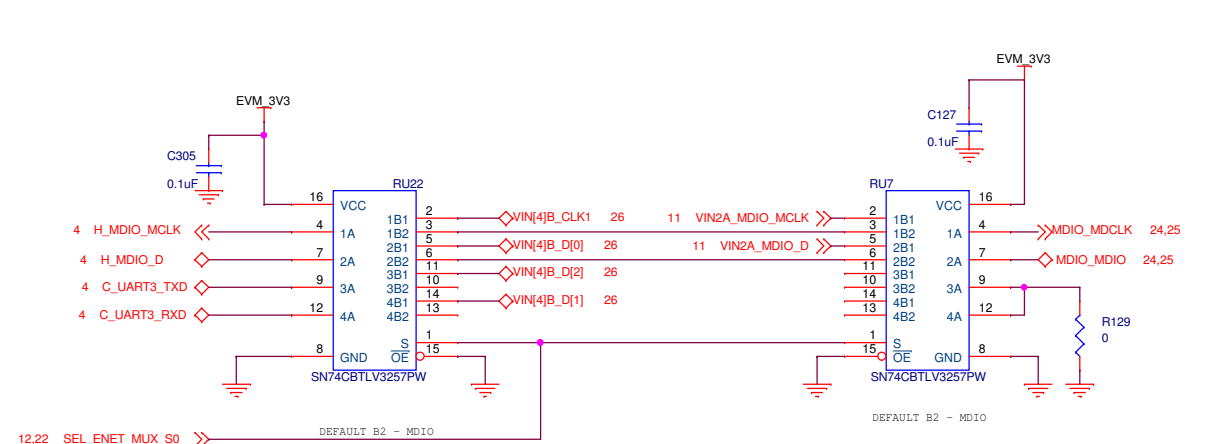
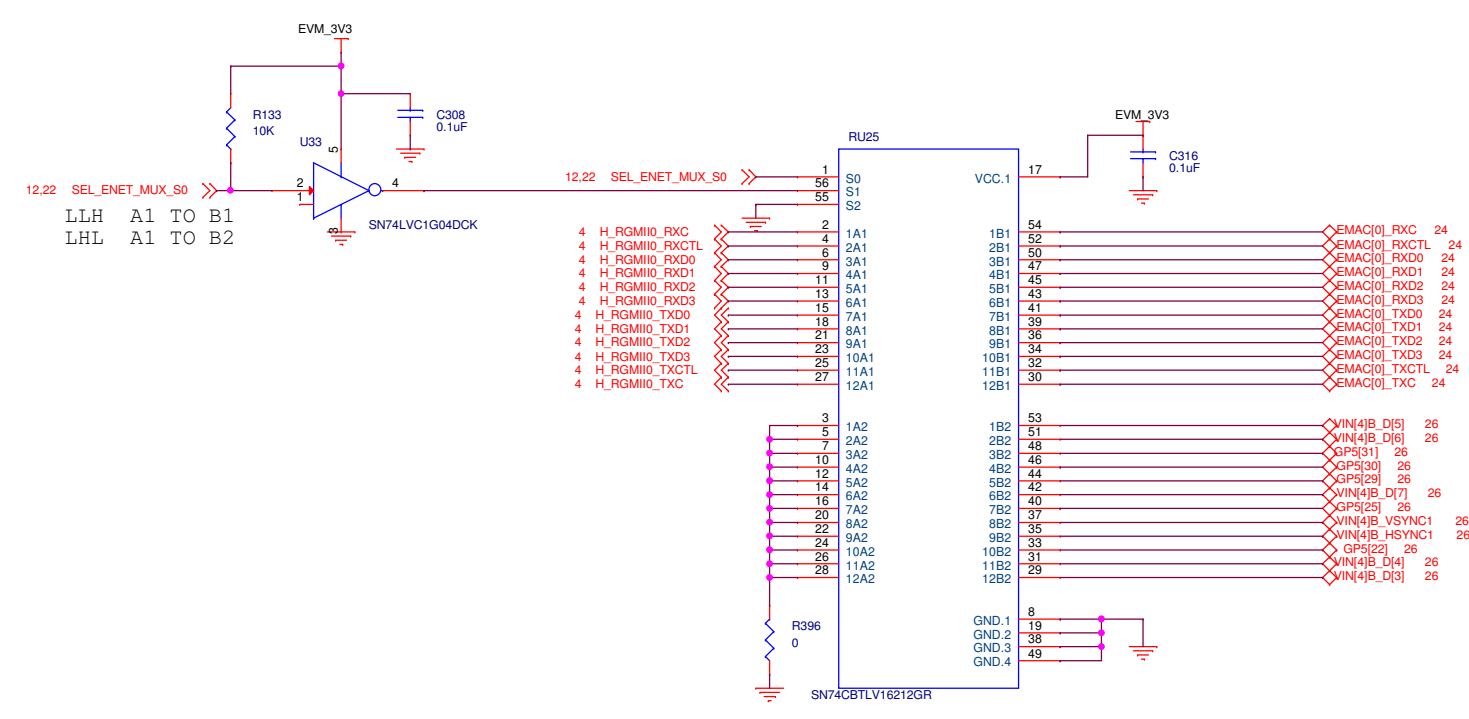
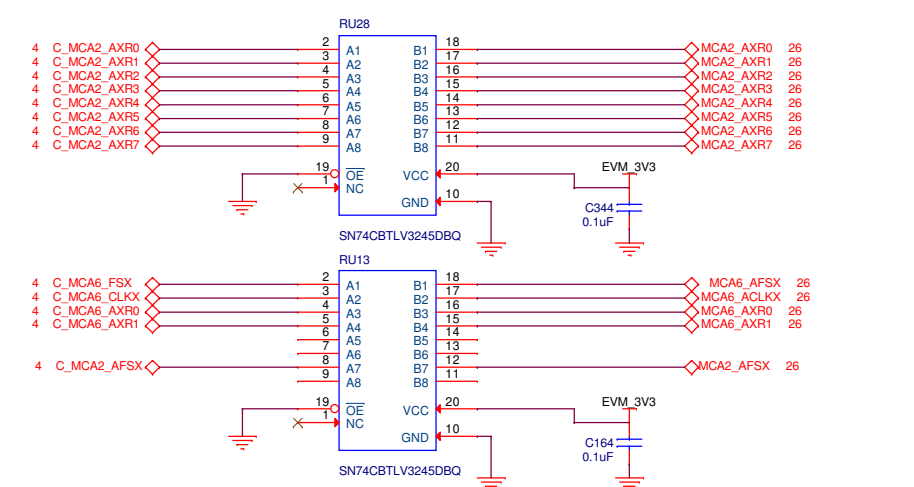
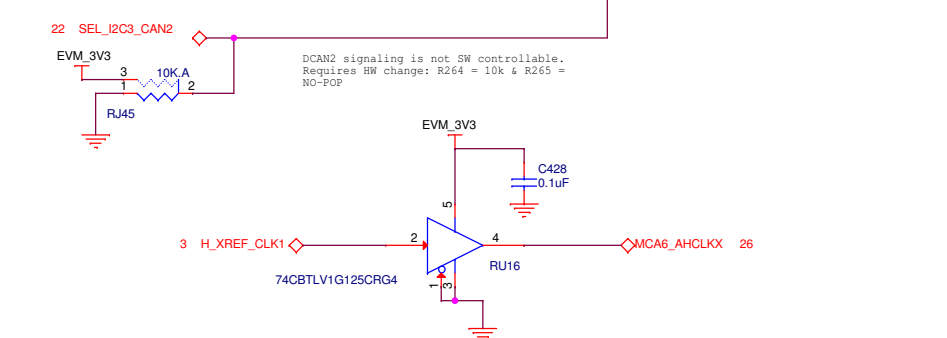
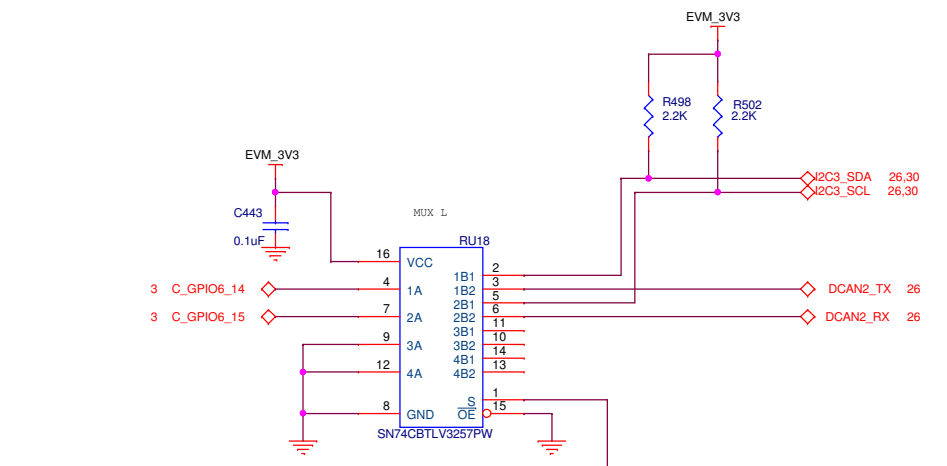
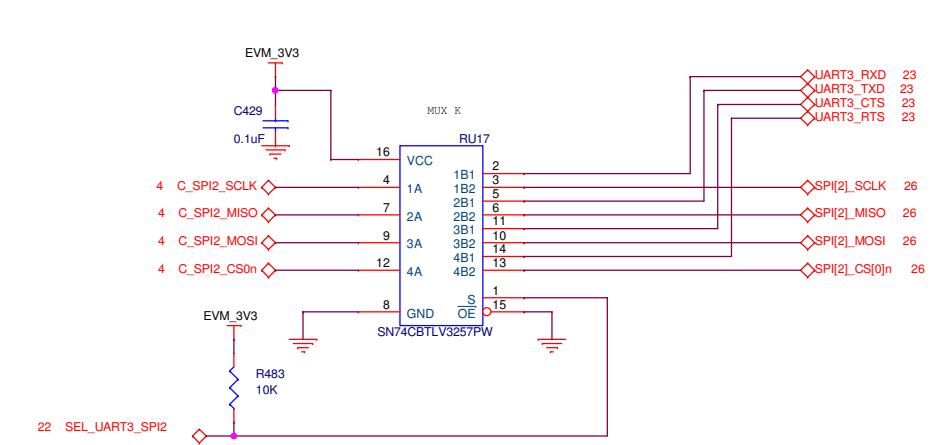
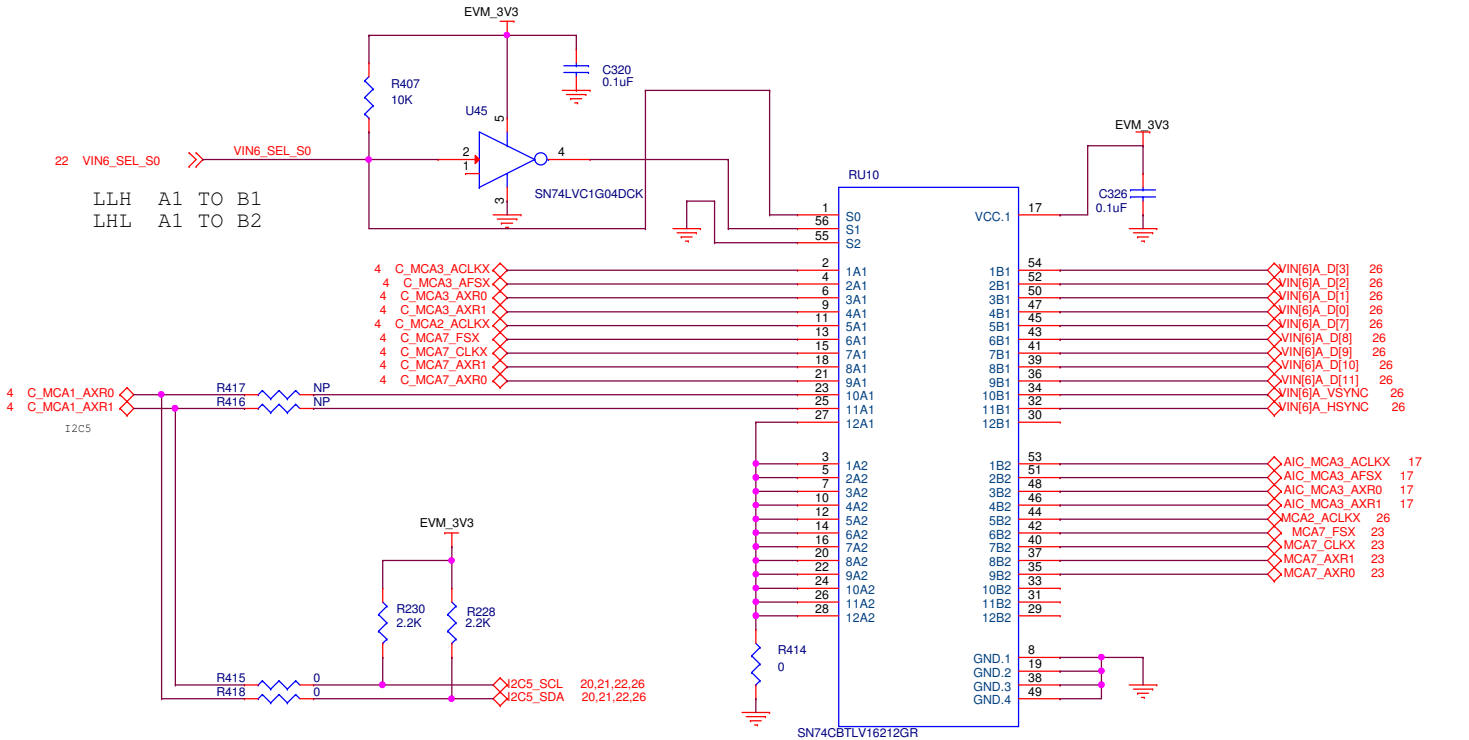
A = B1 LLH : ENET, xxx_S2=1, xxx_S0=1
 A = B2 LHL : VIN2, xxx_S2=1, xxx_S0=0
 A = B3 HLH : M_VIN2, xxx_S2=0, xxx_S0=1



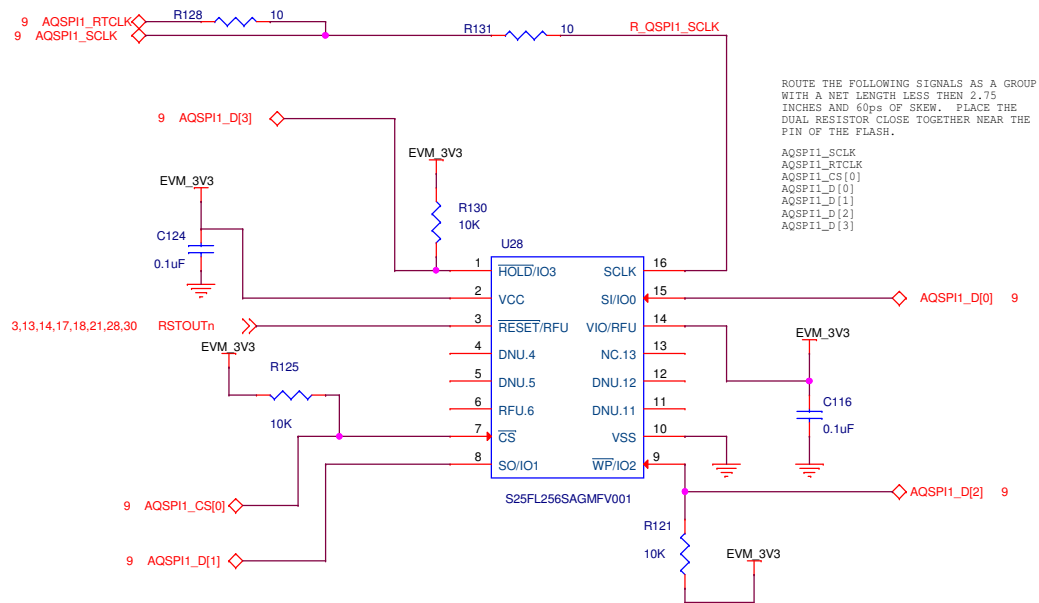
A = ZZ LLL : XXX, xxx_S1=1, xxx_S0=1
 A = B1 LLH : CAM, xxx_S1=1, xxx_S0=0
 A = B2 LHL : VOUT, xxx_S1=0, xxx_S0=1



TEXAS INSTRUMENTS INCORPORATED			
Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"			
Page Contents: MUX E VIN2			
Size: C	DOC NO: 518202	REV: A	
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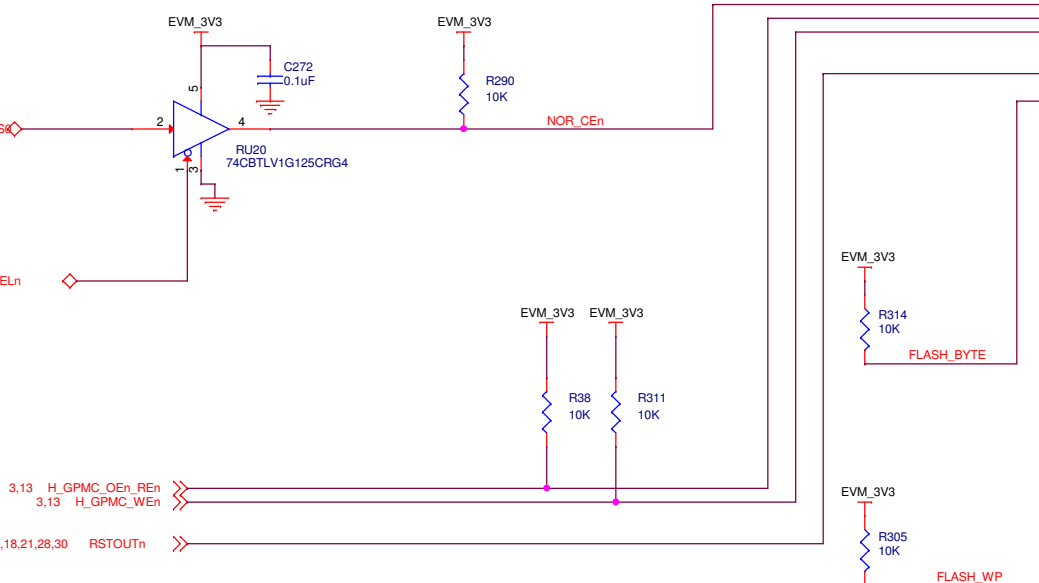
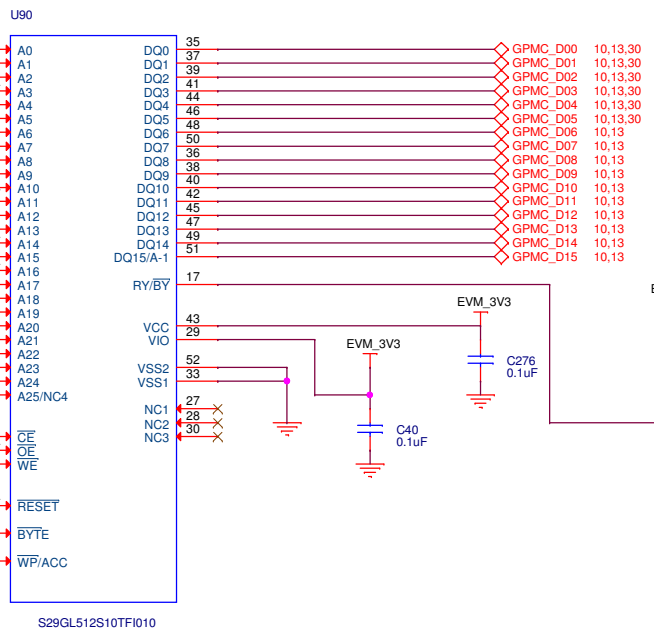
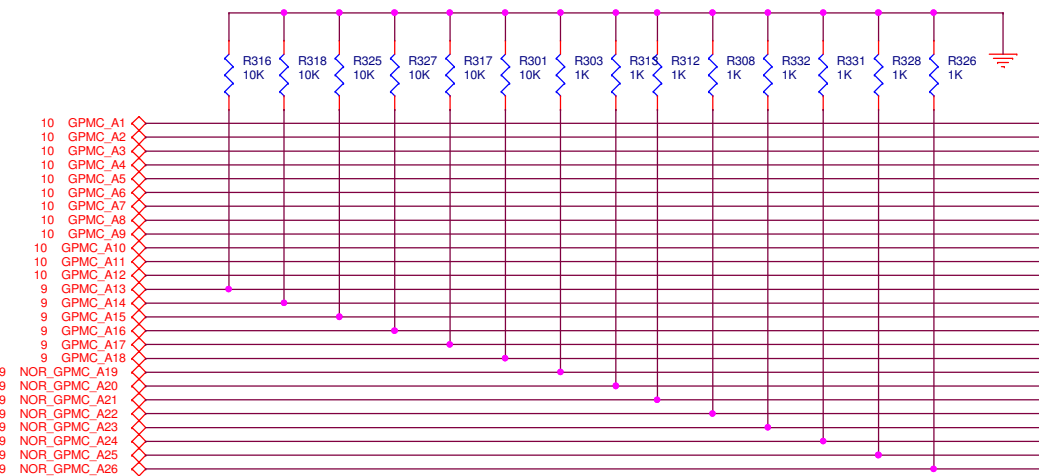
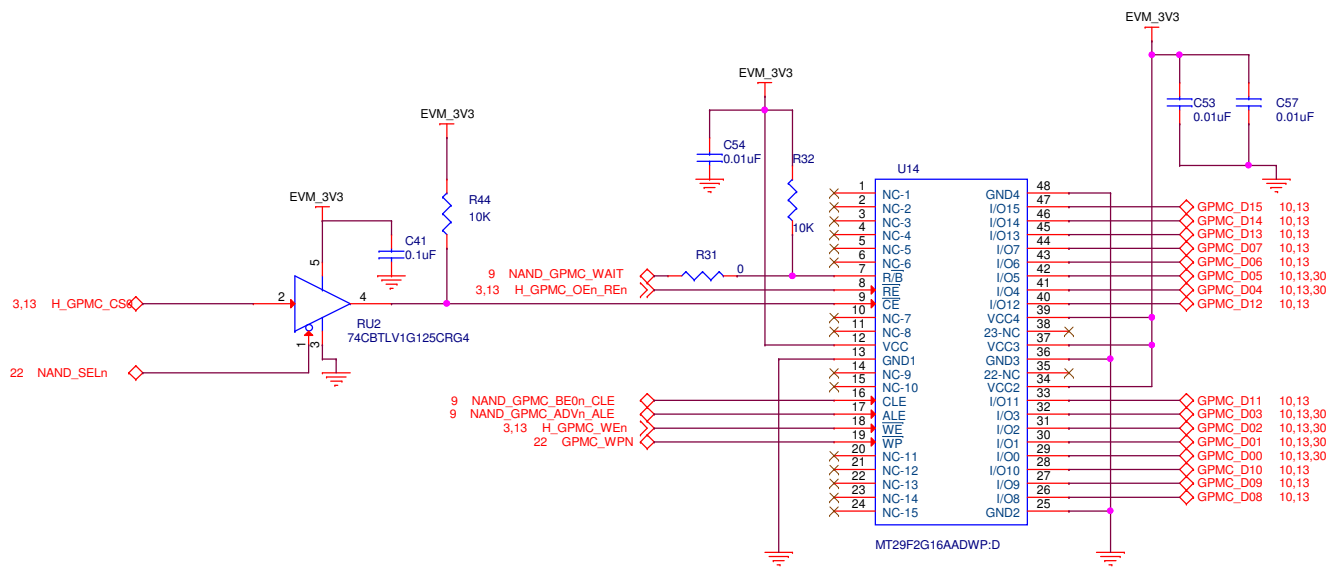


TEXAS INSTRUMENTS INCORPORATED			
Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"			
Page Contents: MUX H/J/K/L MCASP/VIN6A			
Size: C	DOC NO: 518202	REV: A	
Date: Friday, September 08, 2017	Sheet 12	of	30



ROUTE THE FOLLOWING SIGNALS AS A GROUP WITH A NET LENGTH LESS THEN 2.75 INCHES AND 60ps OF SKEW. PLACE THE DUAL RESISTOR CLOSE TOGETHER NEAR THE PIN OF THE FLASH.

AQSPH1_SCLK
AQSPH1_RTCLK
AQSPH1_CS[0]
AQSPH1_D[0]
AQSPH1_D[1]
AQSPH1_D[2]
AQSPH1_D[3]



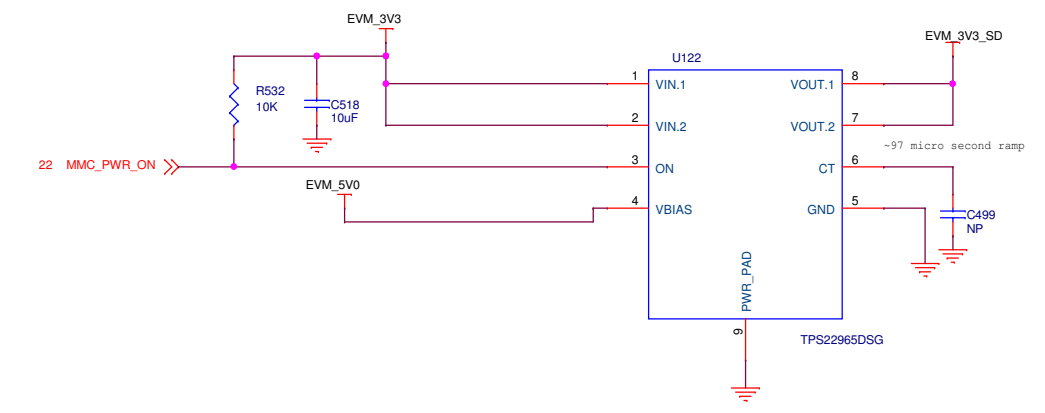
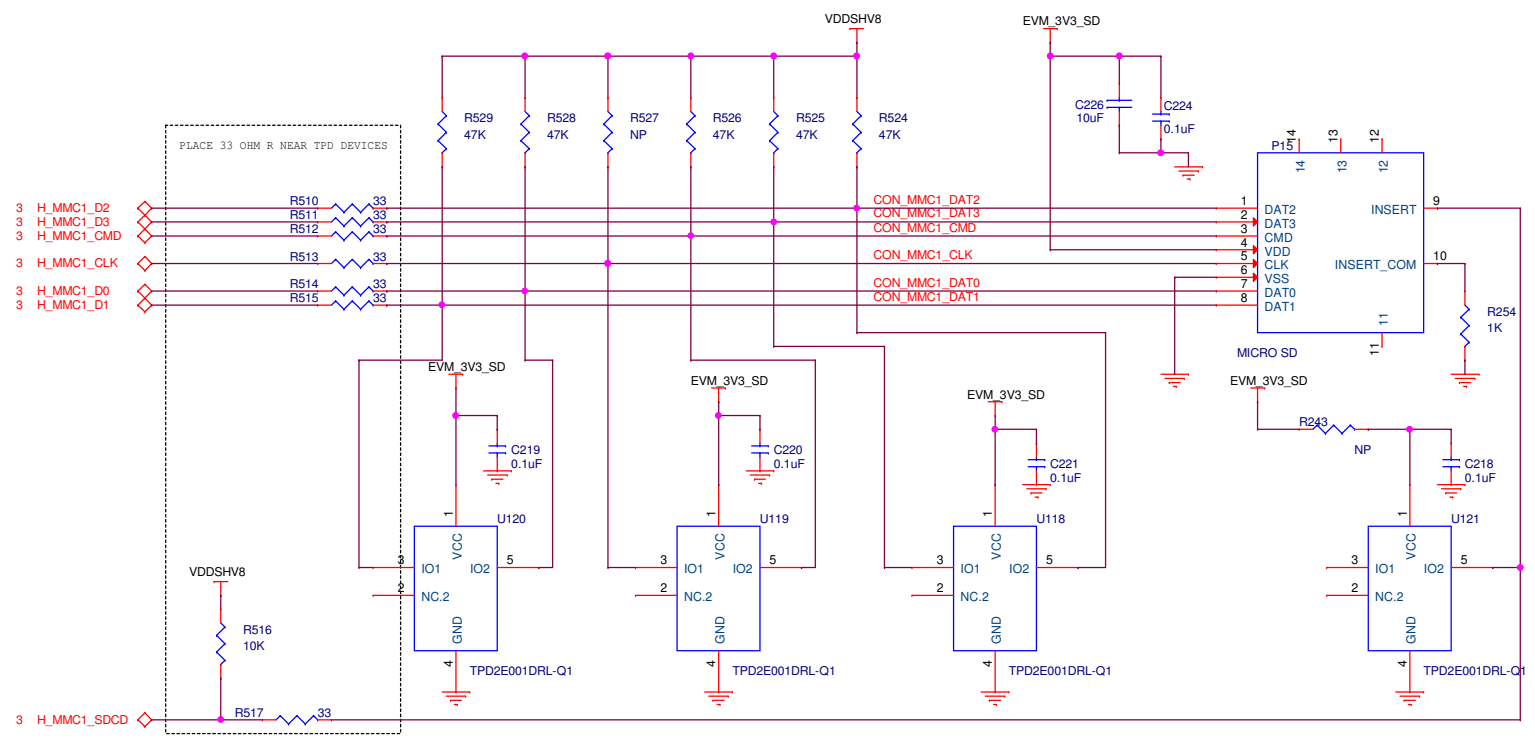
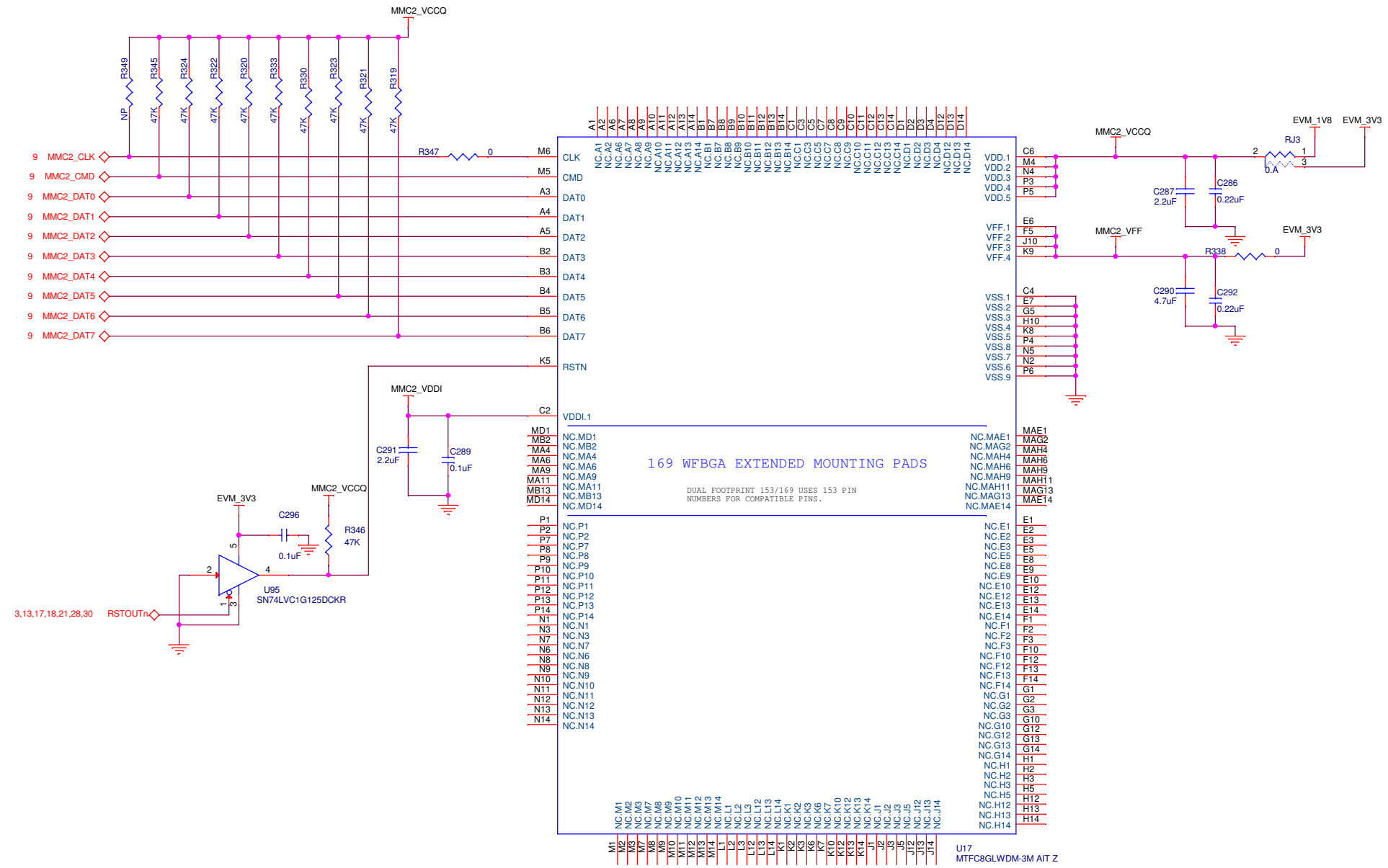
TEXAS INSTRUMENTS INCORPORATED

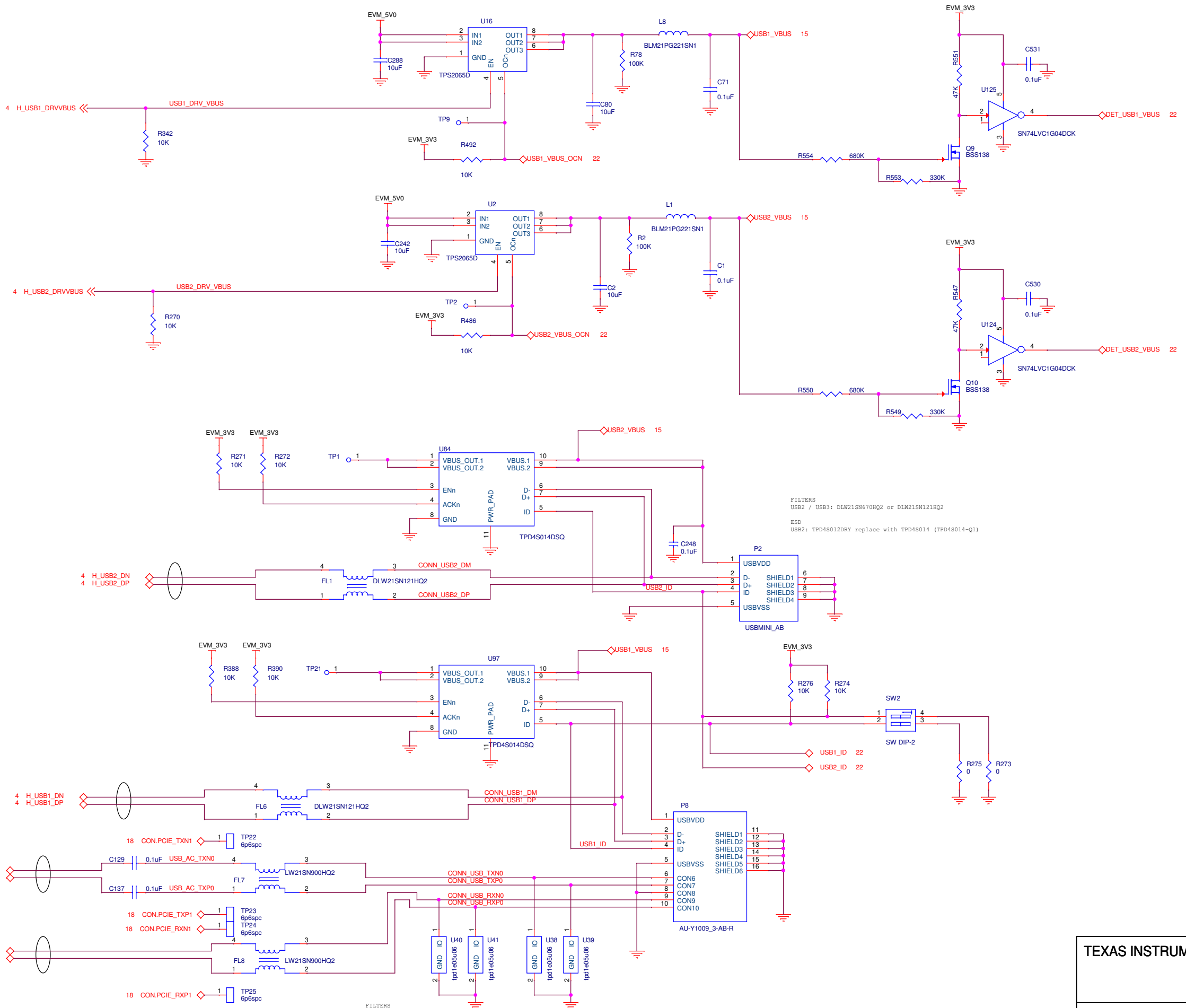
Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: MEM SP/NAND/NOR

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FILTERS
 USB2 / USB3: DLW21SN670HQ2 or DLW21SN121HQ2
 ESD
 USB2: TPD4S012DRY replace with TPD4S014 (TPD4S014-Q1)

FILTERS
 USB2 / USB3: DLW21SN670HQ2 or DLW21SN121HQ2
 ESD
 USB2: TPD4S012DRY replace with TPD4S014 (TPD4S014-Q1)
 USB3: TPD4EUSB930 replace with two TPD2EUSB930 (TPD2EUSB930-Q1) in drt package

PCIE PADS SHARE PIN 1/4 WITH FL2/3.
 FLX NO-POP, PCIE SIGNALS CAN BE POP
 WITH 0201 OR SOLDER BRIDGE.

TEXAS INSTRUMENTS INCORPORATED

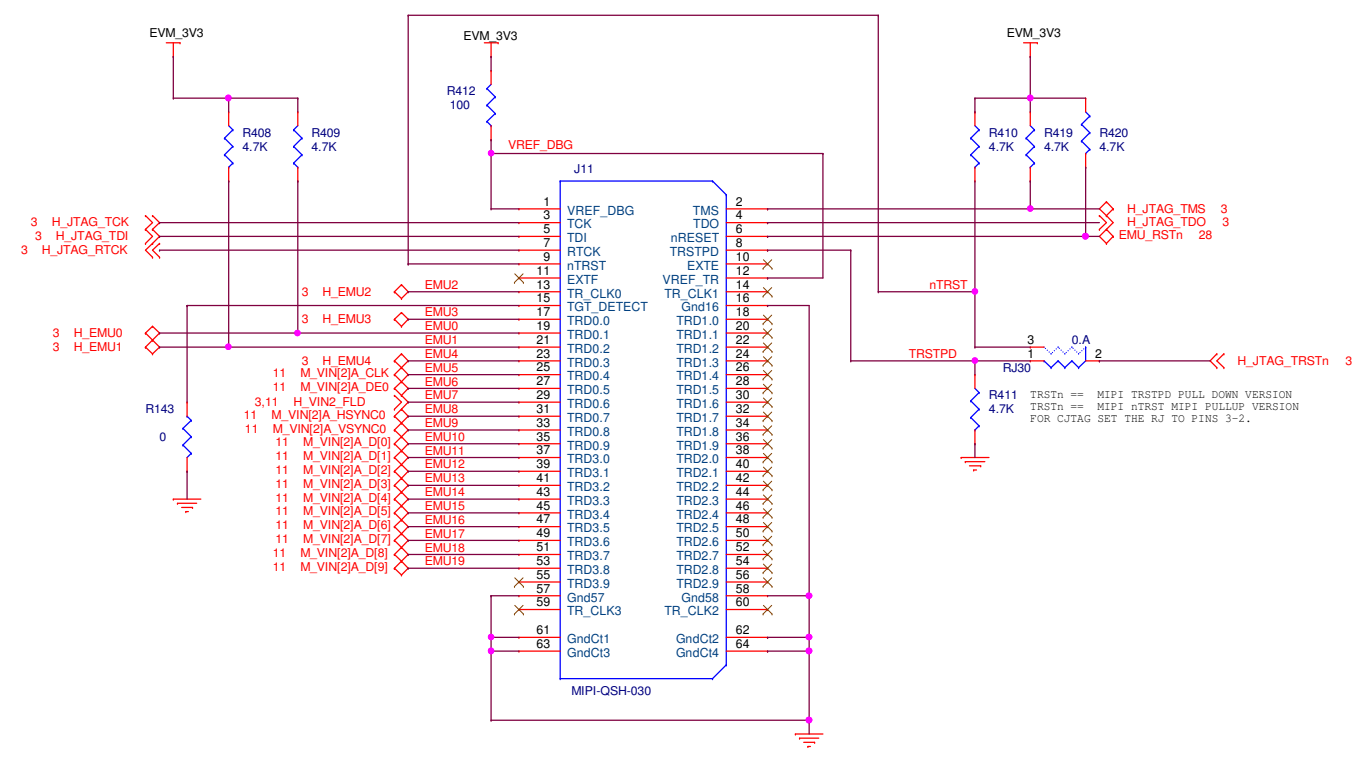
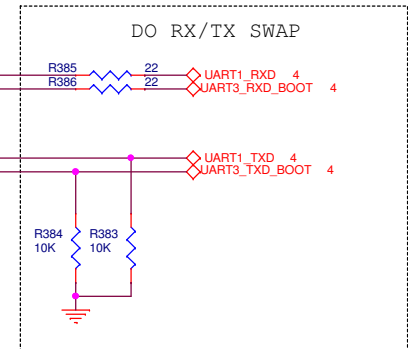
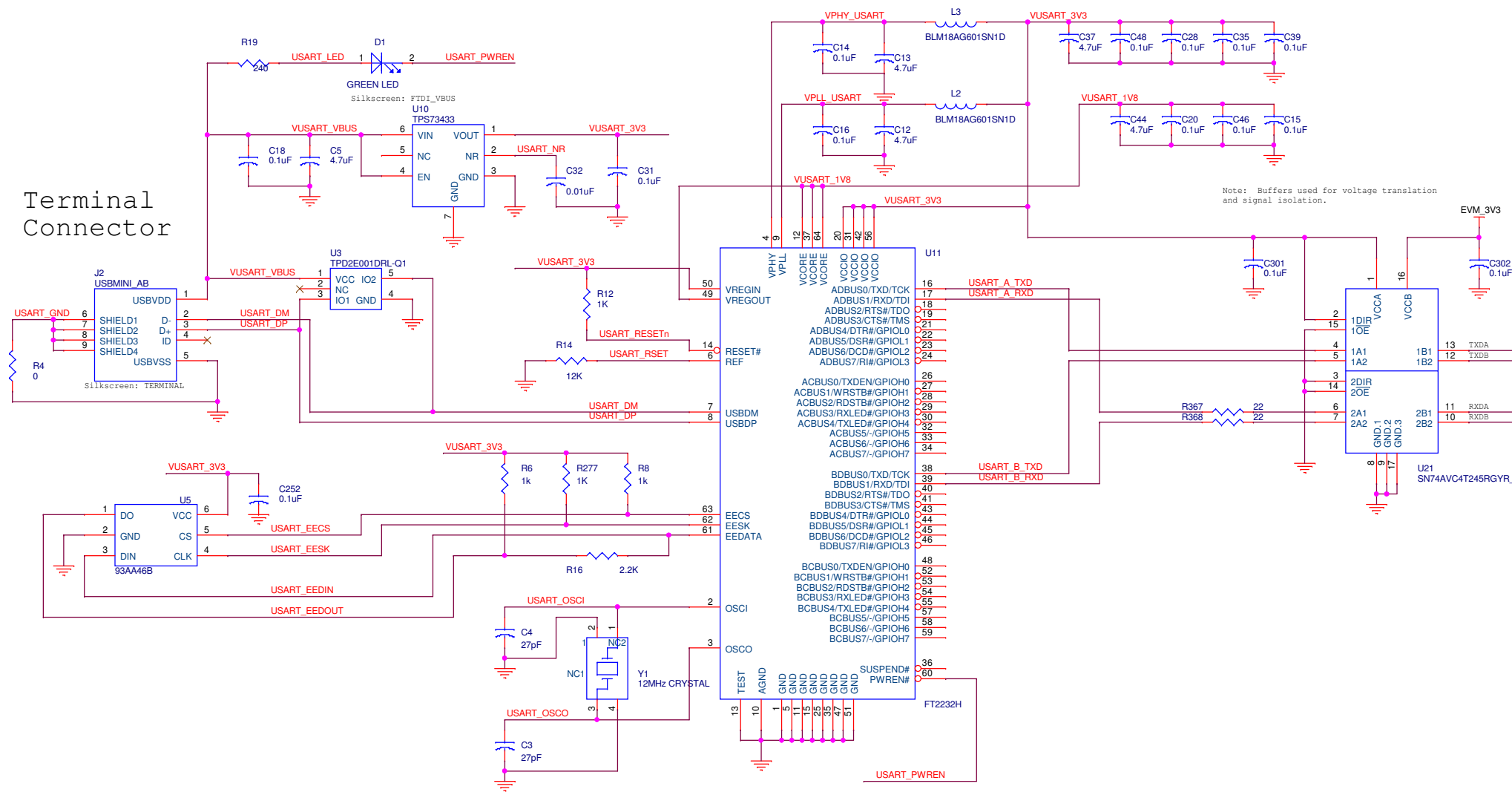
Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: USB VBUS/CONNECTORS

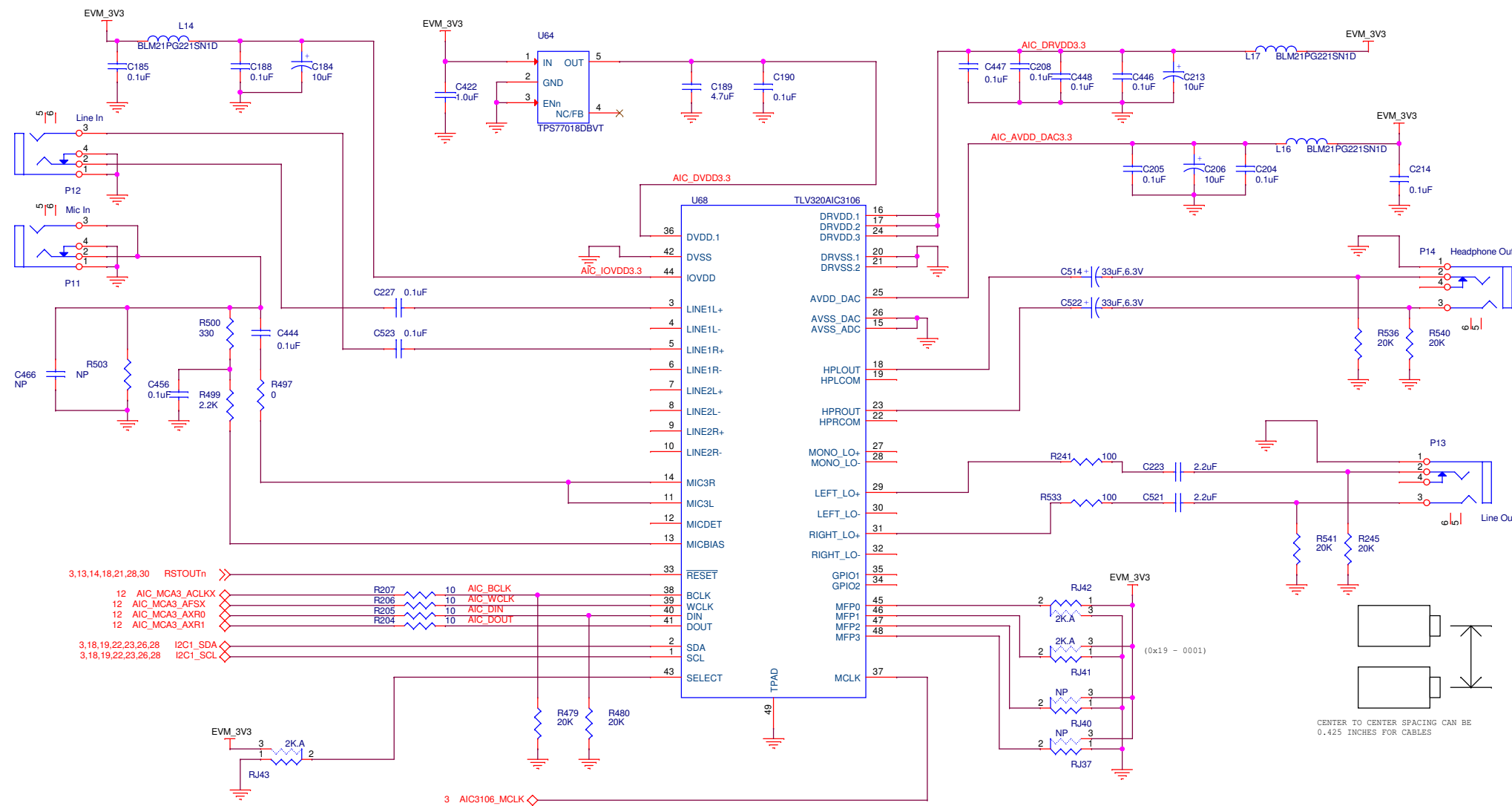
Size: C DOC NO: 518202 REV: A

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Terminal Connector



TEXAS INSTRUMENTS INCORPORATED			
Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"			
Page Contents: USB-UART/JTAG			
Size: C	DOC NO: 518202	REV: A	
Date: Friday, September 08, 2017	Sheet 16	of	30



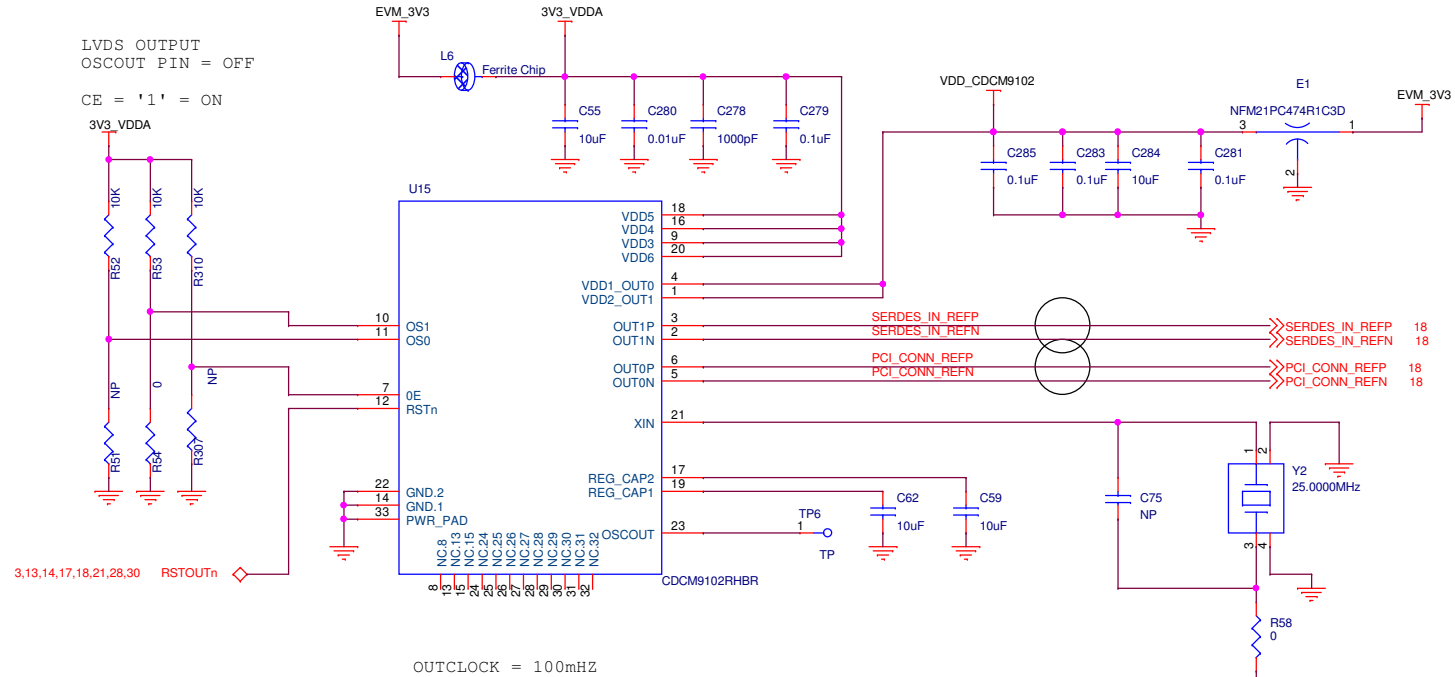
CENTER TO CENTER SPACING CAN BE 0.425 INCHES FOR CABLES

TEXAS INSTRUMENTS INCORPORATED

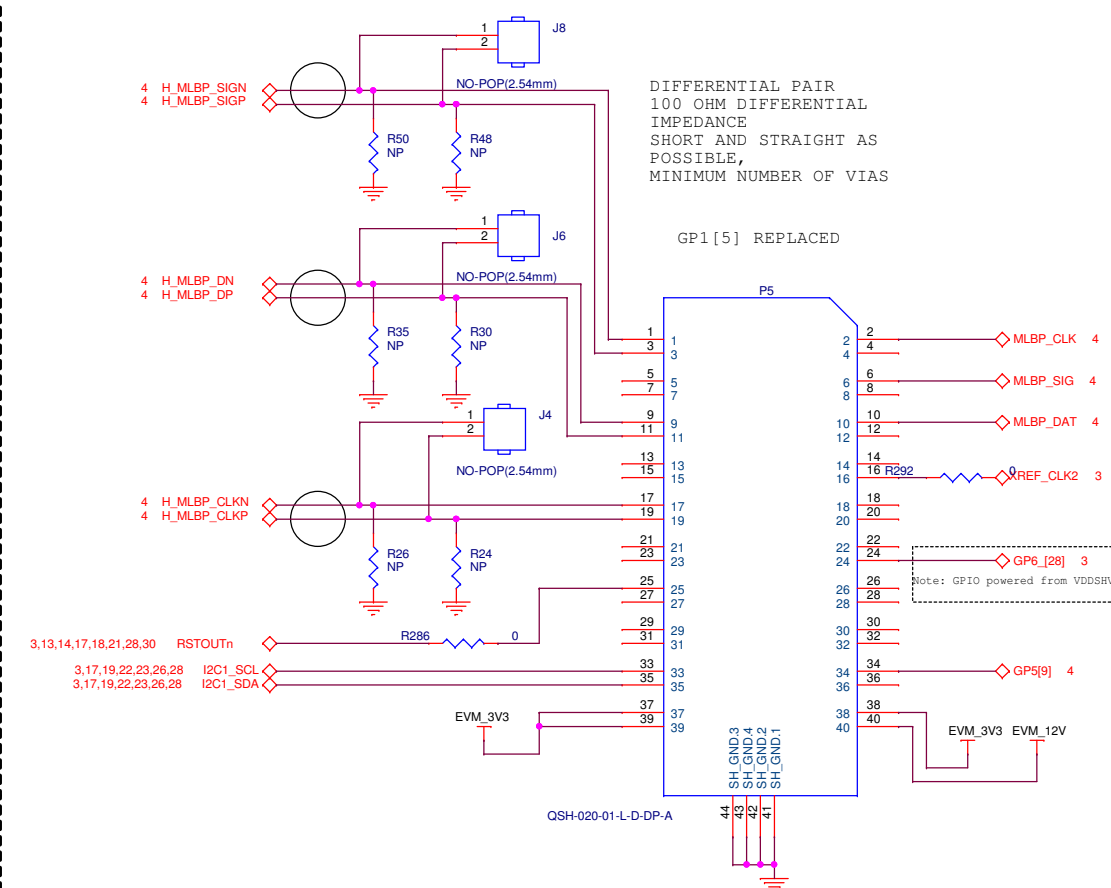
Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"		
Page Contents: AIC3106		
Size: C	DOC NO: 518202	REV: A
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LVDS OUTPUT
OSCOU_T PIN = OFF

CE = '1' = ON



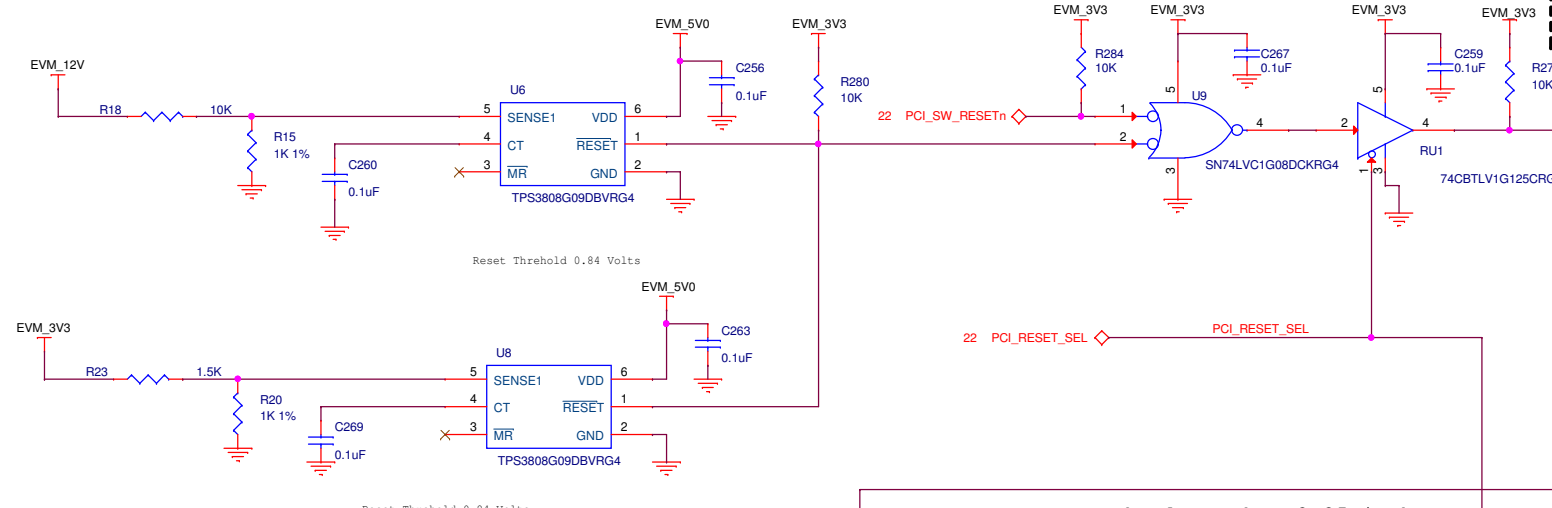
OUTCLOCK = 100mHz



DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

GP1[5] REPLACED

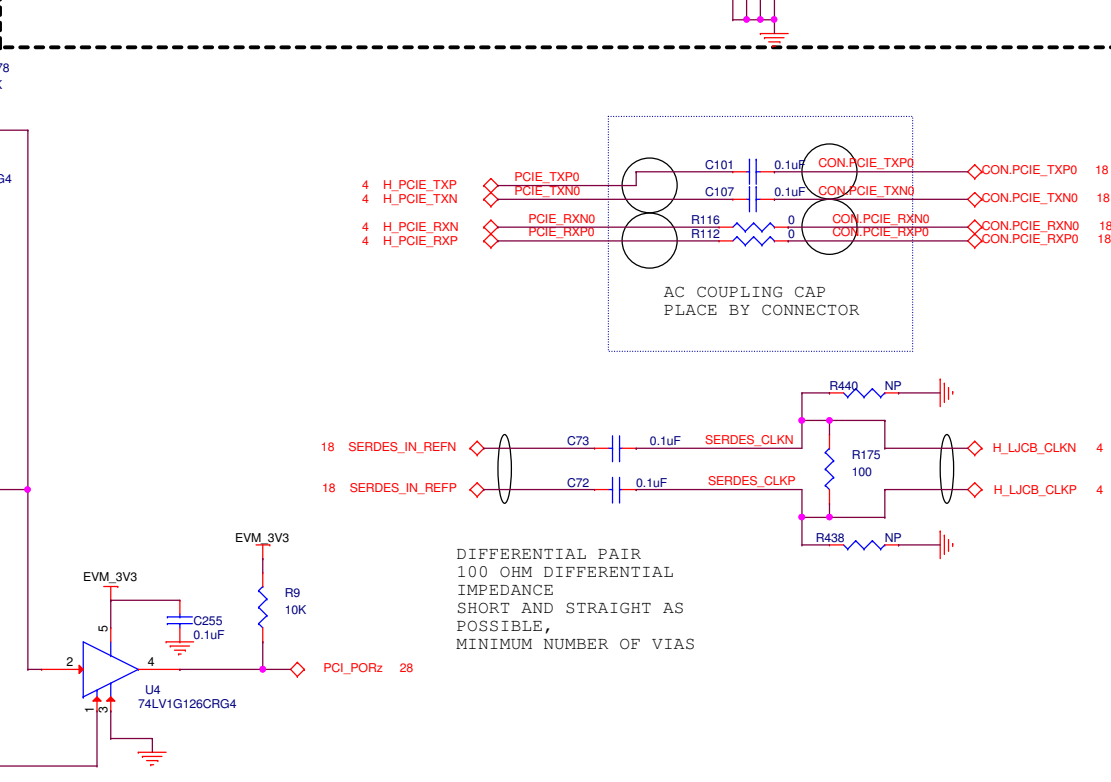
QSH-020-01-L-D-DP-A



Reset Threshold 0.84 Volts

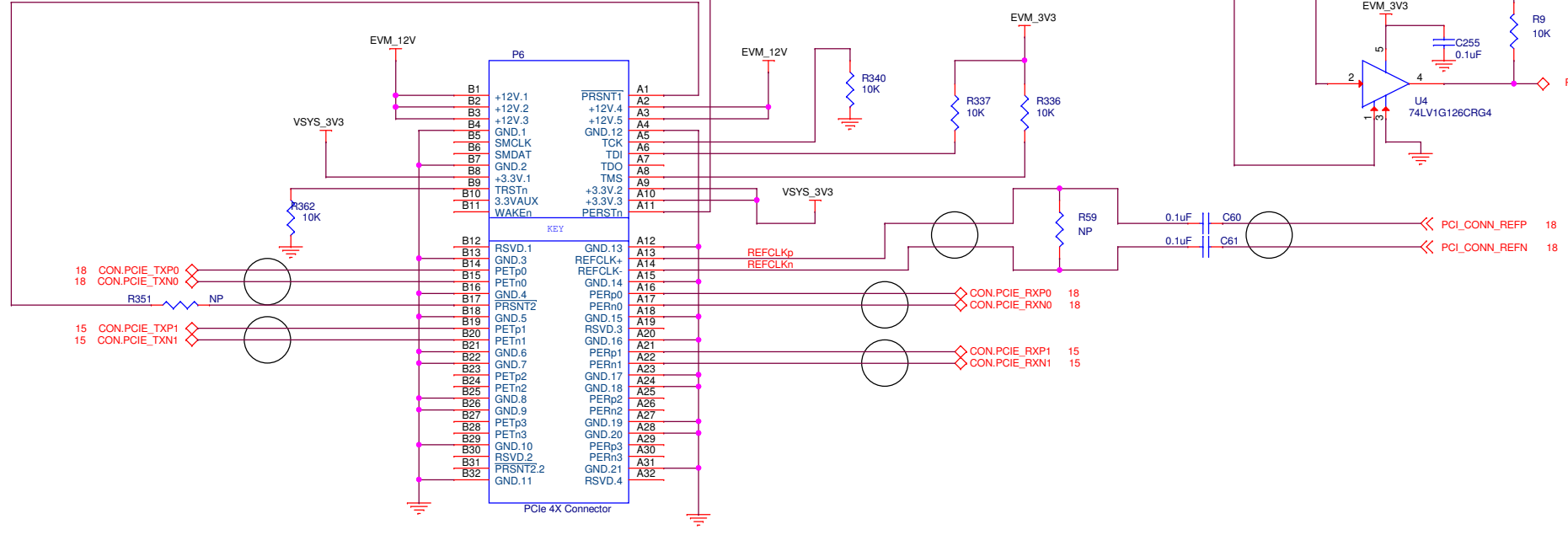
Reset Threshold 0.84 Volts

Connector must be less than 2.25 inches
to board edge from key to board edge



AC COUPLING CAP
PLACE BY CONNECTOR

DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS



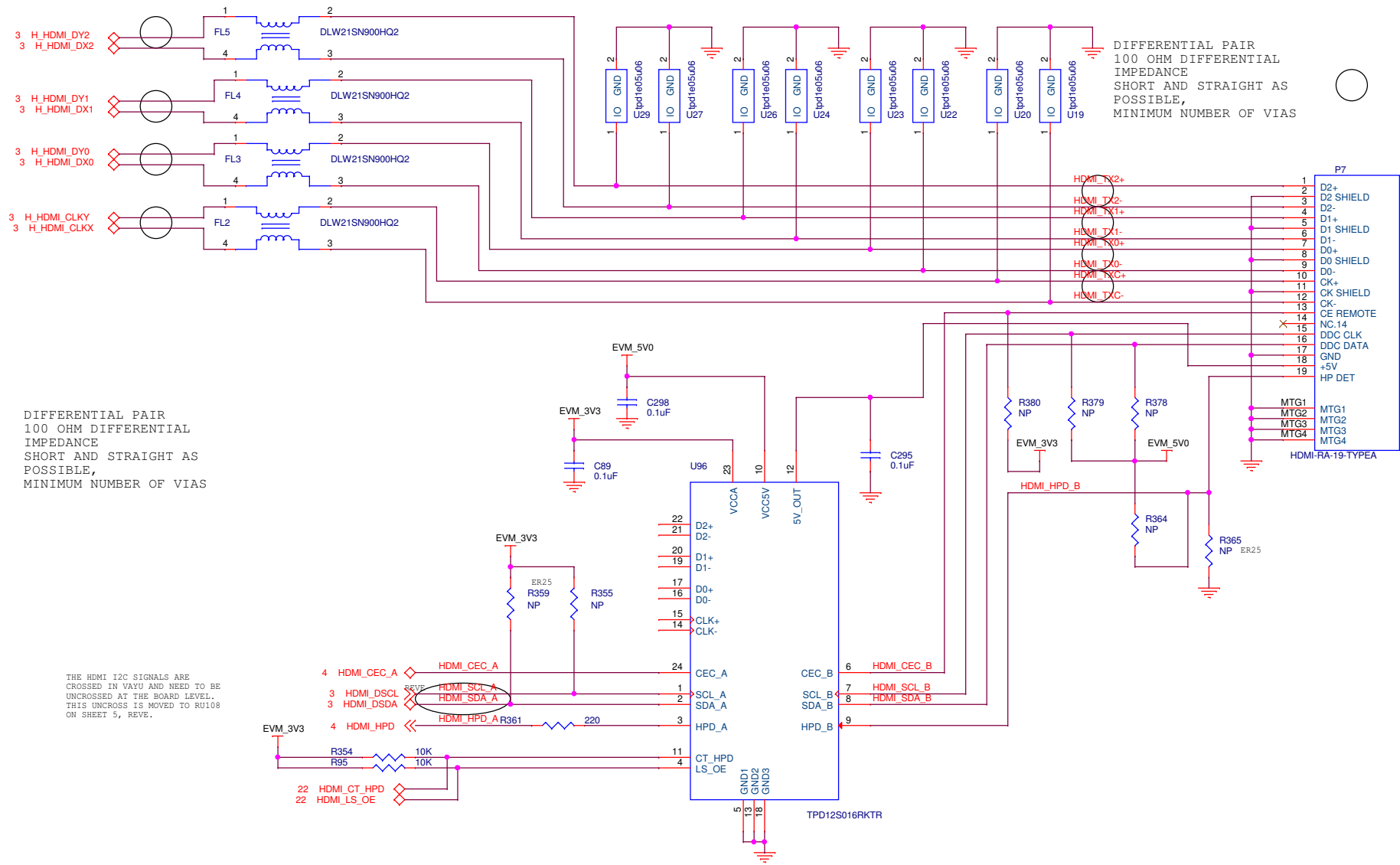
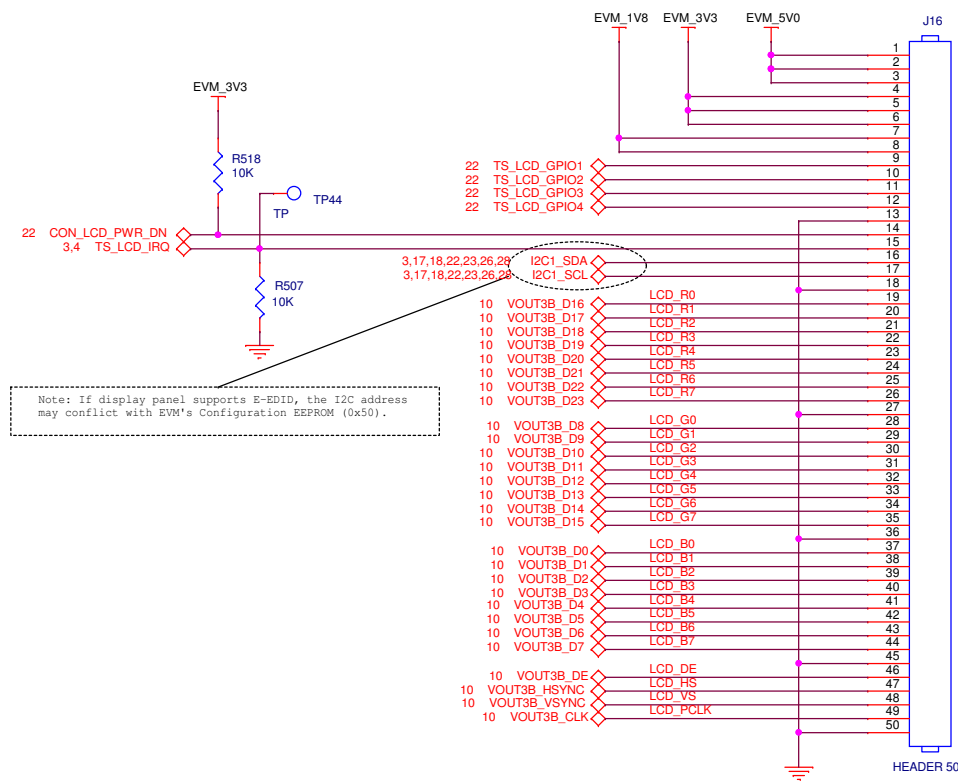
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: SERDES CLK/PCIE/MLB CONN

Size: C DOC NO: 518202 REV: A

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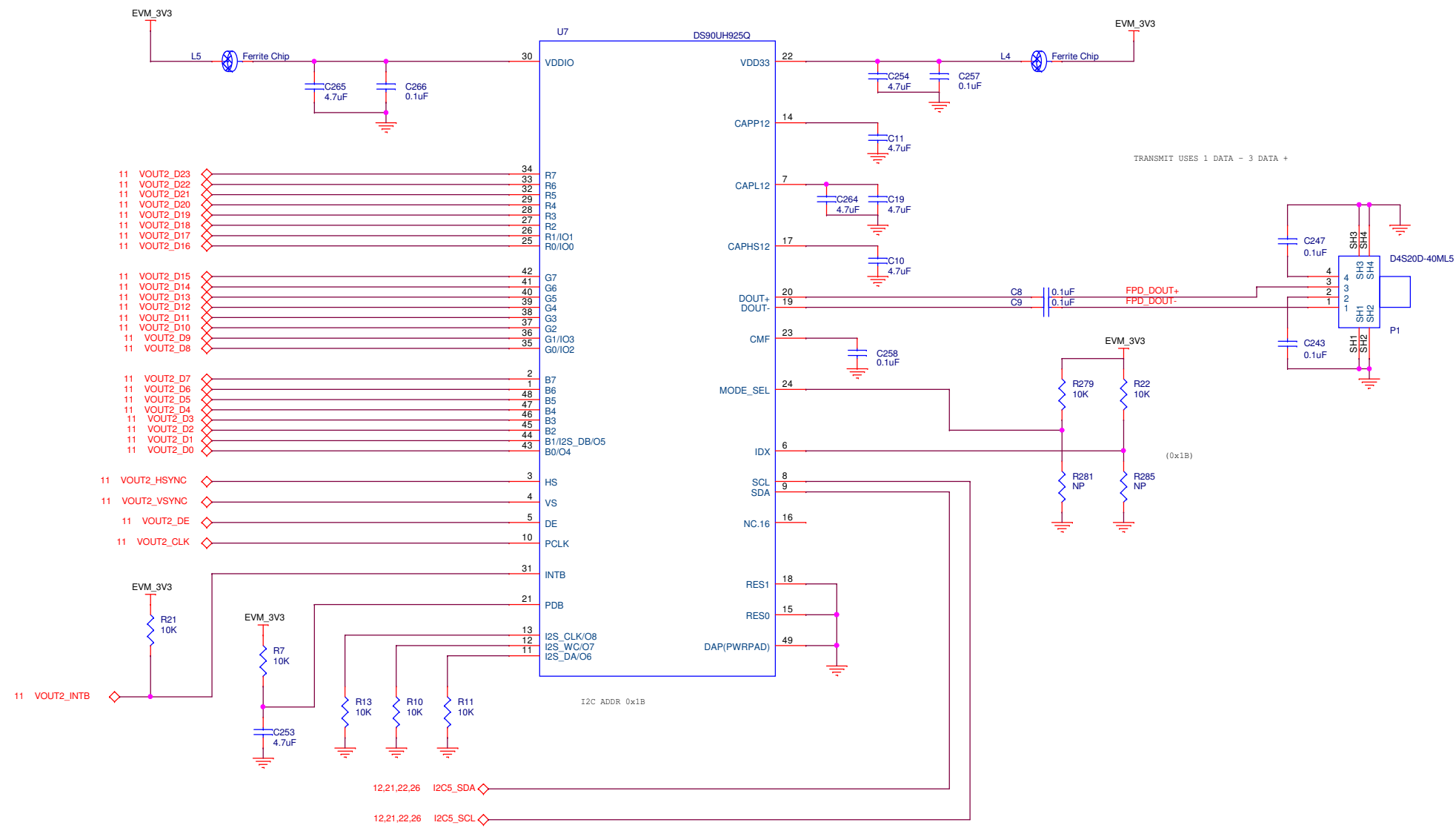
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: LCD/HDMI CONNECTORS

Size: C DOC NO: 518202 REV: A

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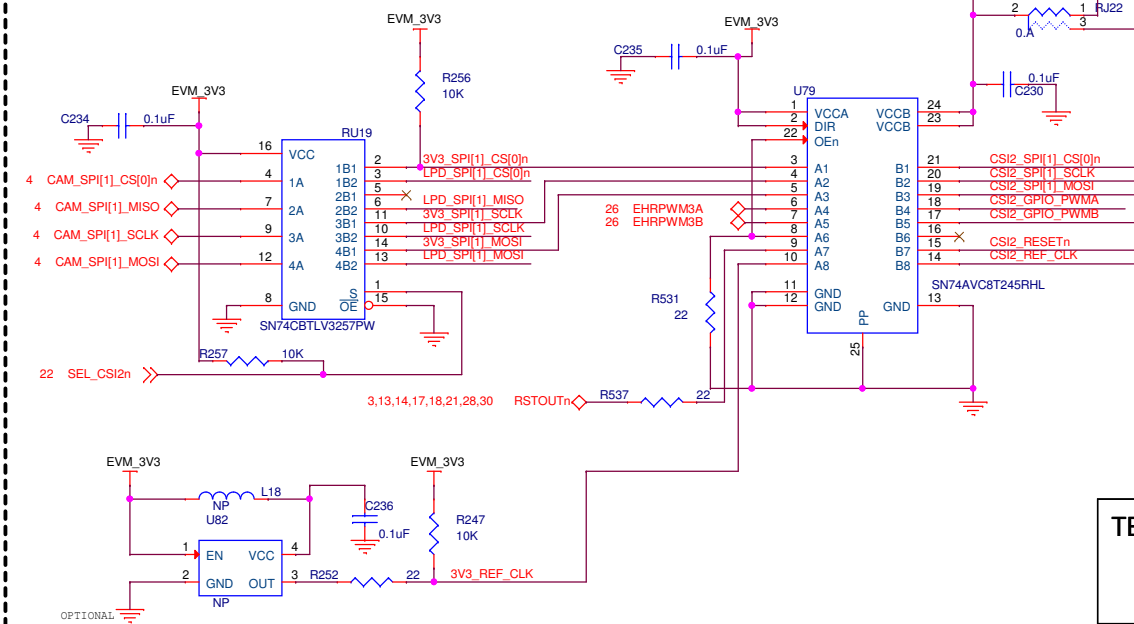
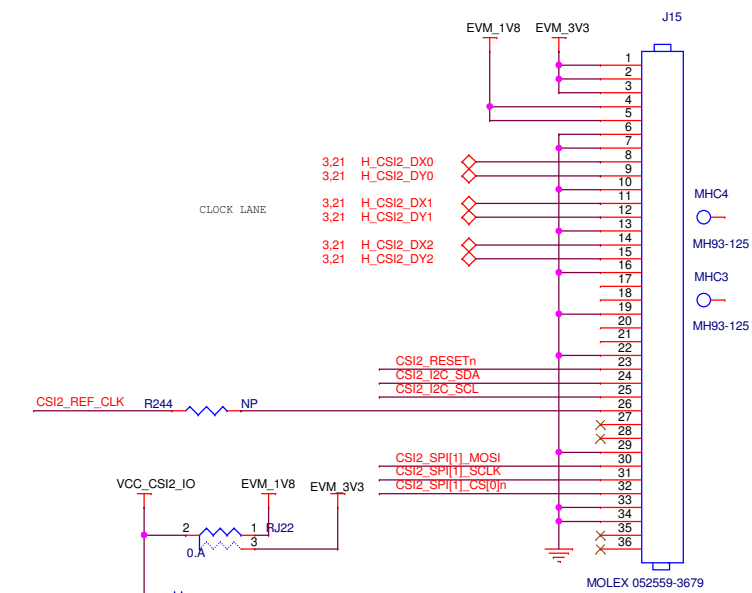
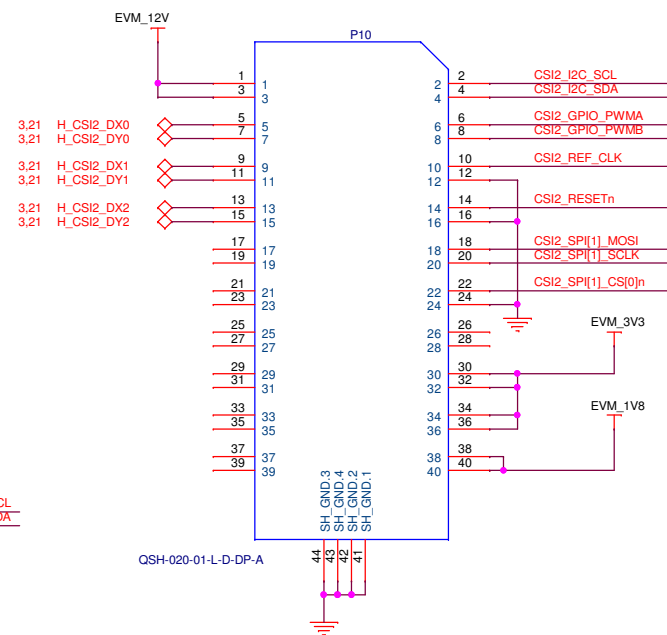
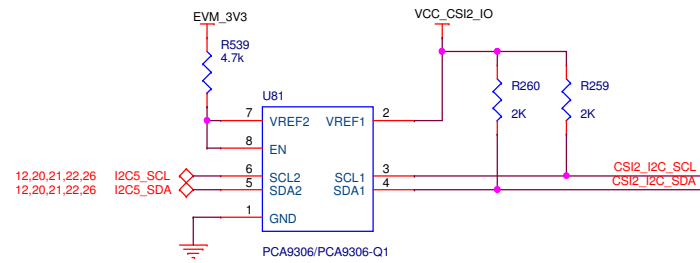
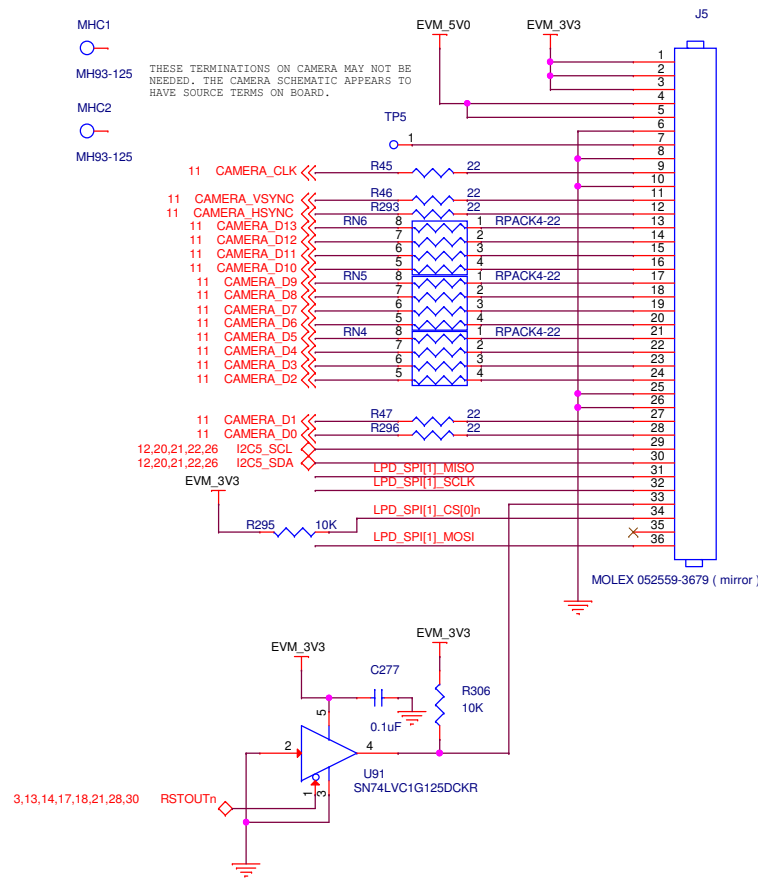
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: FPD LINK

Size: C DOC NO: 518202 REV: A

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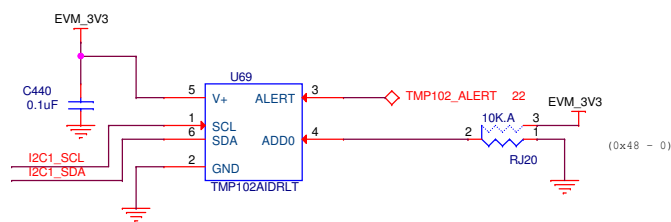
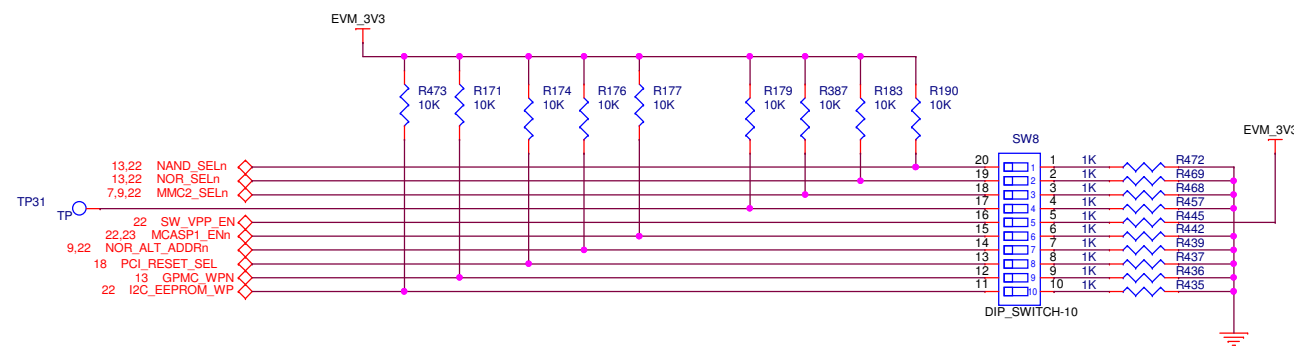
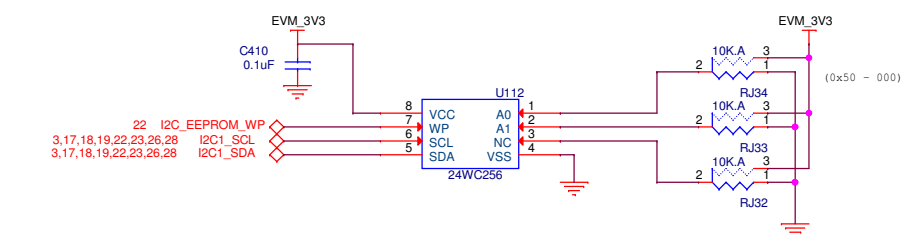
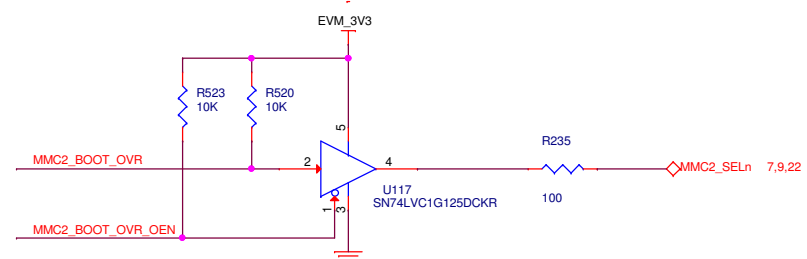
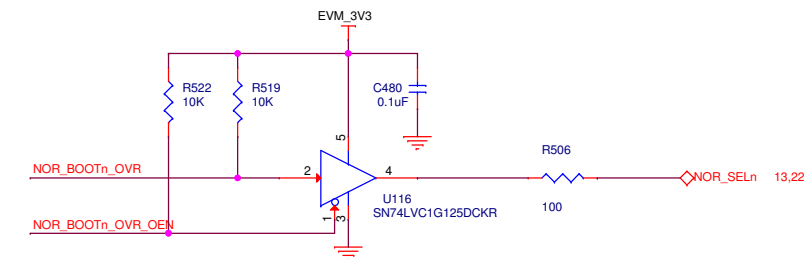
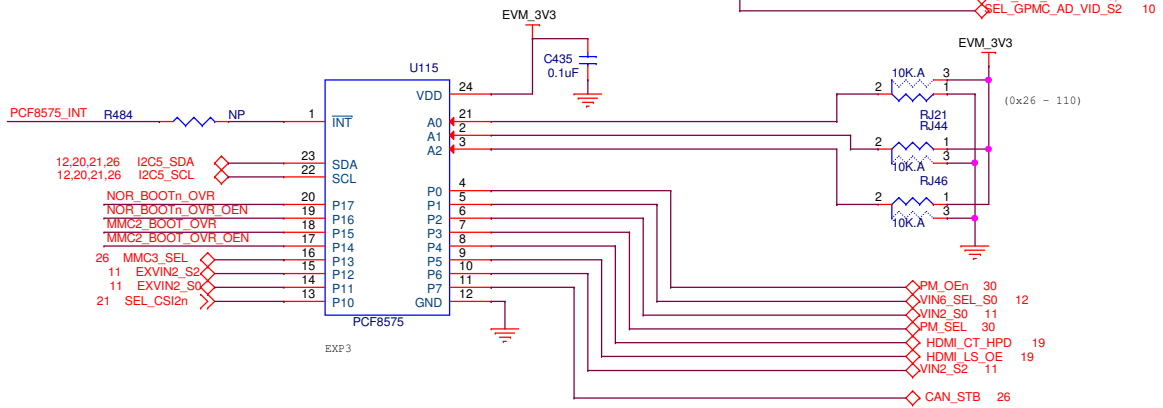
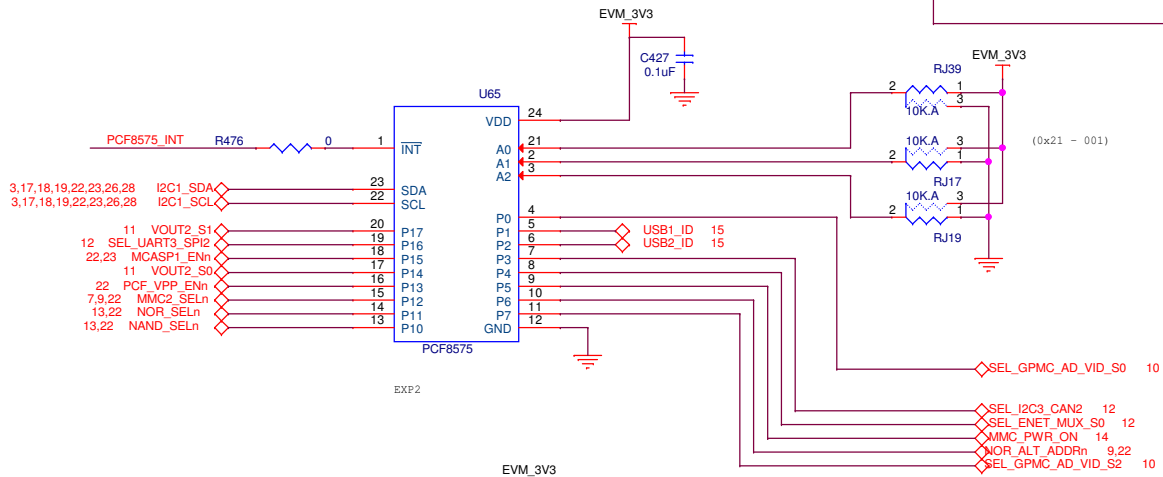
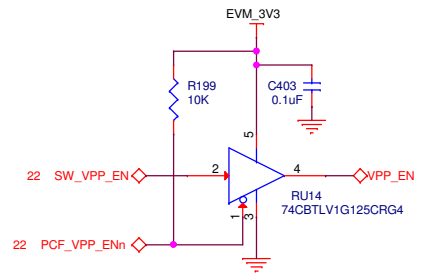
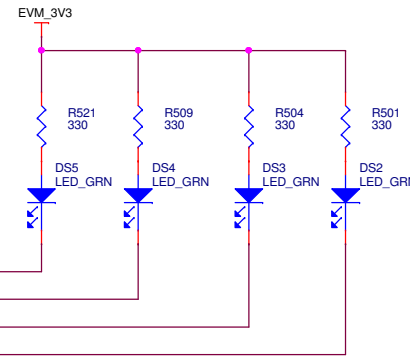
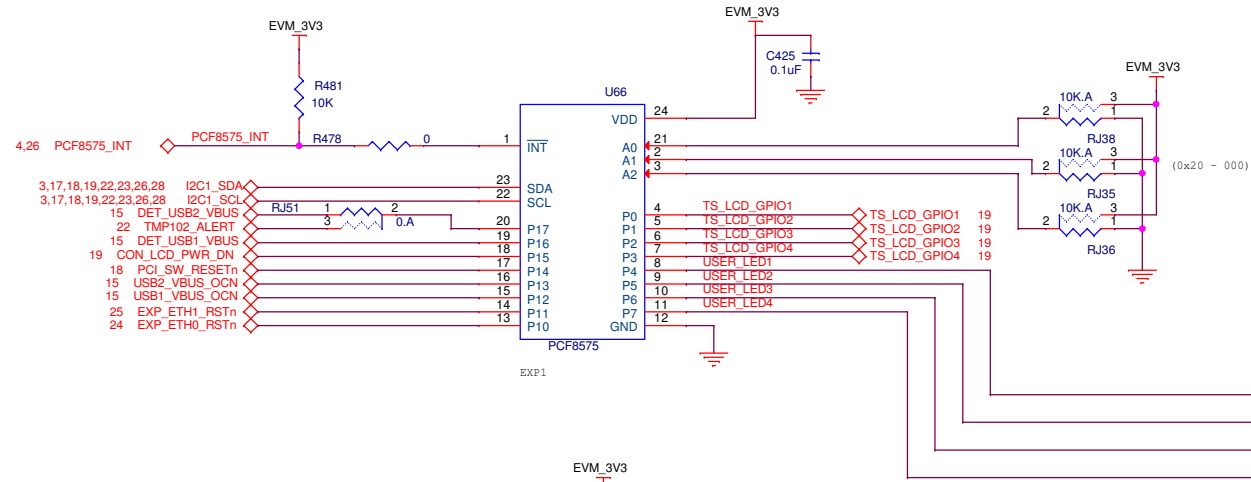
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: CAMERA IF

Size: C DOC NO: 518202 REV: C

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PLACE TEMP SENSOR CLOSE TO PROCESSOR

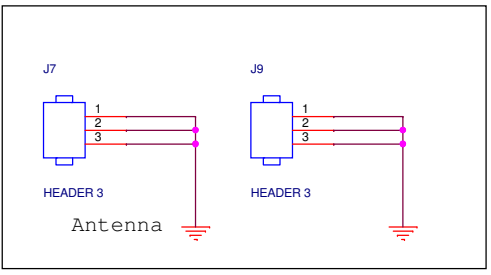
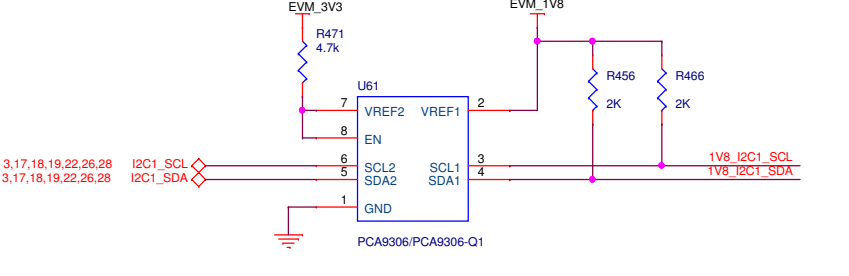
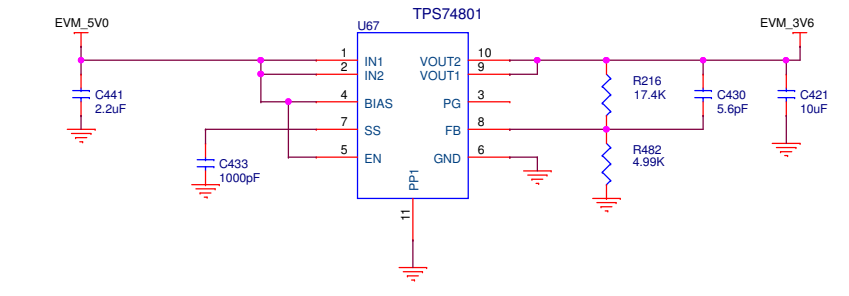
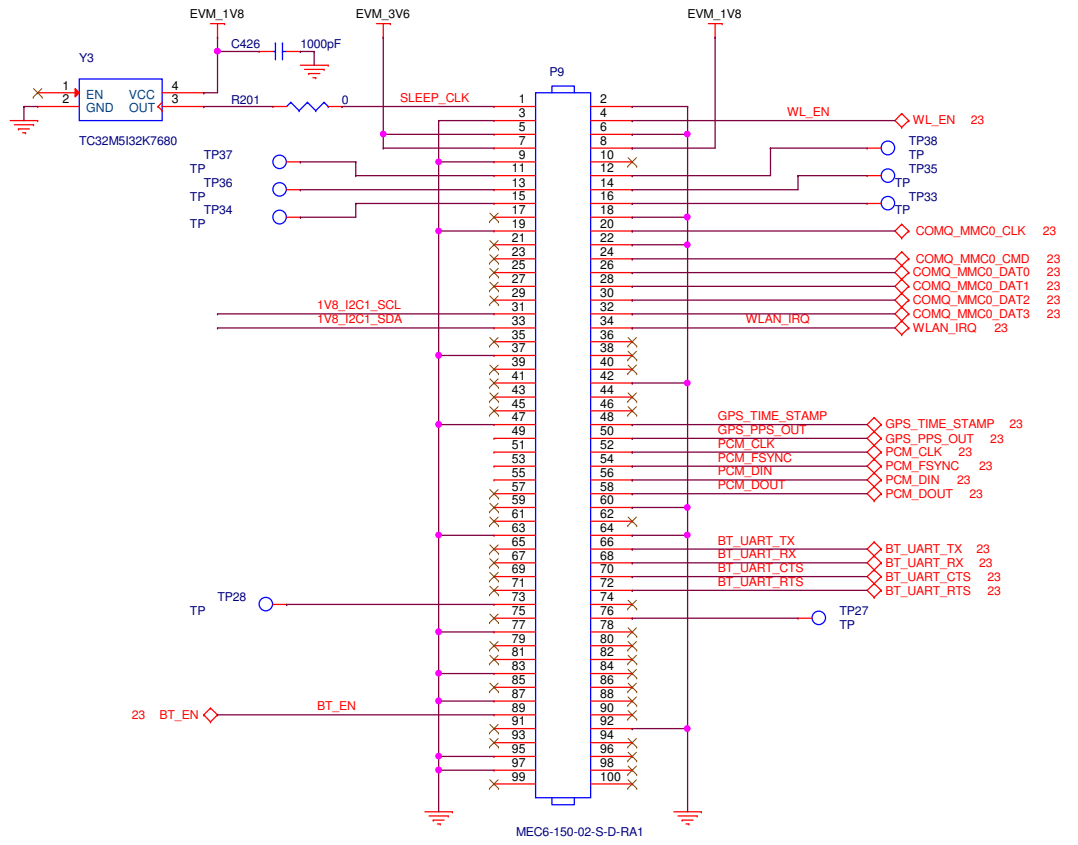
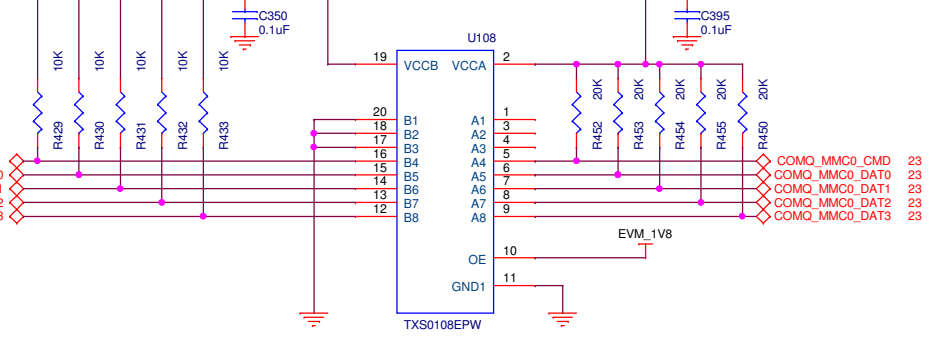
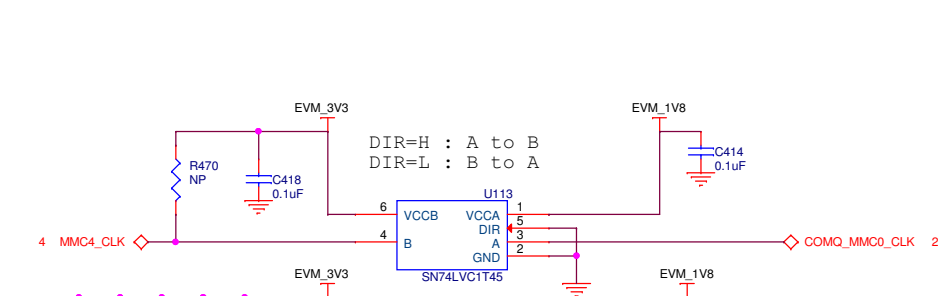
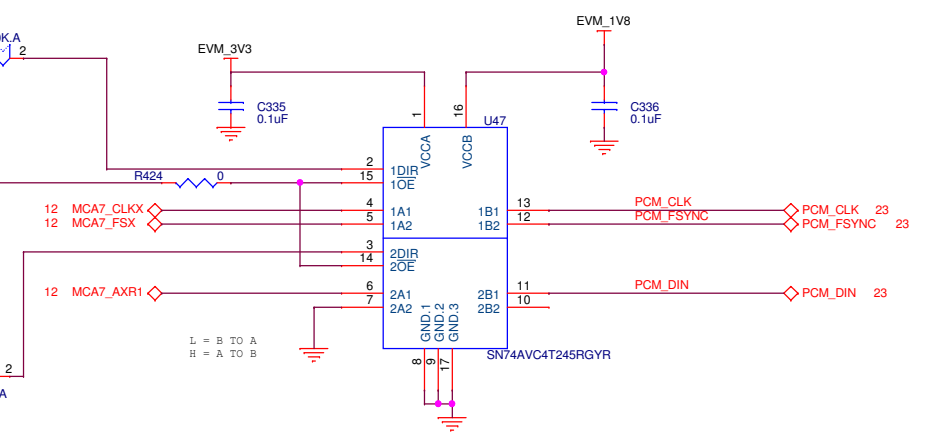
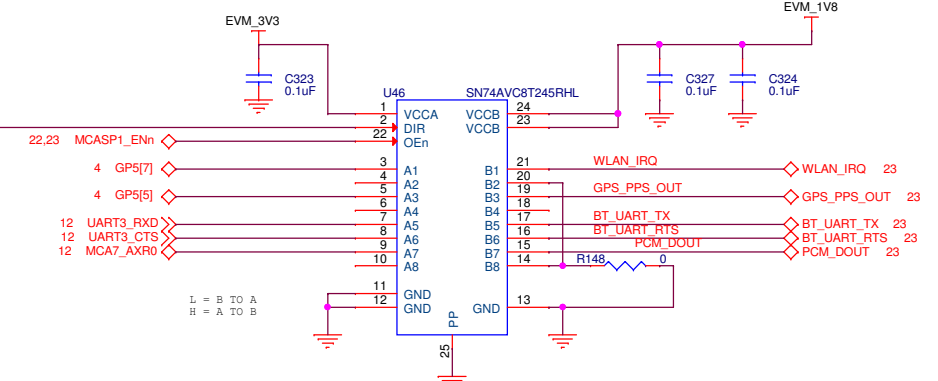
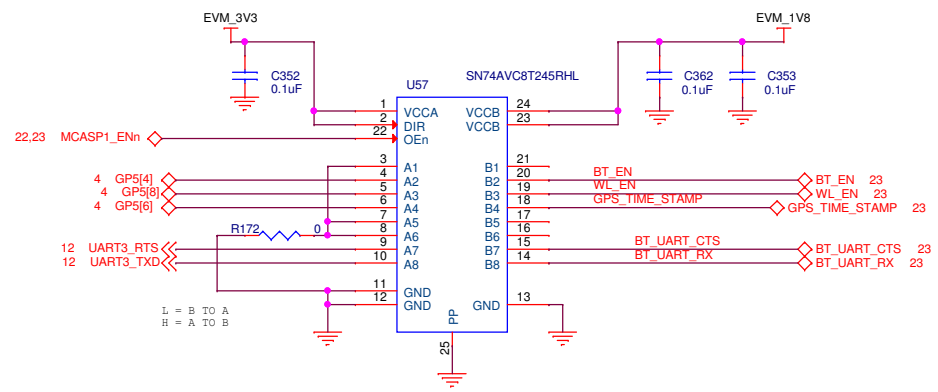
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: I2C EXP/ EEPROM/TEMP

Size: C DOC NO: 518202 REV: C

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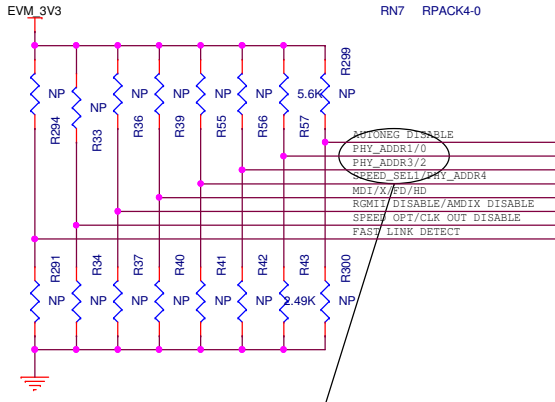
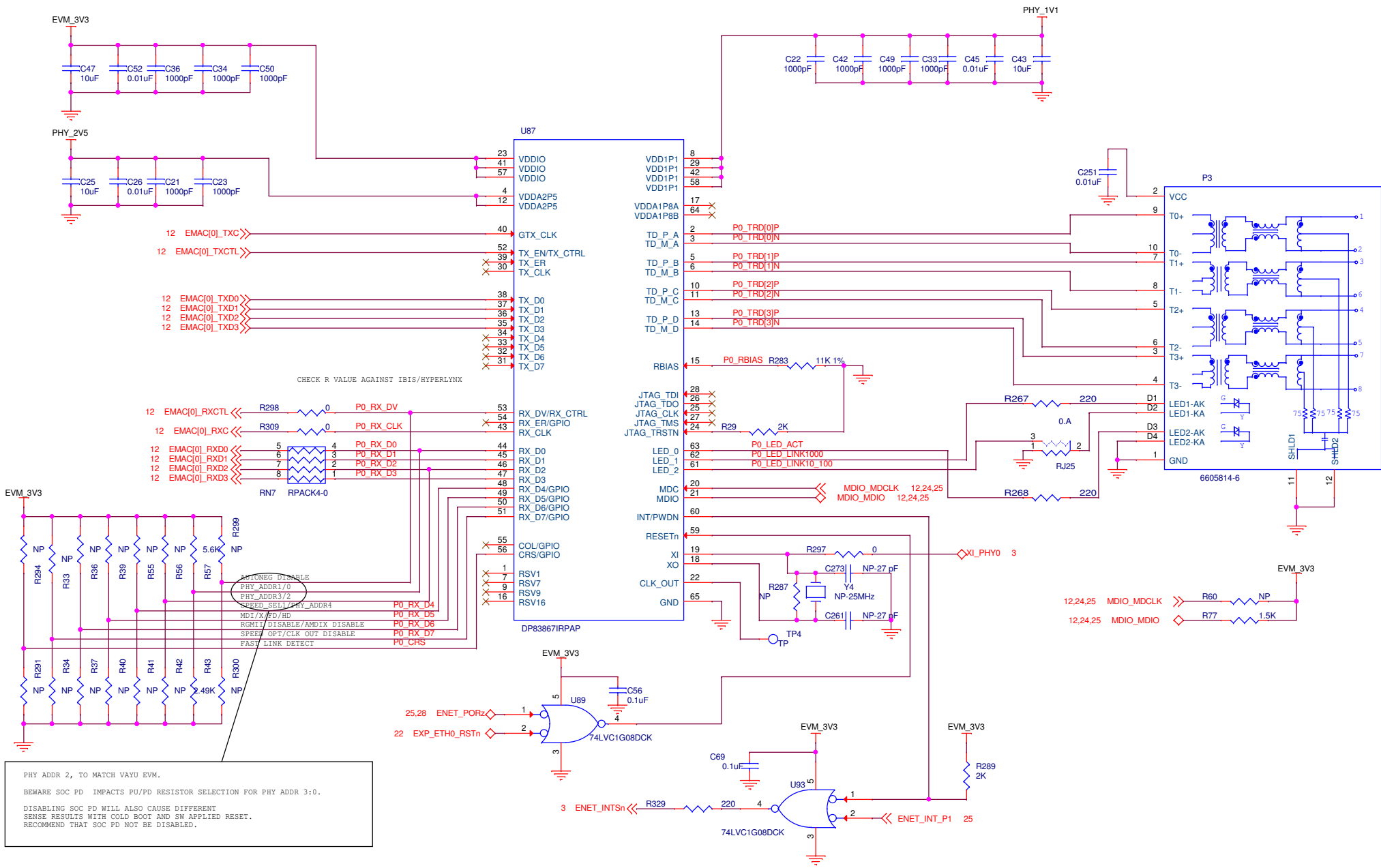
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Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

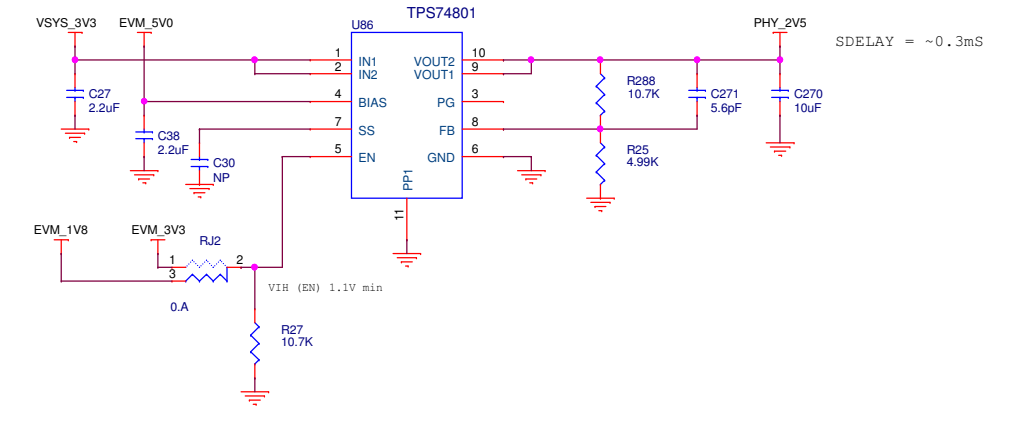
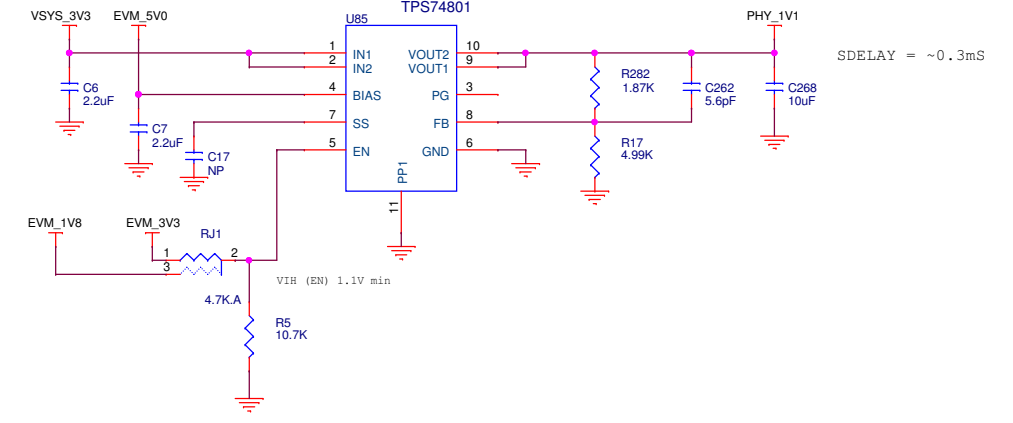
Page Contents: COM8

Size: C	DOC NO: 518202	REV: A
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PHY ADDR 2, TO MATCH VAYU EVM.
 BEWARE SOC PD IMPACTS PU/PD RESISTOR SELECTION FOR PHY ADDR 3:0.
 DISABLING SOC PD WILL ALSO CAUSE DIFFERENT SENSE RESULTS WITH COLD BOOT AND SW APPLIED RESET. RECOMMEND THAT SOC PD NOT BE DISABLED.



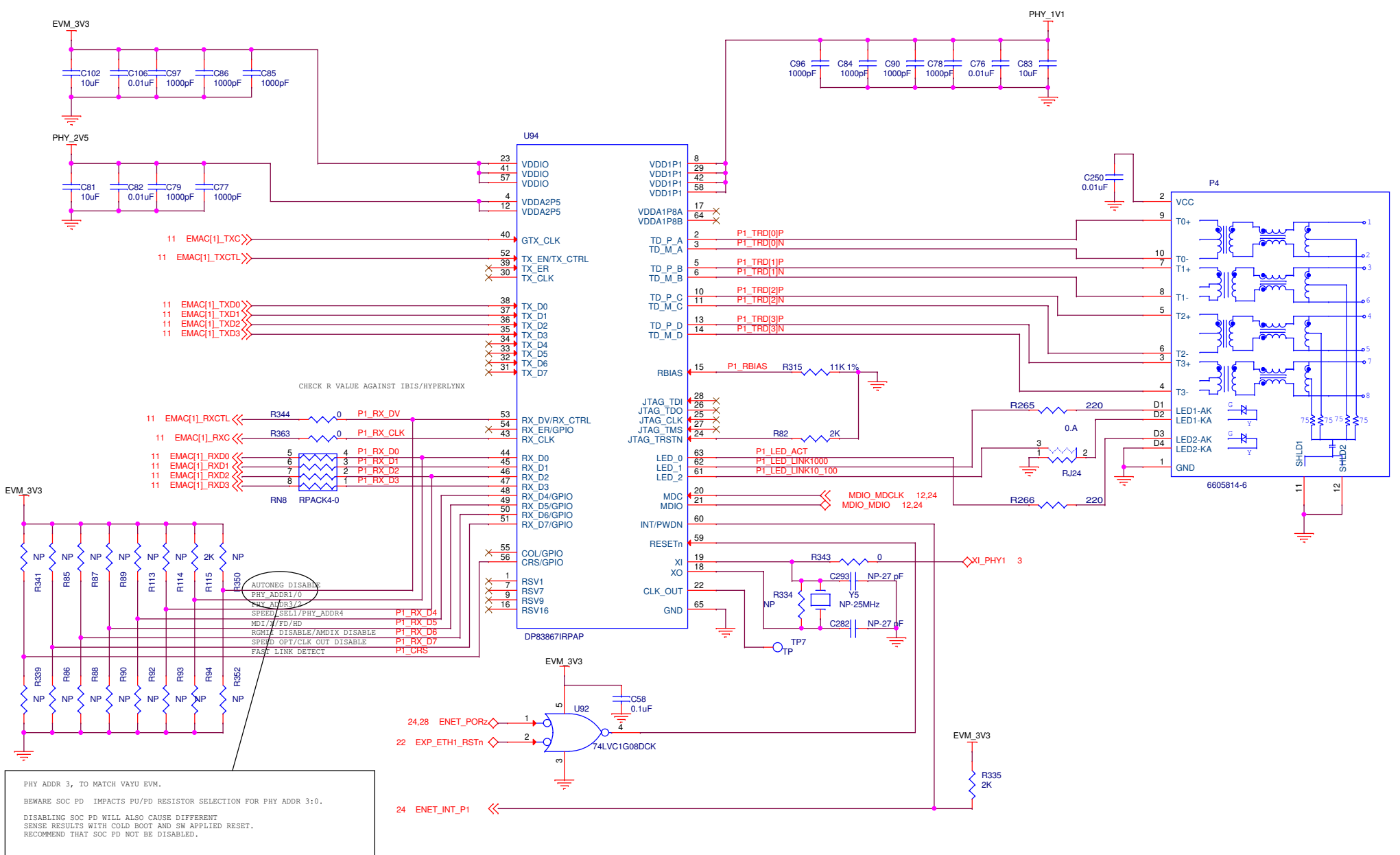
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: ETHERNET PORT0

Size: C DOC NO: 518202 REV: A1

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PHY_ADDR3, TO MATCH VAYU EVM.
 BEWARE SOC PD IMPACTS PU/PD RESISTOR SELECTION FOR PHY_ADDR3:0.
 DISABLING SOC PD WILL ALSO CAUSE DIFFERENT SENSE RESULTS WITH COLD BOOT AND SW APPLIED RESET. RECOMMEND THAT SOC PD NOT BE DISABLED.

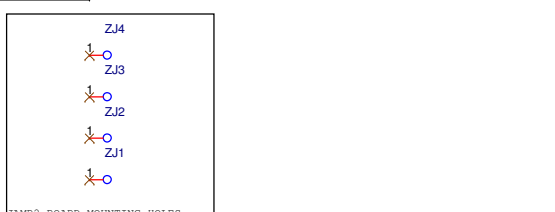
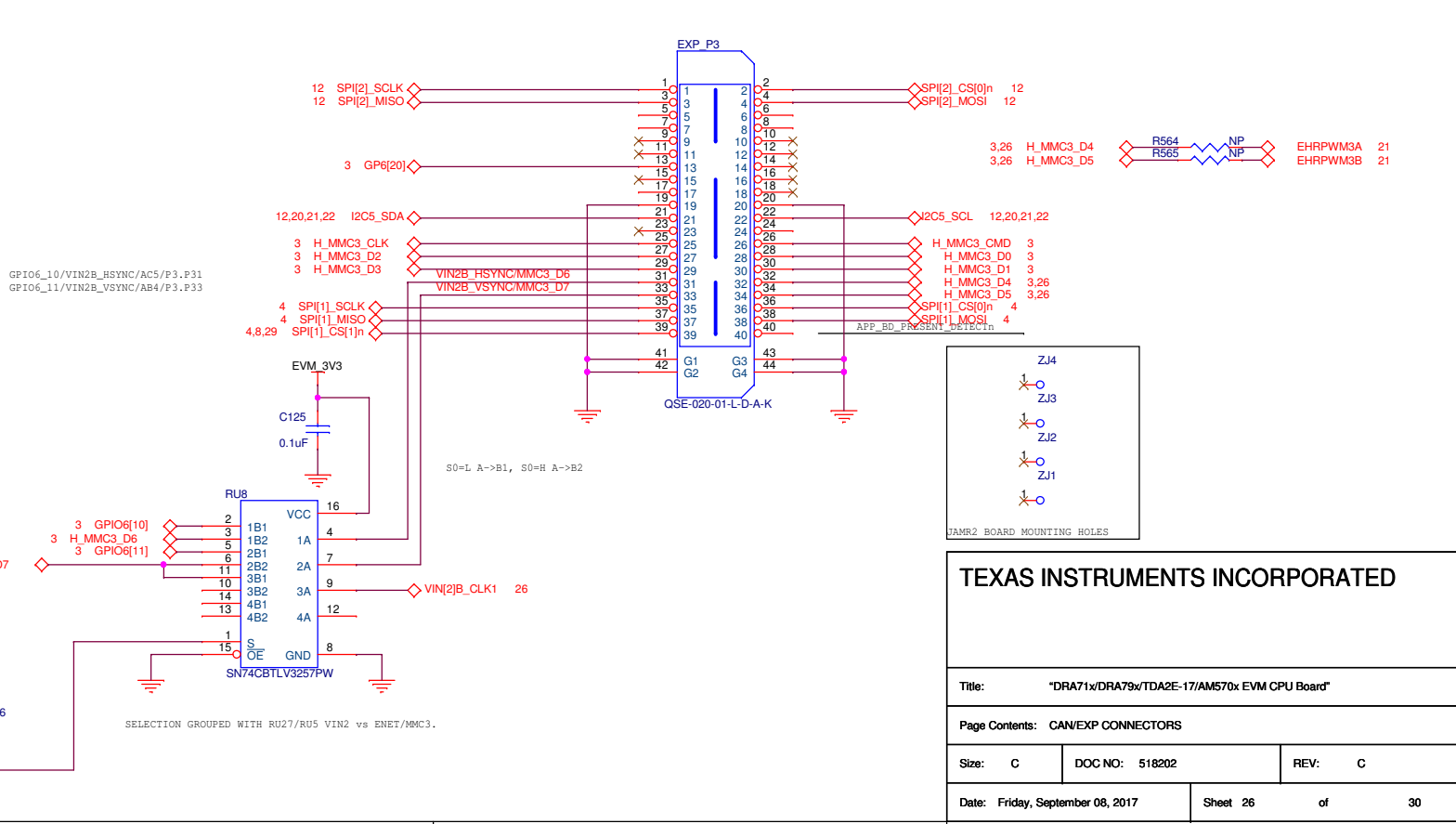
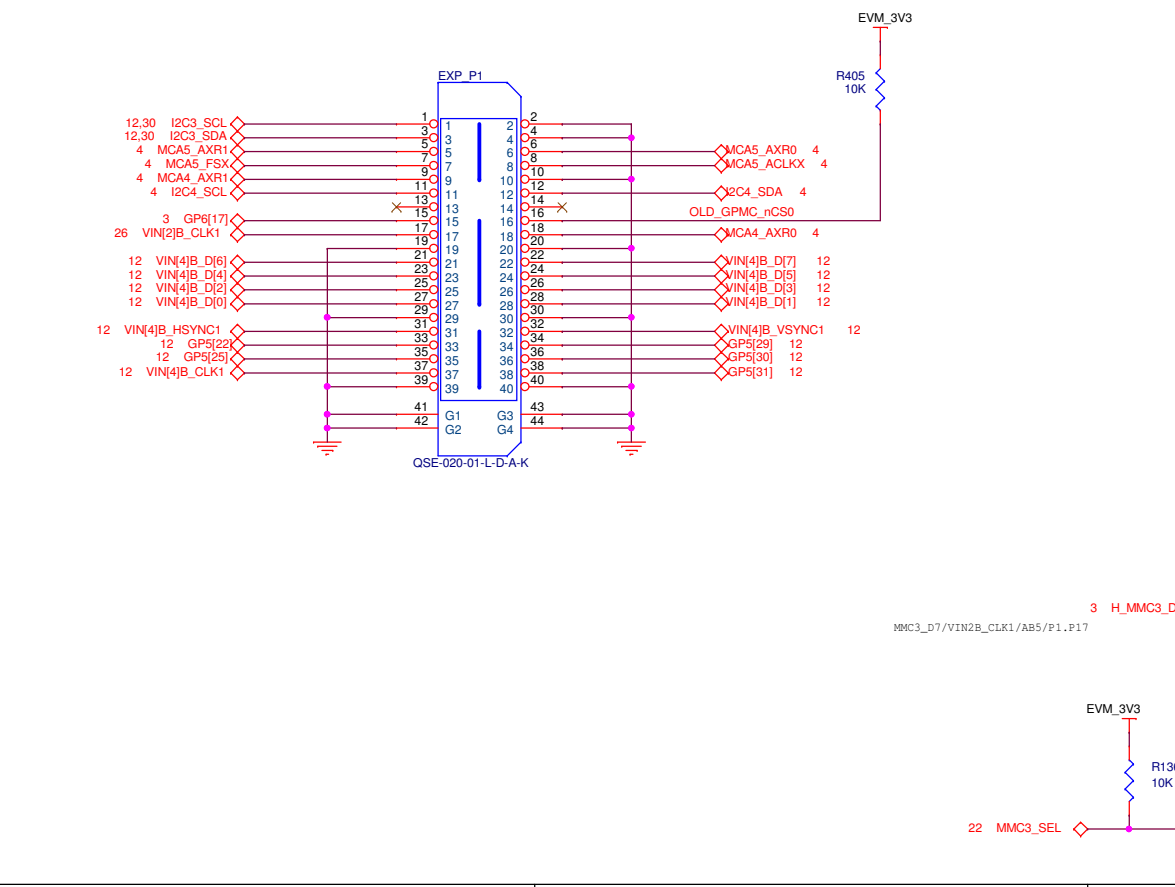
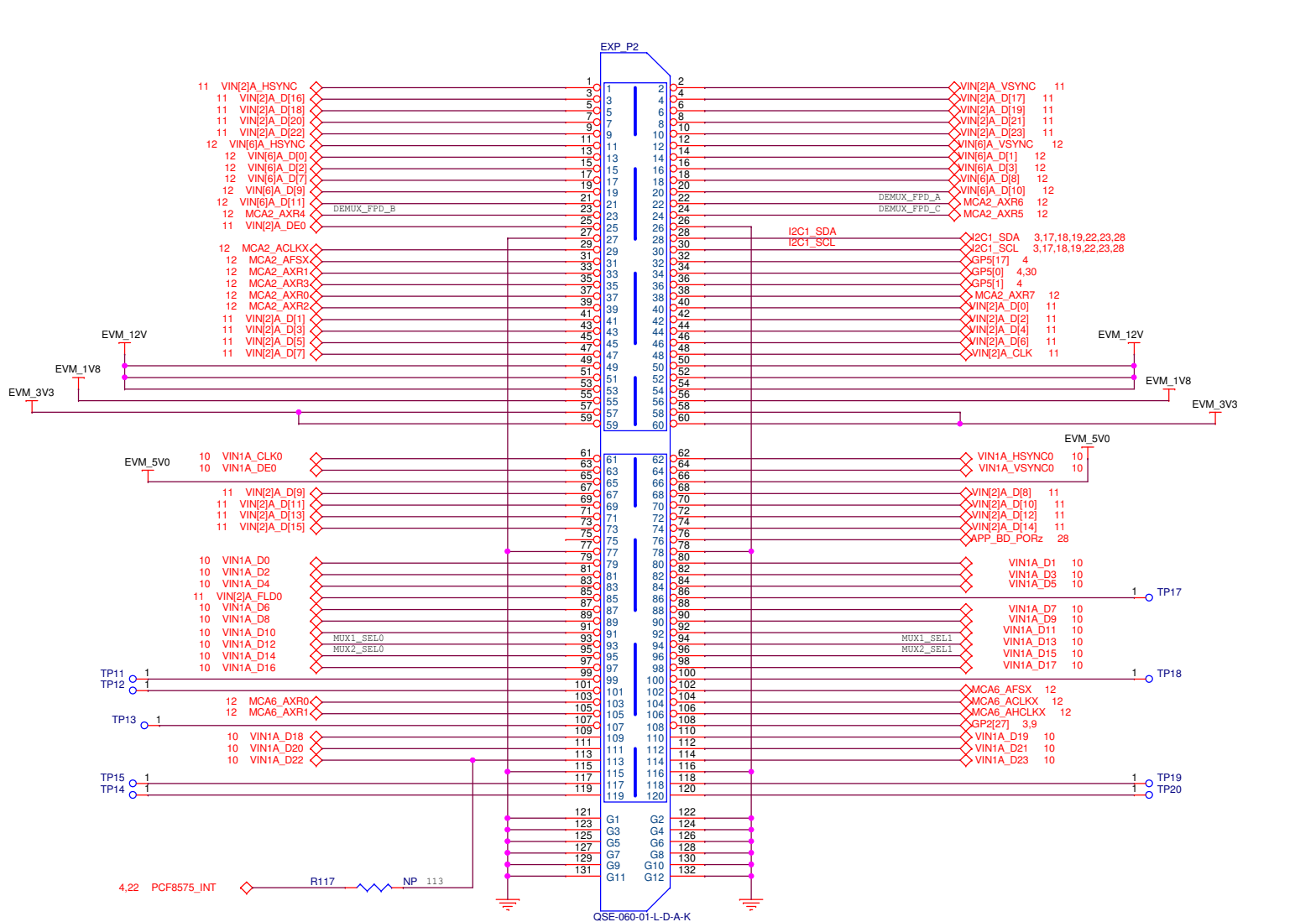
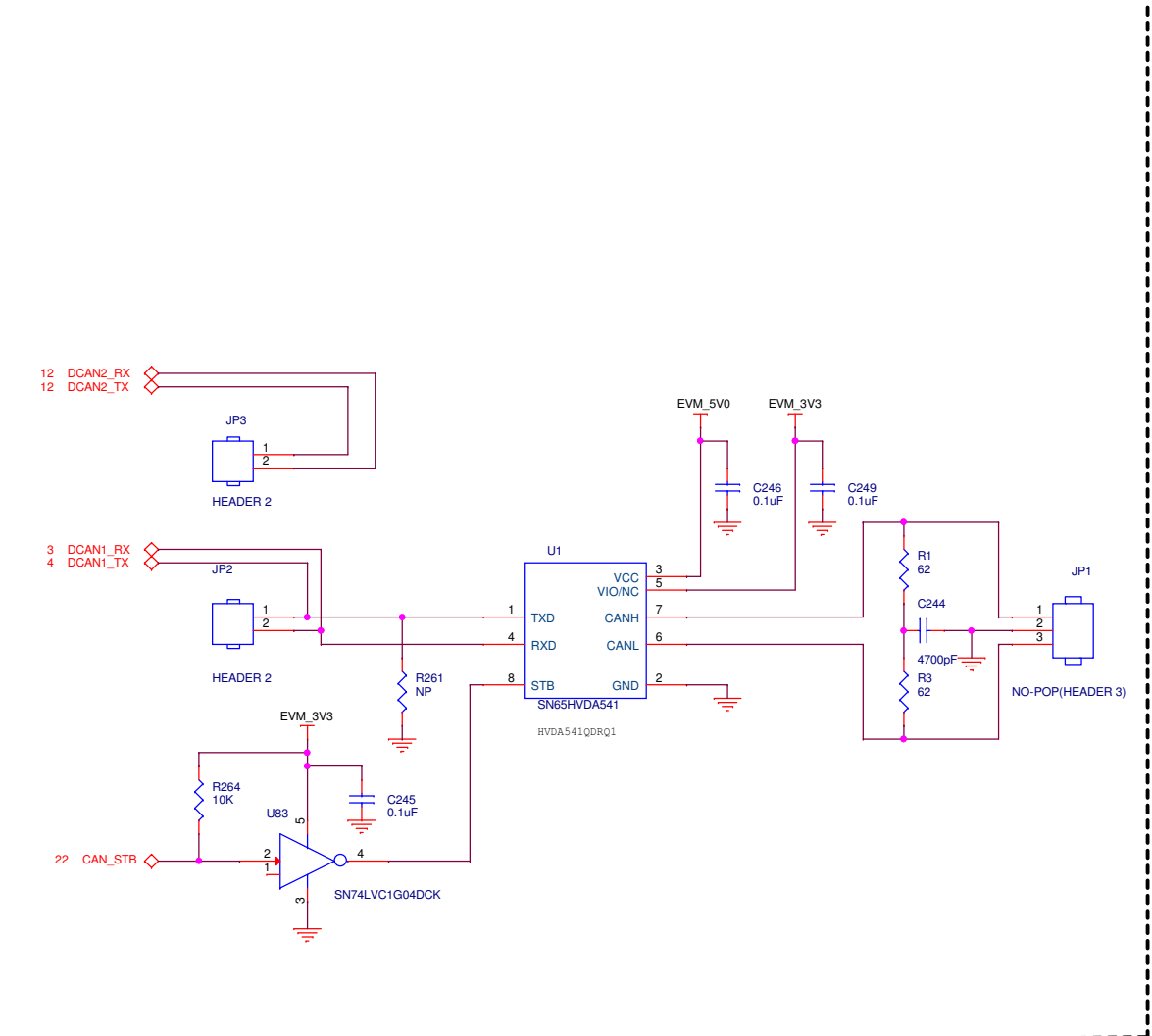
TEXAS INSTRUMENTS INCORPORATED

Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: ETHERNET PORT1

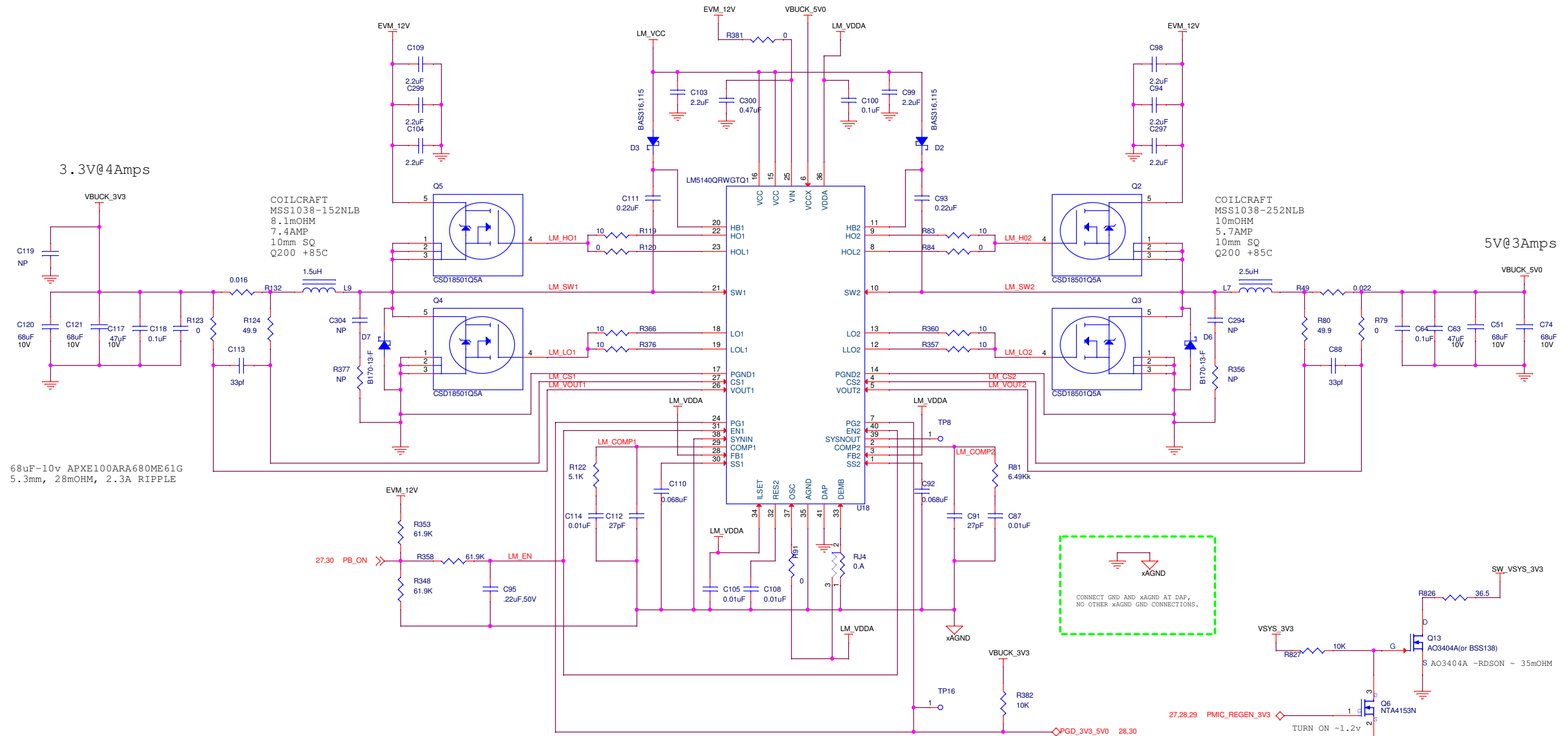
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TEXAS INSTRUMENTS INCORPORATED			
Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"			
Page Contents: CAN/EXP CONNECTORS			
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12V Nom Automotive,
24V Nom Industrial



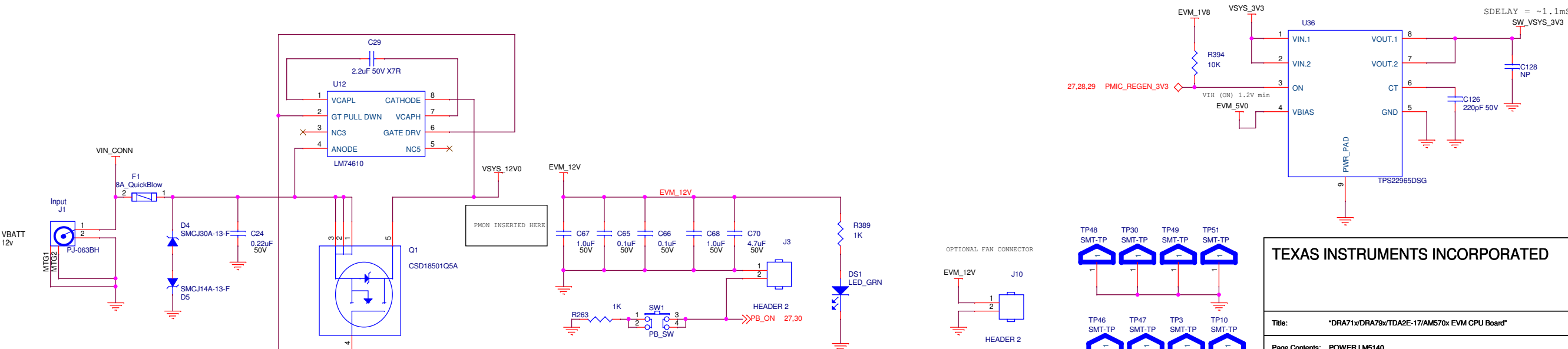
3.3V@4Amps

5V@3Amps

68uF-10V APXE100ARA680ME61G
5.3mm, 28mOHM, 2.3A RIPPLE

CONNECT GND AND xAGND AT DAP.
NO OTHER xAGND GND CONNECTIONS.

PMIC_REGEN_3V3 PULLUP TO 1V8 WHICH IS THE FIRST BUCK REGULATOR TO TURN ON AFTER THE PMIC OTP IS LOADED.



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Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"

Page Contents: POWER LM5140

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THE LP87XX GPx FUNCTIONS ARE NOT ACTIVE UNTIL AFTER THE OTP IS LOADED, ~7.5ms. SELECT PULLUP/PULLDOWN ACCORDINGLY.

=> <"EVM Power Rails">

SDELAY = Startup ms/Shutdown ms

=> VDD_CORE_AVS
SDELAY = 1.5ms/1ms

=> VDD_DSPEVE_AVS
SDELAY = 2.0ms/1ms

=> VDDSHV8
SDELAY = 3.0ms/0.5ms

=> VDDA_USB3V3
SDELAY = 3.5ms/0.5ms

LP873xx PGOOD SIGNAL IS PROGRAMMED FOR UNUSUAL OPERATION. IN THIS MODE IT WILL GO HIGH WELL BEFORE POWER IS GOOD. ORING IN LP8733 GPO2 WILL CREATE THE NECESSARY PORz SIGNAL FOR THE SOC. ALL OF THE OUTPUTS ARE PROGRAMMED FOR OPEN DRAIN.

WHEN PGOOD IS PROGRAMMED FOR UNUSUAL OPERATION IT WILL GO LOW FOR A "FAULT" AND REMAIN LOW UNTIL CLEARED VIA I2C. IN THE CONTEXT OF THIS EVM THE I2C OPERATION IS NOT POSSIBLE SINCE THE SOC IS BEING HELD IN RESET. SO A POWER CYCLE IS REQUIRED TO CLEAR THE FAULT.

=> VDD5_1V8
=> VDD5_SHV11
SDELAY = 0ms/1.5ms

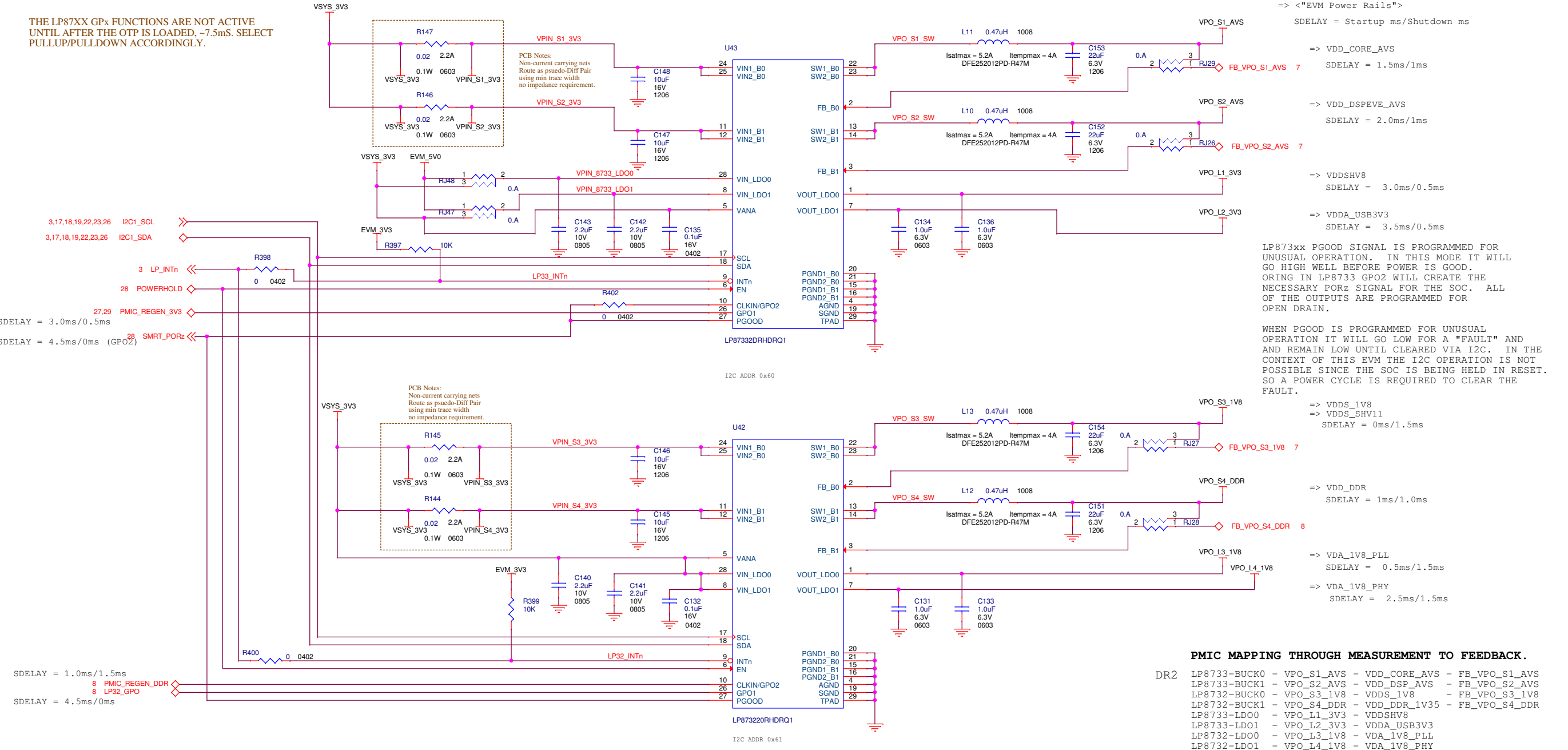
=> VDD_DDR
SDELAY = 1ms/1.0ms

=> VDA_1V8_PLL
SDELAY = 0.5ms/1.5ms

=> VDA_1V8_PHY
SDELAY = 2.5ms/1.5ms

PMIC MAPPING THROUGH MEASUREMENT TO FEEDBACK.

DR2	LP8733-BUCK0	-	VPO_S1_AVS	-	VDD_CORE_AVS	-	FB_VPO_S1_AVS
	LP8733-BUCK1	-	VPO_S2_AVS	-	VDD_DSP_AVS	-	FB_VPO_S2_AVS
	LP8732-BUCK0	-	VPO_S3_1V8	-	VDD5_1V8	-	FB_VPO_S3_1V8
	LP8732-BUCK1	-	VPO_S4_DDR	-	VDD_DDR_1V35	-	FB_VPO_S4_DDR
	LP8733-LDO0	-	VPO_L1_3V3	-	VDDSHV8		
	LP8733-LDO1	-	VPO_L2_3V3	-	VDDA_USB3V3		
	LP8732-LDO0	-	VPO_L3_1V8	-	VDA_1V8_PLL		
	LP8732-LDO1	-	VPO_L4_1V8	-	VDA_1V8_PHY		



3,17,18,19,22,23,26 I2C1_SCL
3,17,18,19,22,23,26 I2C1_SDA

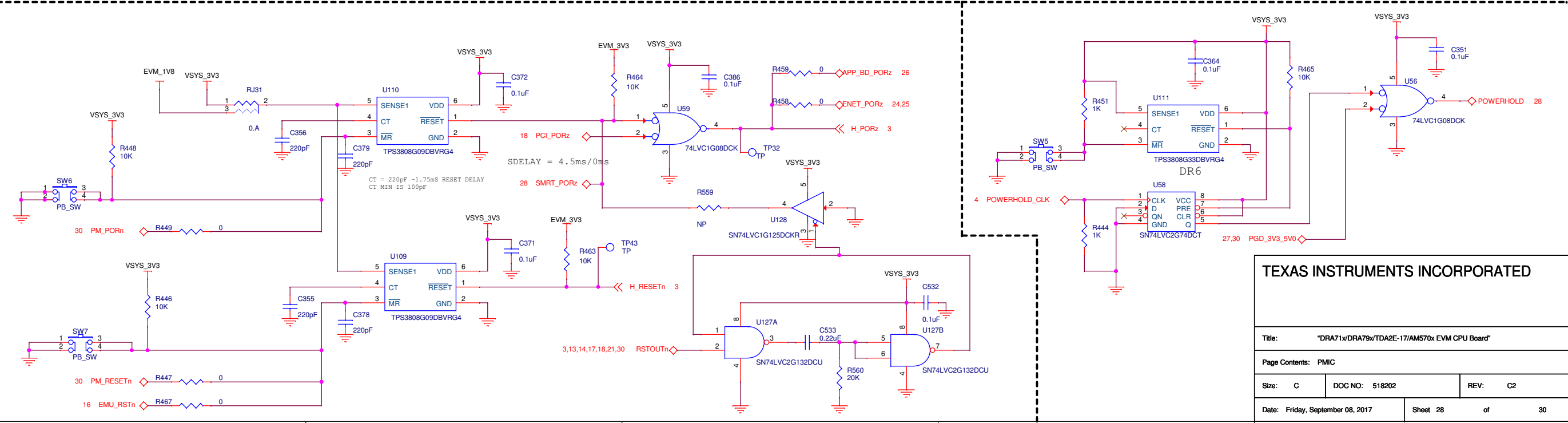
3 LP_INTn
28 POWERHOLD

27,29 PMIC_REGEN_3V3
SDELAY = 3.0ms/0.5ms

28 SMRT_PORz
SDELAY = 4.5ms/0ms (GPO2)

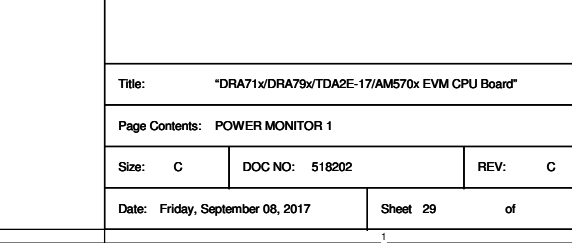
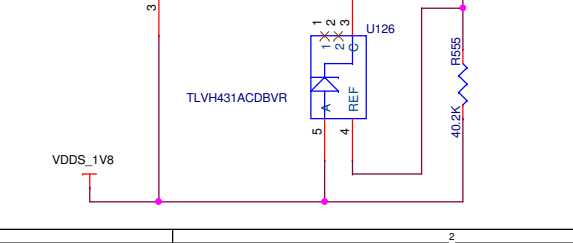
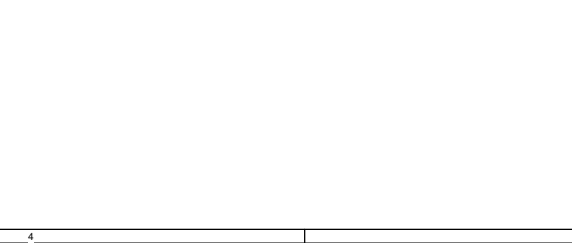
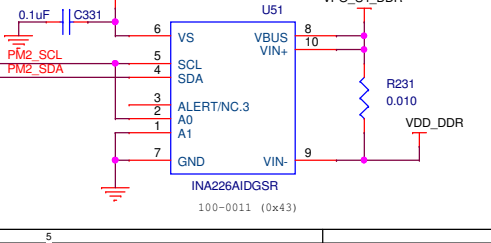
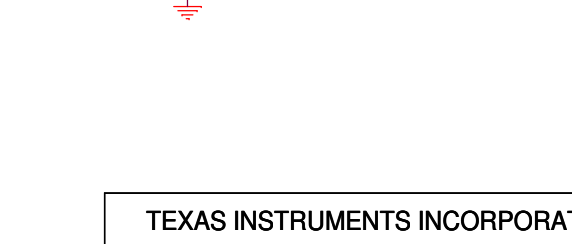
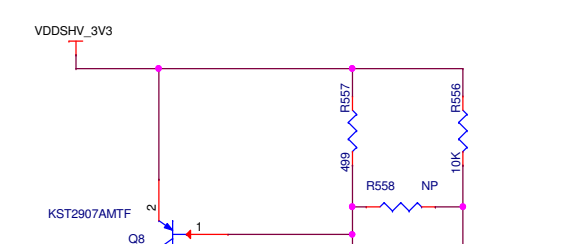
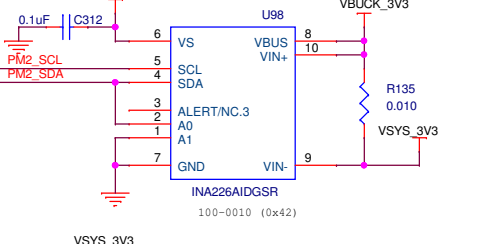
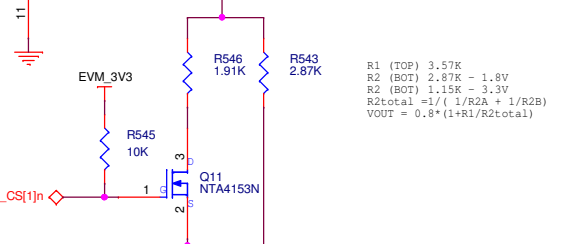
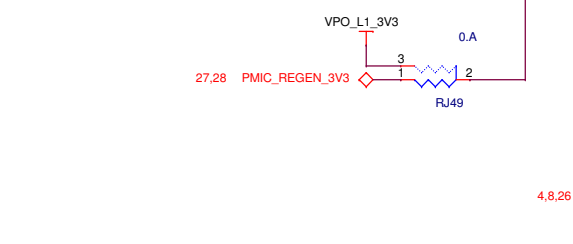
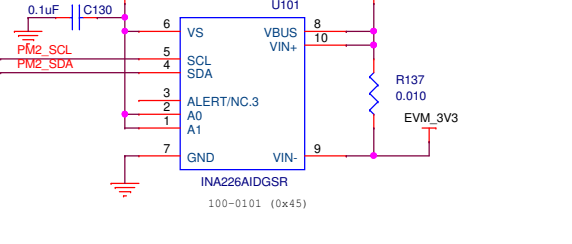
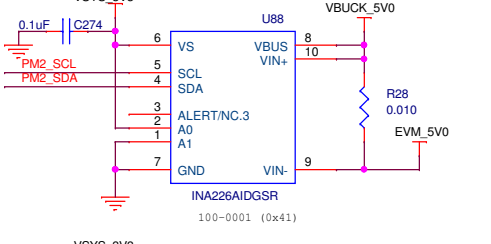
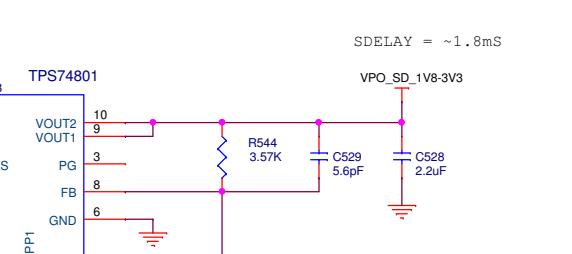
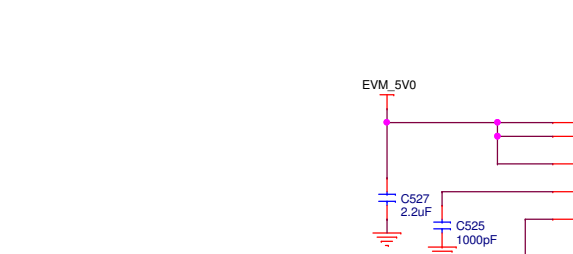
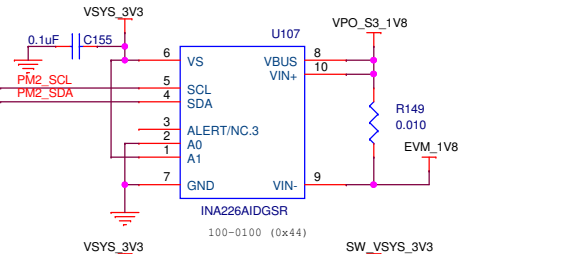
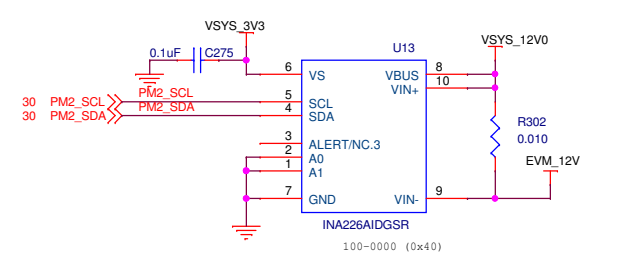
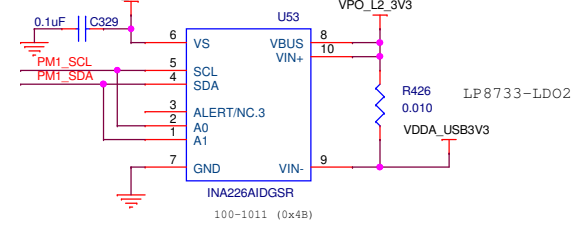
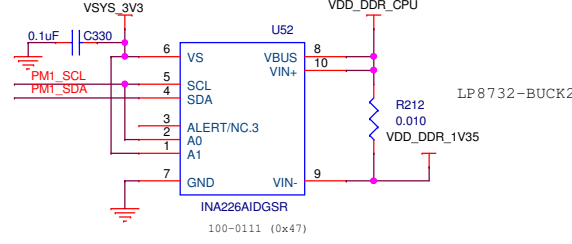
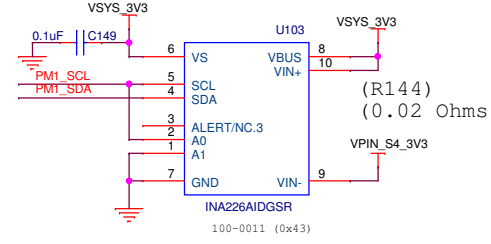
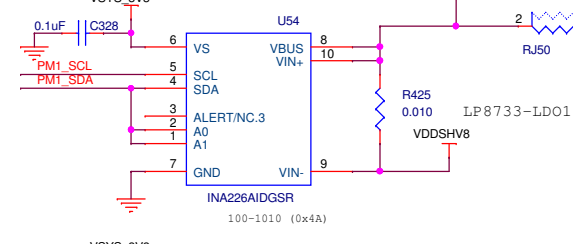
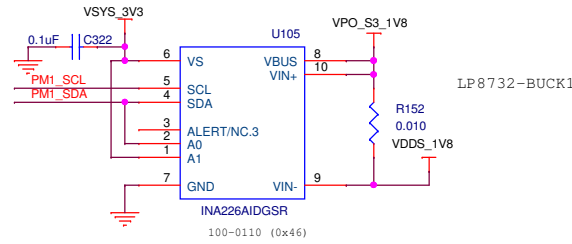
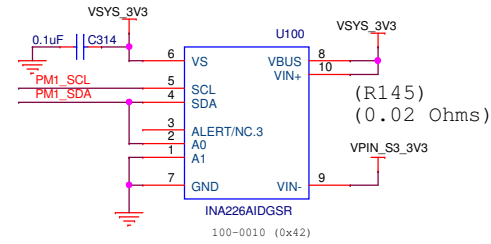
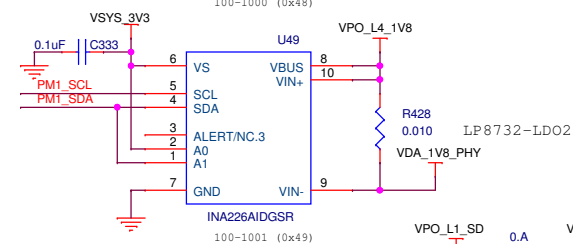
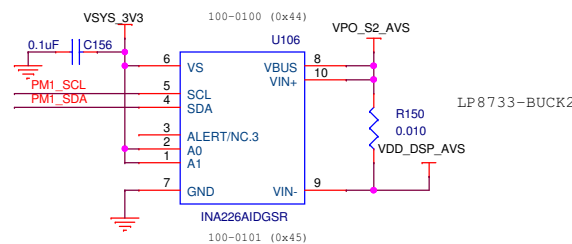
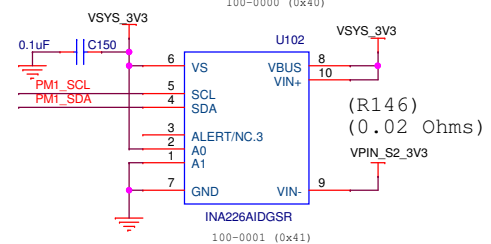
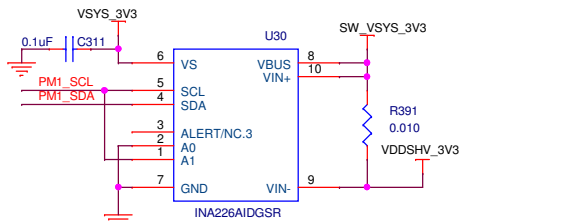
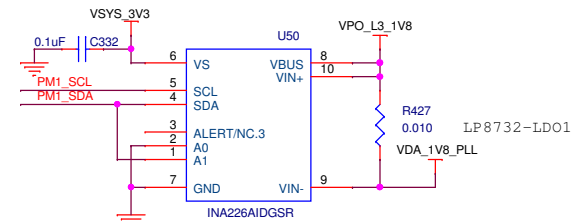
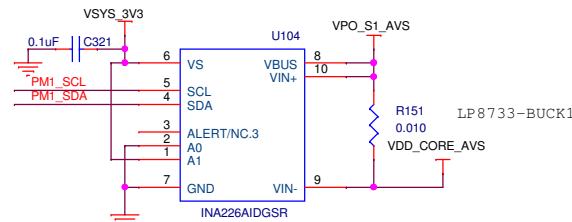
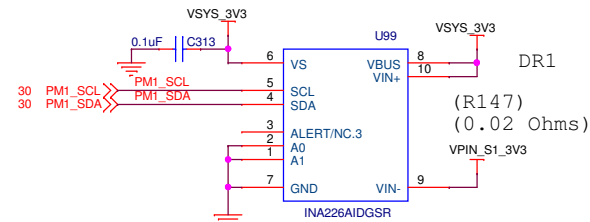
8 PMIC_REGEN_DDR
SDELAY = 1.0ms/1.5ms

8 LP32_GPO
SDELAY = 4.5ms/0ms



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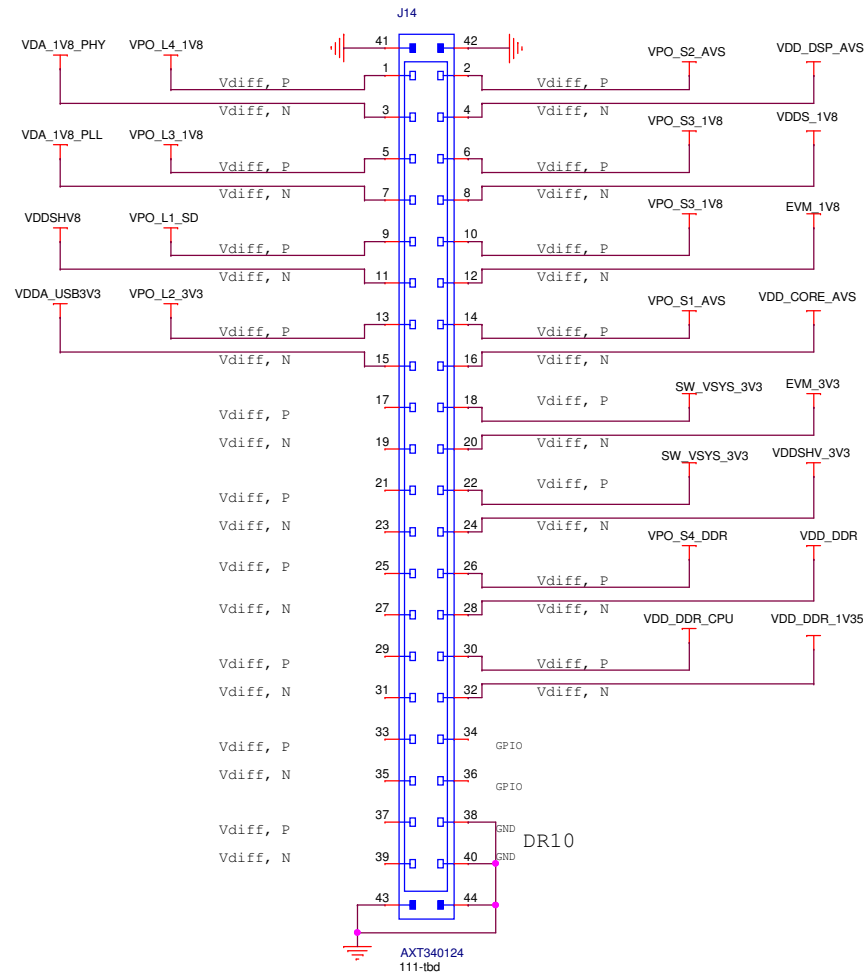
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Page Contents: PMIC			
Size: C	DOC NO: 518202	REV: C2	
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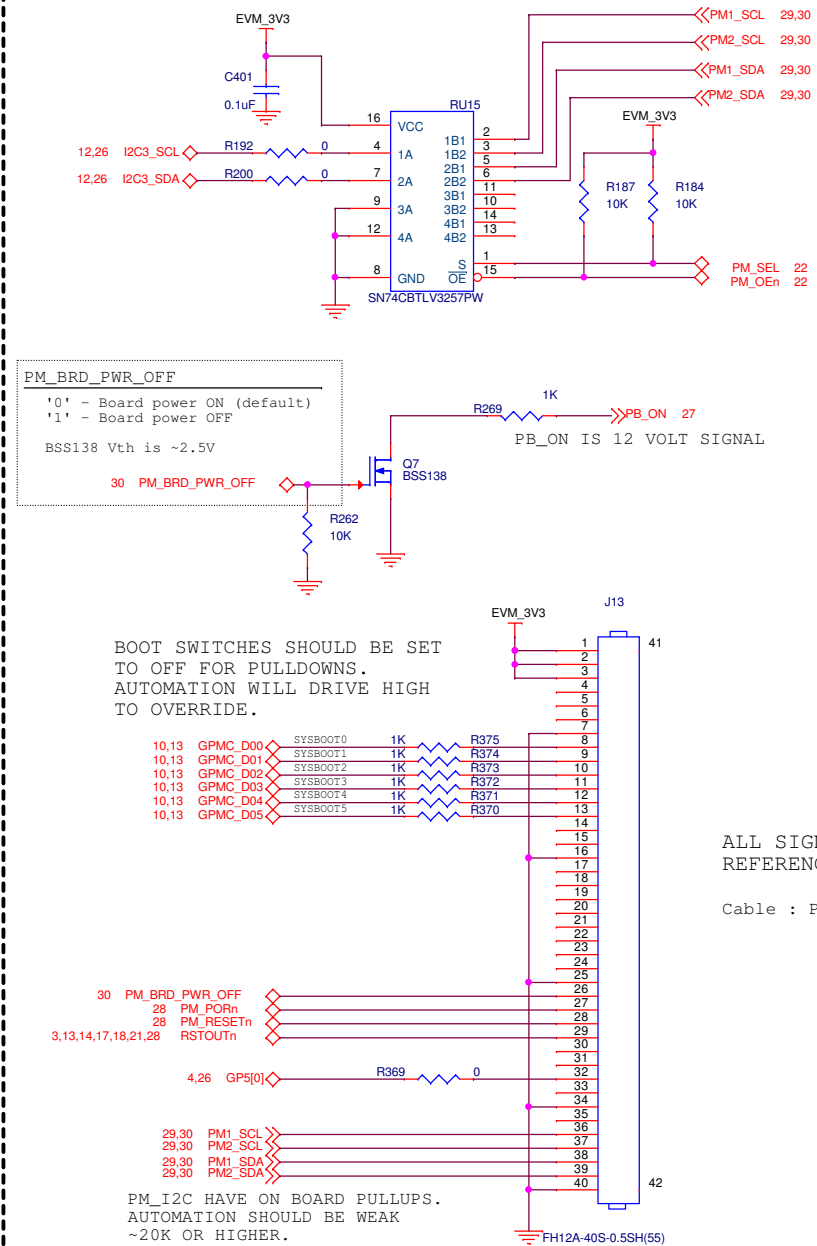
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Page Contents: POWER MONITOR 1		
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DARA Bd Interface Connector

DARA Bd can be interfaced to conduct more in-depth power measurements.
 All Vdiff signal pairs (P & N) shown should be routed as pseudo-Diff Pair segments using min trace widths since these are low voltage sensing nets, not power delivery nets.



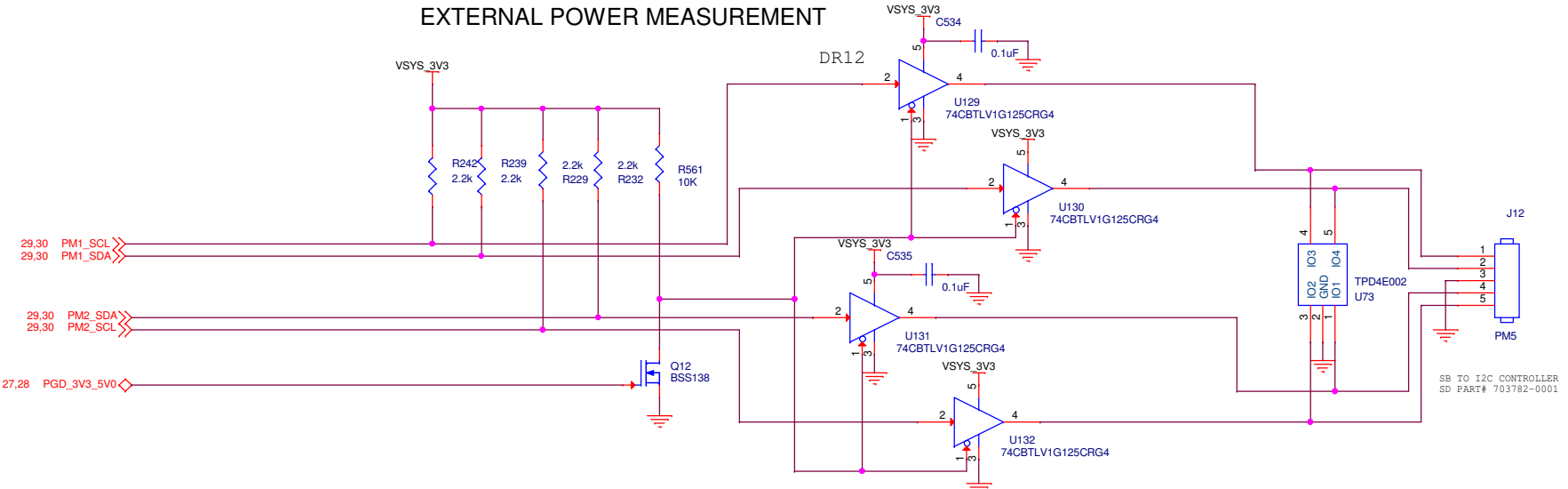
AUTOMATION INTERFACE



BOOT SWITCHES SHOULD BE SET TO OFF FOR PULLDOWNS. AUTOMATION WILL DRIVE HIGH TO OVERRIDE.

ALL SIGNALS SHOULD BE REFERENCED TO EVM_3V3
 Cable : Parlex-050R40-76B, .5mm 3"

EXTERNAL POWER MEASUREMENT



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Title: "DRA71x/DRA79x/TDA2E-17/AM570x EVM CPU Board"		
Page Contents: DARA AND AUTOMATION		
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