TMS320C6474 DSP Software-Programmable Phase-Locked Loop (PLL) Controller

User's Guide

Literature Number: SPRUG09
October 2008

Contents

List of Figures

List of Tables

Read This First

About This Manual

This document describes the operation of the software-programmable phase-locked loop (PLL) controller in the TMS320C6474 digital signal processors (DSPs). The PLL controller offers flexibility and convenience by way of software-configurable multiplier and dividers to modify the input signal internally. The resulting clock outputs are passed to the C6474 DSP core, peripherals, and other modules.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the C6000™ devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the C6000 devices, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRU189 — *TMS320C6000 DSP CPU and Instruction Set Reference Guide.* Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C6000 digital signal processors (DSPs).

SPRU198 — *TMS320C6000 Programmer's Guide.* Describes ways to optimize C and assembly code for the TMS320C6000™ DSPs and includes application program examples.

SPRU301 — *TMS320C6000 Code Composer Studio Tutorial.* Introduces the Code Composer Studio™ integrated development environment and software tools.

SPRU321 — *Code Composer Studio Application Programming Interface Reference Guide.* Describes the Code Composer Studio™ application programming interface (API), which allows you to program custom plug-ins for Code Composer.

SPRU871 — *TMS320C64x+ Megamodule Reference Guide.* Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

Trademarks

C6000, TMS320C6000, Code Composer Studio are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

Phase-Locked Loop (PLL) Controller

This document describes the operation of the software-programmable phase-locked loop (PLL) controller in the TMS320C6474 digital signal processors (DSPs).

1 Overview

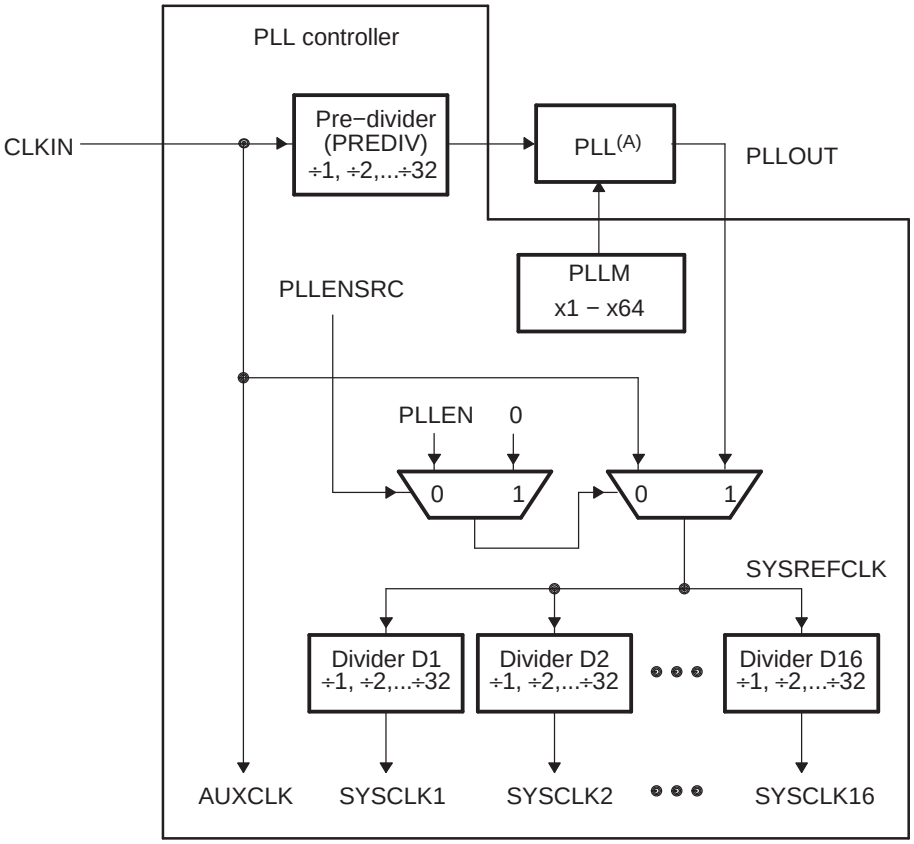
The PLL controller (Figure 1) features a software-configurable PLL multiplier controller (PLLM) and dividers (PREDIV and D1-D16). The PLL controller offers flexibility and convenience with software-configurable multiplier and dividers to modify the input clock signal (CLKIN) internally. The resulting clock outputs are passed to the DSP core, peripherals, and other modules inside the DSP.

The PLL controller has one input clock and several output clocks.

- Input reference clock to the PLL controller:
  - CLKIN: Input signal from external oscillator
- Resulting output clocks from the PLL controller:
  - AUXCLK: Internal clock output signal directly from CLKIN
  - SYSCLK1 to SYSCLK16: System domain clocks, each output from its own divider (see Figure 1)

Note: Not all these output clocks may be used on a specific device. For the uses of the PLL controller inputs and outputs, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).

Figure 1. PLL Controller Block Diagram



A For more details about the PLL, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).

2 Functional Description

The following sections describe the multiplier and dividers in the PLL controller as well as the bypass mode and PLL mode operation.

2.1 Multipliers and Dividers

The PLL controller is capable of programming the PLL through the PLL multiplier control register (PLLM) from a ı to 4 multiplier rate. The clock dividers (PREDIV and D1-D16) are programmable from a ÷1 to ÷32 divider ratio and may be disabled. When a clock divider is disabled, no clock is output from that clock divider. A divider only outputs a clock when it is enabled in the corresponding PLLDIV*n* register.

2.2 PLL Enable Source Bit and PLL Enable Bit

After device reset, the value of the PLL enable bit (PLLEN) in the PLL control register (PLLCTL) can be changed, but it will not have any effect on the function of the PLL controller. To enable the PLLEN bit, the PLLENSRC bit (also in the PLLCTL register) must first be cleared to 0. Once the PLLEN bit has been enabled, it can be used to select the bypass mode or PLL mode of the PLL controller as discussed in the next two sections.

2.3 Bypass Mode

The divider PREDIV and the PLL may be bypassed altogether. The PLL enable bit (PLLEN) in the PLL control register (PLLCTL) determines the PLL controller mode. When PLLEN = 1, PLL mode, PREDIV and PLL are used; when PLLEN = 0, bypass mode, PREDIV and PLL are bypassed and the input reference clock is directly input to the system clock dividers (D1-D16). On the C6474 DSP, the PLL defaults to bypass mode (PLLEN = 0).

2.4 PLL Mode

When in PLL mode (PLLEN = 1), the input reference clock is supplied to divider PREDIV. Divider PREDIV must be enabled (PREDEN = 1) in PLL mode. When divider PREDIV is enabled, the input reference clock is divided-down by the value in the PLL divider ratio bits (RATIO) in PREDIV. The output from divider PREDIV is input to the PLL. The PLL multiplies the clock by the value in the PLL multiplier bits (PLLM) in the PLL multiplier control register (PLLM). The output from the PLL (PLLOUT) is input to the system clock dividers (PLLDIV*n*).

When enabled (D*n*EN = 1), the system clock dividers (D1-D16) divide-down by the RATIO value in PLLDIV*n*, the output clock of the PLL. The system clock dividers generate a 50% duty cycle output clock SYSCLK*n*.

3 Configuration

The following sections provide procedures for initialization, power down, and wake up of the PLL controller.

3.1 Initialization

The PLL and PLL controller are initialized by software after reset. The PLL controller registers should only be modified by the CPU or emulation. External masters, such as the HPI and PCI, should not be used to directly access the PLL controller registers. The initialization of the PLL controller should be performed as soon as possible at the beginning of the program, before initializing any peripherals. Upon device reset, one of the following two software initialization procedures must be done to properly set up the PLL and PLL controller.

3.1.1 Initialization to PLL Mode (PLLEN = 1)

This section shows the initialization sequence if the system intends to use the pre-divider (PREDIV) and PLL. The steps below also show when you should program the multipliers and system clock dividers, if required.

1. If executing this sequence immediately after device power-up, you must allow for the PLL to become stable. For details on PLL stabilization time, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).
2. In PLLCTL, write PLLENSRC = 0 (enable PLLEN bit).
3. In PLLCTL, write PLLEN = 0 (bypass mode).
4. Wait 4 cycles of the slowest of PLLOUT or reference clock source (CLKIN).
5. In PLLCTL, write PLLRST = 1 (PLL is reset).
6. If necessary, program PREDIV and PLLM.
7. If necessary, program PLLDIV1*n*. Note that you must apply the GO operation to change these dividers to new ratios (see Section 3.2.1).
8. Wait for PLL to properly reset. For details on PLL reset time, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).
9. In PLLCTL, write PLLRST = 0 to bring PLL out of reset.
10. Wait for PLL to lock. For details on PLL lock time, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).
11. In PLLCTL, write PLLEN = 1 to enable PLL mode.

Steps 1, 2, and 3 are required when PLLEN and PLLRST bits are not already 0 and 1, respectively.

3.1.2 Initialization to Bypass Mode (PLLEN = 0)

This section shows the initialization sequence, if the system intends to bypass divider PREDIV and PLL. The steps below show when you should program the multipliers and dividers, if needed.

1. If executing this sequence immediately after device power-up, you must allow for the PLL to become stable. Sor PLL stabilization time, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).
2. In PLLCTL, write PLLENSRC = 0 (enable PLLEN bit).
3. In PLLCTL, write PLLEN = 0 (bypass mode).
4. Wait 4 cycles of the slowest of PLLOUT or reference clock source (CLKIN).
5. In PLLCTL, write PLLRST = 1 (PLL is reset).
6. It is not necessary to program PREDIV and PLLM.
7. If necessary, program PLLDIV1*n*. Note that you must apply the GO operation to change these dividers to new ratios (see Section 3.2.1).

Steps 1, 2, and 3 are required when PLLEN and PLLRST bits are not already 0 and 1, respectively.

3.2 Changing Divider/Multiplier Ratio

This section discusses how to change the various divider/multiplier ratios.

3.2.1 Divider *n* (D1 to D*n*) and GO Operation

The GO operation is required to change the divider ratios of the PLLDIV*n* registers. Section 3.2.1.1 discusses the GO operation. Section 3.2.1.2 provides the software steps required to change the divider ratios.

3.2.1.1 GO Operation

Writes to the RATIO field in the PLLDIV*n* registers do not change the dividers' divide ratios immediately. The PLLDIV*n* dividers only change to the new RATIO rates during a GO operation. This section discusses the GO operation and alignment of the SYSCLKs.

The PLL controller clock align control register (ALNCTL) determines which SYSCLKs must be aligned. Before a GO operation, program ALNCTL according to the device-specific data manual requirement so that the appropriate clocks are aligned during the GO operation.

A GO operation is initiated by setting the GOSET bit in PLLCMD to 1. During a GO operation:

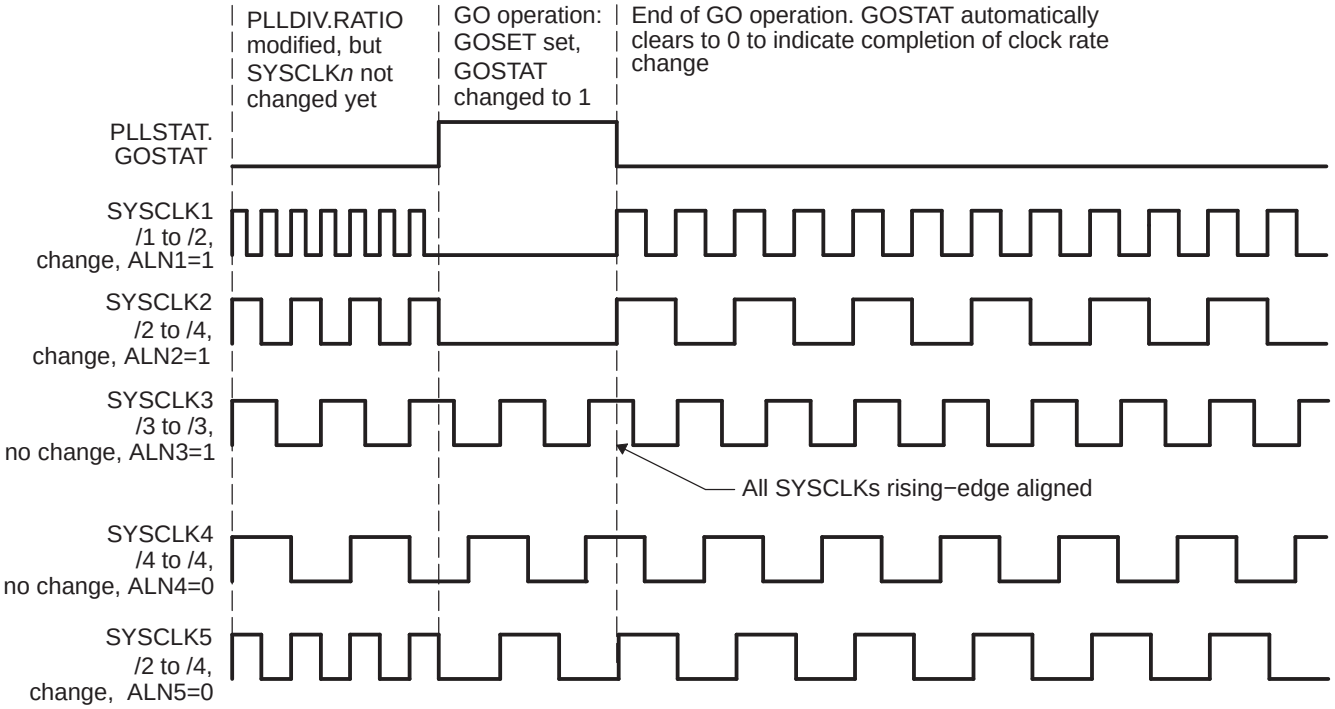
- Any SYSCLK*n* with the corresponding ALN*n* bit in ALNCTL and SYS*n* bit in DCHANGE set to 1 is paused at the low edge. Then the PLL controller restarts all these SYSCLKs simultaneously, aligned at the rising edge. When the SYSCLKs are restarted, SYSCLK*n* toggles at the rate programmed in the RATIO field in PLLDIV*n*.
- Any SYSCLK*n* with the corresponding ALN*n* bit in ALNCTL cleared and the SYS*n* bit in DCHANGE set immediately changes to the new rate programmed in the RATIO field.
- The GOSTAT bit in PLLSTAT is set throughout the duration of a GO operation.

Figure 2 shows how the clocks are rising-edge aligned during a GO operation. Notice that because SYSCLK5 does not need to be aligned with the other clocks, it immediately switches to its new ratio during the GO operation.

CAUTION

To prevent errors, all chip operation must be stopped before the GO operation.

Figure 2. Clock Ratio Change and Alignment with GO Operation



3.2.1.2 *Software Steps to Modify PLLDIVn Ratios*

Perform the following steps to modify PLLDIV*n*.

1. Check that the GOSTAT bit in PLLSTAT is cleared to show that no GO operation is currently in progress.
2. Program the RATIO field in PLLDIV*n* to the desired new divide-down rate. If the RATIO field changed, the PLL controller will flag the change in the corresponding bit of DCHANGE.
3. Set the respective ALN*n* bits in ALNCTL to align any SYSCLKs after the GO operation.
4. Set the GOSET bit in PLLCMD to initiate the GO operation to change the divide values and align the SYSCLKs as programmed.
5. Read the GOSTAT bit in PLLSTAT to make sure the bit returns to 0 to indicate that the GO operation has completed.

3.2.2 Pre-Divider (PREDIV) and PLL Multiplier (PLLM)

To change the values of PREDIV or PLLM, the PLL controller must first be placed in bypass mode. Perform the following steps to modify PREDIV or PLLM ratios.

1. If executing this sequence immediately after device power-up, you must allow for the PLL to become stable. For PLL stabilization time, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).
2. In PLLCTL, write PLLENSRC = 0 (enable PLLEN bit).
3. In PLLCTL, write PLLEN = 0 to place the PLL in bypass mode.
4. Wait 4 cycles of the slowest of PLLOUT or reference clock source (CLKIN).
5. In PLLCTL, write PLLRST = 1 (PLL is reset).
6. Modify PREDIV and/or PLLM ratios.
7. Wait for PLL to reset. For details on PLL reset time, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).
8. In PLLCTL, write PLLRST = 0 to bring PLL out of reset.
9. Wait for PLL to relock. For details on PLL lock time, see the *TMS320C6474 Multicore Digital Signal*

Processor data manual (SPRS552).

10. In PLLCTL, write PLLEN = 1 to switch from bypass mode to PLL mode.

3.3 PLL Power Down

The PLL may be powered down, in which case the PLL controller is in bypass mode and the DSP runs from a divided-down version of the input reference clock. The DSP is able to respond to events because it is still being clocked by the bypass clock (directly from CLKIN), although at a lower frequency.

Perform the following procedure to power down the PLL.

1. In PLLCTL, write PLLENSRC = 0 (enable PLLEN bit).
2. In PLLCTL, write PLLEN = 0 (bypass mode).
3. Wait 4 cycles of the slowest of PLLOUT or CLKIN.
4. In PLLCTL, write PLLPWRDN = 1 to power down the PLL.

The above sequence assumes that the device has been powered up long enough such that the PLL stabilization time has been met. If executing this sequence immediately after device power-up, you must allow for the PLL to become stable before performing these steps. For PLL stabilization time, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).

3.4 PLL Wake Up

Perform the following procedure to wake up the PLL from its power-down mode.

1. Ensure PLLENSRC = 0.
2. Check to be sure PLL is already in bypass mode (PLLEN = 0).
3. In PLLCTL, write PLLPWRDN = 0 to wake up the PLL.
4. Follow the PLL reset sequence in Section 3.1.1 (steps 3 to 9) to reset the PLL. Wait for the PLL to lock and to switch from bypass to PLL mode.

The above sequence assumes that the device has been powered up long enough such that the PLL stabilization time has been met. If executing this sequence immediately after device power-up, you must allow for the PLL to become stable before performing these steps. For PLL stabilization time, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).

4 Registers

The PLL controller registers are listed in Table 1. For the memory address of these registers, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552). All other register offset addresses not listed in Table 1 should be considered as reserved locations and the register contents should not be modified.

CAUTION

Some devices have more than one phase-locked loop (PLL) and therefore, have more than one PLL Controller. This section includes a list of all the PLL Controller registers; however, depending on the PLL being programmed, not all the registers may be used. Furthermore, the reset values for the fields within the registers may be different. For more details, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).

Table 1. PLL Controller Registers

Offset	Acronym	Register Description	See
100h	PLLCTL	PLL control register	Section 4.1
110h	PLLM	PLL multiplier control register	Section 4.2
114h	PREDIV	PLL pre-divider control register	Section 4.3
118h	PLLDIV1	PLL controller divider 1 register	Section 4.4
11Ch	PLLDIV2	PLL controller divider 2 register	Section 4.4
120h	PLLDIV3	PLL controller divider 3 register	Section 4.4
138h	PLLCMD	PLL controller command register	Section 4.5
13Ch	PLLSTAT	PLL controller status register	Section 4.6
140h	ALNCTL	PLL controller clock align control register	Section 4.7
144h	DCHANGE	PLLDIV divider ratio change status register	Section 4.8
148h	CKEN	Clock enable control register	Section 4.9
14Ch	CKSTAT	Clock status register	Section 4.10
150h	SYSTAT	SYSCLK status register	Section 4.11
160h	PLLDIV4	PLL controller divider 4 register	Section 4.4
164h	PLLDIV5	PLL controller divider 5 register	Section 4.4
168h	PLLDIV6	PLL controller divider 6 register	Section 4.4
16Ch	PLLDIV7	PLL controller divider 7 register	Section 4.4
170h	PLLDIV8	PLL controller divider 8 register	Section 4.4
174h-193h	PLLDIV9- PLLDIV16	PLL controller divider 9 to 16 registers	Section 4.4

4.1 PLL Control Register (PLLCTL)

The PLL control register (PLLCTL) is shown in Figure 3 and described in Table 2.

Figure 3. PLL Control Register (PLLCTL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-n															

15	14	13	12	11	10	9	8
Reserved							
R-n							

7	6	5	4	3	2	1	0
Reserved	Reserved	PLLENSRC	Rsvd	PLLRST	Rsvd	PLLPWRDN	PLLEN
R/W-n	R-n	R/W-n	R/W-n	R/W-n	R-n	R/W-n	R/W-n

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset; for reset value, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)

Table 2. PLL Control Register (PLLCTL) Field Descriptions

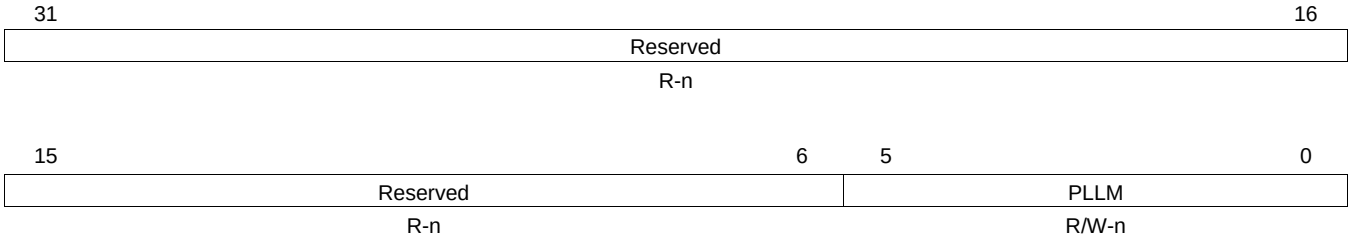
Bit	Field	Value	Description
31-8	Reserved		Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
7	Reserved		Reserved. Writes to this register must keep this bit as 0.
6	Reserved		Reserved. The reserved bit location is always read as 1. A value written to this field has no effect.
5	PLLENSRC		PLL enable source bit.
		0	PLLEN bit is enabled. The value of the PLLEN bit will affect the operation of the PLL controller.
		1	PLLEN bit is disabled. The value of the PLLEN bit has no effect on the operation of the PLL controller.
4	Reserved		Reserved. Writes to this register must keep this bit as 0.
3	PLLRST		PLL reset bit.
		0	PLL reset is released.
		1	PLL reset is asserted.
2	Reserved		Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
1	PLLPWRDN		PLL power-down mode select bit.
		0	PLL is operational.
		1	PLL is placed in a power-down state; i.e., all analog circuitry in the PLL is turned off.
0	PLLEN		PLL enable bit.
		0	Bypass mode. Dividers PREDIV and PLL are bypassed. All the system clocks (SYSCLK*n*) are divided-down directly from input reference clock.
		1	PLL mode. Dividers PREDIV and PLL are not bypassed. PLL output path is enabled. All the system clocks (SYSCLK*n*) are divided down from PLL output.

4.2 PLL Multiplier Control Register (PLLM)

The PLL multiplier control register (PLLM) is shown in Figure 4 and described in Table 3. The PLLM register defines the input reference clock frequency multiplier in conjunction with the PLL divider ratio bits (RATIO) in the PLL controller pre-divider register (PREDIV).

Note: Table 3 lists all the possible values for the PLL multiplier bits (PLLM); however, some of these values may not be valid. For a list of valid values for PLLM, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552).

Figure 4. PLL Multiplier Control Register (PLLM)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset; for reset value, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)

Table 3. PLL Multiplier Control Register (PLLM) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
5-0	PLLM	0-3Fh	PLL multiplier bits. Defines the frequency multiplier of the input reference clock in conjunction with the PLL divider ratio bits (RATIO) in PREDIV.
		0h	×1 multiplier rate.
		1h	×2 multiplier rate.
		2h	×3 multiplier rate.
		3h	×4 multiplier rate.
		4-3h	×5 multiplier rate to ×64 multiplier rate.

4.3 PLL Pre-Divider Registers (PREDIV)

The PLL controller divider register (PREDIV) is shown in Figure 5 and described in Table 4.

Figure 5. PLL Pre-Divider Register (PREDIV)

31	16
Reserved	
R-n	

15	14	5	4	0
PREDEN	Reserved		RATIO	
R/W-n	R-n		R/W-n	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset; for reset value, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)

Table 4. PLL Pre-Divider Register (PREDIV) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15	PREDEN		Pre-divider enable bit.
		0	Pre-divider is disabled. No clock output.
		1	Pre-divider is enabled.
14-5	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
4-0	RATIO	0-1Fh	Divider ratio bits.
		0	÷1. Divide frequency by 1.
		1h	÷2. Divide frequency by 2.
		2h	÷3. Divide frequency by 3.
		3h	÷4. Divide frequency by 4.
		4h-1Fh	÷5 to ÷32. Divide frequency by 4 to divide frequency by 32.

4.4 PLL Controller Divider Register (PLLDIV1-PLLDIV16)

The PLL controller divider registers (PLLDIV1-PLLDIV16) are shown in Figure 6 and described in Table 5.

Figure 6. PLL Controller Divider Register (PLLDIV*n*)

31	16
Reserved	
R-n	

15	14	5	4	0
D*n*EN	Reserved		RATIO	
R/W-n	R-n		R/W-n	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset; for reset value, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)

Table 5. PLL Controller Divider Register (PLLDIV*n*) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15	D*n*EN		Divider D*n* enable bit.
		0	Divider *n* is disabled. No clock output.
		1	Divider *n* is enabled.
14-5	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
4-0	RATIO	0-1Fh	Divider ratio bits.
		0	÷1. Divide frequency by 1.
		1h	÷2. Divide frequency by 2.
		2h	÷3. Divide frequency by 3.
		3h	÷4. Divide frequency by 4.
		4h-1Fh	÷5 to ÷32. Divide frequency by 4 to divide frequency by 32.

4.5 PLL Controller Command Register (PLLCMD)

The PLL controller command register (PLLCMD) contains the command bit for the GO operation. PLLCMD is shown in Figure 7 and described in Table 6.

Figure 7. PLL Controller Command Register (PLLCMD)

31	16
Reserved	
R-n	

15	1	0
Reserved	Rsvd	GOSET
R-n	R/W-n	R/W-n

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset; for reset value, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)

Table 6. PLL Controller Command Register (PLLCMD) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
1	Reserved		Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
0	GOSET		GO operation command for SYSCLK rate change and phase alignment. Before setting this bit to initiate a GO operation, check the GOSTAT bit in the PLLSTAT register to ensure all previous GO operations have completed.
		0	No effect. Write of 0 clears bit.
		1	Initiates GO operation. Write of 1 initiates GO operation. Once set, GOSET remains set but further writes of 1 can reinitiate the GO operation.

4.6 PLL Controller Status Register (PLLSTAT)

The PLL controller status register (PLLSTAT) shows the PLL controller status. PLLSTAT is shown in Figure 8 and described in Table 7.

Figure 8. PLL Controller Status Register (PLLSTAT)

31	16
Reserved	
R-n	

15	1	0
Reserved		GOSTAT
R-n		R-n

LEGEND: R = Read only; -*n* = value after reset; for reset value, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)

Table 7. PLL Controller Status Register (PLLSTAT) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
0	GOSTAT		GO operation status.
		0	GO operation is not in progress. SYSCLK divide ratios are not being changed.
		1	GO operation is in progress. SYSCLK divide ratios are being changed.

4.7 PLL Controller Clock Align Control Register (ALNCTL)

The PLL controller clock align control register (ALNCTL) is shown in Figure 9 and described in Table 8.

Note: The default value of this register should not be changed.

Figure 9. PLL Controller Clock Align Control Register (ALNCTL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-n															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALN16	ALN15	ALN14	ALN13	ALN12	ALN11	ALN10	ALN9	ALN8	ALN7	ALN6	ALN5	ALN4	ALN3	ALN2	ALN1
R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset; for reset value, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)

Table 8. PLL Controller Clock Align Control Register (ALNCTL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	ALN*n*		SYSCLK*n* alignment. Do not change the default values of these fields.
		0	Do not align SYSCLK*n* to other SYSCLKs during GO operation. If SYS*n* in DCHANGE is set, SYSCLK*n* switches to the new ratio immediately after the GOSET bit in PLLCMD is set.
		1	Align SYSCLK*n* to other SYSCLKs selected in ALNCTL when the GOSET bit in PLLCMD is set and SYS*n* in DCHANGE is 1. The SYSCLK*n* rate is set to the ratio programmed in the RATIO bit in PLLDIV*n*.

4.8 PLLDIV Divider Ratio Change Status Register (DCHANGE)

Whenever a different ratio is written to the PLLDIV*n* registers, the PLLCTL flags the change in the DCHANGE status register. During the GO operation, the PLL controller will only change the divide ratio of the SYSCLKs with the bit set in DCHANGE. Note that the ALNCTL register determines if that clock also needs to be aligned to other clocks. The PLLDIV divider ratio change status register is shown in Figure 10 and described in Table 9.

Figure 10. PLLDIV Divider Ratio Change Status Register (DCHANGE)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-n															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS16	SYS15	SYS14	SYS13	SYS12	SYS11	SYS10	SYS9	SYS8	SYS7	SYS6	SYS5	SYS4	SYS3	SYS2	SYS1
R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset; for reset value, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)

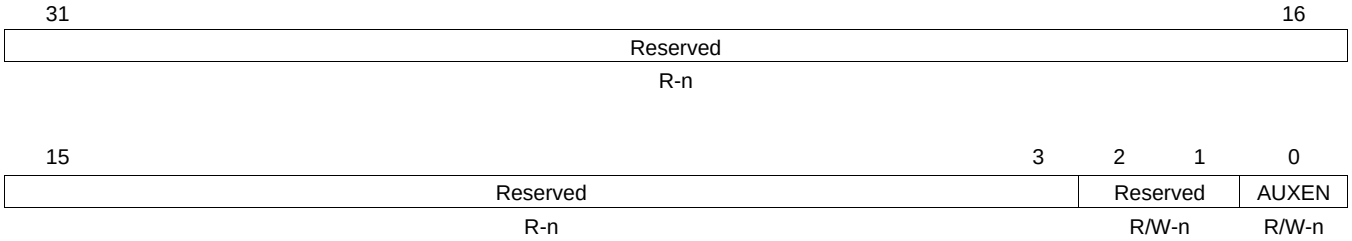
Table 9. PLLDIV Divider Ratio Change Status Register (DCHANGE) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	SYS*n*		Identifies when the SYSCLK*n* divide ratio has been modified.
		0	SYSCLK*n* ratio has not been modified. When GOSET is set, SYSCLK*n* will not be affected.
		1	SYSCLK*n* ratio has been modified. When GOSET is set, SYSCLK*n* will change to the new ratio.

4.9 Clock Enable Control Register (CKEN)

The clock enable control register (CKEN) enables or disables the PLL controller output clock, AUXCLK. CKEN is shown in Figure 11 and described in Table 10.

Figure 11. Clock Enable Control Register (CKEN)



LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset; for reset value, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)

Table 10. Clock Enable Control Register (CKEN) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
2-1	Reserved		Reserved. Writes to this register must keep this bit as 0.
0	AUXEN		AUXCLK enable control.
		0	Disable AUXCLK.
		1	Enable AUXCLK.

4.10 Clock Status Register (CKSTAT)

The clock status register (CKEN) shows the status of all PLL controller output clocks, AUXCLK. CKSTAT is shown in Figure 12 and described in Table 11.

Figure 12. Clock Status Register (CKSTAT)

31	16
Reserved	
R-n	

15	3	2	1	0
Reserved		Reserved		AUXON
R-n		R-n		R-n

LEGEND: R = Read only; -*n* = value after reset; for reset value, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)

Table 11. Clock Status Register (CKSTAT) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
0	AUXON		AUXCLK on status.
		0	AUXCLK is gated.
		1	AUXCLK is on.

4.11 SYSCLK Status Register (SYSTAT)

The SYSCLK status register (SYSTAT) shows the status of SYSCLK1, SYSCLK2, and SYSCLK3. SYSTAT is shown in Figure 13 and described in Table 12.

Figure 13. SYSCLK Status Register (SYSTAT)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-n															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS16 ON	SYS15 ON	SYS14 ON	SYS13 ON	SY123 ON	SYS11 ON	SYS10 ON	SYS9 ON	SYS8 ON	SYS7 ON	SYS6 ON	SYS5 ON	SYS4 ON	SYS3 ON	SYS2 ON	SYS1 ON
R-n	R-n	R-n	R-n	R-n	R-n	R-n	R-n	R-n	R-n	R-n	R-n	R-n	R-n	R-n	R-n

LEGEND: R = Read only; -*n* = value after reset; for reset value, see the *TMS320C6474 Multicore Digital Signal Processor* data manual (SPRS552)

Table 12. SYSCLK Status Register (SYSTAT) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	SYS*n*ON		SYSCLK*n* on status.
		0	SYSCLK*n* is gated.
		1	SYSCLK*n* is on.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265