

***AM/DM37x Multimedia Device***  
***Silicon Revision 1.x***  
***Texas Instruments OMAP™ Family of Products***

***Technical Reference Manual***  
***Delta between version Q and version R***



Literature Number: SPRUGW9Q  
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## AM/DM37x ES1.x TRM Delta introduction

This document contains all the differences between AM/DM37x\_ES1.x\_TRM\_vQ (literature number SPRUGN4Q) and AM/DM37x\_ES1.x\_TRM\_vR (literature number SPRUGN4R).

### **Reading rules:**

~~Strike through~~ = removed.

**Highlighted in yellow** = added or updated

Tables and Figures refer to the previous TRM version. In the new TRM version; their numbering may change due to additional or removal of Tables or Figures.

## **Preface**

No difference.

## **Chapter 1: Introduction**

No difference.

## **Chapter 2: Memory Mapping**

No difference.

## **Chapter 3: Power, Reset, and Clock Management**

No difference.

## **Chapter 4: MPU Subsystem**

No difference.

## **Chapter 5: IVA2.2 Subsystem**

No difference.

## **Chapter 6: Camera Image Signal Processor**

No difference.

## Chapter 7: Display Subsystem

### 7.1 ProDB00114644: HDMI support through DSI interface

#### DESCRIPTION

The maximum resolution supported on DSI video port need to be aligned with actual implementation.

#### CORRECTION

The following modifications are applied:

#### 7.1 Display Subsystem Overview

- MIPI DSI
  - Transfer pixels and data received on the video port or L4 interconnect to the display through the DSI DSI\_PHY
  - The maximum resolution supported on the video port is ~~XGA~~ SVGA at 60 fps with 24-bit pixels (maximum pixel clock of ~~67.48~~ MHz) for low voltage, and WXGA at 60 fps with 24-bit pixels (maximum pixel clock of 86.5 MHz) for nominal voltage
  - Supports video mode and command mode

## **Chapter 8: 2D/3D Graphics Accelerator**

No difference.

## **Chapter 9: Interconnect**

No difference.

## **Chapter 10: Memory Subsystem**

No difference.

## **Chapter 11: SDMA**

No difference.

## **Chapter 12: Interrupt Controller**

No difference.

## **Chapter 13: System Control Module**

No difference.

## **Chapter 14: Interprocessor Communication**

No difference.

## **Chapter 15: Memory Management Units**

No difference.

## **Chapter 16: Timers**

No difference.

## **Chapter 17: I<sup>2</sup>C**

No difference.



## Chapter 18: HDQ/1-Wire

No difference.

## Chapter 19: UART/IrDA/CIR

### 19.1 ProDB00121218: THR\_REG register is limited to 8-bit data access

#### DESCRIPTION

THR\_REG register is limited to 8-bit data access.

#### CORRECTION

A note that THR\_REG register is limited to 8-bit data access is added to Table 19-45. THR\_REG register and typo update.

#### 19.6.1 UART/IrDA/CIR Instance Summary

#### CAUTION

~~The UART\_THR register is limited to 8-bit data accesses; 16- and 32-bit data accesses are not allowed and can corrupt the register content.~~

Only 8-bit and 16-bit accesses are allowed for the THR\_REG register. Performing a 32-bit access can result in a data abort.

**Table 19-45. THR\_REG**

<b>Address Offset</b>	0x000
<b>Physical Address</b>	See <a href="#">Table 19-39</a> to <a href="#">Table 19-40</a>
<b>Description</b>	Transmit holding register The transmitter section consists of the transmit holding register (THR_REG) and the transmit shift register. The transmit holding register is a 64-byte FIFO. The MPU writes data to the THR_REG. The data is placed in the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled, location zero of the FIFO is used to store the data. <b>Note:</b> Only 8-bit and 16-bit accesses are allowed for the THR_REG register. Performing a 32-bit access can result in a data abort.
<b>Type</b>	W

## **Chapter 20: Multichannel SPI**

No difference.

## **Chapter 21: Multichannel Buffered Serial Port**

No difference.

## **Chapter 22: High-Speed USB Host Subsystem and High-Speed USB OTG Controller**

No difference.

## **Chapter 23: Memory Stick PRO Host Controller**

No difference.

## **Chapter 24: MMC/SD/SDIO Card Interface**

No difference.

## **Chapter 25: General-Purpose Interface**

No difference.

## **Chapter 26: Initialization**

No difference.

## **Chapter 27: Debug and Emulation**

No difference.

## **A: Glossary**

No difference.

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