KeyStone II Architecture
10 Gigabit Ethernet Subsystem

User Guide

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SPRUHJ5	February 2013	Initial Release.

Contents

List of Tables

List of Figures

List of Procedures

Preface

About This Manual

This document gives a functional description of the 10 Gigabit Ethernet Switch Subsystem and related portions of the Serializer/Deserializer (SerDes) module. The Ethernet Switch Subsystem consists of the Ethernet Media Access Controller (EMAC) module, Serial Gigabit Media Independent Interface (SGMII) modules, Physical Layer (PHY) device Management Data Input/Output (MDIO) module, Ethernet Switch module, and other associated submodules that are integrated on the device.

Notational Conventions

This document uses the following conventions:

- Commands and keywords are in **boldface** font.
- Arguments for which you supply values are in *italic* font.
- Terminal sessions and information the system displays are in `screen font`.
- Information you must enter is in **`boldface screen font`**.
- Elements in square brackets ([ ]) are optional.

Notes use the following conventions:

Note—Means reader take note. Notes contain helpful suggestions or references to material not covered in the publication.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

CAUTION—Indicates the possibility of service interruption if precautions are not taken.

WARNING—Indicates the possibility of damage to equipment if precautions are not taken.

Related Documentation from Texas Instruments

Multicore Navigator for KeyStone Devices User Guide	SPRUGR9
Network Coprocessor (NETCP) for KeyStone Devices User Guide	SPRUGZ6
Packet Accelerator (PA) for KeyStone Devices User Guide	SPRUGS4
Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide	SPRUGV2
Security Accelerator (SA) for KeyStone Devices User Guide	SPRUGY6

Trademarks

Chapter 1

Introduction

IMPORTANT NOTE—The information in this document should be used in conjunction with information in the device-specific Keystone Architecture data manual that applies to the part number of your device.

This document gives a functional description of the 10 Gigabit Ethernet Subsystem. The 10 Gigabit Ethernet Subsystem combines a 3-port Ethernet switch sub-module and a packet DMA to create a fully contained sub-system capable of 10Gb/s and 1Gb/s rates per Ethernet port. The 3-port Ethernet switch sub-module contains an Ethernet Media Access Controller (EMAC) module, Serial Gigabit Media Independent Interface (SGMII) modules for 1Gb/s operations, 10GBase-R module for 10Gb/s operations, Serializer/Deserializer (SERDES) module, Physical Layer (PHY) device Management Data Input/Output (MDIO) module, Ethernet Switch module, and other associated submodules that are integrated on the device. Included in this document are the features of the packet DMA and 3-port Ethernet switch sub-module, a discussion of their architecture and operation, an overview of the internal and external connections, and descriptions of the registers for each module.

1.1 Purpose of the Peripheral

The 10 Gigabit Ethernet (10GbE) Subsystem purpose is to provide an interface to transfer data at both 10Gb/s and 1Gb/s between the host device and another connected device in compliance with the Ethernet protocol.

1.2 Features

- Provides High Performance DMA Controller
- 128 bit wide primary data path
- 8 Transmit Channels
- 16 Receive Channels
- Supports flexible scatter-gather memory allocation
- Supports intelligent buffer allocation based on packet size
- Provides 10G Ethernet Switch
- Two 10/100/1GIG/10GIG Ethernet ports
- SGMII Interface for 10/100/1000 and 10GBASE-R for 10G
- Wire rate switching (802.1d)
- Non-Blocking switch fabric
- Flexible logical FIFO based packet buffer structure
- Eight priority level QOS support (802.1p)
- Host Port 0 Streaming Packet Interface
- IEEE 1588 Clock Synchronization Support (2008 Annex D, E, and F)
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Ethernet port reset isolation
- MACSEC on Ethernet ports
- Address Lookup Engine
  - 2048 addresses plus VLAN's
  - Wire rate lookup
  - VLAN support
  - Host controlled time-based aging
  - Spanning tree support
  - L2 address lock and L2 filtering support
  - MAC authentication (802.1x : AES-GCM-128 support)
  - Receive or destination based Multicast and Broadcast limits
  - MAC address blocking
  - Source port locking
  - OUI host accept/deny feature
- Flow Control Support (802.3x)
- Castagnoli or Ethernet CRC selectable per port
- EtherStats and 802.3Stats RMON statistics gathering (shared)
- Support for external packet dropping engine.
- MAC transmit to MAC receive loopback mode (digital loopback) supported
- MAC receive to MAC transmit loopback mode (FIFO loopback) supported
- SGMII or SerDes loopback modes (transmit to receive)
- Maximum frame size 9600 bytes (9604 with VLAN)

- MDIO module for PHY management
- Programmable interrupt control with selected interrupt pacing
- Emulation Support

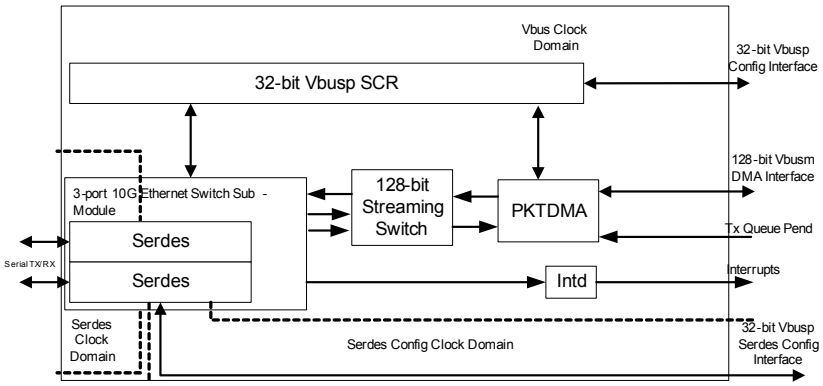
The 10 Gigabit Ethernet (10GbE) Switch Subsystem does not support 1Gb/10Gb half duplex mode

1.3 10 Gigabit Ethernet Subsystem Functional Block Diagram

Figure 1-1 shows the 10 GbE subsystem functional block diagram. The 10GbE subsystem consists of 4 major modules:

- 3-port 10 Gigabit Ethernet switch
- PKTDMA
- Interrupt Distributor
- SERDES (x2)

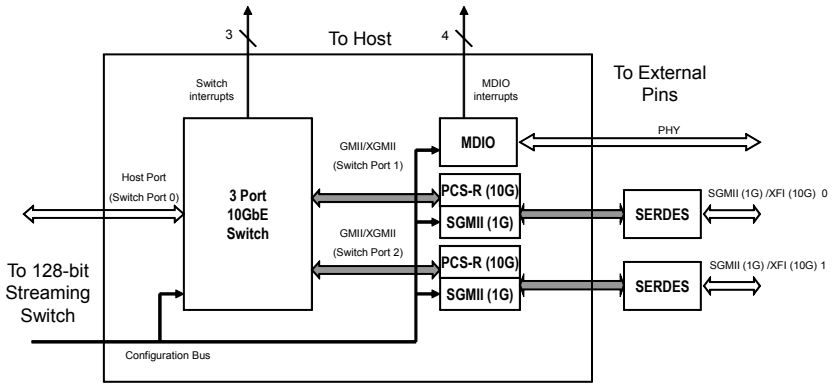
Figure 1-1 10 Gigabit Ethernet Subsystem Block Diagram



The 10 GbE subsystem, as shown in Figure 1-1, has 2 external ports, 1 internal port connecting through an internal bus to PKTDMA, and a set of interrupts going to the host.

1.4 3-Port 10GbE Switch Sub-Module Functional Block Diagram

Figure 1-2 3-port 10 Gigabit Ethernet Switch Sub-module Block Diagram



The 3-port 10GbE switch sub-module contains the following components:

- 10GbE Switch
- MDIO Module
- 2 PCS-R Modules (10GBase-R)
- 2 SGMII modules (10/100/1000Base-T)

The GbE switch, as shown in Figure 1-2, has 3 ports, bus configuration through the 10GbE subsystem, and a set of interrupts going to the host.

- Port 0 is the host port, which allows bidirectional communication between the GbE Switch and the NETCP.
- Port 1 is the XGMII 0 port, which allows bidirectional communication between the GbE switch and the SGMII & PCS-R 1 module.
- Port 2 is the XGMII 1 port, which allows bidirectional communication between the GbE switch and the SGMII & PCS-R 2 module.
- Interrupts from the GbE switch are connected to the DSP to allow communication of the switch status.
- A configuration bus connects the GbE to the NETCP to allow the user to configure the switch.

The SGMII and PCS-R modules, as shown in Figure 1-2, each have a separate connection to the GbE switch, the SerDes, and the configuration bus.

- The GMII & XGMII connection to the GbE switch allows bidirectional communication between the SGMII /PCS-R modules respectively and the switch.
- The SGMII connection to the SerDes allows bidirectional communication between the SGMII module and the SerDes.
- The XSBI connection to the SerDes allows bidirectional communication between the PCS-R module and the SerDes.
- A configuration bus connects each SGMII & PCS-R to the 10GbE subsystem to allow the user to configure these modules.

MDIO module, as shown in Figure 1-2, contains a connection to an external PHY device, a set of interrupts going to the host, and bus configuration through the network coprocessor.

- The connection to an external PHY device allows the MDIO module to monitor the link status of up to 32 addresses.
- Interrupts from the MDIO module are connected to the host to allow communication of changes in link status.
- A configuration bus connects the MDIO to the 10GbE sub-system to allow the user to configure the MDIO.

1.5 Industry Standard(s) Compliance Statement

The 10 Gigabit Ethernet subsystem conforms to the following industry standards:

- Supports IEEE 802.3 specification
  - 10GBASE-R (10G)
  - 10/100/1000Base-T (1G)
- Supports IEEE 1588 (v2008) specification
- Electrical Interfaces
  - Supports XFI SFF INF-8077i spec (no SFP/SFP+) for 10Gb
  - Supports Serial-GMII (SGMII) Specification for 10/100/1000Mb

Chapter 2

Architecture

2.1 Clock Control

This section describes the clocks used by the 10 Gigabit Ethernet (10GbE) subsystem.

The 10GbE subsystem uses the following clocks:

- 10GbE subsystem clock (Vbus Domain)
- SerDes Configuration Clock Domain
- SerDes Clock Domain
- CPTS reference clock
- MDIO clock
- MAC-MII clocks

2.1.1 10GbE Subsystem Clock & SerDes Configuration Clock

The 10GbE subsystem clock is used for most of the logic in the 10GbE subsystem. It is targeted to run at 500 MHz. The clock however can be configured at lower speeds, but it will affect throughput. Minimum frequency to guarantee 10Gb switch rate is 350mhz. However, at this frequency full 20Gb forwarding rate (10Gb x2 ports) is not guaranteed. User must look into the specific data sheet of the Keystone 2 device to determine setup. The 10GbE subsystem clock domain must be enabled before using the subsystem. The Serdes Configuration Clock is derived from the same source as the 10GbE subsystem clock, but it is rate limited to 250mhz. This clock domain does not affect throughput as it is meant for configuration purposes of Serdes modules.

2.1.2 SerDes Clock Domain

The SerDes reference clock is a clock input to the DSP. The SerDes reference clock serves as the input to the SerDes PLL. The output from the SerDes PLL controls the rate at which data is transferred between the SGMII and the SerDes modules. These output frequencies are 644.53mhz in 10G mode and 125mhz in 1G mode. They are also output to the system level for Synchronous Ethernet (SyncE) support. For pin level information and full support please see the device-specific data manual. For the input clock ranges for the SerDes reference clock, see the device-specific data manual.

2.1.3 MDIO Clock

The MDIO clock is divided down from the peripheral system clock. The MDIO clock can operate at up to 2.5 MHz, but typically operates at 1.0 MHz.

2.1.4 CPTS reference clock

The CPTS reference clock is used for the clock synchronization module in the 10GbE subsystem. There are several possible inputs that can be used for the time synchronization clock. To select an input clock source for the CPTS_RCLK, program the CPTS_RFTCLK_SEL field in the CPTS_RFTCLK_SEL register. For a list of clock sources corresponding to the values in the CPTS_RFTCLK_SEL register, see the device-specific data manual.

2.1.5 MAC-MII Clocks

The MAC and MII clock frequencies are fixed by the 802.3 specification as follows:

- 2.5 MHz at 10 Mbps
- 25 MHz at 100 Mbps
- 125 MHz at 1000 Mbps
- 156.25MHz at 10Gbps (XGMII)

2.2 Memory Map

The memory map for the modules in the 10GbE switch subsystem is shown in Table 2-1. The addresses listed are offset addresses, which are dependant on a device-specific base address. For the base address of the 10GbE switch subsystem, see the memory map in the device-specific data manual.

Table 2-1 10 Gigabit Ethernet Subsystem Modules

Module Region	Offset Address[1]
3-port 10 Gigabit Ethernet (10GbE) switch sub-module	00000h
Port 1 SGMII module	00100h
Port 2 SGMII module	00200h
Reserved	00300h-004ffh
MDIO module	00500h-005FFh
Port 1 PCS-R module	00600h-0062Ch
Reserved	00630h-0067fh
Port 2 PCS-R module	00680h-006ach
Reserved	006b0h-00fffh
10 Gigabit Ethernet (10GbE) switch	01000h-01fffh
Reserved	02000h-1fffh
Port 1 MACSEC module	20000h-3fffh
Port 2 MACSEC module	40000h-5fffh
Rserved	60000h-9fffh
10 Gigabit Ethernet (10GbE) Subsystem	A0000h-A00ffh
Packet Streaming Switch Registers	A0600h-A06ffh
PKT DMA Registers	A1000h-A23ffh
INTD Registers	Af000h-Af3ffh
Reserved	Af400h-fffffh
End of Table 2-1	

1. The addresses provided in the table are offsets from a device specific base address. To determine the base address of these registers, see the device-specific data manual.

2.3 Packet DMA Architecture

The packet DMA controller in 10GbE subsystem is responsible for transferring data between 10GbE subsystem and the Host. Data received through the packet DMA from the Host is forwarded via the packet streaming switch to the 3-port 10GbE switch sub-module. Data received by the 10GbE switch sub-module is forwarded via the packet streaming switch to the packet DMA to be delivered to the Host

The subsystem has 8 transmit queues assigned to it. These queues are mapped to PKTDMA TX channels 0-7. Each channel corresponds to a switch priority on port 1 and port 2 (channel 0 corresponds to priority 0, channel1 corresponds to priority 1 etc….). The subsystem has 16 RX channels. Each channel can have its own flow indicating the destination queue. RX channel 0-7 correspond to port 1 and RX channels 8-15 correspond to port 2. Which channel is used depends on priority. The actual priority used is port's 0 switch priority, therefore (channel 0 is port 1 priority 0, channel1 is port 1 priority 1 …channel 8 is port 2 priority 0 channel 9 is port 2 priority 1 etc….).

VLAN information is used to obtain priority on port 1 and port 2 ingress packets. When the 3-port 10GbE switch sub-module is not set for VLAN all packets obtain priority 0 by default. Thus all port 2 packets are transferred to RX channel 8 while all port 1 packets are transferred to RX channel 0. More information on how priority is handled by the switch is found on Section 2.4.7.1.

For more information about packet DMA, see the Multicore Navigator User Guide in "Related Documentation from Texas Instruments" on page ø-x.

2.4 10 Gigabit Ethernet Switch Architecture

This section describes the architecture of the 10 gigabit Ethernet (10GbE) switch.

The 10GbE provides an interface between the packet streaming switch at the 10GbE subsystem level and the two SGMII and PCS-R modules in the 3-port 10GbE switch sub-module. The following modules are part of the 10GbE switch, plus an additional section detailing additional features of the 10GbE switch:

- Streaming Packet Interface
- Media Access Controller Module Architecture (2)
- MAC FIFO Architecture (2)
- Statistics Module Architecture (2)
- Time Synchronization Module Architecture
- Address Lookup Engine (ALE) Module Architecture
- 10GbE Additional Features (non-module specific)

The 10GbE switch has three ports; port 0 communicates with the packet streaming switch, port 1 communicates with the SGMII/PCS-R0 modules, and port 2 communicates with the SGMII/PCS-R1 modules. Throughout the rest of the document port 0 will be referred to as "host port" and port 1 and 2 will be referred to as Ethernet ports. Only when referring to specific modules (i.e. MAC) will port 1 and port 2 will be referred to as MAC ports or Ethernet MAC ports.

To interface to the packet streaming switch, the 10GbE switch contains transmit and receive interfaces to convert between the signals used by the 10GbE switch and the signals used by the packet streaming switch. The 10GbE switch provides two MAC modules to convert between the signals internal to the switch and the GMII/XGMII signals required by the SGMII/PCS-R modules respectively. Also provided are two MACSEC modules Ethernet side port providing encryption for transmitted and received packets over the Ethernet network. Information on how MACSEC packets are processed is described throughout the next sections. Configuration of the MACSEC module has a separate section.

The 10GbE switch also contains several other modules which provide additional features. The 10GbE switch has two modules that provide Ethernet statistics for the packets transmitted and received by the Ethernet switch subsystem. The 10GbE switch also contains a clock synchronization submodule to support IEEE 1588 v2 & Synchronous Ethernet. Lastly, the 10GbE switch provides an address lookup engine (ALE), which is responsible for forwarding and filtering packets based on address. Each of these modules is covered in more detail in the respective sections.

2.4.1 Streaming Packet Interface

This section describes the details of the streaming packet interface. The streaming packet interface is responsible for communication between the 10GbE switch and the packet streaming switch in the 10GbE subsystem.

2.4.1.1 Transmit Streaming Packet Interface

The transmit interface is responsible for transmitting packets from the 10GbE switch port 0 to the packet DMA over the packet streaming switch. The 10GbE switch has two identical transmit streaming packet interfaces. The first interface (TXA) outputs packets received on port 1 that are destined for port 0. The second interface (TXB) outputs packets that were received on port 2 and are destined for port 0. The data on the streaming interface data is equivalent to MAC output data with the difference being that instead of outputting X/GMII data, the data output is formatted for transmission on the streaming interface.

In addition to the packet data, the transmit streaming interface also provides additional information that is placed in the descriptor of the received packet by the receive flow of the packet DMA. This extra information is included in the PS_FLAGS of the packet descriptor and in the SRC_TAG of the packet descriptor.

Table 2-1 PS_FLAGS for 10GbE Switch Egress Packets

PS_FLAGS Bits	Field	Description
3	RX_PASS_CRC	Passed CRC – The CRC is always passed on Host port egress. This bit is always set
2	CRC_TYPE	CRC Type 0 – Ethernet CRC 1 – Castagnoli CRC
1-0	Reserved	

Table 2-2 SRC_TAG for 10GbE Switch Egress Packets

PS_FLAGS Bits	Field	Description
15-8	src_id	Source ID - This is a unique value to inform user if the packet was received over port 1 or port 2. The packet src_id value comes from the p[N]_src_id field in the P0_SRC_ID register. Where N is 1 for Ethernet port 1 and 2 for Ethernet port 2. See Chapter 3 "CPPI Threshold" on page 3-40 for more information.
7-4	Reserved	
3	from_port	From Port - 0 – The packet was received on Ethernet port 1 1 – The packet was received on Ethernet port 2
2-0	sw_pri	Switch Priority – The actual hardware switch priority that the packet was stored in on the Host Port transmit FIFO.

Both TXA and TXB transmit interfaces have a 22k byte buffer to enable more efficient transmit packet operations. The transmit interfaces do not transmit packets on the streaming interface until there is an entire packet in the output buffer or until there is at least CPSW_CPPI_THRESH plus two words (not bytes) in the output buffer. The "plus two" is there because a two-word double buffer is also present.

2.4.1.2 Transmit VLAN Processing

This section covers transmit processing when in VLAN-aware mode. The 10GbE switch is in VLAN-aware mode when the VLAN_AWARE bit is set in the CPSW_CONTROL register. While in VLAN-aware mode, VLAN is added, removed, or replaced according to the same rules as the MAC transmit (egress) output packet VLAN process. Transmit packets are not modified when VLAN_AWARE is cleared to zero.

2.4.1.3 Receive Streaming Packet Interface

The receive streaming interface on port 0 of the 10GbE switch is responsible for receiving packets from the packet DMA over the packet streaming switch. The 10GbE switch has one receive streaming packet interface for port 0. The Host receive port is equivalent to an Ethernet port with the difference being that the data is provided to the 10GbE switch in the streaming interface data format instead of X/GMII data format.

In addition to the packet data, the receive streaming interface can also provide additional control information that resides in the PS_FLAGS field and DST_TAG field of the descriptor of the packet that was transmitted to the 10GbE switch.

For packets being transmitted to the 10GbE, the PS_FLAGS field has the following configuration:

Table 2-3 PS_FLAGS for 10GbE Switch Ingress Packets

PS_FLAGS Bits	Field	Description
3	RX_PASS_CRC	Receive pass CRC. 0 = The packet does not contain a CRC. The CRC should be generated by the MAC module. 1 = The packet already contains a CRC. The CRC should not be generated by the MAC module. • Please see Section 2.4.7.3 and Section 2.4.2 for more information on CRC handling.
2	CRC_TYPE	CRC Type 0 – Ethernet CRC 1 – Castagnoli CRC
1	macsec_controlled	MACSEC Controlled – This bit should be set for every packet to indicate the ALE it needs to be encrypted.
0	macsec_debug	MACSEC Debug – Setting this bit causes the ALE to drop the packet.

Setting the RX_PASS_CRC bit indicates that the CRC is passed with the packet.

Table 2-4 DST_TAG for 10GbE Switch Ingress Packets

DST_TAG Bits	Field	Description
2-0	to_port	Directed packet to port. Setting these bits to a non-zero value indicates that the packet is a directed packet. Packets with the these bits set will bypass the ALE and send the packet directly to the port indicated. 0 = No effect 1 = Send packet to 10GbE switch port 1 2 = Send packet to 10GbE switch port 2 3-7 = Reserved

The packet is a directed packet when any of the TO_PORT bits are nonzero. The packet will be sent to the port indicated.

2.4.2 Media Access Controller Module Architecture

This section describes the architecture of the media-access-controller (MAC) submodule. The MAC submodule is IEEE 802.3 compliant and supports 10/100/1000 megabit per second (Mbps) modes of operation. The MAC module provides an interface between the 10GbE switch and the SGMII modules. For transmit operations, the MAC module converts between the data signals used by the 10GbE switch and the GMII signals used by the SGMII modules. For receive operations, the MAC module converts between the GMII signals from the SGMII module to the signals used by the 10GbE switch. The transmit and receive operations are described in more detail in subsequent sections.

In addition to translating between the SGMII modules and the 10GbE switch, the MAC module is responsible operations related to IEEE 802.3 Ethernet frames. For all packets, the MAC module adds or removes the preamble, start of frame delimiter, and Interpacket gap to a packet. The MAC module verifies and optionally generates CRC checksums.

2.4.2.1 Data Receive Operations

This section describes the data-receive operations of the MAC module.

2.4.2.1.1 Receive Control

The MAC module is responsible for interpreting X/GMII data received from the PCS-R and SGMII modules respectively. Interpretation of X/GMII data involves the following operations:

- Detection and removal of the preamble
- Detection and removal of the start of frame delimiter
- Extraction of the address
- Extraction of the frame length
- Data handling
- Error checking and reporting
- Cyclic redundancy checking (CRC)
- Statistics signal generation

All statistics signal generation is reported to the proper statistics module in the 10GbE switch.

2.4.2.1.2 Receive Interframe Interval

The 802.3 required interpacket gap (IPG) is 24 GMII clocks (96 bit times) for 10/100 Mbps modes, and 12 GMII clocks (96 bit times) for 1000 Mbps mode. However, the MAC module can tolerate a reduced IPG (2 GMII clocks in 10/100 mode and 5 GMII clocks in 1000 mode) with a correct preamble and start of frame delimiter.

This interval between frames must comprise (in the following order):

1. An interpacket gap (IPG)
2. A seven-octet preamble (all octets 0x55)
3. A one-octet start of frame delimiter (0x5D)

2.4.2.1.3 Receive Flow Control

This section describes the receive flow control functionality. When under heavy load, the MAC module can limit further frame reception through receive frame flow control. Receive flow control is enabled by setting the RX_FLOW_EN bit in the MAC_CONTROL register. When enabled, flow control events are triggered by the receive FIFO in the 10GbE switch module. When receive flow control is enabled, and a flow control event is triggered, receive flow control is initiated. When in half-duplex mode, receive flow control is collision based. While in full duplex mode, flow control is handled by issuing 802.3X pause frames. In either case, receive flow control prevents frame reception by issuing the flow control appropriate for the current mode of operation. The MAC module is configured for collision or IEEE 802.3X flow control via the FULLDUPLEX bit in the MAC_CONTROL register.

2.4.2.1.4 Collision Based Receive Flow Control

This section describes collision-based receive flow control. Collision-based receive flow control provides a means of preventing frame reception when the port is operating in half-duplex mode (the FULLDUPLEX bit is cleared in MAC_CONTROL register). When receive flow control is enabled and triggered, the port generates collisions for received frames. The jam sequence transmitted will be the twelve byte sequence C3.C3.C3.C3.C3.C3.C3.C3.C3.C3.C3.C3 (hex). The jam sequence begins no later than approximately as the source address starts to be received. Note that these forced collisions will not be limited to a maximum of 16 consecutive collisions and are independent of the normal back-off algorithm. Receive flow control does not depend on the value of the incoming frame destination address. A collision is generated for any incoming packet, regardless of the destination address.

2.4.2.1.5 IEEE 802.3X Based Receive Flow Control

This section describes IEEE 802.3x based receive flow control. IEEE 802.3x-based receive flow control provides a means of preventing frame reception when the port is operating in full-duplex mode (the FULLDUPLEX bit is set in MAC_CONTROL register). When receive flow control is enabled and triggered, the port transmits a pause frame to request that the sending station stop transmitting for the period indicated within the transmitted pause frame.

The MAC module transmits a pause frame to the reserved multicast address at the first available opportunity. If the MAC module is idle, a pause frame is transmitted immediately, otherwise the pause frame is sent following the completion of the frame currently being transmitted. When issuing a pause frame, the frame contains 0xFFFF, which is the maximum possible pause time value. The MAC module counts the receive pause frame time, decrementing 0xFF00 down to zero, and retransmits an outgoing pause frame if the count reaches zero. When the flow control request is removed, the MAC module transmits a pause frame with a zero pause time to cancel the pause request.

Note—Transmitted pause frames are only a request to the other end station to stop transmitting. Frames that are received during the pause interval are received normally (provided the receive FIFO is not full).

Pause frames are transmitted if enabled and triggered regardless of whether the port is observing the pause time period from an incoming pause frame.

The MAC module transmits pause frames as described below:

- The 48-bit reserved multicast destination address 01.80.C2.00.00.01
- The 48-bit source address found in the SLx_SA_HI and SLx_SA_LO registers in the 10GbE switch
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 00.01
- The 16-bit pause time value FF.FF. A pause-quantum is 512 bit-times. Pause frames sent to cancel a pause request will have a pause time value of 00.00.
- Zero padding to 64-byte data length (The MAC module will transmit only 64 byte pause frames)
- The 32-bit frame-check sequence (CRC word)

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

If RX_FLOW_EN is cleared to zero while the pause time is nonzero, the pause time will be cleared to zero, and a zero-count pause frame will be sent.

2.4.2.2 Data Transmission

This section describes transmit data operations for the MAC module. The MAC module accepts data from the 10GbE switch, converts the data to X/GMII format, and transmits the data to the PCS-R and SGMII modules respectively. Data transmission is synchronized to the transmit clock rate. The smallest frame that can be sent is two bytes of data with four bytes of CRC (6 byte frame).

2.4.2.2.1 Transmit Control

This section describes transmit control operations for the MAC module. If a collision is detected on a transmit packet, the MAC module outputs a jam sequence. If the collision was late (after the first 64 bytes have been transmitted) the collision is ignored. If the collision is not late, the controller will back off before retrying the frame transmission. When operating in full duplex mode, the carrier sense (CRS) and collision sensing modes are disabled.

2.4.2.2.2 CRC Insertion

This section describes the procedure for inserting CRC checksums into Ethernet frames. The MAC module can generate and append a 32-bit Ethernet CRC onto transmitted data. By default, the MAC module generates and appends a CRC. If the user does not want the MAC module to generate a CRC, bit 19 of the packet data word 2 (bit 3 of protocol specific flags) of the descriptor must be set before transmitting the packet via the packet DMA to the 10GbE subsystem. If bit 19 of the packet data word 2 (bit 3 of protocol specific flags) is set in the descriptor, the last four bytes of the TX data are transmitted as the frame CRC. The four CRC data bytes should be the last four bytes of the frame and should be included in the packet byte count value. The MAC performs no error checking on the outgoing CRC when bit of the packet data word 2 (bit 3 of protocol specific flags) is set in the descriptor.

2.4.2.2.3 MTXER

The GMII MTXER signal is not used in the MAC module. If an underflow condition occurs on a transmitted frame, the frame CRC will be inverted to indicate the error to the network. Underflow is a hardware error.

2.4.2.2.4 Adaptive Performance Optimization (APO)

This section describes Adaptive Performance Optimization (APO) implemented in the MAC module. The Ethernet MAC port incorporates APO logic that may be enabled by setting the TX_PACE bit in the MAC_CONTROL register. When the TX_PACE bit is set, transmission pacing to enhance performance is enabled. Adaptive performance pacing introduces delays into the normal transmission of frames, delaying transmission attempts between stations. By introducing delays, the probability of collisions will be reduced during heavy traffic (as indicated by frame deferrals and collisions), thereby increasing the chance of successful transmission.

When a frame is deferred, suffers a single collision, multiple collisions, or excessive collisions, the pacing counter is loaded with an initial value of 31. When a frame is transmitted successfully (without experiencing a deferral, single collision, multiple collision, or excessive collision) the pacing counter is decremented by one, down to zero.

With pacing enabled, a new frame is permitted to immediately (after one IPG) attempt transmission only if the pacing counter is zero. If the pacing counter is non zero, the frame is delayed by the pacing delay, which is equivalent to approximately four Interpacket gap delays. APO only affects the IPG preceding the first attempt at transmitting a frame. It does not affect the back-off algorithm for retransmitted frames.

2.4.2.2.5 Interpacket Gap Enforcement

This section describes the enforcement of interpacket gap for the MAC module. The measurement reference for the IPG of 96 bit times is changed depending on frame traffic conditions. If a frame is successfully transmitted without collision, and the MCRS signal is deasserted within approximately 48 bit times of the MTXEN signal being deasserted, 96 bit times is measured from MTXEN. If the frame suffered a collision, or if the MCRS signal is not de-asserted until more than approximately 48 bit times after MTXEN is deasserted, 96 bit times (approximately, but not less) is measured from MCRS.

The transmit IPG can be shortened by eight bit times when enabled and triggered. The TX_SHORT_GAP_EN bit in the MAC_CONTROL register enables the TX_SHORT_GAP input to determine whether the transmit IPG is shorted by eight bit times.

2.4.2.2.6 Back Off

The MAC module implements the 802.3 binary exponential back-off algorithm.

2.4.2.2.7 Programmable Transmit Interpacket Gap

The transmit interpacket gap (IPG) is programmable through the TX_GAP register. The default value is decimal 12. The transmit IPG may be increased to the maximum value of 0x1ff. Increasing the IPG is not compatible with transmit pacing. The short gap feature will override the increased gap value, so the short gap feature may not be compatible with an increased IPG.

2.4.2.2.8 Transmit Flow Control

This section describes the transmit flow control implemented on MAC module. When enabled, incoming pause frames are acted upon to prevent the MAC module from transmitting any further frames. Incoming pause frames are only acted upon when the FULLDUPLEX and TX_FLOW_EN bits are set in the MACCONTROL register. Pause frames are not acted upon in half-duplex mode. Pause frame action will be taken if

enabled, but normally the frame will be filtered and not transferred to memory. MAC control frames will be transferred to memory if the RX_CMF_EN (copy MAC Frames) bit in the MAC_CONTROL register is set. The TX_FLOW_EN and FULLDUPLEX bits effect whether or not MAC control frames are acted upon, but they have no effect upon whether or not MAC control frames are transferred to memory or filtered.

Pause frames are a subset of MAC control frames with an opcode field=0x0001. Incoming pause frames will only be acted upon by the port if all the following conditions are met:

- TX_FLOW_EN is set in the MAC_CONTROL register
- The frame's length is 64 to MAC_RX_MAXLEN bytes inclusive
- The frame contains no CRC error or align/code errors

The pause-time value from valid frames is extracted from the two bytes following the opcode. The pause time will be loaded into the port's transmit pause timer and the transmit pause time period will begin.

If a valid pause frame is received during the transmit pause time period of a previous transmit pause frame then:

- if the destination address is not equal to the reserved multicast address or any enabled or disabled unicast address, then the transmit pause timer will immediately expire, or
- if the new pause time value is zero then the transmit pause timer will immediately expire, else
- the port transmit pause timer will immediately be set to the new pause frame pause time value. (Any remaining pause time from the previous pause frame will be discarded)

If the TX_FLOW_EN field in the MAC_CONTROL register is cleared, then the pause-timer will immediately expire.

The port will not start the transmission of a new data frame any sooner than 512-bit times after a pause frame with a non-zero pause time has finished being received (MRXDV going inactive). No transmission will begin until the pause timer has expired (the port may transmit pause frames in order to initiate outgoing flow control). Any frame already in transmission when a pause frame is received will be completed and unaffected.

Incoming pause frames consist of the below:

- A 48-bit destination address equal to:
  - The reserved multicast destination address 01.80.C2.00.00.01, or
  - The 48-bit MAC source address found in the SLx_SA_HI and SLx_SA_LO registers in the 10GbE switch
- The 48-bit source address of the transmitting device
- The 16-bit length/type field containing the value 88.08
- The 16-bit pause opcode equal to 00.01
- The 16-bit pause_time. A pause-quantum is 512 bit-times
- Padding to 64-byte data length
- The 32-bit frame-check sequence (CRC word)

All quantities above are hexadecimal and are transmitted most-significant byte first. The least-significant bit is transferred first in each byte.

The padding is required to make up the frame to a minimum of 64 bytes. The standard allows pause frames longer than 64 bytes to be discarded or interpreted as valid pause frames. The MAC module will recognize any pause frame between 64 bytes and MAC_RX_MAXLEN bytes in length.

2.4.2.2.9 Speed, Duplexity, and Pause Frame Support Negotiation

The MAC module can operate in half duplex or full duplex in 10/100 Mbps modes, and can operate in full duplex only in 1000 Mbps mode. Pause frame support is included in 10/100/1000 Mbps modes as configured by the host.

2.4.2.2.10 Frame Classification

Received frames are proper (good) frames if they are between 64 and MAC_RX_MAXLEN in length (inclusive) and contain no errors (code/align/CRC).

Received frames are long frames if their frame count exceeds the value in the MAC_RX_MAXLEN register. The default MAC_RX_MAXLEN register value is 1518 (decimal). Long received frames are either oversized or jabber frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment errors are jabber frames.

Received frames are short frames if their frame count is less than 64 bytes. Short frames that contain no errors are undersized frames. Short frames with CRC, code, or alignment errors are fragment frames.

A received long packet will always contain MAC_RX_MAXLEN number of bytes transferred to memory (if RX_CEF_EN = 1). An example with MAC_RX_MAXLEN = 1518 is below:

- If the frame length is 1518, then the packet is not a long packet and there will be 1518 bytes transferred to memory
- If the frame length is 1519, there will be 1518 bytes transferred to memory. The last three bytes will be the first three CRC bytes
- If the frame length is 1520, there will be 1518 bytes transferred to memory. The last two bytes will be the first two CRC bytes
- If the frame length is 1521, there will be 1518 bytes transferred to memory. The last byte will be the first CRC byte
- If the frame length is 1522, there will be 1518 bytes transferred to memory. The last byte will be the last data byte

2.4.3 MAC FIFO Architecture

This section describes the architecture of the MAC FIFOs. Internal to the 10GbE switch, both Ethernet ports have an identical packet FIFO. Each packet FIFO contains a single logical receive queue and eight logical transmit queues (priority 0 through 7). Each transmit FIFO memory contains 81,920 bytes (80k) total organized as 2056 by 256-bit words contained in a single memory instance. Each receive FIFO memory contains a total of 32768 bytes total organized as 1024 by 256-bit words contained in a single memory instance. The FIFO memory is used for the associated port transmit and receive queues. The TX_BLK_CNT field in the FIFO's associated BLK_CNT register determines the maximum number of FIFO memory blocks to be allocated to the eight logical transmit queues (transmit total). The RX_BLK_CNT field in the FIFO's

associated BLK_CNT register determines the maximum number of memory blocks to be allocated to the logical receive queue. When a port is configured for flow control mode, the receive FIFO blocks allocation should be increased with a corresponding decrease in transmit FIFO blocks.

Note—Careful consideration must be put if changing this configuration. The recommended setup is default TX_BLK_CNT and RX_BLK_CNT

2.4.4 Statistics Module Architecture

This section describes the architecture of the statistics modules in the 10GbE switch. The 10GbE switch has three sets of statistics modules that record events associated with packets entering and exiting the switch. The statistics for switch port 0 are recorded on statistics module 0 (STATS0), statistics for ports 1 are recorded on statistics module 1 (STATS1) and statistics port 2 are recorded on statistics module 2(STATS2). Each statistic register is 32-bits wide and will automatically increment when a certain statistics condition is met. Each statistic will rollover from 0xFFFFFFFF to 0x00000000.

2.4.4.1 Accessing Statistics Registers

This section describes how to correctly read and write to the registers in the statistics modules while the modules are disabled or enabled. By default, the statistics modules are disabled. While disabled, all statistics registers can be read and written normally, so writing to 0x00000000 clears a statistics register. After the statistics modules are enabled, all statistics can still be read normally; however, register writes will become write to decrement, meaning that the value written to the register will be subtracted from the register value, with the result being stored in the register (new register value = old register value - write value). If the value written is greater than the value in the statistics register, then 0 will be written to that register. When a statistics module is enabled, writing a value of 0xFFFFFFFF will clear a statistics location. When writing to a statistics register, 32-bit accesses must be used. The statistics modules can be enabled by writing to bits 2:0 the STAT_PORT_EN register.

2.4.4.2 Statistics Interrupts

This section describes interrupts generated by the statistics modules. Each of the three statistics modules have the ability to send an interrupt to the host. The interrupt for the STATS0 module will occur on the STAT_PEND_RAW[0] signal, the interrupt for the STATS1 module will occur on the STAT_PEND_RAW[1] signal and so on. The interrupt will be triggered when any of the values in the statistics registers become greater than or equal to 0x80000000. The statistics interrupt can be removed by writing a value greater than 0x80000000.

2.4.4.3 Receive Statistics Descriptions

2.4.4.3.1 Good Receive Frames

The good receive frames statistic is the total number of good frames received on the port. A good frame has the following characteristics:

- Any data or MAC control frame which matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error, or code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.4.4.3.2 Broadcast Receive Frames

The broadcast receive frames statistic is the total number of good broadcast frames received on the port. A good broadcast frame has the following characteristics:

- Any data or MAC control frame which was destined for address 0xFFFFFFFFFFFF only
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error, or code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.4.4.3.3 Multicast Receive Frames

The multicast receive frames statistic is total number of good multicast frames received on the port. A good multicast frame has the following characteristics:

- Any data or MAC control frame which was destined for any multicast address other than 0xFFFFFFFFFFFF
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error, or code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.4.4.3.4 Pause Receive Frames

The pause receive frames statistic is total number of IEEE 802.3X pause frames received by the port (whether acted upon or not). Such a frame has the following characteristics:

- Contained any unicast, broadcast, or multicast address
- Contained the length/type field value 88.08 (hex) and the opcode 0x0001
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error
- Pause-frames had been enabled in the MAC module on that port (TX_FLOW_EN = 1)

The port could have been in either half-duplex or full-duplex mode.

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect on this statistic.

2.4.4.3.5 Receive CRC Errors

The receive CRC errors statistic is the total number of frames received on the port that experienced a CRC error. Such a frame has the following characteristics:

- Was any data or MAC control frame which matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had no code/align error, and
- Had a CRC error

Overruns have no effect on this statistic.

A CRC error has the following characteristics:

- A frame containing an even number of nibbles
- Fails the frame check sequence test

2.4.4.3.6 Receive Align/Code Errors

The receive align/code errors statistic is the total number of frames received on the port that experienced an alignment error or code error. Such a frame has the following characteristics:

- Was any data or MAC control frame which matched a unicast, broadcast. or multicast address, or matched due to promiscuous mode
- Was of length 64 to RX_MAXLEN bytes inclusive
- Had either an alignment error or a code error

Over-runs have no effect on this statistic.

An alignment error has the following characteristics:

- A frame containing an odd number of nibbles
- Fails the frame check sequence test if the final nibble is ignored

A code error is defined to be a frame which has been discarded because the port's MRXER pin driven with a one for at least one bit-time's duration at any point during the frame's reception.

Note—RFC 1757 etherStatsCRCAlignErrors Ref. 1.5 can be calculated by summing the receive align/code errors and receive CRC errors (see below).

2.4.4.3.7 Oversize Receive Frames

The oversize receive frames statistic is total number of oversized frames received on the port. An oversized frame has the following characteristics:

- Was any data or MAC control frame which matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode
- Was greater than RX_MAXLEN in bytes
- Had no CRC error, alignment error, or code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.4.4.3.8 Receive Jabber Frames

The receive jabber frames statistic is the total number of jabber frames received on the port. A jabber frame has the following characteristics:

- Was any data or MAC control frame which matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode
- Was more than RX_MAXLEN bytes long
- Had a CRC error, an alignment error, or a code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.4.4.3.9 Undersize (Short) Receive Frames

The undersize receive frames statistic is the total number of undersized frames received on the port. An undersized frame has the following characteristics:

- Any data frame which matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode
- Was less than 64 bytes long
- Had no CRC error, alignment error, or code error

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.4.4.3.10 Receive Fragments

The receive fragments statistic is the total number of frame fragments received on the port. A frame fragment has the following characteristics:

- Any data frame (address matching does not matter)
- Was less than 64 bytes long
- Had a CRC error, an alignment error, or a code error
- Was not the result of a collision caused by half duplex, collision based flow control

See the receive align/code errors and receive CRC errors statistic descriptions for definitions of alignment, code, and CRC errors. Overruns have no effect on this statistic.

2.4.4.3.11 Receive IPG Error

The total number of 10G frames received on a port that had a correct preamble but did not have at least five bytes of IDLE preceding the frame. This does not indicate if the frame with the IPG error was kept or ignored.

2.4.4.3.12 Receive Start of Frame Overruns

The receive start of frame overruns statistic is the total number of frames received on the port that had a start of frame (SOF) overrun or were dropped by due to FIFO resource limitations. SOF overrun frame has the following characteristics:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was any length (including <64 bytes and > RX_MAXLEN bytes)
- The packet was dropped due to FIFO resource limitations

2.4.4.3.13 Overrun Type 1

STAT 0-2

The total number of frames received on a port that overran the port.s receive FIFO and were dropped. Port 0 (Host receive port) should not drop packets on receive because port 0 receive flow control should be enabled. The Ethernet ports will only drop packets in the receive FIFO when receive flow control is enabled and the sending port ignores sent pause frame and then overruns the receive FIFO. The overrun frame is defined to be:

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- was any length (including <64 bytes and > rx_maxlen bytes), and
- was dropped on port 0 due to a lack of memory space in the receive FIFO.

STAT 0

This statistic also counts frames dropped on port 0 that were 17 to 33 bytes (only for port 0). For Ethernet ports, the drop count for frames shorter than 33 bytes is included in the undersized or fragment count. Port 0 simply gives an indication that a packet with 33 bytes was dropped. No other statistics are counted for frames shorter than 33 bytes.

2.4.4.3.14 Overrun Type 2

STAT 0-2

The total number of frames received on a port that were dropped by the ALE (the ALE did not forward the packet to any port). The frame was defined to be:

- Was any data or MAC control frame
- Was any length greater than 33 bytes
- Was dropped by the ALE - ale_portmask = 0 (was not sent to any destination port)
- The frame could have been dropped due to error so it could be counted elsewhere also.

2.4.4.3.15 Overrun Type 3

STAT 0-2

The total number of frames received on a port that had a START of frame (SOF) overrun on any destination port egress (when attempting to load the packet into any other port.s transmit FIFO). SOF overrun is defined to be

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- was any length (including <64 bytes and > rx_maxlen bytes), and
- had a SOF of frame overrun on another port egress.

2.4.4.3.16 Overrun Type 4

STAT 0-2

The total number of frames received on a port such that the destination port was not equal to the source port but the frame was not forwarded to any port.

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- was any length (including <64 bytes and > rx_maxlen bytes), and
- the destination port was not equal to the source port and had a zero port_mask

2.4.4.3.17 Overrun Type 5

STAT 1-2

The total number of frames received on a port that were dropped (zero port_mask) due to exceeding the maximum ALE lookup rate (Port 0 should have no type 5 overruns).

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- was any length (including <64 bytes and > rx_maxlen bytes), and
- the maximum ALE lookup rate was exceeded so the lookup was aborted and the packet was dropped.

2.4.4.3.18 Rx Octets

The total number of bytes in all good frames received on the port. A good frame is defined to be

- was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and
- was of length 64 to rx_maxlen bytes inclusive, and
- had no CRC error, alignment error or code error.

See the Rx Align/Code Errors and Rx CRC errors statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

2.4.4.4 Transmit (only) Statistics Descriptions

The maximum and minimum transmit frame size is software controllable.

2.4.4.4.1 Good Transmit Frames

The good transmit frames statistic is the total number of good frames transmitted on the port. A good frame has the following characteristics:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Was any length
- Had no late or excessive collisions, no carrier loss, and no underrun

2.4.4.4.2 Broadcast Transmit Frames

The broadcast transmit frames statistic is the total number of good broadcast frames transmitted on the port. A good broadcast frame has the following characteristics:

- Any data or MAC control frame destined for address 0xFFFFFFFFFFFF only
- Was of any length
- Had no late or excessive collisions, no carrier loss, and no underrun

2.4.4.4.3 Multicast Transmit Frames

The multicast transmit frames statistic is the total number of good multicast frames transmitted on the port. A good multicast frame has the following characteristics:

- Any data or MAC control frame destined for any multicast address other than 0xFFFFFFFFFFFF
- Was of any length
- Had no late or excessive collisions, no carrier loss, and no underrun

2.4.4.4.4 Pause Transmit Frames

The pause transmit frames statistic indicates the number of IEEE 802.3X pause frames transmitted by the port.

Pause frames cannot underrun or contain a CRC error because they are created in the transmitting MAC, so these error conditions have no effect on the statistic. Pause frames sent by software will not be included in this count.

Since pause frames are only transmitted in full duplex, carrier loss and collisions have no effect on this statistic.

Transmitted pause frames are always 64 byte multicast frames so they will appear in the transmit multicast frames and 64 octet frames statistics.

2.4.4.4.5 Collisions

The collisions statistic records the total number of times that the port experienced a collision. Collisions occur under two circumstances.

1. When a transmit data or MAC control frame has the following characteristics:
   - Was destined for any unicast, broadcast or multicast address
   - Was any size
   - Had no carrier loss and no underrun
   - Experienced a collision

   A jam sequence is sent for every non-late collision, so this statistic increments on each occasion a frame experiences multiple collisions (and increments on late collisions).

   CRC errors have no effect on this statistic.
2. When the port is in half-duplex mode, flow control is active, and a frame reception begins

2.4.4.4.6 Single Collision Transmit Frames

The single collision transmit frames statistic is the total number of frames transmitted on the port that experienced exactly one collision. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced one collision before successful transmission. The collision was not late

CRC errors have no effect on this statistic.

2.4.4.4.7 Multiple Collision Transmit Frames

The multiple collision transmit frames statistic is the total number of frames transmitted on the port that experienced multiple collisions. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 2 to 15 collisions before being successfully transmitted. None of the collisions were late

CRC errors have no effect on this statistic.

2.4.4.4.8 Excessive Collisions

The excessive collisions statistic is the total number of frames for which transmission was abandoned due to excessive collisions. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 16 collisions before abandoning all attempts at transmitting the frame. None of the collisions were late

CRC errors have no effect on this statistic.

2.4.4.4.9 Late Collisions

The late collisions statistic is the total number of frames on the port for which transmission was abandoned because they experienced a late collision. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- Experienced a collision later than 512 bit-times into the transmission. There may have been up to 15 previous (non-late) collisions which had previously required the transmission to be re-attempted

This statistic dominates over the single, multiple, and excessive collisions statistics - if a late collision occurs the frame will not be counted in any of these other three statistics.

CRC errors, carrier loss, and underrun have no effect on this statistic.

2.4.4.4.10 Deferred Transmit Frames

The deferred transmit frames statistic is the total number of frames transmitted on the port that first experienced deferment. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced no collisions before being successfully transmitted
- Found the medium busy when transmission was first attempted, so had to wait

CRC errors have no effect on this statistic

Note—See RFC1623 Ref. 2.6 dot3StatsDefferredTransmissions.

2.4.4.4.11 Carrier Sense Errors

The carrier sense errors statistic is the total number of frames on the port that experienced carrier loss. Such a frame has the following characteristics:

- Was any data or MAC control frame destined for any unicast, broadcast, or multicast address
- Was any size
- The carrier sense condition was lost or never asserted when transmitting the frame (the frame is not retransmitted)

This is a transmit only statistic. Carrier Sense is a don't care for received frames. Transmit frames with carrier sense errors are sent until completion and are not aborted.

CRC errors and underrun have no effect on this statistic.

2.4.4.4.12 Transmit Octets

The transmit octets statistic is the total number of bytes in all good frames transmitted on the port. A good frame has the following characteristics:

- Any data or MAC control frame which was destined for any unicast, broadcast, or multicast address
- Was any size
- Had no late or excessive collisions, no carrier loss, and no underrun

2.4.4.5 Receive and Transmit (shared) Statistics Descriptions

2.4.4.5.1 Net Octets

The total number of bytes of frame data received and transmitted on the port. Each frame counted

- was any data or MAC control frame destined for any unicast, broadcast or multicast address (address match does not matter), and
- was of any size (including <64 byte and > rx_maxlen byte frames).

Also counted in this statistic are:

- every byte transmitted before a carrier-loss was experienced,
- every byte transmitted before each collision was experienced, (i.e. multiple retries are counted each time),
- every byte received if the port is in half-duplex mode until a jam sequence was transmitted to initiate flow control. (The jam sequence was not counted to prevent double-counting).

Error conditions such as alignment errors, CRC errors, code errors, overruns and underruns do not affect the recording of bytes by this statistic.

The objective of this statistic is to give a reasonable indication of Ethernet utilization.

2.4.4.5.2 Receive + Transmit 64 Octet Frames

The receive and transmit 64 octet frames statistic is the total number of 64-byte frames received and transmitted on the port. Such a frame has the following characteristics:

- Any data or MAC control frame which was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was exactly 64 bytes long

If the frame was being transmitted and experienced carrier loss that resulted in a frame of this size being transmitted, then the frame will be recorded in this statistic.

CRC errors, code/align errors, and overruns do not affect the recording of frames in this statistic.

2.4.4.5.3 Receive + Transmit 65-127 Octet Frames

The receive and transmit 64-127 octet frames statistic is the total number of frames of size 65 to 127 bytes received and transmitted on the port. Such a frame has the following characteristics:

- Any data or MAC control frame which was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 65 to 127 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

2.4.4.5.4 Receive + Transmit 128-255 Octet Frames

The receive and transmit 128-255 octet frames statistic is the total number of frames of size 128 to 255 bytes received and transmitted on the port. Such a frame has the following characteristics:

- Any data or MAC control frame which was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 128 to 255 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

Note—For receive reference only, see RFC1757 Ref. 1.13 etherStatsPkts128to255Octets.

2.4.4.5.5 Receive + Transmit 256-511 Octet Frames

The receive and transmit 256-511 octet frames statistic is the total number of frames of size 256 to 511 bytes received and transmitted on the port. Such a frame has the following characteristics:

- Any data or MAC control frame which was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 256 to 511 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

2.4.4.5.6 Receive + Transmit 512-1023 Octet Frames

The receive and transmit 512-1023 octet frames statistic is the total number of frames of size 512 to 1023 bytes received and transmitted on the port. Such a frame has the following characteristics:

- Any data or MAC control frame which was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 512 to 1023 bytes long

CRC errors, code/align errors and overruns do not affect the recording of frames in this statistic.

2.4.4.5.7 Receive + Transmit 1024 and Above Octet Frames

The receive and transmit 1024 and above octet frames statistic is the total number of frames of size 1024 to RX_MAXLEN bytes for receive or 1024 or more bytes for transmit on the port. Such a frame has the following characteristics:

- Any data or MAC control frame which was destined for any unicast, broadcast, or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 1024 to RX_MAXLEN bytes long on receive, or 1024 or more bytes on transmit

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

2.4.5 Time Synchronization Module Architecture

This section describes the time synchronization module in the 10GbE switch. The time synchronization module is used to facilitate host control of time synchronization operations in accordance with Annex F, E & D of the IEEE 1588 specification and frequency synchronization in accordance to Synchronous Ethernet. Much of the IEEE 1588 standard and Synchronous Ethernet specification is outside of the scope of the time synchronization module, and must be handled by host software. The main purpose of the time synchronization module is to detect time synchronization events and generate timestamps, and then provide the this information to host software for processing. For receive time synchronization packets, the time synchronization module is able to support one-step or two-step operations. For transmit packets, the time synchronization module only supports the two-step operation. The time synchronization submodule detects the following 7 types of time synchronization events:

- Ethernet receive event
- Ethernet transmit event
- Software time stamp push event
- Hardware time stamp push events
- Time stamp rollover event
- Time stamp half-rollover event

Each Ethernet port can cause transmit and receive events. The time stamp push is initiated by software. Each of these 7 events will be covered in more detail later in this section.

2.4.5.1 Time Synchronization Submodule Components

The time synchronization module has several components that together provide the functionality of the time synchronization module. The time synchronization module is made up of the following components:

- Time Stamp Counter
- Ethernet Port 1 and Port 2 Interfaces
- Event FIFO
- Event Pending Interface
- Timestamp Compare Pulse Out
- Timestamp Synchronization pulse Out

Each component is described individually.

2.4.5.1.1 Time Stamp Counter

This section describes the time stamp counter for the time synchronization module. The time stamp counter contains a 32-bit value that is maintained internally within the time synchronization module. The value in the time stamp counter is initialized to 0 when the CPTS_EN bit in the TS_CONTROL register is cleared to 0. When the CPTS_EN bit is set to 1, the time stamp value increments on each rising edge of the CPTS_RCLK. The time stamp value can be written by using the TS_LOAD_EN and TS_LOAD_VAL registers; however, this functionality is provided primarily for test purposes. Host software must maintain the required number of upper bits of the time stamp value, and must be incremented when the rollover event is detected.

2.4.5.1.2 Ethernet Port 1 and Port 2 Interfaces

This section describes the Ethernet port 1 and Ethernet port 2 interfaces to the time synchronization module. The time synchronization module contains two identical port interfaces. One of the interfaces is connected the port 1 of the 10GbE switch and one is connected to port 2 of the 10GbE switch. Each of the time synchronization Ethernet port interfaces contains separate receive and transmit interfaces. The receive interface is used to generate time sync events for valid time synchronization packets that are received on that port. Similarly, the transmit interface is used to is used to generate time sync events for time synchronization packets that are transmitted on that port. Details concerning receive synchronization events can be found in Section 2.4.5.2.6. Details concerning transmit synchronization events can be found in Section 2.4.5.2.7.

2.4.5.1.3 Event FIFO

This section describes the event FIFO in the time synchronization submodule. The event FIFO contains time synchronization events that are waiting to be processed by host software. Events can be processed using interrupts by enabling the event pending interface, or by polling the INTSTAT_RAW register. The event FIFO can hold up to 16 events, and events must be processed in a timely manner to prevent overruns. The time synchronization submodule does not contain any logic to indicate when an overrun has occurred.

2.4.5.1.4 Event Pending Interface

This section describes the event pending interface. The event pending interface is used to signal to the host processor when a time synchronization event is detected in the event FIFO. This interface is only valid when using interrupts to process events. The event pending interface is active when the TS_PEND_EN bit in the TS_INT_ENABLE

register is set to 1. When this bit is set, interrupts will be used to notify of the host of any time synchronization events that are detected by the time synchronization module. When the TS_PEND_EN bit in the TS_INT_ENABLE register is set to 0, the event pending interface is inactive.

2.4.5.1.5 Timestamp Compare Pulse Out

The TS_COMP output is asserted for ts_comp_length[15:0] RCLK periods when the time_stamp value compares with the ts_comp_val[31:0] and the length value is non-zero. The TS_COMP rising edge occurs three RCLK periods after the values compare. A timestamp compare event is pushed into the event FIFO when TS_COMP is asserted. The polarity of the TS_COMP output is determined by the ts_polarity bit. The output is asserted low when the polarity bit is low.

2.4.5.1.6 Timestamp Synchronization pulse Out

The TS_SYNC output is a selected bit of the time_stamp[31:0] counter value. The TS_SYNC output is disabled when ts_sync_sel[3:0] is zero. If the selected counter bit is high when the ts_sync_sel[3:0] value is written then a rising edge will not occur on the TS_SYNC output until the next rising edge of the selected counter bit (a rising edge on the selected bit is required in order to cause a rising edge on TS_SYNC). The ts_sync_sel[3:0] value should be written to zero before changing to a different nonzero value. No events are generated due to the TS_SYNC operation. The TS_SYNC output is two RCLK periods after the actual count value. When ts_sync_sel[3:0] is non-zero the TS_SYNC output is enabled and is selected from the time_stamp[31:0] counter according to Table 2-5.

Table 2-5 Timestamp Synchronization Selection

ts _sync_sel	Selected time_stamp[31:0] bit
0000	TS_SYNC is disabled
0001	TS_SYNC is bit 17
0010	TS_SYNC is bit 18
...	...
1110	TS_SYNCis bit 30
1110	TS_SYNC is bit 31
End of Table 2-5	

2.4.5.2 Time Synchronization Events

This section describes time synchronization events. Time synchronization events are 96-bit values that are pushed onto the event FIFO, which can then be read in the three 32-bit EVENT_LOW, EVENT_MID and EVENT_HIGH registers. Table 2-6 shows the data that is stored in a time synchronization event. See the EVENT_LOW, EVENT_MID and EVENT_HIGH registers for bit field information.

Table 2-6 Time Synchronization Event Fields

Name	Description
Time Stamp	The time stamp field in a contains the 32-bit time stamp value for a given packet. The timestamp field is only valid for time stamp push events, Ethernet receive events, and Ethernet transmit events. The time stamp value is not valid for counter roll over event types.
Port Number	The port number is used to indicate the port number of an ethernet event.
Event Type	The event field contains the type of event that is represented. The available event types are: • Software time stamp push event • Hardware time stamp Push Event • Time stamp rollover event • Time stamp half rollover event • Ethernet receive event • Ethernet transmit event • Time stamp compare event
Message Type	The message type field contains the message type value that was found in an Ethernet receive or transmit event. This field is only valid for Ethernet receive and transmit events.
Sequence ID	The sequence ID field contains the 16-bit sequence ID that was contained in an Ethernet receive or transmit time sync packet. This field is only valid for Ethernet receive and transmit events.
Domain	The 8-bit domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.
End of Table 2-6	

The subsequent sections describes the different event types supported by the time synchronization submodule.

2.4.5.2.1 Software Time Stamp Push Event

This section describes the time stamp push event. The time stamp push event is an event generated by host software, and is used to obtain the current time stamp value. The time stamp push event is initiated by writing the TS_PUSH register. After writing the TS_PUSH register, the time stamp event is generated and pushed into the time synchronization event FIFO with the time stamp push event code. The time stamp value that is returned will be the value of the time stamp at the time that the TS_PUSH register was written.

2.4.5.2.2 Hardware Time Stamp Push Event

There are up to eight hardware time stamp inputs (HW1/8_TS_PUSH) that can cause hardware time stamp push events to be loaded into the event FIFO. The port_number field in the event indicates the hardware push input that caused the event (encoded). The hardware time stamp inputs are asynchronous and are low frequency signals. The CPTS logic synchronizes and performs a rising edge detect on the incoming asynchronous input. Each hardware timestamp input must be asserted for at least 10 periods of the fastest clock that will be selected for the timestamp block (RCLK). Hardware timestamps are intended to be extremely low frequency signals such that the event FIFO does not overrun. Software must keep up with the event FIFO and ensure that no overrun occurs or events will be lost. The signals connected to these hardware push events are device specific. They can be 1pps GPS signal, RX recovered ethernet clock for Synchronous Ethernet support, or any other clock input. Please see your specific device data manual for full details.

2.4.5.2.3 Time Stamp Counter Rollover Event

This section describes the time stamp counter rollover event. The time stamp rollover event is used to indicate that the 32-bit time stamp maintained by the time synchronization module has rolled over from 0xFFFFFFFF to 0x00000000. When the rollover occurs, the time stamp rollover event will be pushed into the event FIFO for processing by host software with the time stamp counter rollover event code. The host should use this event to increment any upper time stamp bits that are being maintained in software.

2.4.5.2.4 Time Stamp Counter Half Rollover Event

This section describes the time stamp counter half-rollover event. The half-rollover event indicates to software that the time stamp value maintained internally by the time synchronization module has incremented from 0x7FFF_FFFF to 0x8000_0000. The half-rollover event is included to enable software to correct a misaligned event condition.

The half-rollover event is included to enable software to determine the correct time for each event that contains a valid timestamp value - such as an Ethernet event. If an Ethernet event occurs around a counter rollover (full rollover), then the rollover event could possibly be loaded into the event FIFO before the Ethernet event is loaded into the event FIFO even though the Ethernet event time was actually taken before the rollover. This misaligned event condition arises because an Ethernet event time stamp occurs at the beginning of a packet and time passes before the packet is determined to be a valid synchronization packet. The misaligned event condition occurs if the rollover occurs in the middle, after the packet time stamp has been taken, but before the packet has been determined to be a valid time sync packet.

Host Software must detect and correct for the misaligned event condition. For every event time stamp after a rollover and before a half-rollover, software must examine the most significant bit of the time stamp. If the most significant bit of the time stamp is 1, then the time stamp value was before the rollover occurred. If the most significant bit of the time stamp is 0, then the event time stamp was taken after the rollover and no correction is required. The misaligned event can occur only on the rollover boundary and not on the half-rollover boundary. Software does not correct for the misaligned time stamp between a half-rollover and a rollover event, only between a rollover event and a half-rollover event.

When a full rollover occurs, software increments the software time stamp upper value. The misaligned case indicates to software that the misaligned event time stamp has a valid upper value that is pre-increment, so one must be subtracted from the upper value to allow software to calculate the correct time for the misaligned event.

2.4.5.2.5 Time stamp compare event

The CPTS can generate an event for a time stamp comparison. The TS_COMP output is also asserted when the event is generated. The event is generated when the time_stamp value compares with the ts_comp_val[31:0] register and the ts_comp_length[15:0] value is non-zero. The ts_comp_length[15:0] value should be written by software after the ts_comp_val[31:0] register is written and should be zero when the comparison value is written.

2.4.5.2.6 Ethernet Receive Event

This section describes Ethernet port receive events. Ethernet ports 1 and 2 can generate Ethernet receive events. Each port has an identical interface and can independently generate time synchronization events for valid received time sync packets. For every packet received on the Ethernet ports, a timestamp will be captured by the receive module inside the CPTS for the corresponding port. The time stamp will be captured by the receive module regardless of whether or not the packet is a time synchronization packet to make sure that the time stamp is captured as soon as possible. The packet is sampled on both the rising and falling edges of the CPTS_RCLK, and the time stamp will be captured once the start of frame delimiter for the receive packet is detected.

After the time stamp has been captured, the receive interface will begin parsing the packet to determine if it is a valid Ethernet time synchronization packet. The receive interface for the port will use to the following criteria to determine if the packet is a valid time synchronization Ethernet receive event. The 10GbE switch 1588v2 decoder determines if the packet is a valid ethernet receive time synchronization event.

If all of the criteria described in 10GbE Switch 1588 Decoder Rules are met, and the packet is determined to be a valid time synchronization packet, then the RX interface will push an Ethernet receive event into the event FIFO. For more information about event formatting please see Table 2-6. For more information on how to detect and process transmit events, please see Section 2.4.5.4.

2.4.5.2.7 Ethernet Transmit Event

This section describes Ethernet port transmit events. Ethernet ports 1 and 2 can generate Ethernet transmit events. Each port has an identical interface and can independently generate time synchronization events for valid transmit time sync packets. For every packet transmitted on the Ethernet ports, the port transmit interface will begin parsing the packet to determine if it is a valid Ethernet time synchronization packet. The CPTS transmit interface for the port will use to the following criteria to determine if the packet is a valid time synchronization Ethernet transmit event. To be a valid Ethernet transmit time synchronization event, all of the 4 conditions listed below must be true.The 10GbE switch 1588v2 decoder determines if the packet is a valid ethernet receive time synchronization event.

If all of the criteria in 10GbE Switch 1588 Decoder Rules are met, and the packet is determined to be a valid time synchronization packet, then the time stamp for the transmit event will not be generated until the start of frame delimiter of the packet is actually transmitted. The start of frame delimiter will be sampled on every rising and falling edge of the CPTS_RCLK. Once the packet is transmitted, then the TX interface will push an Ethernet transmit event into the event FIFO. For more information about event formatting please see Table 2-6. For more information on how to detect and process transmit events, please see Section 2.4.5.4.

2.4.5.2.8 10GbE Switch 1588 Decoder Rules

Annex F

1. Transmit time sync is enabled (pX_ts_tx_annex_f_en is set in the switch Px_TS_Ctl register).
2. One of the sequences below is true.
   a. The first packet LTYPE matches pX_ts_ltype1. LTYPE 1 should be used when only one time sync LTYPE is to be enabled.

b. The first packet LTYPE matches pX_ts_ltype2 and pX_ts_ltype2_en is set
c. The first packet LTYPE matches pX_ts_vlan_ltype1 and pX_ts_tx_vlan_ltype1_en is set and the second packet LTYPE matches pX_ts_ltype1
d. The first packet LTYPE matches pX_ts_vlan_ltype1 and pX_ts_tx_vlan_ltype1_en is set and the second packet LTYPE matches pX_ts_ltype2 and pX_ts_ltype2_en is set
e. The first packet LTYPE matches pX_ts_vlan_ltype2 and pX_ts_tx_vlan_ltype2_en is set and the second packet LTYPE matches pX_ts_ltype1
f. The first packet LTYPE matches pX_ts_vlan_ltype2 and pX_ts_tx_vlan_ltype2_en is set and the second packet LTYPE matches pX_ts_ltype2 and pX_ts_ltype2_en is set
g. The first packet LTYPE matches pX_ts_vlan_ltype1 and pX_ts_tx_vlan_ltype1_en is set and the second packet LTYPE matches pX_ts_vlan_ltype2 and pX_ts_tx_vlan_ltype2_en is set and the third packet LTYPE matches pX_ts_ltype1
h. The first packet LTYPE matches pX_ts_vlan_ltype1 and pX_ts_tx_vlan_ltype1_en is set and the second packet LTYPE matches pX_ts_vlan_ltype2 and pX_ts_tx_vlan_ltype2_en is set and the third packet LTYPE matches pX_ts_ltype2 and pX_ts_ltype2_en is set

3. The packet message type is enabled in the pX_ts_msg_type_en field in the Px_TS_Ctl register.
4. The packet was sent by the host (port 0).

Annex E

5. Transmit annex E time sync is enabled (pX_ts_tx_annex_e_en is set in the Px_TS_Ctl register).
6. One of the sequences below is true.
   a. The first packet LTYPE matches 0x86dd.
   b. The first packet LTYPE matches pX_ts_vlan_ltype1 and pX_ts_tx_vlan_ltype1_en is set and the second packet LTYPE matches 0x86dd.
   c. The first packet LTYPE matches pX_ts_vlan_ltype2 and pX_ts_tx_vlan_ltype2_en is set and the second packet LTYPE matches 0x86dd.
   d. The first packet LTYPE matches pX_ts_vlan_ltype1 and pX_ts_tx_vlan_ltype1_en is set and the second packet LTYPE matches pX_ts_vlan_ltype2 and pX_ts_tx_vlan_ltype2_en is set and the third packet LTYPE matches 0x86dd.
7. Byte 14 (the byte after the LTYPE) contains 0x6X (IP_VERSION in most significant nibble).
8. Byte 20 contains 0x11 (UDP Fixed Next Header).
9. Byte 21 contains 0x01 (Hop Limit = 1).
10. The pX_ts_uni_en bit in the Px_TS_Ctl_Ltype2 register is zero and Bytes 38 through 53 contain:
    a. FF0M:0:0:0:0:0:0:0181 and the pX_ts_129 bit in the switch Px_TS_Ctl_Ltype2 register is set, or

b. FF0M:0:0:0:0:0:0:0182 and the pX_ts_130 bit in the switch Px_TS_Ctl_Ltype2 register is set, or

c. FF0M:0:0:0:0:0:0:0183 and the pX_ts_131 bit in the switch Px_TS_Ctl_Ltype2 register is set, or

d. FF0M:0:0:0:0:0:0:0184 and the pX_ts_132 bit in the switch Px_TS_Ctl_Ltype2 register is set, or

e. FF0M:0:0:0:0:0:0:006B and the pX_ts_107 bit in the switch Px_TS_Ctl_Ltype2 register is set (all values above are 16-bit hex numbers with M is enabled in the pX_ts_mcast_type_en field in the Px_TS_Ctl2 register.

Or:

11. The pX_ts_uni_en bit in the Px_TS_Ctl_Ltype2 register is set and Bytes 38 through 53 contain
12. any value.
13. Bytes 56 and 57 contain (UDP Header in bytes 54 through 61):
    a. Decimal 0x01 and 0x3f respectively and the pX_ts_319 bit in the Px_TS_Ctl_Ltype2 register is set, or
    b. Decimal 0x01 and 0x40 respectively and the pX_ts_320 bit in the Px_TS_Ctl_Ltype2 register is set.
14. The PTP message begins in byte 62.
15. The packet message type is enabled in the pX_ts_msg_type_en field in Px_TS_Ctl.
16. The packet was sent by the host (port 0).

Annex D

17. Transmit time sync is enabled (pX_ts_tx_annex_d_en is set in the switch Px_TS_Ctl register).
18. One of the sequences below is true.
    a. The first packet LTYPE matches 0x0800
    b. The first packet LTYPE matches pX_ts_vlan_ltype1 and pX_ts_tx_vlan_ltype1_en is set and the second packet LTYPE matches 0x0800
    c. The first packet LTYPE matches pX_ts_vlan_ltype2 and pX_ts_tx_vlan_ltype2_en is set and the second packet LTYPE matches 0x0800
    d. The first packet LTYPE matches pX_ts_vlan_ltype1 and pX_ts_tx_vlan_ltype1_en is set and the second packet LTYPE matches pX_ts_vlan_ltype2 and pX_ts_tx_vlan_ltype2_en is set and the third packet LTYPE matches 0x0800
19. Byte 14 (the byte after the LTYPE) contains 0x45 (IP_VERSION).

Note—* note that the byte numbering assumes that there are no VLANs. The byte number is intended to show the relative order of the bytes. If VLAN(s) are present then the byte numbers push down.

20. Byte 20 contains 0bXXX00000 (5 lower bits zero) and Byte 21 contains 0x00 (fragment offset zero)

21. Byte 22 contains 0x00 if the pX_ts_ttl_nonzero bit in the switch Px_TS_Ctl register is zero or byte 22 contains any value if pX_ts_ttl_nonzero is set. Byte 22 is the time to live field.
22. Byte 23 contains 0x11 (Next Header UDP Fixed).
23. The pX_ts_uni_en bit in the Px_TS_Ctl_Ltype2 register is zero and bytes 30 through 33 contain:
    a. Decimal 224.0.1.129 and the pX_ts_129 bit in the switch Px_TS_Ctl_Ltype2 register is set, or
    b. Decimal 224.0.1.130 and the pX_ts_130 bit in the switch Px_TS_Ctl_Ltype2 register is set, or
    c. Decimal 224.0.1.131 and the pX_ts_131 bit in the switch Px_TS_Ctl_Ltype2 register is set, or
    d. Decimal 224.0.1.132 and the pX_ts_132 bit in the switch Px_TS_Ctl_Ltype2 register is set, or
    e. Decimal 224.0.0.107 and the pX_ts_107 bit in the switch Px_TS_Ctl_Ltype2 register is set

    Or:
24. The pX_ts_uni_en bit in the Px_TS_Ctl_Ltype2 register is set and Bytes 30 through 33 contain any values.
25. Bytes 36 and 37 contain:
    a. Decimal 0x01 and 0x3f respectively and the pX_ts_319 bit in the Px_TS_CTL_Ltype2 register is set, or
    b. Decimal 0x01 and 0x40 respectively and the pX_ts_320 bit in the Px_TS_CTL_Ltype2 register is set.
26. The PTP message begins in byte 42 (this is offset 0).
27. The packet message type is enabled in pX_ts_msg_type_en field in the Px_TS_Ctl register.
28. The packet was sent by the host (port 0).

2.4.5.3 Time Synchronization Initialization

The time synchronization registers and 10GbE switch should be configured as shown below:

Procedure 2-1 Time Synchronization Module Configuration

Step	Action
1	Clear the CPTS_EN bit to 0 in the TS_CONTROL register. The CPTS module is in reset while this bit is 0.
2	Write the CPTS_RFTCLK_SEL value in the CPTS_RFTCLK_SEL register with the desired reference clock multiplexor value. This value is allowed to be written only when the CPTS_EN bit is cleared to 0.
3	Write a 1 to the CPTS_EN bit in the TS_CONTROL register.
4	Program the P1/2_TS_Ctl, P1/2_TS_LTYPE1/2, P1/2_TS_VLAN_LTYPE1/2, P1/2_TS_VLAN_LTYPE_1/2_en and P1/2_TS_MSG_EN registers according to the decoder rules described in 10GbE Switch 1588 Decoder Rules.

End of Procedure 2-1

2.4.5.4 Detecting and Processing Time Synchronization Events

This section describes detecting and processing time synchronization events. Section 2.4.5.4.1 discusses how to detect time synchronization events through the use of interrupts and through the use of register polling. Section 2.4.5.4.2 discusses how to use the register interface to pop time synchronization events from the event FIFO.

Note—These sections will only cover how to detect an event, and pop the event from the event FIFO for processing. It is up to the application software how to process the time synchronization event.

2.4.5.4.1 Detecting Time Synchronization Events

This section describes detecting time synchronization events. The time synchronization module allows time synchronization events to be detected through the use of interrupts or through the use of polling.

If using interrupts, then the time synchronization event pending interrupt will signal when an event is pending. Please see Section 2.4.5.1.4 for more information about how to configure the time synchronization event pending interrupt.

If polling is the preferred method for detecting time synchronization events, then events can be detected by directly reading the INTSTAT_RAW register. When the TS_PEND_RAW bit in the INTSTAT_RAW register is a 1, then it means that there are 1 or more events pending in the event FIFO.

2.4.5.4.2 Popping Time Synchronization Events from the Event FIFO

This section describes how to pop time synchronization events from the event FIFO. Once a time synchronization event has been detected, Procedure 2-2 can be used to pop time synchronization events from the event FIFO. If there is more than one event in the event FIFO, multiple events can be processed back-to-back before returning from the event processing routine.

Procedure 2-2 Popping Time Synchronization Events from the Event FIFO

Step	Action
1	Read the EVENT_LOW, EVENT_MID and EVENT_HIGH register values
2	Write a 1 to the EVENT_POP bit of the EVENT_POP register
3	If not processing multiple events, then go to step 5. Otherwise, wait for at least 4 CPTS_RCLK periods, plus 4 CPU/3 clock periods
4	Read the TS_PEND_RAW bit in the INTSTAT_RAW register to determine if another valid event is in the event FIFO. If the TS_PEND_RAW bit is nonzero, then go to step 1. Otherwise, go to the next step.
5	Return from the event processing routine.

End of Procedure 2-2

2.4.6 Address Lookup Engine (ALE) Module Architecture

The address lookup engine (ALE) processes all received packets to determine which port(s) if any that the packet should the forwarded to. The ALE uses the incoming packet received port number, destination address, source address, length/type, and VLAN information to determine how the packet should be forwarded. The ALE

outputs the port mask to the switch fabric that indicates the port(s) the packet should be forwarded to. The ALE is enabled when the ALE_ENABLE bit in the ALE_CONTROL register is set. All packets are dropped when the ALE_ENABLE bit is cleared to zero.

In normal operation, the MAC modules are configured to issue an abort, instead of an end of packet, at the end of a packet that contains an error (runt, frag, oversize, jabber, CRC, alignment, code etc.) or at the end of a mac control packet. However, when the CEF, CSF, or CMF MAC configuration bit(s) are set, error frames, short frames or MAC control frames have a normal end of packet instead of an abort at the end of the packet. When the ALE receives a packet that contains errors, or a MAC control frame, and does not receive an abort, the packet will be forwarded only to the host port (port 0). No ALE learning occurs on packets with errors or MAC control frames. Learning is based on source address and lookup is based on destination address. Directed packets from the HOST are not learned, updated, or touched.

The ALE may be configured to operate in bypass mode by setting the ale_bypass bit in the ALE_Control register. When in bypass mode, all CPXMAC_SL received packets are forwarded only to the host port (port 0). In bypass mode, the ALE processes host port transmit packets the same as in normal mode. The host port is also capable of sending packets directly to either or both of the CPXMAC_SL ports, bypassing the ALE.

The ALE may be configured to operate in OUI deny mode by setting the enable_oui_deny bit in the ALE_Control register. When in OUI deny mode, any packet with a non-matching OUI source address will be dropped to the host unless the packet destination address matches with a supervisory table entry. (Non-matching OUI source address broadcast/multicast packets will be dropped to the host unless the packet destination address is entered into the table with the super bit set.

Non-matching OUI source address unicast packets will be dropped to the host unless the unicast destination address is in the table with block and secure both set). When enable_oui_deny is cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory address table entry. (Broadcast packets matching the OUI source address will be dropped to the host unless the broadcast destination address is entered into the table with the super bit set. Unicast packets matching the OUI source address will be dropped to the host unless the unicast destination address is in the table with block and secure both set).

Multicast supervisory packets are designated by the super bit in the table entry. Unicast supervisory packets are indicated when block and secure are both set. Supervisory packets are not dropped due to rate limiting, OUI, or VLAN processing.

The ALE learn rate in packets per second is calculated as shown below:

PPS = VBUSP_GCLK / 16

At 500Mhz the ALE learn rate is 31.25 million packets per second total for all ports.

2.4.6.1 ALE Table

The ALE table contains 2048 entries. Each table entry represents a free entry, an address, a VLAN, an address/VLAN pair, or an OUI address. Software should ensure that there are not double address entries in the table. The double entry used would be indeterminate.

Source Address learning occurs for packets with a unicast, multicast or broadcast destination address, and a unicast or multicast (including broadcast) source address. Multicast source addresses have the group bit (bit 40) cleared before ALE processing begins, which changes the multicast source address to a unicast source address. A multicast address of all ones is the broadcast address, which may be added to the table. A learned unicast source address is added to the table with the following control bits:

Table 2-7 ALE Table Learned Address Control Bits

Unicast Type	11
Block	0
Secure	0

If a received packet has a source address that is equal to the destination address then the following occurs:

- The address is learned if the address is not found in the table
- The address is updated if the address is found
- The packet is dropped

2.4.6.2 Reading Entries from the ALE Table

This section will provide the procedure for reading entries to the ALE table. To read an entry from the ALE table, the user must use the following steps:

1. Program the ENTRY_POINTER field in WRITE_RDZ fields ALE_TBL_CTL register
   - The ENTRY_POINTER value is the address entry number that will be accessed in the ALE table. Valid entry numbers are 0-1023.
   - Setting the WRITE_RDZ field to 0 will cause the entry values to be read from the table
2. Once the write to ALE_TABLE_CTL register has completed, the entry in the ALE table at the ENTRY_POINTER location will be programmed in to the ALE_TBLW[0:2] register

2.4.6.3 Writing Entries to the ALE Table

This section will provide the procedure for writing entries to the ALE table. To add an entry to the ALE table, the user must use the following steps:

1. Program the ALE_TBLW[0:2] registers with the desired values for the desired entry type

2. Program the ENTRY_POINTER and WRITE_RDZ fields ALE_TBL_CTL register to add the entry to the table
   - The ENTRY_POINTER value is the address entry number that will be written to in the ALE table. Valid entry numbers are 0-1023.
   - Setting the WRITE_RDZ field to 1 will cause the entry to be added to the table

When adding an entry to the ALE Table, the entry must be one of the types defined in the ALE Table Entry Types section. Before adding an entry to the ENTRY_POINTER location in the ALE table, the user may want to read the entry to see if the entry is free (ENTRY_TYPE = 00). For the procedure to read an entry from the ALE table, please see the "Reading Entries from the ALE Table" section.

2.4.6.4 ALE Table Entry Types

This section will describe the allowable configurations for entries to the ALE table. All entries in the ALE table must be one of the following types. ALE table entries can be read using the procedure described in the "Reading Entries from the ALE Table" section. Entries can be added to ALE table using the procedure described in the "Writing Entries to the ALE Table" section.

2.4.6.4.1 Free Table Entry

The format for a free table entry is shown in Figure 2-1, and the required field configuration is described in Table 2-8. A free table entry is an entry in the table this is currently unused.

Figure 2-1 Free Table Entry

71						62	61	60	59						0
Reserved							ENTRY_TYPE		Reserved						

For a free table entry, the fields must be set as shown in Table 2-8. General descriptions of the ALE table entry fields are provided in Table 2-15.

Table 2-8 Free Table Entry Field Configuration

Field Name	Configuration
ENTRY_TYPE[1:0]	00

2.4.6.4.2 Multicast Address Table Entry

The format for a multicast address table entry is shown in Figure 2-2, and the required field configuration is described in Table 2-9.

Figure 2-2 Multicast Address Table Entry

71	69	68	66	65	64	63	62	61	60	59		48	47		0
Reserved		PORT_MASK		SUPER	Reserved	MCAST_FWD_ STATE		ENTRY_TYPE		Reserved			MULTICAST_ADDRESS		

For a multicast address table entry, the fields must be set as shown in Table 2-9. General descriptions of the ALE table entry fields are provided in Table 2-15.

Table 2-9 Multicast Address Table Entry Field Configuration

Field Name	Configuration
PORT_MASK[2:0]	User configurable
SUPER	User configurable
MCAST_FWD_STATE[1:0]	User configurable
ENTRY_TYPE[1:0]	01
MULTICAST_ADDRESS[47:0]	User configurable

2.4.6.4.3 VLAN/Multicast Address Table Entry

The format for a VLAN/multicast address table entry is shown in Figure 2-3, and the required field configuration is described in Table 2-10.

Figure 2-3 VLAN/Multicast Table Entry

71	69	68	66	65	64	63	62	61	60	59		48	47		0
Reserved		PORT_MASK		SUPER	Reserved	MCAST_FWD_ STATE		ENTRY_TYPE		VLAN_ID			MULTICAST_ADDRESS		

For a VLAN/multicast address table entry, the fields must be set as shown in Table 2-10. General descriptions of the ALE table entry fields are provided in Table 2-15.

Table 2-10 VLAN/Multicast Address Table Entry Field Configuration

Field Name	Configuration
PORT_MASK[2:0]	User configurable
SUPER	User configurable
MCAST_FWD_STATE[1:0]	User configurable
ENTRY_TYPE[1:0]	11
VLAN_ID[11:0]	User configurable
MULTICAST_ADDRESS[47:0]	User configurable

2.4.6.4.4 Unicast Address Table Entry

The format for a unicast address table entry is shown in Figure 2-4, and the required field configuration is described in Table 2-11.

Figure 2-4 Unicast Table Entry

71	68	67	66	65	64	63	62	61	60	59		48	47		0
Reserved		PORT_NUMBER		BLOCK	SECURE	UNICAST_TYPE		ENTRY_TYPE		Reserved			UNICAST_ADDRESS		

For a unicast address table entry, the fields must be set as shown in Table 2-11. General descriptions of the ALE table entry fields are provided in Table 2-15.

Table 2-11 Unicast Address Table Entry Field Configuration

Field Name	Configuration
PORT_NUMBER[1:0]	User configurable
BLOCK	User configurable
SECURE	User configurable
UNICAST_TYPE[1:0]	00 or X1
ENTRY_TYPE[1:0]	01
UNICAST_ADDRESS[47:0]	User configurable

2.4.6.4.5 OUI Unicast Address Table Entry

The format for an OUI unicast address table entry is shown in Figure 2-5, and the required field configuration is described in Table 2-12.

Figure 2-5 OUI Unicast Table Entry

71					64	63	62	61	60	59	48	47	24	23	0
Reserved						UNICAST_TYPE		ENTRY_TYPE		Reserved		UNICAST_OUI		Reserved	

For an OUI unicast address table entry, the fields must be set as shown in Table 2-12. General descriptions of the ALE table entry fields are provided in Table 2-15.

Table 2-12 OUI Unicast Address Table Entry Field Configuration

Field Name	Configuration
UNICAST_TYPE[1:0]	10
ENTRY_TYPE[1:0]	01
UNICAST_OUI[23:0]	User configurable

2.4.6.4.6 VLAN/Unicast Table Entry

The format for a VLAN/unicast address table entry is shown in Figure 2-6, and the required field configuration is described in Table 2-13.

Figure 2-6 VLAN/Unicast Table Entry

71	68	67	66	65	64	63	62	61	60	59		48	47		0
Reserved		PORT_NUMBER		BLOCK	SECURE	UNICAST_TYPE		ENTRY_TYPE		VLAN_ID			UNICAST_ADDRESS		

For a VLAN/unicast address table entry, the fields must be set as shown in Table 2-13. General descriptions of the ALE table entry fields are provided in Table 2-15.

Table 2-13 VLAN/Unicast Table Entry Field Configuration (Part 1 of 2)

Field Name	Configuration
PORT_NUMBER[1:0]	User configurable
BLOCK	User configurable
SECURE	User configurable
UNICAST_TYPE[1:0]	00 or X1
ENTRY_TYPE[1:0]	11

Table 2-13 VLAN/Unicast Table Entry Field Configuration (Part 2 of 2)

Field Name	Configuration
VLAN_ID[11:0]	User configurable
UNICAST_ADDRESS[47:0]	User configurable
End of Table 2-13	

2.4.6.4.7 VLAN Table Entry

The format for a VLAN table entry is shown in Figure 2-7, and the required field configuration is described in Table 2-14.

Figure 2-7 VLAN Table Entry

71	62	61	60	59	48	47	27	26	24	23	19	18	16	15	11	10	8	7	3	2	0
Reserved		ENTRY_TYPE		VLAN_ID		Reserved		FORCE_ UNTAGGED_ EGRESS		Reserved		REG_ MCAST_ FLOOD_ MASK		Reserved		UNREG_ MCAST_ FLOOD_ MASK		Reserved		VLAN_ MEMBER_ LIST	

For a VLAN table entry, the fields must be set as shown in Table 2-14. General descriptions of the ALE table entry fields are provided in Table 2-15.

Table 2-14 VLAN Table Entry Field Configuration

Field Name	Configuration
ENTRY_TYPE[1:0]	10
VLAN_ID[11:0]	User configurable
FORCE_UNTAGGED_EGRESS[2:0]	User configurable
REG_MCAST_FLOOD_MASK[2:0]	User configurable
UNREG_MCAST_FLOOD_MASK[2:0]	User configurable
VLAN_MEMBER_LIST[2:0]	User configurable
End of Table 2-14	

2.4.6.4.8 ALE Table Entry Field Descriptions

General ALE Table entry field descriptions are shown in Table 2-15.

Table 2-15 ALE Table Entry Field Descriptions (Part 1 of 2)

ALE Table Entry Field Name	Description
ENTRY_TYPE[1:0]	Table Entry Type. 00 = Free Entry 01 = Address Entry: unicast or multicast determined by bit 40 of the MAC destination address 10 = VLAN entry 11 = VLAN Address Entry: unicast or multicast determined by bit 40 of the MAC destination address
SUPER	Supervisory Packet. Indicates that the packet with a matching multicast destination address is a supervisory packet. 0 = Non-supervisory packet 1 = Supervisory packet
PORT_MASK[2:0]	Port Mask. This field is the port bit mask that is returned with a found multicast destination address. There may be multiple bits set indicating that the multicast packet may be forwarded to multiple ports (but not the receiving port).
PORT_NUMBER[1:0]	Port Number. This field indicates the which port number (not port mask) that the packet with a unicast destination address may be forwarded. Packets with unicast destination addresses are forwarded only to a single port (but not the receiving port).

Table 2-15 ALE Table Entry Field Descriptions (Part 2 of 2)

ALE Table Entry Field Name	Description
BLOCK	Block. The block bit indicates that a packet with a matching source or destination address should be dropped (block the address). 0 = Address is not blocked. 1 = Drop a packet with a matching source or destination address (SECURE must be zero) If BLOCK and SECURE are both set, then they no longer mean block and secure. When both are set, the BLOCK and SECURE bits indicate that the packet is a unicast supervisory (SUPER) packet and they determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the forwarding state.
SECURE	Secure. This bit indicates that a packet with a matching source address should be dropped if the received port number is not equal to the table entry PORT_NUMBER. 0 = Received port number is a don't care 1 = Drop the packet if the received port is not the secure port for the source address and do not update the address (BLOCK must be zero)
UNICAST_TYPE[1:0]	Unicast Type. This field indicates the type of unicast address the table entry contains. 00 = Unicast address that is not ageable 01 = Ageable unicast address that has not been touched 10 = OUI address - lower 24-bits are don't cares (not ageable) 11 = Ageable unicast address that has been touched
MCAST_FWD_STATE[1:0]	Multicast Forward State. Indicates the port state(s) required for the received port on a destination address lookup in order for the multicast packet to be forwarded to the transmit port(s). A transmit port must be in the Forwarding state in order to forward the packet. If the transmit PORT_MASK has multiple set bits then each forward decision is independent of the other transmit port(s) forward decision. 00 = Forwarding 01 = Blocking/Forwarding/Learning 10 = Forwarding/Learning 11 = Forwarding The forward state test returns a true value if both the receive and transmit ports are in the required state.
VLAN_ID	VLAN_ID. This is the 12-bit VLAN ID.
ADDRESS	Packet Address. This is the 48-bit packet MAC address. For an OUI address, only the upper 24-bits of the address are used in the source or destination address lookup. Otherwise, all 48-bits are used in the lookup.
VLAN_MEMBER_LIST	VLAN Member List. This six bit field indicates which port(s) are a member of the associated VLAN.
UNREG_MCAST_FLOOD_MASK	Unregistered Multicast Flood Mask. Mask used for multicast when the multicast address is not found
REG_MCAST_FLOOD_MASK	Registered Multicast Flood Mask. Mask used for multicast when the multicast address is found.
FORCE_UNTAGGED_EGRESS	Force Untagged Packet Egress. Causes the packet VLAN tag to be removed on egress.
End of Table 2-15	

2.4.6.5 ALE Packet Forwarding Process

This section describes the packet forwarding process used by the ALE. For each packet sent to the ALE, it will decide whether or not the packet should be dropped or forwarded. If the packet is forwarded, then the ALE needs to determine which switch port or ports a packet the should be forwarded to. Each port has an associated packet forwarding state that can be set to one of four values:

- Disabled
- Blocked
- Learning
- Forwarding

By default, all ports are Disabled. To enable a port, the host must set the packet forwarding state in the respective ALE_PORTCTL register. The receive packet processes are described in the following sections. The state of each port will affect whether or not a packet is forwarded.

There are four processes that an packet may go through to determine packet forwarding. The processes are:

- Ingress Filtering
- VLAN Aware Lookup
- VLAN Unaware Lookup
- Egress

The packet forwarding process begins with the ingress filtering process. In the packet ingress process, there is one forward state test for unicast destination addresses, and another forward state test for multicast addresses. The forward state test that is used is determined by bit 40 of the destination address in the packet, which will designate the packet as multicast or unicast.The multicast forward state test indicates the port states required for the receiving port in order for the multicast packet to be forwarded to the transmit port(s). A transmit port must be in the Forwarding state for the packet to be forwarded for transmission. The MCAST_FWD_STATE indicates the required port state for the receiving port as indicated in the preceding table.

The unicast forward state test indicates the port state required for the receiving port in order to forward the unicast packet. The transmit port must be in the Forwarding state in order to forward the packet. The block and secure bits determine the unicast forward state test criteria. If both bits are set then the packet is forwarded if the receive port is in the Forwarding/Blocking/Learning state. If both bits are not set then the packet is forwarded if the receive port is in the Forwarding state. The transmit port must be in the Forwarding state regardless.

In general, packets received with errors are dropped by the address lookup engine in the ingress filtering process without learning, updating, or touching the addresses in the ALE table. The error condition and the abort are indicated by the MAC module to the ALE. Packets with errors may be passed to the host (not aborted) by a MAC port if the RX_CMF_EN, RX_CEF_EN, or RX_CSF_EN bit(s) have been set in the MAC_CONTROL register in the MAC module. Error packets that are passed to the host by the MAC module are considered to be bypass packets by the ALE and are sent only to the host. Error packets do not learn, update, or touch addresses in the ALE table regardless of whether they are aborted or sent to the host. Packets with errors received by the host are dropped.

- RX_CEF_EN – This bit in the MAC_CONTROL register enables frames that are fragments, long, jabber, CRC, code, and alignment errors to be forwarded
- RX_CSF_EN – This bit in the MAC_CONTROL register enables short frames to be forwarded
- RX_CMF_EN – This bit in the MAC_CONTROL register enables MAC control frames to be forwarded.

When one of the above bits, any error packet that are forwarded to the host will have the error that occurred placed in the Error Flags section of the descriptor. The error values are shown in Table 2-16.

Table 2-16 Gigabit Ethernet Switch Subsystem Descriptor Error Flags

Error
The values listed in the error flags field of the descriptor are defined as follows: x000 – no error x001 – packet CRC error on ingress x010 – packet code error on ingress x011 – packet alignment error on ingress x1xx – middle of packet overrun on egress 1xxx – Indicates that the descriptor protocol specific flags section has a set long, short, or mac_ctl bit

2.4.6.5.1 ALE Ingress Filtering Process

This section will outline the ALE ingress packet filtering process.

Table 2-17 ALE Ingress Filtering Process (Part 1 of 2)

if ((ale_bypass) and (host port is not the receive port)) then use host portmask and go to Egress process
if (directed packet) then use directed port number and go to Egress process
If (Receive PORT_STATE is Disabled) then discard the packet
if ((error packet) and (host port is not the receive port)) then use host portmask and go to Egress process
if ((macsec_en and not(macsec_controlled)) then use host portmask and go to Egress process
if ((macsec_en and macsec_controlled and not(ingress port secure_port)) then use host portmask and go to Egress process
if (macsec_en and macsec_debug) then use host portmask and go to Egress process
if (((BLOCK) and (unicast source address found)) or ((BLOCK) and (unicast destination address found))) then discard the packet
if ((ENABLE_RATE_LIMIT) and (rate limit exceeded) and (not RATE_LIMIT_TX) then if (((multicast or broadcast destination address found) and (not SUPER)) or (multicast/broadcast destination address not found)) then discard the packet
if ((not forward state test valid) and (destination address found)) then discard the packet for any port not meeting the requirements Unicast destination addresses use the unicast forward state test and multicast destination addresses use the multicast forward state test.
if ((destination address not found) and ((not transmit port forwarding) or (not receive port forwarding))) then discard the packet to any ports not meeting the above requirements
if (source address found) and (SECURE) and (receive port number != PORT_NUMBER)) then discard the packet
if ((not SUPER) and (DROP_UNTAGGED) and ((non-tagged packet) or ((priority tagged) and not(EN_VID0_MODE)) then discard the packet

Table 2-17 ALE Ingress Filtering Process (Part 2 of 2)

If (VLAN_Unaware)
FORCE_UNTAGGED_EGRESS = "000000"
REG_MCAST_FLOOD_MASK = "111111"
UNREG_MCAST_FLOOD_MASK = "111111"
VLAN_MEMBER_LIST = "111111"
else if (VLAN not found)
FORCE_UNTAGGED_EGRESS = UNKNOWN_FORCE_UNTAGGED_EGRESS
REG_MCAST_FLOOD_MASK = UNKNOWN_REG_MCAST_FLOOD_MASK
UNREG_MCAST_FLOOD_MASK = UNKNOWN UNREG_MCAST_FLOOD_MASK
VLAN_MEMBER_LIST = UNKNOWN_VLAN_MEMBER_LIST
else
FORCE_UNTAGGED_EGRESS = FOUND FORCE_UNTAGGED_EGRESS
REG_MCAST_FLOOD_MASK = FOUND REG_MCAST_FLOOD_MASK
UNREG_MCAST_FLOOD_MASK = FOUND UNREG_MCAST_FLOOD_MASK
VLAN_MEMBER_LIST = FOUND VLAN_MEMBER_LIST

IF ((NOT SUPER) AND (VID_INGRESS_CHECK) AND (RECEIVE PORT IS NOT VLAN MEMBER)) THEN DISCARD THE PACKET
if ((ENABLE_AUTH_MODE) and (source address not found) and not (destination address found and (SUPER))) then discard the packet
if (destination address not found) and (destination address equals source address) then discard the packet
if (VLAN_AWARE) go to VLAN aware lookup process else go to VLAN unaware lookup process
End of Table 2-17

2.4.6.5.2 ALE VLAN Aware Lookup Process

This section describes the behavior of the ALE VLAN aware lookup process.

Table 2-18 VLAN Aware Lookup Process (Part 1 of 2)

if ((unicast packet) and (destination address found with or without VLAN) and (not SUPER)) then portmask is the logical "AND" of the PORT_NUMBER and the VLAN_MEMBER_LIST and go to Egress process
if ((unicast packet) and (destination address found with or without VLAN) and (SUPER)) then portmask is the PORT_NUMBER and go to Egress process
if (unicast packet) then use VLAN_MEMBER_LIST less host port and go to Egress process
if ((multicast packet) and (destination address found with or without VLAN) and (not SUPER)) then portmask is the logical "AND" of REG_MCAST_FLOOD_MASK and found destination address/VLAN portmask (PORT_MASK) and VLAN_MEMBER_LIST and go to Egress process
if ((multicast packet) and (destination address found with or without VLAN) and (SUPER)) then portmask is the PORT_MASK and go to Egress process

Table 2-18 VLAN Aware Lookup Process (Part 2 of 2)

if ((multicast packet) and (destination address not found)) then portmask is the logical "AND" of UNREG_MCAST_FLOOD_MASK and VLAN_MEMBER_LIST then go to Egress process
if (broadcast packet) then use VLAN_MEMBER_LIST and go to Egress process
End of Table 2-18

2.4.6.5.3 ALE VLAN Unaware Lookup Process

This section describes the behavior of the ALE VLAN unaware lookup process.

Table 2-19 VLAN Unaware Lookup Process

if ((unicast packet) and (destination address found with or without VLAN) and (not SUPER)) then portmask is the logical "AND" of the PORT_NUMBER and the VLAN_MEMBER_LIST and go to Egress process
if ((unicast packet) and (destination address found with or without VLAN) and (SUPER)) then portmask is the PORT_NUMBER and go to Egress process
if (Unicast packet) # destination address not found then portmask is VLAN_MEMBER_LIST less host port and go to Egress process
if ((multicast packet) and (destination address found with or without VLAN) and (not SUPER)) then portmask is the logical "AND" of REG_MCAST_FLOOD_MASK and found destination address/VLAN portmask (PORT_MASK) and VLAN_MEMBER_LIST and go to Egress process
if ((multicast packet) and (destination address found with or without VLAN) and (SUPER)) then portmask is the PORT_MASK and go to Egress process
if (multicast packet) # destination address not found then portmask is the logical "AND" of UNREG_MCAST_FLOOD_MASK and VLAN_MEMBER_LIST then go to Egress process
if (broadcast packet) then use found VLAN_MEMBER_LIST and go to Egress process
End of Table 2-19

2.4.6.5.4 ALE Egress Process

This section describes behavior of the ALE egress process.

Table 2-20 ALE Egress Process (Part 1 of 2)

Clear receive port from portmask (don't send packet to receive port)
Clear disabled ports from portmask
if (macsec_en and not(directed) and not(macsec_debug) and macsec_controlled and (ingress port secure_port) then Clear non secure_port ports from portmask.
if ((ENABLE_OUI_DENY) and (OUI source address not found) and (not ALE_BYPASS) and (not error packet) and not ((multicast destination address) and (SUPER))) then clear host port from portmask
if ((ENABLE_RATE_LIMIT) and (RATE_LIMIT_TX)) then if (not SUPER) and (rate limit exceeded on any tx port) then clear rate limited tx port from portmask If address not found then SUPER cannot be set.

Table 2-20 ALE Egress Process (Part 2 of 2)

If portmask is zero then discard packet
Send packet to portmask ports
End of Table 2-20

2.4.6.6 ALE Learning Process

The learning process is applied to each receive packet that is not aborted. The learning process is a concurrent process with the packet forwarding process.

Table 2-21 ALE Learning Process

If (not (Learning or Forwarding) or (ENABLE_AUTH_MODE) or (packet error) or (NO_LEARN)) then do not learn or update address else continue
if ((Non-tagged packet) and (DROP_UNTAGGED)) then do not learn or update address else continue
if ((VLAN_AWARE) and (VLAN not found) and (UNKNOWN_VLAN_MEMBER_LIST = "000")) then do not learn or update address else continue
if ((VID_INGRESS_CHECK) and (Receive port is not VLAN member) and (VLAN found)) then do not learn or update address else continue
if ((source address found) and (receive port number != PORT_NUMBER) and (SECURE or BLOCK)) then do not update address else continue
if ((source address found) and (receive port number != PORT_NUMBER)) then update address else continue
if ((source address found) and (AGEABLE) and (not TOUCHED)) then set TOUCHED else continue
if ((source address not found) and (VLAN_AWARE) and not (LEARN_NO_VID)) then learn address with VLAN
if ((source address not found) and ((not VLAN_AWARE) or (VLAN_AWARE and LEARN_NO_VID))) then learn address without VLAN
End of Table 2-21

2.4.7 10GbE Additional Features

2.4.7.1 Packet Priority Handling

Overall the 10GbE switch handles priority in 3 stages:

1. Packet Priority - This is the priority carried by the Ethernet frame. If the switch is configured to be VLAN unaware then all packets are considered to be “priority untagged”. When the switch is configured to be VLAN aware then only packets carrying valid VLAN tags are considered to be “priority tagged”.
2. Header Packet Priority - Each port on ingress uses its "packet priority to header packet priority mapping register" to determine the priority at which the packet is forwarded to the destination port. The header packet priority is communicated to the destination port as well.
3. Switch Priority - Each port on egress uses its associated “header packet priority to switch priority mapping register” to determine the actual priority used for transmission.

2.4.7.1.1 Ethernet Port Ingress

Packets received on Ethernet ports have a received packet priority (0 to 7 with 7 being the highest priority). The received packet priority is the source port priority for untagged packets, and the actual packet priority for VLAN tagged packets. The received packet priority is mapped through the receive port’s associated “packet priority to header packet priority mapping register” to obtain the header packet priority. The header packet priority is mapped through each destination port “header priority to switch priority mapping register” to obtain the transmit hardware switch priority (0 to 7 with 7 being the highest priority). At the destination port the priority enforced will be determined by this mapping.

Note—The header packet priority is still used on egress as the actual transmit priority value on the VLAN tag if the VLAN information is to be sent on egress. Please see Section 2.4.7.5 for more information on VLAN tag processing.

2.4.7.1.2 Host Port Ingress

Packets received on the host port have a received packet priority (0 to 7 with 7 being the highest priority). The received packet priority is the source port priority for untagged packets, and the actual packet priority for VLAN tagged packets. The received packet priority is mapped through the port’s associated “packet priority to header packet priority mapping register” to obtain the header packet priority. For the switch priority when the packet is forwarded to the destination port the switch considers this a special case. The actual transmit priority will be determined by the PKTDMA TX channel over which the packet was sent to the Host port. So, PKTDMA TX channel 0 is priority 0, TX channel 1 is priority 1 and so on.

Note—The header packet priority is still used on egress as the actual transmit priority value on the VLAN tag if the VLAN information is to be sent on egress. Please see Section 2.4.7.5 for more information on VLAN tag processing.

2.4.7.1.3 Priority Protocols

The switch employs always fixed priority handling. However, since this can cause starvation for lower packet priorities it allows for priority "escalation". Register CPSW_PTYPE allows users to turn on and off escalation for all three ports. When escalation is turned on, the value on esc_pri_Id_val is used to determine how many packets of a higher priority is allowed to be transmitted before the next lower priority is allowed to send a packet. For example, let us say the esc_pri_Id_val is set to 2 (minimum allowed) and the particular egress port has 4 priority 7 packets, 1 priority 6 packet and 2 priority 4 packets. The port will send two priority 7 packets then it will allow priority 6 to send two packets, but since there is only one, after it is sent it allows priority 5 to send two packets, since there is none it skips over this priority and allows priority 4 to send its two packets. After this round, it will allow priority 7 to send its two remaining packets.

The host port has another exception. On ingress, the received priority at which the packet is forwarded to the destination port can be set to either fixed or round robin on P0_PRI_CTL_REG.

2.4.7.2 Rate Limiting

Rate-limit mode is intended to allow some PKTDMA receive (switch ingress) channels and some Ethernet port priorities (switch egress) to be rate-limited. Non rate-limited traffic (bulk traffic) is allowed on non rate-limited channels and FIFO priorities. The bulk traffic does not impact the rate-limited traffic. Rate-limited traffic must be configured to be sent to rate-limited queues (via packet priority handling). The allocated rates for rate-limited traffic must not be oversubscribed. For example, if port 1 is sending 15% rate limited traffic to port 2 priority 3, and port 0 is also sending 10% rate-limited traffic to port 2 priority 3, then the port 2 priority 3 egress rate must be configured to be 25% plus a percent or two for margin. The switch must be configured to allow some percentage of non rate-limited traffic. Non rate-limited traffic must be configured to be sent to non rate-limited queues. No packets from the host should be dropped, but non rate-limited traffic received on an Ethernet port can be dropped.

2.4.7.2.1 Host Port Receive Rate Limiting

Port 0 receive operations can be configured to rate limit the host ingress data for each receive priority. Rate limiting is enabled for a priority when the p0_rx_rlim[7:0] bit associated with that priority is set in the p0_pri_ctl register. Bulk traffic does not impact rate-limited traffic. No bulk priority will be enabled to send unless there are p1_tx_host_blks_rem number of unused blocks remaining in the port 1 transmit FIFO and there are p2_tx_host_blks_rem number of unused blocks remaining in the port 2 transmit FIFO. The "blocks remaining check" ensures that bulk traffic from the host will not block rate-limited traffic from the host. Rate limited channels must be the highest priority channels. For example, if two rate limited channels are required then p0_rx_rlim[7:0] should be set to 11000000 with the msb corresponding to channel 7. When any channels are configured to be rate-limited, the priority type must be fixed for receive. Round-robin priority type is not allowed when rate-limiting. Each of the eight receive priorities has two associated registers to control the rate at which the priority is allowed to send data (p0_priN_send and p0_priN_idle) when the channel is rate-limiting. Each priority has a send count (p0_priN_send) and an idle count (p0_priN_idle). In general, smaller values for the idle and send values are better than bigger values. The transfer rate includes the inter-packet gap (12 bytes) and the preamble (8 bytes). The rate in Mbits/second that each priority is allowed to send is controlled by the below equation:

Priority Transfer rate in Mbit/s = ((pN_priN_idle/(pN_priN_idle + pN_priN_send)) * frequency * 256

Where the frequency is the VBUSP_GCLK frequency (350 for 350Mhz).

2.4.7.2.2 Ethernet Port Transmit Rate Limiting

Ethernet port transmit operations can be configured to rate limit egress data for each egress priority. Rate limiting is enabled for a priority when the pN_tx_rlim[7:0] bit associated with that priority is set in the pN_pri_ctl register. Bulk traffic does not impact the overall rates at which rate-limited priorities are sent. Bulk priorities are enabled to send only during times that rate-limited priorities are not allowed to send due to rate limits being reached. Rate limited channels must be the highest priority channels. For example, if two rate limited channels are required then pN_tx_rlim[7:0] should be set to 11000000 with the msb corresponding to channel 7. When any channels are configured to be rate-limiting, the priority type must be fixed for receive. Round-robin priority type is not allowed when rate-limiting. Each of the eight receive priorities has two associated registers to control the rate at which the priority is allowed to send data (p0_priN_send and p0_priN_idle) when the channel is rate-limiting. Each priority has a send count (p0_priN_send) and an idle count (p0_priN_idle). In general, smaller values for the idle and send values are better than bigger values. The transfer rate includes the inter-packet gap (12 bytes) and the preamble (8 bytes). The rate in Mbits/second that each priority is allowed to send is controlled by the below equation:

Priority Transfer rate in Mbit/s = ((pN_priN_idle/(pN_priN_idle + pN_priN_send)) * frequency * 256

Where the frequency is the VBUSP_GCLK frequency (350 for 350Mhz).

2.4.7.3 Packet CRC Handling

2.4.7.3.1 Ethernet Port Ingress

All Ethernet ports check the ingress packet CRC in all modes/speeds. The receive port can check either Ethernet CRC or Castagnoli CRC as determined by the crc_type bit in the MAC_MAC_CTL register.

2.4.7.3.2 Ethernet Port Egress

The MAC module transmits each egress packet with the CRC selected by the crc_type bit in the MAC_MAC_CTL register, regardless of the type of CRC that the packet had on ingress to the switch. Each packet CRC is checked for correctness and if the CRC is correct then the packet is output with the generated selected output CRC. If the input packet CRC is incorrect (due either to a bit flip in a memory or an error CRC passed in on host ingress), then the generated egress CRC type is used with at least a single byte of the CRC inverted to indicate the error.

2.4.7.3.3 Host Port Ingress

Host port ingress packets can be passed in with or without a CRC. Host port ingress packets are not checked for CRC correctness on Host port ingress (however they are checked for correctness on MAC egress and output with a CRC error if they came in with a CRC error). If a Host port ingress packet does not have the info0 passed_crc bit set then a CRC will be generated for the packet on Host port ingress. If the passed_crc bit is set then the packet is received unchanged. The CRC type is input in the INFO0 word crc_type bit and can be either Ethernet or Castagnoli and can be different from packet to packet. The p0_tx_crc_type bit in the CPSW_Control register is for Host port transmit (egress) only.

2.4.7.3.4 Host Port Egress

The Host port streaming interface INFO0 passed_crc bit is always set indicating that a CRC is output for each Host port transmit egress packet. The CRC type is determined by the p0_tx_crc_type bit in the CPSW_Control register.

2.4.7.4 Flow Control

2.4.7.4.1 Ethernet Port Flow Control

The Ethernet ports have flow control available for receive operations (packet ingress). Ethernet port receive flow control is initiated when enabled and triggered. Packets received on an Ethernet port can be sent to the other Ethernet ports or the Host port. Each destination port can trigger the receive Ethernet port flow control. An Ethernet destination port triggers another Ethernet receive flow control when the destination port is full. The Host destination port triggers an Ethernet receive flow control port when the associated Host transmit buffer contains CPSW_CPPI_THRESH number of 4-byte words.

When a packet is received on an Ethernet port interface with enabled flow control the below occurs:

- The packet will be sent to all ports that currently have room to take the entire packet.
- The packet will be retried until successful transmission to all ports that first indicated they did not have room for the packet.

The flow control trigger to the MAC will be asserted until the packet has been sent, and there is room in the logical receive FIFO for packet runout from another flow control trigger (rx_pkt_cnt = 0). Ethernet port receive flow control is disabled by default on reset. Ethernet port receive flow control requires that the rx_flow_en bit in the associated MAC be set to one. If a sending port ignores a pause frame then packets may be dropped on overrun.

2.4.7.4.2 Host Port Flow Control

The Host FIFO port has flow control for receive operations (packet ingress). Host port receive flow control is initiated when enabled (default) and triggered. When enabled receive flow control is accomplished through pushback. The pushback will cause the Host port logical receive FIFO to fill up with packet data. Flow control is accomplished with a deasserted RXST_THREAD_SREADY on the streaming interface.

2.4.7.5 More on VLAN Egress Packet processing

All ports (Ethernet and Host) process packet VLAN's identically on egress. Receive packet VLAN's are not modified on ingress regardless of the port type or VLAN mode. Also, if the port is operating in VLAN unaware mode then the packet is not modified on egress or ingress.

An egress port is operating in the VLAN aware mode when the VLAN_AWARE bit in the CPSW_Control register is set. In VLAN aware mode, transmitted packet data is changed depending on the packet type, packet priority (pkt_pri), and VLAN information as shown in the below tables:

Table 2-22 VLAN Aware Mode Non Tagged Transmit Packet Processing

Type - Non-VLAN Tagged Packet	
Insert VLAN Case	Non tagged input packets have the header packet VLAN inserted when the no_vlan bit in the transmit packet header is deasserted. The VLAN LTYPE 0x8100 is inserted after the source address followed by the two byte header packet VLAN. The header packet VLAN is composed of the hdr_pkt_pri, the hdr_pkt_cfi, and the hdr_pkt_vid. The packet length/type field is output four bytes later than it is input and is not removed or replaced. If the CRC is present in the packet data (pass_crc is asserted), then the packet CRC is replaced with a MAC generated CRC
No Change Case	Non tagged input packets are output unchanged when the no_vlan transmit packet header bit is asserted.

Table 2-23 VLAN Aware Mode Priority Tagged Transmit Packet Processing

Type - VLAN Tagged packet with VID = 0	
Replace PRI/VID Case	Priority tagged input packets have the packet VLAN ID (VID) and the packet priority replaced with the hdr_pkt_vid and the hdr_pkt_pri when the transmit packet header no_vlan bit is deasserted.
Remove VLAN Case	Priority tagged input packets have the 4-byte packet VLAN information removed when the transmit packet header no_vlan bit is asserted. The 0x8100 length type is removed as is the two byte packet VLAN. Input 64-67 byte priority tagged packets go out with the VLAN removed and padded to 64-bytes if the pass_crc input bit is asserted. The input CRC bytes are used as the pad data. Input 64-byte priority tagged packets use all four input CRC bytes as pad, input 65-byte priority tagged packets use three of the input CRC bytes as pad, and so on. No pad is performed if the pass_crc input bit is not asserted - input 64-67 byte (on the wire) priority tagged packets go out as 60-63 byte packets. The output CRC is generated by the MAC when the VLAN is removed regardless of whether a pad is added or not. The input CRC is either discarded or used as pad. Input priority tagged packets shorter than 64-bytes with pass_crc asserted and with no_vlan asserted are not allowed. Input priority tagged packets shorter than 68-bytes (on the wire) with pass_crc deasserted and with no_vlan asserted are not allowed.

Table 2-24 VLAN Aware Mode VLAN Tagged Transmit Packet Processing

Type - VLAN Tagged packet with VID != 0	
Replace PRI Case	VLAN tagged input packets are output with the packet priority replaced with the hdr_pkt_pri when the transmit packet header no_vlan bit is deasserted. If the CRC is present in the packet data (pass_crc is asserted), then the packet CRC is replaced with a MAC generated CRC.
Remove VLAN Case	VLAN tagged input packets have the 4-byte packet VLAN information removed when the transmit packet header no_vlan bit is asserted. The 0x8100 length type is removed as is the two byte packet VLAN. Input 64-67 byte VLAN tagged packets go out with the VLAN removed and padded to 64-bytes if the pass_crc input bit is asserted. The input CRC bytes are used as the pad data. Input 64-byte VLAN tagged packets use all four input CRC bytes as pad, input 65-byte VLAN tagged packets use three of the input CRC bytes as pad, and so on. No pad is performed if the pass_crc input bit is not asserted - input 64-67 byte (on the wire) VLAN tagged packets go out as 60-63 byte packets. The output CRC is generated by the MAC when the VLAN is removed regardless of whether there is a pad or not. The input CRC is either discarded or used as pad. Input VLAN tagged packets shorter than 64-bytes with pass_crc asserted and with no_vlan asserted are not allowed. Input VLAN tagged packets shorter than 68-bytes (on the wire) with pass_crc deasserted and with no_vlan asserted are not allowed.

2.5 Serial Gigabit Media Independent Interface (SGMII) Architecture

This section provides an overview of the SGMII architecture. The main function of this module is to translate between the GMII data format used by the CPGMAC module and the 8B/10B encoded data format used by the SerDes module. The SGMII module is also responsible for establishing a link and autonegotiating with other devices. This section will cover the receive interface, the transmit interface, and several configurations for connecting to other PHY or SGMII devices.

2.5.1 SGMII Receive Interface

The SGMII receive interface converts the encoded receive input from the SerDes into the GMII signals required by the MAC module.

2.5.2 SGMII Transmit Interface

The SGMII transmit interface converts the GMII input data from the MAC module into the 8B/10B encoded output required by the SerDes module. The MAC module does not source the transmit error signal. Any transmit frame from the MAC with an error will be indicated as an error. Transmit error is assumed to be zero at all times, and is not input to the CRC module.

When operating in 10/100 mode, the GMII_MTXD(7:0) data bus uses only the lower nibble.

Any packet in data transmission from the CPGMAC while the link signal is deasserted will be ignored. Only packets that begin after the rising edge of link will be transferred.

2.5.3 Modes of Operation

This section describes the modes of operation supported by the SGMII module.

2.5.3.1 Digital Loopback

This section describes the loopback mode supported by the SGMII, and give instructions on how to configure the SGMII module in loopback mode.

The SGMII module supports the ability to internally connect the transmit signals to the receive signals. It is important to note that this is digital loopback, because the transmit and receive signals are connected before reaching the SerDes module. When in this configuration, the transmit clock (TX_CLK) is used to for transmit and receive clocking. Loopback mode can be entered by asserting the LOOPBACK bit in the SGMII_CONTROL register. When entering or exiting loopback mode, it is important to reset the transmit and receive logic using the RT_SOFT_RESET bit in the SOFT_RESET register.

The sequence for entering or exiting loopback mode is shown in Procedure 2-3.

Procedure 2-3 Digital Loopback Configuration

Step	Action
1	Clear to zero the MR_AN_ENABLE bit in the SGMII_CONTROL register
2	Write to one the RT_SOFT_RESET bit in the SOFT_RESET register
3	Write to one the LOOPBACK bit in the SGMII_CONTROL register
4	Write to zero the RT_SOFT_RESET bit in the SOFT_RESET register

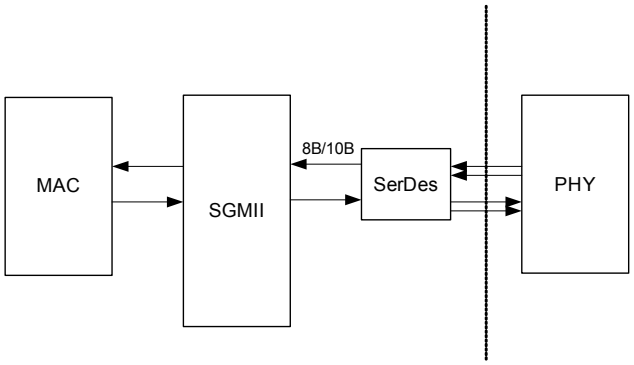
End of Procedure 2-3

2.5.3.2 SGMII to PHY Configuration

This section describes how to configure the SGMII to connect with an external PHY when operating SGMII mode. Figure 2-8 shows an example of this configuration.

To connect with an external PHY, the PHY will be the master, and the SGMII module needs to be configured in slave mode. The procedure for setting the SGMII in slave mode is shown below:

Figure 2-8 SGMII Mode with PHY Configuration



Procedure 2-4 SGMII to PHY Configuration

Step - Action

1 Setup the SGMII and enable autonegotiation:

1a Set bit 0 of the MR_ADV_ABILITY register

```
MR_ADV_ABILITY &= 0xFFFF0000; /* Clear the register contents */

MR_ADV_ABILITY |= 0x00000001;
```

1b Enable autonegotiation by setting the MR_AN_ENABLE bit in the SGMII_CONTROL Register:

```
SGMII_CONTROL |= 0x00000001; /* Enable autonegotiation */
```

2 Poll the SGMII_STATUS register to determine when autonegotiation is complete without error. The AN_ERROR bit in the SGMII_STATUS register will be set if the mode was commanded to be half-duplex gigabit.

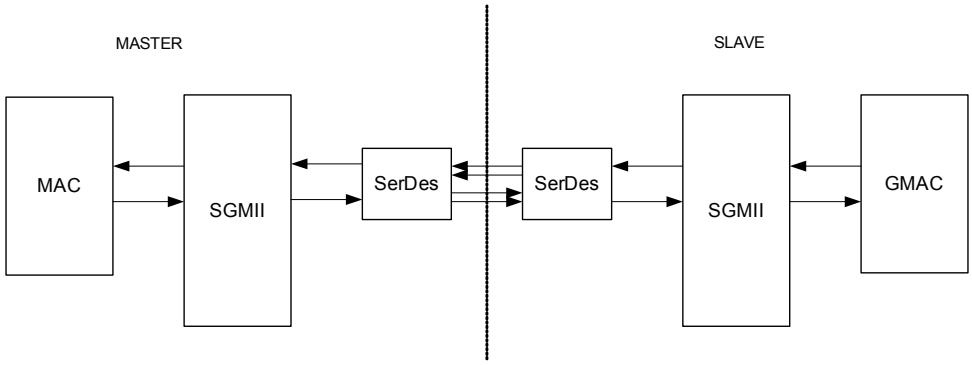
3 In the MAC module, set the EXT_EN bit in the MAC_CONTROL register to allow the speed and duplex mode to be set by the signals from the SGMII.

End of Procedure 2-4

2.5.3.3 SGMII to SGMII with Autonegotiation Configuration

This section describes how to configure an SGMII device to connect with another SGMII device with auto-negotiation. in The diagram below shows an example of this configuration.

Figure 2-9 SGMII Master to SGMII Slave with Autonegotiation Configuration



When connecting two SGMII devices with autonegotiation, one SGMII device must be configured as the master, and the other SGMII device must be configured as the slave.

2.5.3.3.1 SGMII Master Mode with Autonegotiation

The procedure for setting the SGMII in master mode with autonegotiation is shown below:

Procedure 2-5 Setting up the SGMII in Master Mode with Autonegotiation

Step - Action

1 Setup the SGMII and enable autonegotiation:

1a Set the MR_ADV_ABILITY register

```
MR_ADV_ABILITY &= 0xFFFF0000; /* Clear the register contents */

MR_ADV_ABILITY |= 0x00009801; /* Full duplex gigabit configuration */
```

1b Enable autonegotiation by setting the MR_AN_ENABLE bit in the SGMII_CONTROL Register:

```
SGMII_CONTROL |= 0x00000021; /* Master Mode with autonegotiation enabled */
```

2 Poll the LINK and MR_AN_COMPLETE bits in the SGMII_STATUS register to determine when the link is up and autonegotiation is complete.

3 In the MAC module, the user can optionally set the EXT_EN bit in the MAC_CONTROL register to allow the speed and duplex mode to be set by the signals from the SGMII.

End of Procedure 2-5

2.5.3.3.2 SGMII Slave Mode with Autonegotiation

The procedure for setting the SGMII in slave mode with autonegotiation is shown below:

Procedure 2-6 Setting up the SGMII in Slave Mode with Autonegotiation

Step - Action

1 Setup the SGMII and enable autonegotiation:

1a Set the MR_ADV_ABILITY register

```
MR_ADV_ABILITY &= 0xFFFF0000; /* Clear the register contents*/

MR_ADV_ABILITY |= 0x00000001;
```

1b Enable autonegotiation by setting the MR_AN_ENABLE bit in the SGMII_CONTROL Register:

```
SGMII_CONTROL |= 0x00000001; /* Enable autonegotiation */
```

2 Poll the SGMII_STATUS register to determine when autonegotiation is complete without error. The AN_ERROR bit in the SGMII_STATUS register will be set if the mode was commanded to be half-duplex gigabit.

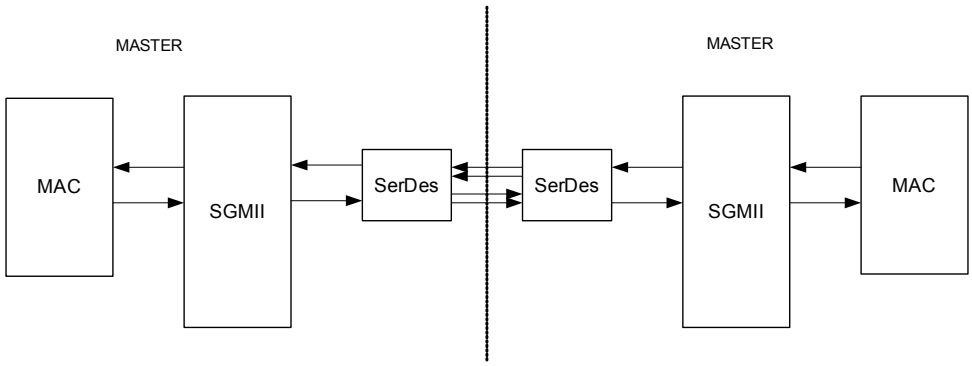
3 In the MAC module, set the EXT_EN bit in the MAC_CONTROL register to allow the speed and duplex mode to be set by the signals from the SGMII.

End of Procedure 2-6

2.5.3.4 SGMII to SGMII with Forced Link Configuration

This section describes how to configure an SGMII device to connect with another SGMII device with a forced link. in The diagram below shows an example of this configuration.

Figure 2-10 SGMII Master to SGMII Master with Forced Link Configuration



When connecting two SGMII devices with forced link, both SGMII devices must be configured as masters.

The procedure for setting the SGMII in master mode with forced link is shown below:

Procedure 2-7 SGMII to SGMII with Forced Link

Step - Action

1 Setup the SGMII:

1a Set the MR_ADV_ABILITY register

```
MR_ADV_ABILITY &= 0xFFFF0000; /* Clear the register contents */

MR_ADV_ABILITY |= 0x00009801; /* Full duplex gigabit configuration */
```

1b Set the device in master mode without autonegotiation by setting the MASTER bit in the SGMII_CONTROL Register:

```
SGMII_CONTROL |= 0x00000020; /* Master Mode, no autonegotiation */
```

2 Poll the LINK bit in the SGMII_STATUS register to determine when the link is up.

3 In the MAC module, the user must set the EXT_EN bit in the MAC_CONTROL register to allow the speed and duplex mode to be set by the signals from the SGMII.

End of Procedure 2-7

2.6 PCS-R

The 10GBASE-R Physical Coding Sublayer (PCS-R) module provides the functionality of a physical coding sublayer (PCS) on data being transferred between a demuxed XGMII and 10 Gigabit SerDes supporting a 16 or 32 bit interface.

PCS-R feature summary:

- 10 Gigabit Ethernet serial 10GBASE-R PCS as described in IEEE 802.3 Clause 49
- Connects to a 10 Gigabit Ethernet MAC (XGM) using a demultiplexed XGMII interface
- Connects to a 10 Gigabit SerDes using a 16 (XSBI) or 32 bit interface
- 64/66B encoding and decoding with support for all reserved codes and signal ordered set for fibre channel use
- Optional support for Forward Error Correction (FEC) sublayer as described in IEEE
- 802.3 Clause 74 Support for Energy Efficient Ethernet (EEE) by transporting Low Power Idle (LPI) as described in IEEE 802.3az Clause 49

Programming PCS-R is simpler than SGMII. Set control register to 0x2 hex value to enable. PCS-R is always enabled in 10G speed.

2.7 MACSEC Module

2.7.0.1 MACSEC Architecture

The MACSec provided in the 10GbE switch is a high performance (> 20 Gbps total throughput) MACsec engine with integrated VLAN and MACsec packet classification logic as well as a large number of statistics counters. It is integrated with the Ethernet MAC to form a plugin MACsec solution between the Ethernet Switch and the Ethernet MAC modules. There is one instance per Ethernet port. The MACSec is composed of the following primary modules:

- Input adapter
- Input Classification engine
- Packet engine
- Consistency Checking engine
- Output Post-processing engine
- Statistics Update engine
- Output adapter

2.7.0.1.1 Input adapter

The Input adapter manages the Input Packet interface and ensures interface protocol compliance, isolating the internals of the MACSec from the switch interface.

2.7.0.1.2 Input Classification engine

The Input Classification engine inspects the received frame data and performs the following functions on it:

- Control frame classification – a total of 21 programmable rules to classify the frame as a control frame.

- VLAN tag detection – programmable functionality to detect VLAN tags and extract information before further classification. MACsec tag detection – programmable functionality to detect MACsec tags and check whether or not they are valid.
- Default frame handling – the outputs of the control frame classification and MACsec tag detection modules are used to classify packets into 8 different classes, with control registers to define what to do with a packet (drop or bypass) for each of those classes.
- Flow lookup frame classification and frame handling – a Content Addressable Memory (CAM) module used to classify frames based on frame header field contents and outputs of the control frame classification, VLAN tag detection and MACsec tag detection modules. Flow control registers define what to do with a frame (drop, bypass or MACsec process) when matching one of those entries. A programmable per-rule priority level resolves any overlap between these rules.
- Flow lookup / default classification multiplexer – this multiplexer gives priority to the CAM module decision in the flow lookup frame classification module. Only if none of the CAM entries matched, the default frame handling is used for a frame.

2.7.0.1.3 Packet engine

The Packet engine is a standard IP core for MACsec encapsulation/decapsulation processing. It is capable of autonomously encapsulating or decapsulating a MACsec frame, including header insertion and removal. It does not perform MACsec header parsing, but relies on external logic to provide a processing 'token' that tells it how to process the incoming frame. Supports AES-GCM-128 authenticated encryption and decryption.

2.7.0.1.4 Consistency Checking engine

The Consistency Checking engine checks the contents of a frame at the output of the Packet engine (thus after any MACsec decryption) against a set of 8 programmable rules for consistency. A programmable per-rule priority level resolves any overlap between these rules.

2.7.0.1.5 Output Post-processing engine

The Output Post-processing engine checks the classification and Packet engine processing results against a fixed set of MACsec compliance rules, resulting in a drop decision if the rules are violated. Additionally, it performs programmable MTU checking on the output frame, with individual global and per-VLAN-user-priority MTU settings.

It combines these internal decisions with decisions made by the Classification and Consistency Checking engines into a final pass/drop decision to the Output adapter.

Furthermore, based on all the information from the Packet engine and the Consistency Checking engine available to it, the Output Post-processing engine decides which statistics counters to increment.

2.7.0.1.6 Statistics Update engine

The Statistics Update engine takes care of the actual statistics counter updating in the external on-chip RAM, as instructed by the Output Post-process engine. This allows the updating to be scheduled with any external statistics accesses and to occur in parallel with the Post-processing of the next frame. This engine also can be configured to skip certain statistics counters.

2.7.0.1.7 Output adapter

The Output adapter manages the Output Packet interface and ensures interface protocol compliance, isolating the internals of the MACSec from the switch interface.

2.7.0.2 MACSEC Egress/Ingress Operations

Each MACSec instance is associated with an Ethernet port. Both instances handle ingress and egress traffic. Rules and decisions made for packets in to- and from-network directions are configured with flows. Below an overview of the ingress and egress operations and flow configuration.

2.7.0.2.1 Egress Operation

The MACSec module always operates in cut-through mode for egress operation. The length of the frame need not be known before the start of processing and is calculated on the fly. This means that MACsec egress processing encrypts/protects all bytes of the frame that were fed into the MACsec core. If the frame contains Ethernet padding, this padding is encrypted/protected by MACsec and the ICV is appended after it

2.7.0.2.2 Ingress Operation

The MACsec core always operates in cut-through mode for ingress operation. The length of the frame generally need not be known before the start of processing. Frames that go out of the ingress MACsec core are passed unmodified to the Output Packet interface.

2.7.0.2.3 Flows

Flows configure what MACsec module does with a packet on ingress and egress. Essentially a each MACSec instance needs two flows configured, one for ingress and one for egress. The MACSec modules as instantiated in the 10GbE always use controlled ports configuration on the flows. Always program the flow for non-drop action on packets. Flows are programme d via the SAM_FLOW_CTRL_n registers. For full details of what flows control see the register definition.

2.8 Management Data Input/Output (MDIO) Architecture

This section describes the architecture of the Management Data Input/Output (MDIO) module. The MDIO module manages up to 32 physical layer (PHY) devices connected to the Ethernet Media Access Controller (EMAC). The MDIO module allows almost transparent operation of the MDIO interface with little maintenance from the DSP.

The MDIO module enumerates all PHY devices in the system by continuously polling 32 MDIO addresses. Once it detects a PHY device, the MDIO module reads the PHY status register to monitor the PHY link state. The MDIO module stores link change events that can interrupt the CPU. The event storage allows the DSP to poll the link status of the PHY device without continuously performing MDIO module accesses. When the system must access the MDIO module for configuration and negotiation, the MDIO module performs the MDIO read or write operation independent of the DSP. This independent operation allows the DSP to poll for completion or interrupt the CPU once the operation has completed.

2.8.1 Global PHY Detection and Link State Monitoring

The MDIO module enumerates all PHY devices in the system by continuously polling the link status from the Generic Status Register of all 32 MDIO addresses. The module tracks whether a PHY on a particular address has responded, storing the results in the ALIVE register. The MDIO module also tracks whether the PHY currently has a link, storing the results in the LINK register. This information allows the software

application to quickly determine which MDIO address the PHY is using and if the system is using more than one PHY. The software application can then quickly switch between PHYs based on their current link status. The link status of two of the 32 possible PHY addresses can also be determined using the MLINK pin inputs. The LINKSEL bit in the USERPHYSELn register determines the status input that is used. A change in the link status of the two PHYs being monitored will set the appropriate bit in the LINKINTRAW register and the LINKINTMASKED register, if enabled by the LINKINTENB bit in the USERPHYSELn register.

2.8.2 PHY Register User Access

When the DSP must access the MDIO for configuration and negotiation, the PHY access module performs the actual MDIO read or write operation independent of the DSP. Thus, the DSP can poll for completion or receive an interrupt when the read or write operation has been performed. There are two user access registers, USERACCESS0 and USERACCESS1, which allow the software to submit up to two access requests simultaneously. The requests are processed sequentially.

At any time, the host can define a transaction for the MDIO module to undertake using the DATA, PHYADR, REGADR, and WRITE fields in a USERACCESSn register. When the host sets the GO bit in this register, the MDIO module will begin the transaction without any further intervention from the host. Upon completion, the MDIO interface will clear the GO bit and set the USERINTRAW bit in the USERINTRAW register corresponding to the USERACCESSn register being used. The corresponding bit in the USERINTMASKED register may also be set depending on the mask setting in the UINTMASKSET and USERINTMASKCLK registers. A round-robin arbitration scheme is used to schedule transactions which may queued by the host in different USERACCESS registers. The host should check the status of the GO bit in the USERACCESSn register before initiating a new transaction to ensure that the previous transaction has completed. The host can use the ACK bit in the USERACCESSn register to determine the status of a read transaction. In addition, any PHY register read transactions initiated by the host also cause the MDIOALIVE register to be updated.

2.8.2.1 Writing Data to a PHY Register

The MDIO module includes a user access register (USERACCESSn) to directly access a specified PHY device. To write a PHY register, perform the following steps:

1. Ensure that the GO bit in the USERACCESSn register is cleared.
2. Write to the GO, WRITE, REGADR, PHYADR, and DATA bits in USERACCESSn corresponding to the desired PHY and PHY register.
3. The write operation to the PHY is scheduled and completed by the MDIO module.
4. Completion of the write operation will clear the GO bit to 0, and sets the corresponding bit in the USERINTRAW register for the corresponding USERACCESSn.
   - If interrupts have been enabled on this bit using the USERINTMASKSET register, then the bit is also set in the USERINTMASKED register and an interrupt is triggered on the DSP.
   - If interrupts have not been enabled, then completion can be determined by polling the GO bit in USERACCESSn for a 0.

2.8.2.2 Reading Data from a PHY Register

The MDIO module includes a user access register (USERACCESSn) to directly access a specified PHY device. To read a PHY register, perform the following:

1. Ensure that the GO bit in the USERACCESSn register is cleared.
2. Write to the GO, REGADR, and PHYADR bits in USERACCESSn corresponding to the desired PHY and PHY register.
3. The read data value is available in the DATA bits of USERACCESSn after the module completes the read operation on the serial bus.
4. Completion of a successful read operation will clear the GO bit, set the ACK bit, and set the corresponding bit in the USERINTRAW register for the USERACCESSn used.
   - If interrupts have been enabled on this bit using the USERINTMASKSET register, then the bit is also set in the USERINTMASKED register and an interrupt is triggered on the DSP.
   - If interrupts have not been enabled, then completion can be determined by polling the GO bit in USERACCESSn for a 0, and the ACK bit for a 1.

2.8.3 MDIO Interrupts

The MDIO module provides 2 sets of interrupts that can be enabled by the user. The first set of interrupts is triggered when there is a change in link state of a PHY that is being monitored. The second set of interrupts will occur when a PHY register access initiated through the USERACCESS registers has completed.

2.8.3.1 MDIO Link Status Interrupts

The MDIO module will assert the MDIO_LINKINT signals if there is a change in the link state of the PHY corresponding to the address in the PHYADR_MON field of the USERPHYSELn register and the corresponding LINKINTENB bit is set. The LINKINTMASKED event is also captured in the LINKINTMASKED register. LINKINTMASKED[0] and LINKINTMASKED[1] correspond to the USERPHYSEL0 and USERPHYSEL1 registers, respectively.

2.8.3.2 MDIO User Access Interrupts

When the GO bit in the USERACCESS registers transitions from 1 to 0, indicating the completion of a user access, and the corresponding USERINTMASKED bit in the USERINTMASKSET register is set, the USERINTMASKED signal is asserted to 1. The USERINTMASKED event is also captured in the USERINTMASKED register. USERINTMASKED[0] and USERINTMASKED[1] correspond to the USERACCESS0 and USERACCESS1 registers, respectively.

2.8.4 Initializing the MDIO Module

To have the application software or device driver initialize the MDIO device, perform the following steps:

1. Configure the PREAMBLE and CLKDIV bits in the MDIO_CONTROL register.
2. Enable the MDIO module by setting the ENABLE bit in the MDIO_CONTROL register.
3. The ALIVE register can be read after a delay to determine which PHYs responded, and the LINK register can determine which of those (if any) already have a link.
4. Set up the appropriate PHY addresses in the USERPHYSELn register, and set the LINKINTENB bit to enable a link change event interrupt if desirable.

5. If an interrupt on a general MDIO register access is desired, set the corresponding bit in the USERINTMASKSET register to use the USERACCESSn register. If only one PHY is to be used, the application software can set up one of the USERACCESSn registers to trigger a completion interrupt. The other register is not set up.

2.9 Serializer/Deserializer (SerDes) Architecture

SerDes module information for KeyStone II devices is not provided in this user guide. Please check for availability of the SerDes User Guide for KeyStone II Devices on the device product page.

2.10 Reset Considerations

The 10GbE switch subsystem supports reset isolation of the two Ethernet switch ports. The intent of reset isolation is to allow packets to switch between the two ethernet ports while the remainder of the system is undergoing a reset. When the ISOLATE input is asserted the below occur simultaneously:

- The 10GbE switch host port (port 0) is removed from ALE processing (packets received on ports 1 and 2 intended for port 0 will be dropped)
- Packets from the queue manager subsystem intended the 10GbE switch host port (port 0) are dropped. Any packet currently in progress when ISOLATE is asserted is dropped due to a receive packet code error (and possible a CRC or FRAG error)
- 10GbE switch host port (port 0) egress packets in queue are dropped

For more information about reset isolation for the 10GbE switch subsystem, see the device-specific data manual.

2.11 Initialization

This section describes the 10GbE switch subsystem initialization procedure.

Procedure 2-8 10GbE Switch Subsystem Initialization Procedure

Step	Action
1	Configure SERDES. (See Section 2.9)
2	Configure the CPSW_CONTROL register
3	Configure the MAC1_SA and MAC2_SA source address hi and lo registers
4	Enable the desired statistics ports by programming the CPSW_STAT_PORT_EN register
5	Configure the ALE
6	Configure MAC modules
7	Configure the MDIO and external PHY (if used)
8	Configure the SGMII modules

End of Procedure 2-8

2.12 Interrupt Support

2.12.1 Interrupt Events

This section describes the interrupts generated in the 10GbE switch subsystem. Within the 10GbE switch subsystem, there are three modules that can generate interrupts: the MDIO module, the statistics module, and the time synchronization module. For more information about the interrupts generated by the MDIO module, see Section 2.8. For more information about the interrupts generated by the statistics modules, see Section 2.4.4. For more information about the interrupts generated by the time synchronization module, see Section 2.4.5.

2.13 Power Management

The gigabit Ethernet (10GbE) switch subsystem provides power management in the form of clock gating. For more information, please see the device specific data manual.

Chapter 3

Registers

This chapter describes the registers available in the 10Gigabit Ethernet switch subsystem, its submodules, and the related registers in the SerDes module. For clarity, the registers for each module and submodule are described separately. Provided for each register is a bit field description and a memory offset address. The offset address values provided are relative to the associated base address of the module. See the device-specific data manual for the memory address of these registers.

3.1 Summary of Modules

Table 3-1 lists the module regions in the Ethernet switch subsystem and the corresponding address offset for each module. For convenience, an entire listing of all of the registers is provided in Table 3-2.

Table 3-1 10 Gigabit Ethernet Subsystem Modules

Offset Address[1]	Module Region	Section
00000h	3-port 10 Gigabit Ethernet (10GbE) switch sub-module	Section 3.2
00100h	Port 1 SGMII module	Section 3.3
00200h	Port 2 SGMII module	Section 3.3
00300h	Reserved	Reserved
00500h	MDIO module	Section 3.4
00600h	Port 1 PCS-R module	Section 3.5
00630h	Reserved	
00680h	Port 2 PCS-R module	Section 3.5
006b0h	Reserved	
01000h	10 Gigabit Ethernet (10GbE) switch	Section 3.6
02000h	Reserved	
20000h	Port 1 MACSEC module	Section 3.7
40000h	Port 2MACSEC module	Section 3.7
60000h	Rserved	
A0000h	10 Gigabit Ethernet (10GbE) Subsystem	Section 3.8
A0600h	Reserved	
A1000h	PKT DMA Registers	
Af000h	INTD Registers	
End of Table 3-1		

1. The addresses provided in the table are offsets from a device specific base address. To determine the base address of these registers, see the device-specific data manual.

Table 3-2 10 Gigabit Ethernet Subsystem Complete Register Listing (Part 1 of 8)

Offset Address [1]	Module	Acronym	Register Name	Section
00000h	10 GbE Switch Sub-module)	ES_SS_IDVER	10Gigabit Ethernet switch sub-module Identification and Version Register	Section 3.2.1
00004h	10 GbE Switch Sub-module)	SyncE_Count	Synchronous Ethernet Count Register	Section 3.2.1
00008h	10 GbE Switch Sub-module)	SyncE_Mux	Synchronous Ethernet Mux Register	Section 3.2.1
0000Ch	10 GbE Switch Sub-module)	Control	Submodule Control Register	Section 3.2.1
0001Ch-000FCh	Reserved			
00100h	Port 1 SGMII	SGMII_IDVER	Identification and Version Register	Section 3.3.1
00104h	Port 1 SGMII	SOFT_RESET	Soft Reset Register	Section 3.3.2
00108h-0010Ch	Reserved			
00110h	Port 1 SGMII	SGMII_CONTROL	Control Register	Section 3.3.3
00114h	Port 1 SGMII	STATUS	Status Register (read only)	Section 3.3.4
00118h	Port 1 SGMII	MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
0011Ch	Reserved			

Table 3-2 10 Gigabit Ethernet Subsystem Complete Register Listing (Part 2 of 8)

Offset Address [1]	Module	Acronym	Register Name	Section
00120h	Port 1 SGMII	MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.6
00124h-001FCh	Reserved			
00200h	Port 2 SGMII	SGMII_IDVER	Identification and Version Register	Section 3.3.1
00204h	Port 2 SGMII	SOFT_RESET	Soft Reset Register	Section 3.3.2
00208h-0020Ch	Reserved			
00210h	Port 2 SGMII	SGMII_CONTROL	Control Register	Section 3.3.3
00214h	Port 2 SGMII	STATUS	Status Register (read only)	Section 3.3.4
00218h	Port 2 SGMII	MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
0021Ch	Port 2 SGMII	Reserved	Reserved	Reserved
00220h	Port 2 SGMII	MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.6
00224h-004FFh	Reserved			
00500h	MDIO	MDIO_VERSION	MDIO Version Register	Section 3.4.1
00504h	MDIO	MDIO_CONTROL	MDIO Control Register	Section 3.4.2
00508h	MDIO	ALIVE	PHY Alive Status Register	Section 3.4.3
0050Ch	MDIO	LINK	PHY Link Status Register	Section 3.4.4
00510h	MDIO	LINKINTRAW	MDIO Link Status Change Interrupt (Unmaksed) Register	Section 3.4.5
00514h	MDIO	LINKINTMASKED	MDIO Link Status Change Interrupt (Masked) Register	Section 3.4.6
00518h–0051Ch	Reserved			
00520h	MDIO	USERINTRAW	MDIO User Command Complete Interrupt (Unmasked) Register	Section 3.4.7
00524h	MDIO	USERINTMASKED	MDIO User Command Complete Interrupt (Masked) Register	Section 3.4.8
00528h	MDIO	USERINTMASKSET	MDIO User Interrupt Mask Set Register	Section 3.4.9
0052Ch	MDIO	USERINTMASKCLEAR	MDIO User Interrupt Mask Clear Register	Section 3.4.10
00530h–0057Ch	Reserved			
00580h	MDIO	USERACCESS0	MDIO User Access Register 0	Section 3.4.11
00584h	MDIO	USERPHYSEL0	MDIO User PHY Select Register 0	Section 3.4.12
00588h	MDIO	USERACCESS1	MDIO User Access Register 1	Section 3.4.13
0058Ch	MDIO	USERPHYSEL1	MDIO User PHY Select Register 1	Section 3.4.14
00590h–007FCh	Reserved			
00600h	Port 1 PCS-R	PCSR1_TX_CTL	PCSR1 Transmit Control Register	Section 3.5.1
00604h	Port 1 PCS-R	PCSR1_TX_STATUS	PCSR1 Transmit Status Register	Section 3.5.2
00608h	Port 1 PCS-R	PCSR1_RX_CTL	PCSR1 Receive Control Register	Section 3.5.3
0060Ch	Port 1 PCS-R	PCSR1_RX_STATUS	PCSR1 Receive Status Register	Section 3.5.4
00610h	Port 1 PCS-R	PCSR1_SEED_A_LO	PCSR1 Seed A Low Register	Section 3.5.5
00614h	Port 1 PCS-R	PCSR1_SEED_A_HI	PCSR1 Seed A High Register	Section 3.5.6
00618h	Port 1 PCS-R	PCSR1_SEED_B_LO	PCSR1 Seed B Low Register	Section 3.5.7
0061Ch	Port 1 PCS-R	PCSR1_SEED_B_HI	PCSR1 Seed B High Register	Section 3.5.8
00620h	Port 1 PCS-R	PCSR1_FEC	PCSR1 Seed A High Register	Section 3.5.9
00624h	Port 1 PCS-R	PCSR1_CTL	PCSR1 Control Register	Section 3.5.10
00628h	Port 1 PCS-R	PCSR1_RX_FEC_CNT	PCSR1 Receive FEC Count Register	Section 3.5.11
0062Ch	Port 1 PCS-R	PCSR1_RX_ERR_FIFO	PCSR1 Receive Error FIFO Register	Section 3.5.12
00630h-00670hf	Reserved			
00680h	Port 2 PCS-R	PCSR2_TX_CTL	PCSR2 Transmit Control Register	Section 3.5.1
00684h	Port 2 PCS-R	PCSR2_TX_STATUS	PCSR2 Transmit Status Register	Section 3.5.2

Table 3-2 10 Gigabit Ethernet Subsystem Complete Register Listing (Part 3 of 8)

Offset Address [1]	Module	Acronym	Register Name	Section
00688h	Port 2 PCS-R	PCSR2_RX_CTL	PCSR2 Receive Control Register	Section 3.5.3
0068Ch	Port 2 PCS-R	PCSR2_RX_STATUS	PCSR2 Receive Status Register	Section 3.5.4
00690h	Port 2 PCS-R	PCSR2_SEED_A_LO	PCSR2 Seed A Low Register	Section 3.5.5
00694h	Port 2 PCS-R	PCSR2_SEED_A_HI	PCSR2 Seed A High Register	Section 3.5.6
00698h	Port 2 PCS-R	PCSR2_SEED_B_LO	PCSR2 Seed B Low Register	Section 3.5.7
0069Ch	Port 2 PCS-R	PCSR2_SEED_B_HI	PCSR2 Seed B High Register	Section 3.5.8
006A0h	Port 2 PCS-R	PCSR2_FEC	PCSR2 Seed A High Register	Section 3.5.9
006A4h	Port 2 PCS-R	PCSR2_CTL	PCSR2 Control Register	Section 3.5.10
006A8h	Port 2 PCS-R	PCSR2_RX_FEC_CNT	PCSR2 Receive FEC Count Register	Section 3.5.11
006ACh	Port 2 PCS-R	PCSR2_RX_ERR_FIFO	PCSR2 Receive Error FIFO Register	Section 3.5.12
006b0h-00fff	Reserved			
01000h	10 GbE Switch	CPSW_IDVER	10GbE switch identification and version register	Section 3.6.1.1
01004h	10 GbE Switch	CPSW_CONTROL	10GbE switch Control Register	Section 3.6.1.2
01008h	10 GbE Switch	CPSW_EMCONTROL	10GbE switch Emulation Control Register	Section 3.6.1.3
0100Ch	10 GbE Switch	CPSW_STAT_PORT_EN	10GbE switch Statistics Port Enable Register	Section 3.6.1.4
01010h	10 GbE Switch	CPSW_PTYPE	10GbE switch Transmit Priority Type Register	Section 3.6.1.5
01014h	10 GbE Switch	CPSW_SOFT_IDLE	10GbE switch Software Idle	
01018h	10 GbE Switch	CPSW_THRU_RATE	10GbE switch Thru Rate Register	Section 3.6.1.7
0101Ch	10 GbE Switch	CPSW_GAP_THRESH	Transmit FIFO Short Gap Threshold Register	Section 3.6.1.8
01020h	10 GbE Switch	CPSW_TX_START_WDS	Transmit FIFO Start Words Register	Section 3.6.1.9
01024h	10 GbE Switch	CPSW_FLOW_CONTROL	Flow Control Register	Section 3.6.1.10
01028h	10 GbE Switch	CPSW_CPPI_THRESH	CPPI Threshold	Section 3.6.1.11
0102Ch-01030h	Reserved			
01034h	10 GbE Switch	P0_BLK_CNT	Port 0 Block Count	Section 3.6.1.12
01038h	10 GbE Switch	P0_PORT_VLAN	Port 0 VLAN Register	Section 3.6.1.13
0103Ch	10 GbE Switch	P0_Tx_Pri_Map	Port 0 Receive Packet Priority to Header Priority Mapping Register	Section 3.6.1.14
01040h	10 GbE Switch	P0_SRC_ID	Port 0 Source ID Register	Section 3.6.1.15
01044h	10 GbE Switch	P0_Rx_Pri_Map	Port 0 RX Pkt Pri to Header Pri Map Reg (ingress)	Section 3.6.1.16
01048h	10 GbE Switch	P0_Rx_Maxlen	Port 0 Receive Frame Max Length Register	Section 3.6.1.17
0104C-01060h	Reserved			
01064h	10 GbE Switch	P1_BLK_CNT	Port 1 FIFO Block Usage Count	Section 3.6.1.18
01068h	10 GbE Switch	P1_PORT_VLAN	Port 1 VLAN Register	Section 3.6.1.19
0106Ch	10 GbE Switch	P1_TX_PRI_MAP	Port 1 Tx Header Priority to switch Queue Mapping Reg	Section 3.6.1.20
01070h	10 GbE Switch	MAC1_SA_LO	MAC1 Source Address Low Register	Section 3.6.1.21
01074h	10 GbE Switch	MAC1_SA_HI	MAC1 Source Address High Register	Section 3.6.1.22
01078h	10 GbE Switch	P1_TS_CTL	Port 1 Time Sync Control Register	Section 3.6.1.23
0107Ch	10 GbE Switch	P1_TS_SEQ_LTYPE	Port 1 Time Sync LTYPE (and SEQ_ID_OFFSET)	Section 3.6.1.24
01080h	10 GbE Switch	P1_TS_VLAN	Port 1 Time Sync VLAN2 and VLAN2 Register	Section 3.6.1.25
01084h	10 GbE Switch	P1_TS_CTL_LTYPE2	Port 1 Time Sync Control and LTYPE2 Register	Section 3.6.1.26
01088h	10 GbE Switch	P1_TS_CTL2	Port 1 Time Sync Control 2 Register	Section 3.6.1.27
0108Ch	10 GbE Switch	P1_Control	Port 1 Control Register	Section 3.6.1.28
01090h	Reserved			
01094h	10 GbE Switch	P2_BLK_CNT	Port 2 FIFO Block Usage Count	Section 3.6.1.29

Table 3-2 10 Gigabit Ethernet Subsystem Complete Register Listing (Part 4 of 8)

Offset Address [1]	Module	Acronym	Register Name	Section
01098h	10 GbE Switch	P2_PORT_VLAN	Port 2 VLAN Register	Section 3.6.1.30
0109Ch	10 GbE Switch	P2_TX_PRI_MAP	Port 2 Tx Header Priority to switch Queue Mapping Register	Section 3.6.1.31
010A0h	10 GbE Switch	MAC2_SA_LO	MAC2 Source Address Low Register	Section 3.6.1.32
010A4h	10 GbE Switch	MAC2_SA_HI	MAC2 Source Address High Register	Section 3.6.1.33
010A8h	10 GbE Switch	P2_TS_CTL	Port 2 Time Sync Control Register	Section 3.6.1.34
010ACh	10 GbE Switch	P2_TS_SEQ_LTYPE	Port 2 Time Sync LTYPE (and SEQ_ID_OFFSET)	Section 3.6.1.35
010B0h	10 GbE Switch	P2_TS_VLAN	Port 2 Time Sync VLAN2 and VLAN2 Register	Section 3.6.1.36
010B4h	10 GbE Switch	P2_TS_CTL_LTYPE2	Port 2 Time Sync Control and LTYPE2 Register	Section 3.6.1.37
010B8h	10 GbE Switch	P2_TS_CTL2	Port 2 Time Sync Control 2 Register	Section 3.6.1.38
010BCh	10 GbE Switch	P2_Control	Port 2 Control Register	Section 3.6.1.39
010C0--013FFh	Reserved			
01400h	Port 1 MAC	MAC_IDVER	MAC Identification and Version Register	Section 3.6.2.1
01404h	Port 1 MAC	MAC_MAC_CTL	MAC Control Register	Section 3.6.2.3
01408h	Port 1 MAC	MAC_MAC_STATUS	MAC Status Register	Section 3.6.2.3
0140Ch	Port 1 MAC	MAC_SOFT_RESET	Soft Reset Register	Section 3.6.2.4
01410h	Port 1 MAC	MAC_RX_MAXLEN	RX Maximum Length Register	Section 3.6.2.5
01414h	Reserved			
0141Ch	Port 1 MAC	MAC_RX_PAUSE	Receive Pause Timer Register	Section 3.6.2.6
01420h	Port 1 MAC	MAC_TX_PAUSE	Transmit Pause Timer Register	Section 3.6.2.7
01424h	Port 1 MAC	MAC_EM_CTL	Emulation Control	Section 3.6.2.8
01428h	Reserved			
0142Ch	Port 1 MAC	MAC_Tx_Gap	Tx Inter-Packet Gap Register	Section 3.6.2.9
01430h-0143Ch	Reserved			
01440h	Port 2 MAC	MAC_IDVER	MAC Identification and Version Register	Section 3.6.2.1
01444h	Port 2 MAC	MAC_MAC_CTL	MAC Control Register	Section 3.6.2.3
01448h	Port 2 MAC	MAC_MAC_STATUS	MAC Status Register	Section 3.6.2.3
0144Ch	Port 2 MAC	MAC_SOFT_RESET	Soft Reset Register	Section 3.6.2.4
01450h	Port 2 MAC	MAC_RX_MAXLEN	RX Maximum Length Register	Section 3.6.2.5
01454h				
01458h	Port 2 MAC	MAC_RX_PAUSE	Receive Pause Timer Register	Section 3.6.2.6
0145Ch	Port 2 MAC	MAC_TX_PAUSE	Transmit Pause Timer Register	Section 3.6.2.7
01460h	Port 2 MAC	MAC_EM_CTL	Emulation Control	Section 3.6.2.8
01464h	Reserved			
01468h	Port 2 MAC	MAC_Tx_Gap	Tx Inter-Packet Gap Register	Section 3.6.2.9
0146Ch-015FC	Reserved			
01600h	Time Sync	CPTS_IDVER	Identification and Version Register	Section 3.6.4.1
01604h	Time Sync	CPTS_CTL	Time Sync Control Register	Section 3.6.4.2
01608h	Time Sync	CPTS_RFTCLK_SEL	Reference Clock Select Register	Section 3.6.4.3
0160Ch	Time Sync	TS_PUSH	Time Stamp Event Push Register	Section 3.6.4.4
01610h	Time Sync	TS_Load_Val	Time Stamp Load Value Register	Section 3.6.4.5
01614h	Time Sync	TS_Load_En	Time Stamp Load Enable Register	Section 3.6.4.6
01618h	Time Sync	TS_Comp_Val	Time Stamp Comparison Value Register	Section 3.6.4.7
0161Ch	Time Sync	TS_Comp_Length	Time Stamp Comparison Length Register	Section 3.6.4.8

Table 3-2 10 Gigabit Ethernet Subsystem Complete Register Listing (Part 5 of 8)

Offset Address [1]	Module	Acronym	Register Name	Section
01620h	Time Sync	INTSTAT_RAW	Interrupt Status Raw Register	Section 3.6.4.9
01624h	Time Sync	INTSTAT_MASKED	Interrupt Status Masked Register	Section 3.6.4.10
01628h	Time Sync	INT_ENABLE	Interrupt Enable Register	Section 3.6.4.11
0162Ch	Reserved			
01630h	Time Sync	EVENT_POP	Event Interrupt Pop Register	Section 3.6.4.12
01634h	Time Sync	EVENT_LOW	Lower 32-bits of the event value	Section 3.6.4.13
01638h	Time Sync	EVENT_MID	Mid 32-bits of the event value	
0163Ch	Time Sync	EVENT_HIGH	Upper 32-bits of the event value	Section 3.6.4.14
01640h-016FCh	Reserved			
01700h	ALE	ALE_IDVER	Address Lookup Engine ID/Version Register	Section 3.6.5.1
01704h	ALE			
01708h	ALE	ALE_CONTROL	Address Lookup Engine Control Register	Section 3.6.5.2
0170Ch	Reserved			
01710h	ALE	ALE_PRESCALE	Address Lookup Engine Prescale Register	Section 3.6.5.3
01714h	ALE	ALE_AGING_TIMER	ALE Aging Timer Register	
01718h	ALE	ALE_UNKNOWN_VLAN	Address Lookup Engine Unknown VLAN Register	Section 3.6.5.4
0171Ch	Reserved			
01720h	ALE	ALE_TBLCTL	Address Lookup Engine Table Control	Section 3.6.5.5
01724h-01730h	Reserved			
01734h	ALE	ALE_TBLW2	Address Lookup Engine Table Word 2 Register	Section 3.6.5.6
01738h	ALE	ALE_TBLW1	Address Lookup Engine Table Word 1 Register	Section 3.6.5.7
017Ch	ALE	ALE_TBLW0	Address Lookup Engine Table Word 0 Register	Section 3.6.5.8
01740h	ALE	ALE_PORTCTL0	Address Lookup Engine Port 0 Control Register	Section 3.6.5.9
01744h	ALE	ALE_PORTCTL1	Address Lookup Engine Port 1 Control Register	Section 3.6.5.10
01748h	ALE	ALE_PORTCTL2	Address Lookup Engine Port 2 Control Register	Section 3.6.5.11
0174Ch-017FFh	Reserved			
01800h	STATS0	RXGOODFRAMES	Total number of good frames received	Section 3.6.3.1
01804h	STATS0	RXBROADCASTFRAMES	Total number of good broadcast frames received	Section 3.6.3.2
01808h	STATS0	RXMULTICASTFRAMES	Total number of good multicast frames received	Section 3.6.3.3
0180Ch-01814h	STATS0	Reserved	Total number of pause frames received	Section 3.6.3.4
01818h	STATS0	RXOVERSIZEDFRAMES	Total number of CRC errors frames received	Section 3.6.3.5
0181Ch	Reserved			
01820h	STATS0	RXUNDERSIZEDFRAMES	Total number of oversized frames received	Section 3.6.3.7
01824h	STATS0	Reserved	Total number of jabber frames received	Section 3.6.3.8
01828h	STATS0	Overrun Type 4	Type 4 Overrun Stat	Section 3.6.3.11
0182Ch	STATS0	Overrun Type 5	Type 5Overrun Stat	Section 3.6.3.12
01830h	STATS0	RXOCTETS	Total number of received bytes in good frames	Section 3.6.3.11
01834h	STATS0	TXGOODFRAMES	Total number of good frames transmitted	Section 3.6.3.14
01838h	STATS0	TXBROADCASTFRAMES	Total number of good broadcast frames transmitted	Section 3.6.3.15
0183Ch	STATS0	TXMULTICASTFRAMES	Total number of good multicast frames transmitted	Section 3.6.3.16
01840h-01860	Reserved			
01864h	STATS0	TXOCTETS	Total number of octets transmitted	Section 3.6.3.26
01868h	STATS0	64OCTETFRAMES	Total number of 64 octet frames transmitted	Section 3.6.3.27

Table 3-2 10 Gigabit Ethernet Subsystem Complete Register Listing (Part 6 of 8)

Offset Address [1]	Module	Acronym	Register Name	Section
0186Ch	STATS0	65T127OCTETFRAMES	Total number of 65-127 octet frames transmitted	Section 3.6.3.28
01870h	STATS0	128T255OCTETFRAMES	Total number of 128-255 octet frames transmitted	Section 3.6.3.29
01874h	STATS0	256T511OCTETFRAMES	Total number of 256-511 octet frames transmitted	Section 3.6.3.30
01878h	STATS0	512T1023OCTETFRAMES	Total number of 512-1023 octet frames transmitted	Section 3.6.3.31
0187Ch	STATS0	1024TUPOCTETFRAMES	Total number of 1023-1518 octet frames transmitted	Section 3.6.3.32
01880h	STATS0	NETOCTETS	Total number of net octets	Section 3.6.3.33
01884h	STATS0	RXSOFOVERRUNS	Total number of receive FIFO or DMA start of frame overruns	Section 3.6.3.34
01888h	STATS0	RXMOFOVERRUNS	Total number of receive FIFO or DMA middle of frame overruns	Section 3.6.3.35
0188Ch	STATS0	RXDMAOVERRUNS	Total number of receive DMA start of frame and middle of frame overruns	Section 3.6.3.36
01890h-018FCh	Reserved			
01900h	STATS1	RXGOODFRAMES	Total number of good frames received	Section 3.6.3.1
01904h	STATS1	RXBROADCASTFRAMES	Total number of good broadcast frames received	Section 3.6.3.2
01908h	STATS1	RXMULTICASTFRAMES	Total number of good multicast frames received	Section 3.6.3.3
0190Ch	STATS1	RXPAUSEFRAMES	Total number of pause frames received	Section 3.6.3.4
01910h	STATS1	RXCRCERRORS	Total number of CRC errors frames received	Section 3.6.3.5
01914h	STATS1	RXALIGNCODEERRORS	Total number of alignment/code errors received	Section 3.6.3.6
01918h	STATS1	RXOVERSIZEDFRAMES	Total number of oversized frames received	Section 3.6.3.7
0191Ch	STATS1	RXJABBERFRAMES	Total number of jabber frames received	Section 3.6.3.8
01920h	STATS1	RXUNDERSIZEDFRAMES	Total number of undersized frames received	Section 3.6.3.9
01924h	STATS1	RXFRAGMENTS	Total number of fragment frames received	Section 3.6.3.10
01928h	STATS1	Overrun Type 4	Type 4 Overrun Stat	Section 3.6.3.11
0192Ch	STATS1	Overrun Type 5	Type 5Overrun Stat	Section 3.6.3.12
01930h	STATS1	RXOCTETS	Total number of received bytes in good frames	Section 3.6.3.11
01934h	STATS1	TXGOODFRAMES	Total number of good frames transmitted	Section 3.6.3.14
01938h	STATS1	TXBROADCASTFRAMES	Total number of good broadcast frames transmitted	Section 3.6.3.15
0193Ch	STATS1	TXMULTICASTFRAMES	Total number of good multicast frames transmitted	Section 3.6.3.16
01940h	STATS1	TXPAUSEFRAMES	Total number of pause frames transmitted	Section 3.6.3.17
01944h	STATS1	TXDEFERREDFRAMES	Total number of frames deferred	Section 3.6.3.18
01948h	STATS1	TXCOLLISIONFRAMES	Total number of collisions	Section 3.6.3.19
0194Ch	STATS1	TXSINGLECOLLFRAMES	Total number of single collision transmit frames	Section 3.6.3.20
01950h	STATS1	TXMULTCOLLFRAMES	Total number of multiple collision transmit frames	Section 3.6.3.21
01954h	STATS1	TXEXCESSIVECOLLISIONS	Total number of transmit frames aborted due to excessive collisions	Section 3.6.3.22
01958h	STATS1	TXLATECOLLISIONS	Total number of late collisions	Section 3.6.3.23
0195Ch	STATS1	RxIPGError	Total number of transmit underrun errors	Section 3.6.3.24
01960h	STATS1	TXCARRIERSENSEERRORS	Total number of carrier sense errors	Section 3.6.3.25
01964h	STATS1	TXOCTETS	Total number of octets transmitted	Section 3.6.3.26
01968h	STATS1	64OCTETFRAMES	Total number of 64 octet frames transmitted	Section 3.6.3.27
0196Ch	STATS1	65T127OCTETFRAMES	Total number of 65-127 octet frames transmitted	Section 3.6.3.28
01970h	STATS1	128T255OCTETFRAMES	Total number of 128-255 octet frames transmitted	Section 3.6.3.29
01974h	STATS1	256T511OCTETFRAMES	Total number of 256-511 octet frames transmitted	Section 3.6.3.30
01978h	STATS1	512T1023OCTETFRAMES	Total number of 512-1023 octet frames transmitted	Section 3.6.3.31
0197Ch	STATS1	1024TUPOCTETFRAMES	Total number of 1023-1518 octet frames transmitted	Section 3.6.3.32

Table 3-2 10 Gigabit Ethernet Subsystem Complete Register Listing (Part 7 of 8)

Offset Address [1]	Module	Acronym	Register Name	Section
01980h	STATS1	NETOCTETS	Total number of net octets	Section 3.6.3.33
01984h	STATS1	RXSOFOVERRUNS	Total number of receive FIFO or DMA start of frame overruns	Section 3.6.3.34
01988h	STATS1	RXMOFOVERRUNS	Total number of receive FIFO or DMA middle of frame overruns	Section 3.6.3.35
0198Ch	STATS1	RXDMAOVERRUNS	Total number of receive DMA start of frame and middle of frame overruns	Section 3.6.3.36
01990h-019FCh	Reserved			
01A00h	STATS2	RXGOODFRAMES	Total number of good frames received	Section 3.6.3.1
01A04h	STATS2	RXBROADCASTFRAMES	Total number of good broadcast frames received	Section 3.6.3.2
01A08h	STATS2	RXMULTICASTFRAMES	Total number of good multicast frames received	Section 3.6.3.3
01A0Ch	STATS2	RXPAUSEFRAMES	Total number of pause frames received	Section 3.6.3.4
01A10h	STATS2	RXCRCERRORS	Total number of CRC errors frames received	Section 3.6.3.5
01A14h	STATS2	RXALIGNCODEERRORS	Total number of alignment/code errors received	Section 3.6.3.6
01A18h	STATS2	RXOVERSIZEDFRAMES	Total number of oversized frames received	Section 3.6.3.7
01A1Ch	STATS2	RXJABBERFRAMES	Total number of jabber frames received	Section 3.6.3.8
01A20h	STATS2	RXUNDERSIZEDFRAMES	Total number of undersized frames received	Section 3.6.3.9
01A24h	STATS2	RXFRAGMENTS	Total number of fragment frames received	Section 3.6.3.10
01A28h	STATS2	Overrun Type 4	Type 4 Overrun Stat	Section 3.6.3.11
01A2Ch	STATS2	Overrun Type 5	Type 5 Overrun Stat	Section 3.6.3.12
01A30h	STATS2	RXOCTETS	Total number of received bytes in good frames	Section 3.6.3.13
01A34h	STATS2	TXGOODFRAMES	Total number of good frames transmitted	Section 3.6.3.14
01A38h	STATS2	TXBROADCASTFRAMES	Total number of good broadcast frames transmitted	Section 3.6.3.15
01A3Ch	STATS2	TXMULTICASTFRAMES	Total number of good multicast frames transmitted	Section 3.6.3.16
01A40h	STATS2	TXPAUSEFRAMES	Total number of pause frames transmitted	Section 3.6.3.17
01A44h	STATS2	TXDEFERREDFRAMES	Total number of frames deferred	Section 3.6.3.18
01A48h	STATS2	TXCOLLISIONFRAMES	Total number of collisions	Section 3.6.3.19
01A4Ch	STATS2	TXSINGLECOLLFRAMES	Total number of single collision transmit frames	Section 3.6.3.20
01A50h	STATS2	TXMULTCOLLFRAMES	Total number of multiple collision transmit frames	Section 3.6.3.21
01A54h	STATS2	TXEXCESSIVECOLLISIONS	Total number of transmit frames aborted due to excessive collisions	Section 3.6.3.22
01A58h	STATS2	TXLATECOLLISIONS	Total number of late collisions	Section 3.6.3.23
01A5Ch	STATS2	RxIPGError	Total number of transmit underrun errors	Section 3.6.3.24
01A60h	STATS2	TXCARRIERSENSEERRORS	Total number of carrier sense errors	Section 3.6.3.25
01A64h	STATS2	TXOCTETS	Total number of octets transmitted	Section 3.6.3.26
01A68h	STATS2	64OCTETFRAMES	Total number of 64 octet frames transmitted	Section 3.6.3.27
01A6Ch	STATS2	65T127OCTETFRAMES	Total number of 65-127 octet frames transmitted	Section 3.6.3.28
01A70h	STATS2	128T255OCTETFRAMES	Total number of 128-255 octet frames transmitted	Section 3.6.3.29
01A74h	STATS2	256T511OCTETFRAMES	Total number of 256-511 octet frames transmitted	Section 3.6.3.30
01A78h	STATS2	512T1023OCTETFRAMES	Total number of 512-1023 octet frames transmitted	Section 3.6.3.31
01A7Ch	STATS2	1024TUPOCTETFRAMES	Total number of 1023-1518 octet frames transmitted	Section 3.6.3.32
01A80h	STATS2	NETOCTETS	Total number of net octets	Section 3.6.3.33
01A84h	STATS2	RXSOFOVERRUNS	Total number of receive FIFO or DMA start of frame overruns	Section 3.6.3.34
01A88h	STATS2	RXMOFOVERRUNS	Total number of receive FIFO or DMA middle of frame overruns	Section 3.6.3.35
01A8Ch	STATS2	RXDMAOVERRUNS	Total number of receive DMA start of frame and middle of frame overruns	Section 3.6.3.36

Table 3-2 10 Gigabit Ethernet Subsystem Complete Register Listing (Part 8 of 8)

Offset Address [1]	Module	Acronym	Register Name	Section
01A90h – 1FFFFh	Reserved			
20000h – 23FFFh	MACSEC1_ING	XFORMREC	Transform records area	Section 3.7.1
24000h – 26FFFh	MACSEC1_ING	SAMPARMS	SA match parameter sets	Section 3.7.2
27000h – 277FFh	MACSEC1_ING	FLOWCTRLWRDS	Flow control words for frames that matched an SA parameter set	Section 3.7.3
27800h – 2C7FFh	Reserved			
28000h – 2C7FFh	MACSEC1_ING	SECURITYSTATS	Security statistics counters of 40 bits each	Section 3.7.4
2C800h – 2CFFFh	MACSEC1_ING	SECOUNTERDBG	Security statistics counter control and debug	Section 3.7.5
2E000h – 2EFFFh	MACSEC1_ING	CCPARAM	Consistency check parameter sets control bits and debug status	Section 3.7.6
2F100h – 2F123h	MACSEC1_ING	VLANCHECKCTRL	9 MTU check control words for VLAN packets and non-VLAN pkts	Section 3.7.7
2F124h – 2F3FFh	MACSEC1_ING	PKTENGINESECFAIL	Security fail control masks and debug registers for Packet Engine	Section 3.7.8
2F400h – 2F7FFh	MACSEC1_ING	PKTENGINEREGS	Access space for Packet Engine	Section 3.7.9
2F800h – 2F81Fh	Reserved			
2FC00h – 2FFFFh	Reserved			
30000h-3FFFFh	MACSEC1_EGR		Egress registers for MACSEC 1	Section 3.7
40000h – 43FFFh	MACSEC2_ING	XFORMREC	Transform records area	Section 3.7.1
44000h – 46FFFh	MACSEC2_ING	SAMPARMS	SA match parameter sets	Section 3.7.2
47000h – 477FFh	MACSEC2_ING	FLOWCTRLWRDS	Flow control words for frames that matched an SA parameter set	Section 3.7.3
27800h – 2C7FFh	Reserved			
48000h – 4C7FFh	MACSEC2_ING	SECURITYSTATS	Security statistics counters of 40 bits each	Section 3.7.4
4C800h – 4CFFFh	MACSEC2_ING	SECOUNTERDBG	Security statistics counter control and debug	Section 3.7.5
4E000h – 4EFFFh	MACSEC2_ING	CCPARAM	Consistency check parameter sets control bits and debug status	Section 3.7.6
4F100h – 4F123h	MACSEC2_ING	VLANCHECKCTRL	9 MTU check control words for VLAN packets and non-VLAN pkts	Section 3.7.7
4F124h – 4F3FFh	MACSEC2_ING	PKTENGINESECFAIL	Security fail control masks and debug registers for Packet Engine	Section 3.7.8
4F400h – 4F7FFh	MACSEC2_ING	PKTENGINEREGS	Access space for Packet Engine	Section 3.7.9
4F800h – 4F81Fh	Reserved			
4FC00h – 4FFFFh	Reserved			
50000h-9FFFFh	MACSEC2_EGR		Egress registers for MACSEC 2	Section 3.7
A0000h	10GbE Subsystem	IDVER	Identification and Version Register	Section 3.8.1
A0004h-A000Ch	Reserved			
A0010h	10GbE Subsystem	CPPI_TS	CPPI Timestamp Register	Section 3.8.2
A0014h	10GbE Subsystem	CPPI_TS_EN	CPPI Timestamp Enable Register	Section 3.8.3
A0018h	10GbE Subsystem	CPPI_TS_DIV	CPPI Timestamp Divider Register	Section 3.8.4
A001Ch-A05FFh	Reserved			
A1000h-AEFFF	PKTDMA	PKTDMA Regs	See Multicore Navigator for Registers	
AF000h-AF3FFh	Interrupt Distributor	INTD Regs	TBD	
AF400h-FFFFFh	Reserved			
End of Table 3-2				

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.2 10 Gigabit Ethernet (10GbE) Switch Submodule

The following section describes the registers for the Ethernet switch subsystem.

Table 3-3 lists the registers in the Ethernet switch subsystem and the corresponding offset address for each register.

Table 3-3 Ethernet switch subsystem module

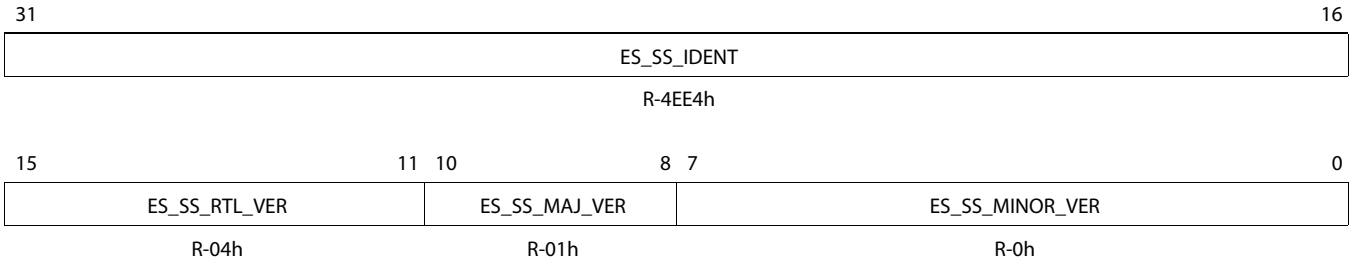
Offset Address [1]	Acronym	Register Name	Section
00000h	ES_SS_IDVER	10Gigabit Ethernet switch submodule Identification and Version Register	Section 3.2.1
00004h	SyncE_Count	Synchronous Ethernet Count Register	
00008h	SyncE_Mux	Synchronous Ethernet Mux Register	
0000Ch	Control	Sub-Module Control Register	
End of Table 3-3			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.2.1 10Gigabit Ethernet Switch Submodule Identification and Version Register (ES_SS_IDVER)

The Ethernet switch subsystem identification and version register is shown in Figure 3-1 and described in Table 3-4.

Figure 3-1 Ethernet switch subsystem Identification and Version Register (ES_SS_IDVER)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-4 Ethernet Switch Subsystem Identification and Version Register (ES_SS_IDVER) Field Descriptions

Bits	Field	Description
31-16	ES_SS_IDENT	10Gigabit Ethernet switch submodule Identification Value
15-11	ES_SS_RTL_VER	10Gigabit Ethernet switch subsystem RTL Version Value
10-8	ES_SS_MAJ_VER	10Gigabit Ethernet switch subsystem Major Version Value
7-0	ES_SS_MINOR_VER	10Gigabit Ethernet switch subsystem Minor Version Value
End of Table 3-4		

3.2.2 Synchronous Ethernet Count Register (SyncE Count)

Figure 3-2 Synchronous Ethernet Count Register (SyncE Count)

31	0
synce_cnt	
RW-0h	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-5 Synchronous Ethernet Count (SyncE)

Bits	Field	Description
31-0	synce_cnt	Sync E Count Value - This value determines the toggle rate of the TS_SYNCE output. When this value is zero the TS_SYNCE output is disabled (low). When this value is non-zero, the TS_SYNCE output toggles each time the synce count value is reached. If this value is to be changed to another non-zero value then it should be written with a zero value before writing the new non-zero value.
End of Table 3-5		

3.2.3 Synchronous Ethernet Mux Register (SyncE Mux)

Figure 3-3 Synchronous Ethernet Mux Register (SyncE Mux)

31	2	1	0
Reserved		synce_mux	
R-0h		RW-0h	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-6 Synchronous Ethernet Mux Register (SyncE Mux)

Bits	Field	Description
31-2	Reserved	
1-0	synce_mux	Sync E Select Value – This value selects the receive clock used to clock the TS_SYNCE counter and output. 00 – Select RXBCLK[0] 01 – Select RXBCLK[1] 1X – Reserved
End of Table 3-6		

3.2.4 Submodule Control Register (Control)

Figure 3-4 Submodule Control Register (Control)

31	18	17	16	15	10
Reserved		ext_en_sl2	ext_en_sl1	Reserved	
R-0h		RW-0h	RW-0h	R-0h	

9	8	7	2	1	0
ext_en_xgmii2	ext_en_xgmii1	Reserved		xgmii2_mode	xgmii1_mode
RW-0h	RW-0h	R-0h		RW-0h	RW-0h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-7 Submodule Control Register (Control)

Bits	Field	Description
31-18	Reserved	
17	ext_en_sl2	External Enable Port2 MAC (write only) – 0 – xgmii2_en = xgmii_en from Port 2 MAC MacControl reg gmii2_en = gmii_en from Port2 MAC MacControl reg 1 – xgmii2_en = SERDES lane 1 link_out[4:3] = 2'b11 gmii2_en = SERDES lane 1 link_out[6:5] = 2'b11
16	ext_en_sl1	External Enable Port1 MAC (write only) – 0 – xgmii1_en = xgmii_en from Port 1MAC MacControl reg gmii1_en = gmii_en from Port1 MAC MacControl reg 1 – xgmii1_en = SERDES lane 1 link_out[4:3] = 2'b11 gmii1_en = SERDES lane 1 link_out[6:5] = 2'b11
15-10	Reserved	
9	ext_en_xgmii2	External Enable XGMII2 (write only) – 0 – xgmii2_mode = xgmii2_mode from bit 1 in this Control reg 1 – xgmii2_mode = SERDES lane 1 link_out[4:3] = 2'b11
8	ext_en_xgmii1	External Enable XGMII1 (write only) – 0 – xgmii1_mode = xgmii1_mode from bit 0 in this Control reg 1 – xgmii1_mode = SERDES lane 0 link_out[4:3] = 2'b11
7-2	Reserved	
1	xgmii2_mode	XGMII2 Mode – 0 – xgmii2_mode is selected from this register bit 1 – xgmii2_mode_sel = SERDES lane 1 link_out[4:3] = 2'b11
0	xgmii1_mode	XGMII1 Mode – 0 – xgmii1_mode is selected from this register bit 1 – xgmii1_mode_sel = SERDES lane 1 link_out[4:3] = 2'b11
End of Table 3-7		

3.3 Serial Gigabit Media Independent Interface (SGMII) module

This section describes the registers available in the Ethernet switch submodule SGMII module. There are two SGMII modules in the Ethernet switch submodule, each with its own set of identical registers. The register address offsets listed in Table 3-8 are relative to the SGMII module. To determine the address offset of each SGMII module, please see Table 3-1. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2. For information regarding the SerDes SGMII registers, please see "MACSEC Module" on page 3-97.

- Section 3.3.1 "SGMII Identification and Version Register (SGMII_IDVER)" on page 3-14
- Section 3.3.2 "Software Reset Register (SOFT_RESET)" on page 3-14
- Section 3.3.3 "SGMII Control Register (SGMII_CONTROL)" on page 3-15
- Section 3.3.4 "Status Register (STATUS)" on page 3-15
- Section 3.3.5 "Advertised Ability Register (MR_ADV_ABILITY)" on page 3-16
- Section 3.3.6 "Link Partner Advertised Ability Register (MR_LP_ADV_ABILITY)" on page 3-17

Table 3-8 lists the registers in the SGMII module and the corresponding address offset for each register.

Table 3-8 SGMII Registers

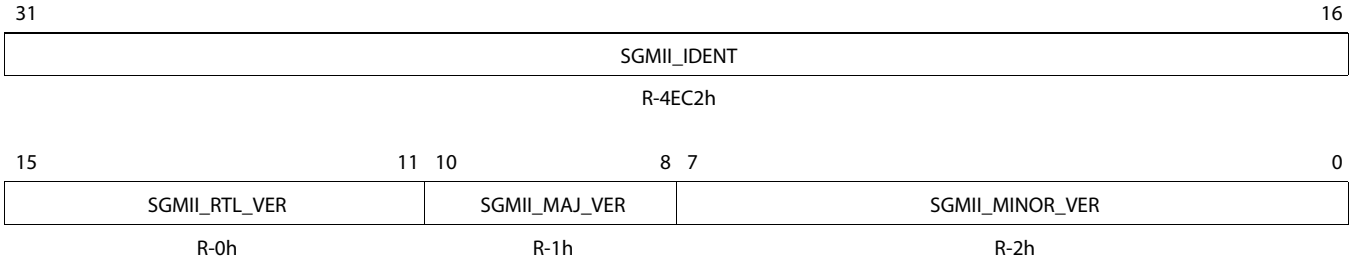
Offset Address[1]	Acronym	Register Name	Section
00h	SGMII_IDVER	Identification and Version Register	Section 3.3.1
04h	SOFT_RESET	Soft Reset Register	Section 3.3.2
08h-0Ch	Reserved	Reserved	Reserved
10h	SGMII_CONTROL	Control Register	Section 3.3.3
14h	STATUS	Status Register (read only)	Section 3.3.4
18h	MR_ADV_ABILITY	Advertised Ability Register	Section 3.3.5
1Ch	Reserved	Reserved	Reserved
20h	MR_LP_ADV_ABILITY	Link Partner Advertised Ability (read only)	Section 3.3.6
24h-7Fh	Reserved	Reserved	Reserved
End of Table 3-8			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.3.1 SGMII Identification and Version Register (SGMII_IDVER)

The SGMII identification and version register is shown in Figure 3-5 and described in Table 3-9.

Figure 3-5 SGMII Identification and Version Register (SGMII_IDVER)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

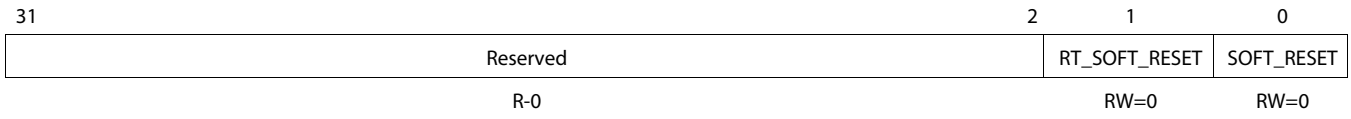
Table 3-9 SGMII Identification and Version Register (SGMII_IDVER) Field Descriptions

Bits	Field	Description
31-16	SGMII_IDENT	SGMII Identification Value
15-11	SGMII_RTL_VER	SGMII RTL Version Value
10-8	SGMII_MAJOR_VER	SGMII Major Version Value
7-0	SGMII_MINOR_VER	SGMII Minor Version Value
End of Table 3-9		

3.3.2 Software Reset Register (SOFT_RESET)

The software reset register is shown in Figure 3-6 and described in Table 3-10.

Figure 3-6 Software Reset Register (SOFT_RESET)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-10 Software Reset Register (SOFT_RESET) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1	RT_SOFT_RESET	Receive and Transmit Software Reset. Writing a one to this bit causes the CPSGMII transmit and receive logic to be in the reset condition The reset condition is removed when a zero is written to this bit. This bit is intended to be used when changing between loopback mode and normal mode of operation.
0	SOFT_RESET	Software Reset. Writing a one to this bit causes the CPSGMII logic to be reset. Software reset occurs immediately. This bit reads as a zero.
End of Table 3-10		

3.3.3 SGMII Control Register (SGMII_CONTROL)

The SGMII control register is shown in Figure 3-7 and described in Table 3-11.

Figure 3-7 SGMII Control Register (SGMII_CONTROL)

31 6	5	4	3 2	1	0
Reserved	MASTER	LOOPBACK	Reserved	MR_AN_RESTART	MR_AN_ENABLE
R-0	RW=0	RW=0	R=0	RW=0	RW=0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-11 SGMII Control Register (SGMII_CONTROL) Field Descriptions

Bits	Field	Description
31-6	Reserved	Reserved
5	MASTER	Master Mode. 0 = Slave Mode 1 = Master mode Set to one for one side of a direct connection. When this bit is set, the control logic uses the MR_ADV_ABILITY register to determine speed and duplexity instead of the MR_LP_ADV_ABILITY register. Master mode allows a CPSGMII direct connection with auto-negotiation or with a forced link.
4	LOOPBACK	Loopback mode. 0 = Not in internal loopback mode 1 = Internal loopback mode. The transmit clock (TX_CLK) is used for transmit and receive.
3-2	Reserved	Reserved
1	MR_AN_RESTART	Auto-Negotiation Restart. Writing a one and then a zero to this bit causes the auto-negotiation process to be restarted.
0	MR_AN_ENABLE	Auto-Negotiation Enable. Writing a one to this bit enables the auto-negotiation process.
End of Table 3-11		

3.3.4 Status Register (STATUS)

The SGMII status register is shown in Figure 3-8 and described in Table 3-12.

Figure 3-8 Status Register (STATUS)

31 5	4	3	2	1	0
Reserved	LOCK	Reserved	MR_AN_COMPLETE	AN_ERROR	LINK
R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-12 Status Register (STATUS) Field Descriptions (Part 1 of 2)

Bits	Field	Description
31-5	Reserved	Reserved
4	LOCK	Lock. This is the LOCK input pin. Indicates that the SerDes PLL is locked.
3	Reserved	Reserved
2	MR_AN_COMPLETE	Auto-negotiation complete. This value is not valid until the LOCK status bit is asserted. 0 = auto-negotiation is not complete. 1 = auto-negotiation is completed.

Table 3-12 Status Register (STATUS) Field Descriptions (Part 2 of 2)

Bits	Field	Description
1	AN_ERROR	Auto-negotiation error. For SGMII mode, an auto-negotiation error occurs when halfduplex gigabit is commanded. This value is not valid until the LOCK status bit is asserted. 0 = no auto-negotiation error. 1 = auto-negotiation error.
0	LINK	Link indicator. This value is not valid until the LOCK status bit is asserted. 0 = Link is not up. 1 = Link is up.
End of Table 3-12		

3.3.5 Advertised Ability Register (MR_ADV_ABILITY)

The advertised ability register is shown in Figure 3-9 and described in Table 3-13.

Figure 3-9 Advertised Ability Register (MR_ADV_ABILITY)

31	16	15	0
Reserved		MR_ADV_ABILITY	
R-0		RW=0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-13 Advertised Ability Register (MR_ADV_ABILITY) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	MR_ADV_ABILITY	Advertised Ability. This value corresponds to the TX_CONFIG_REG[15-0] register value in the SGMII specification.
End of Table 3-13		

The following tables show the **MR_ADV_ABILITY** and **MR_LP_ADV_ABILITY** register values for SGMII mode.

3.3.5.1 SGMII MODE

The advertised ability and link partner advertised ability settings for SGMII mode are shown in Table 3-14.

Table 3-14 Advertised Ability and Link Partner Advertised Ability for SGMII Mode (Part 1 of 2)

TX_CONFIG_REG[15-0]	MAC	PHY
15	Link. 0 = Link is down 1 = Link is up	0
14	auto-negotiation acknowledge	1
13	0	0
12	Duplex mode . 0 = Half-duplex mode 1 = fullduplex mode	0
11-10	Speed. 10 = gig 01 = 100 mbit 00 = 10 mbit	00

Table 3-14 Advertised Ability and Link Partner Advertised Ability for SGMII Mode (Part 2 of 2)

TX_CONFIG_REG[15-0]	MAC	PHY
9-1	0	0
0	1	1
End of Table 3-14		

3.3.6 Link Partner Advertised Ability Register (MR_LP_ADV_ABILITY)

The link partner advertised ability register is shown in Figure 3-10 and described in Table 3-15.

Figure 3-10 Link Partner Advertised Ability Register (MR_LP_ADV_ABILITY)

31	16	15	0
Reserved		MR_LP_ADV_ABILITY	
R-0		R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-15 Link Partner Advertised Ability Register (MR_LP_ADV_ABILITY) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	MR_LP_ADV_ABILITY	Link Partner Advertised Ability. Readable when auto-negotiation is complete. This value corresponds to the TX_CFG[15-0] register value in the SGMII specification.
End of Table 3-15		

3.4 Management Data Input/Output (MDIO) module

This section describes the registers available in the Ethernet switch subsystem MDIO module. The register offset addresses listed in Table 3-16 are relative to the MDIO module offset address. To determine the offset address of the MDIO module, please see Table 3-1. For convenience, a complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-16 lists the registers in the Ethernet switch subsystem and the corresponding address offset for each register.

Table 3-16 MDIO Registers (Part 1 of 2)

Offset Address[1]	Acronym	Register Name	Section
00h	MDIO_VERSION	MDIO Version Register	Section 3.4.1
04h	MDIO_CONTROL	MDIO Control Register	Section 3.4.2
08h	ALIVE	PHY Alive Status Register	Section 3.4.3
0Ch	LINK	PHY Link Status Register	Section 3.4.4
10h	LINKINTRAW	MDIO Link Status Change Interrupt (Unmaksed) Register	Section 3.4.5
14h	LINKINTMASKED	MDIO Link Status Change Interrupt (Masked) Register	Section 3.4.6
18h–1Ch	Reserved	Reserved	Reserved
20h	USERINTRAW	MDIO User Command Complete Interrupt (Unmasked) Register	Section 3.4.7
24h	USERINTMASKED	MDIO User Command Complete Interrupt (Masked) Register	Section 3.4.8
28h	USERINTMASKSET	MDIO User Interrupt Mask Set Register	Section 3.4.9
2ch	USERINTMASKCLEAR	MDIO User Interrupt Mask Clear Register	Section 3.4.10
30h–7Ch	Reserved	Reserved	Reserved
80h	USERACCESS0	MDIO User Access Register 0	Section 3.4.11
84h	USERPHYSEL0	MDIO User PHY Select Register 0	Section 3.4.12

Table 3-16 MDIO Registers (Part 2 of 2)

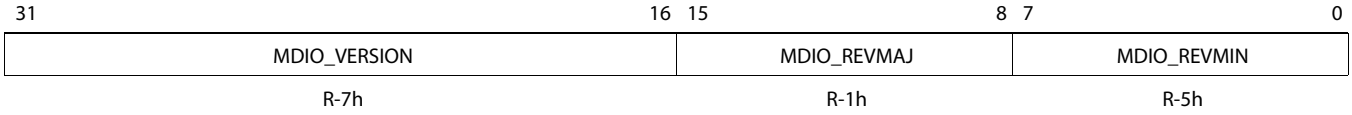
Offset Address[1]	Acronym	Register Name	Section
88h	USERACCESS1	MDIO User Access Register 1	Section 3.4.13
8Ch	USERPHYSEL1	MDIO User PHY Select Register 1	Section 3.4.14
90h–FFh	Reserved	Reserved	Reserved
End of Table 3-16			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.4.1 MDIO Version Register (MDIO_VERSION)

The MDIO version register is shown in Figure 3-11 and described in Table 3-17.

Figure 3-11 MDIO Version Register (MDIO_VERSION)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

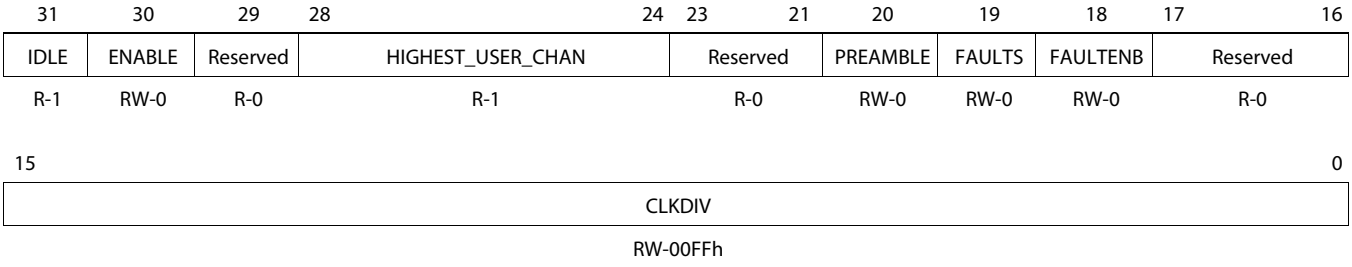
Table 3-17 MDIO Version Register (MDIO _VERSION) Field Descriptions

Bits	Field	Description
31-15	MDIO_MODID	Identifies the type of peripheral.
15-8	MDIO_REVMAJ	Management Interface module major revision value.
7-0	MDIO_REVMIN	Management Interface module minor revision value.
End of Table 3-17		

3.4.2 MDIO Control Register (MDIO_CONTROL)

The MDIO control register is shown in Figure 3-12 and described in Table 3-18.

Figure 3-12 MDIO Control Register (MDIO_CONTROL)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-18 MDIO Control Register (MDIO_CONTROL) Field Descriptions

Bits	Field	Description
31	IDLE	MDIO state machine IDLE status bit. 0 = State machine is not in the idle state. 1 = State machine is in the idle state.
30	ENABLE	Enable control. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. 0 =Disables the MDIO state machine. 1 = Enables the MDIO state machine.
27	Reserved	Reserved
28-24	HIGHEST_USER_CHAN	Highest user channel. This field specifies the highest user access channel that is available in the module and is currently set to 1. This implies that USERACCESS1 is the highest available user access channel.
23-21	Reserved	Reserved
20	PREAMBLE	Preamble disable. 0 = Standard MDIO preamble is used. 1 = Disables this device from sending MDIO frame preambles.
19	FAULT	Fault indicator.This bit is set to 1 if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1 to it clears this bit. 0 = No failure. 1 = physical layer fault. The MDIO state machine is reset.
18	FAULTENB	Fault detect enable. This bit has to be set to 1 to enable the physical layer fault detection. 0 = Disables the physical layer fault detection. 1 = Enables the physical layer fault detection.
17-16	Reserved	Reserved
15-0	CLKDIV	Clock Divider. This field specifies the division ratio between the CBUS peripheral clock and the frequency of MDCLK. MDCLK is disabled when CLKDIV is set to 0. MDCLK frequency = peripheral clock frequency/(CLKDIV+1).
End of Table 3-18		

3.4.3 PHY Alive Status Register (ALIVE)

The PHY alive status register is shown in Figure 3-13 and described in Table 3-19.

Figure 3-13 PHY Alive Status Register (ALIVE)

31	0
ALIVE	
RW-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

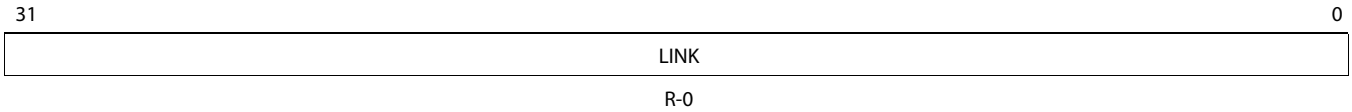
Table 3-19 PHY Alive Status Register

Bits	Field	Description
31-0	ALIVE	MDIO Alive. Each of the 32 bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are only meant to be used to give an indication of the presence or not of a PHY with the corresponding address. Writing a 1 to any bit will clear it, writing a 0 has no effect. 0 = The PHY fails to acknowledge the access 1 = The most recent access to the PHY with an address corresponding to the register bit number was acknowledged by the PHY
End of Table 3-19		

3.4.4 PHY Link Status Register (LINK)

The PHY link status register is shown in Figure 3-14 and described in Table 3-20.

Figure 3-14 PHY Link Status Register (LINK)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

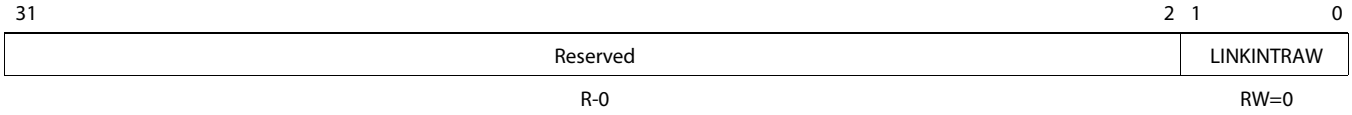
Table 3-20 PHY Link Status Register (LINK) Field Descriptions

Bits	Field	Description
31-0	LINK	MDIO Link state. This register is updated after a read of the Generic Status Register of a PHY. The bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is reset if the PHY indicates it does not have link or fails to acknowledge the read transaction. Writes to the register have no effect. In addition, the status of the two PHYs specified in the MDIOUSERPHYSEL registers can be determined using the MLINK input pins. This is determined by the LINKSEL bit in the MDIOUSERPHYSEL register. 0 = The PHY indicates that it does not have a link or fails to acknowledge the read transaction 1 = The PHY with the corresponding address has a link and the PHY acknowledges the read transaction
End of Table 3-20		

3.4.5 MDIO Link Status Change Interrupt (Unmasked) Register (LINKINTRAW)

The PHY link status change interrupt (unmasked) register is shown in Figure 3-15 and described in Table 3-21.

Figure 3-15 MDIO Link Status Change Interrupt (Unmasked) Register (LINKINTRAW)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

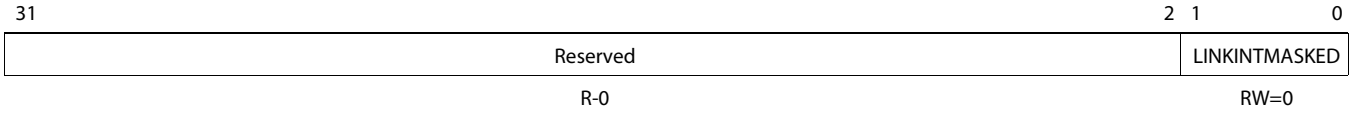
Table 3-21 MDIO Link Status Change Interrupt (Unmasked) Register (LINKINTRAW) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	LINKINTRAW	MDIO link change event, raw value. When asserted 1, a bit indicates that there was an MDIO link change event (i.e. change in the LINK register) corresponding to the PHY address in the USERPHYSEL register. LINKINTRAW[0] and LINKINTRAW[1] correspond to USERPHYSEL0 and USERPHYSEL1, respectively. Writing a 1 will clear the event and writing 0 has no effect.
End of Table 3-21		

3.4.6 MDIO Link Status Change Interrupt (Masked) Register (LINKINTMASKED)

The MDIO link status change interrupt (masked) register is shown in Figure 3-16 and described in Table 3-22.

Figure 3-16 MDIO Link Status Change Interrupt (Masked) Register (LINKINTMASKED)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

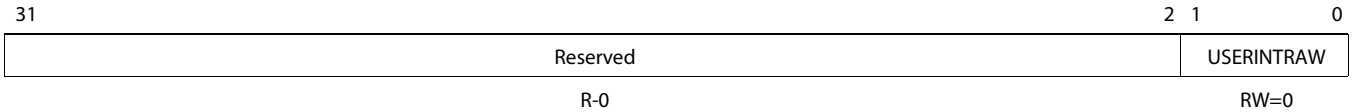
Table 3-22 MDIO Link Status Change Interrupt (Masked) Register (LINKINTMASKED) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	LINKINTMASKED	MDIO link change interrupt, masked value. When asserted 1, a bit indicates that there was an MDIO link change event (i.e. change in the LINK register) corresponding to the PHY address in the USERPHYSEL register and the corresponding LINKINTENB bit was set. LINKINTMASKED[0] and LINKINTMASKED[1] correspond to USERPHYSEL0 and USERPHYSEL0, respectively. Writing a 1 will clear the interrupt and writing 0 has no effect.
End of Table 3-22		

3.4.7 MDIO User Command Complete Interrupt (Unmasked) Register (USERINTRAW)

The MDIO user command complete interrupt (unmasked) register is shown in Figure 3-17 and described in Table 3-23.

Figure 3-17 MDIO User Command Complete Interrupt (Unmasked) Register (USERINTRAW)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

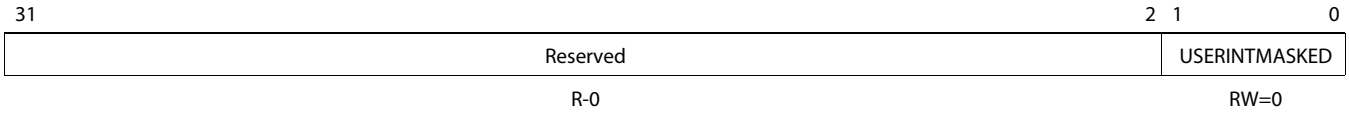
Table 3-23 MDIO User Command Complete Interrupt (Unmasked) Register (USERINTRAW) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	USERINTRAW	MDIO User command complete event bits. When asserted to 1, a bit indicates that the previously scheduled PHY read or write command using that particular USERACCESS register has completed. Writing a 1 will clear the event. Writing 0 has no effect.
End of Table 3-23		

3.4.8 MDIO User Command Complete Interrupt (Masked) Register (USERINTMASKED)

The MDIO user command complete interrupt (masked) register is shown in Figure 3-18 and described in Table 3-24.

Figure 3-18 MDIO User Command Complete Interrupt (Masked) Register (USERINTMASKED)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

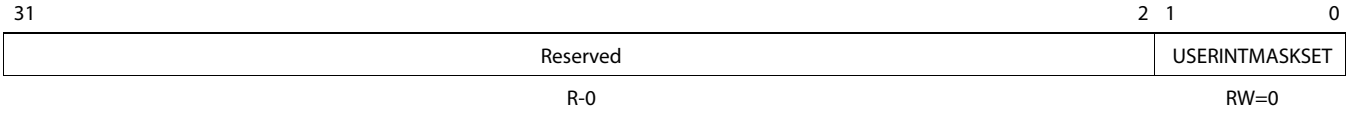
Table 3-24 MDIO User Command Complete Interrupt (Masked) Register (USERINTMASKED) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	USERINTMASKED	Masked value of MDIO user command complete interrupt. When asserted to 1, a bit indicates that the previously scheduled PHY read or write command using that particular USERACCESS register has completed and the corresponding USERINTMASKSET bit is set to 1. Writing a 1 will clear the interrupt. Writing a 0 has no effect.
End of Table 3-24		

3.4.9 MDIO User Command Complete Interrupt Mask Set Register (USERINTMASKSET)

The MDIO user command complete interrupt mask set register is shown in Figure 3-19 and described in Table 3-25.

Figure 3-19 MDIO User Command Complete Interrupt Mask Set Register (USERINTMASKSET)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

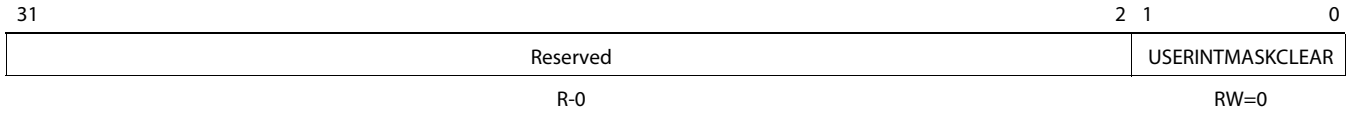
Table 3-25 MDIO User Command Complete Interrupt Mask Set Register (USERINTMASKSET) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	USERINTMASKSET	MDIO user interrupt mask set for USERINTMASKED[1-0], respectively. Setting a bit to 1 will enable MDIO user command complete interrupts for that particular USERACCESS register. MDIO user interrupt for a particular USERACCESS register is disabled if the corresponding bit is 0. Writing a 0 to this register has no effect.
End of Table 3-25		

3.4.10 MDIO User Command Complete Interrupt Mask Clear Register (USERINTMASKCLEAR)

The MDIO user command complete interrupt mask clear register is shown in Figure 3-20 and described in Table 3-26.

Figure 3-20 MDIO User Command Complete Interrupt Mask Clear Register (USERINTMASKCLEAR)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

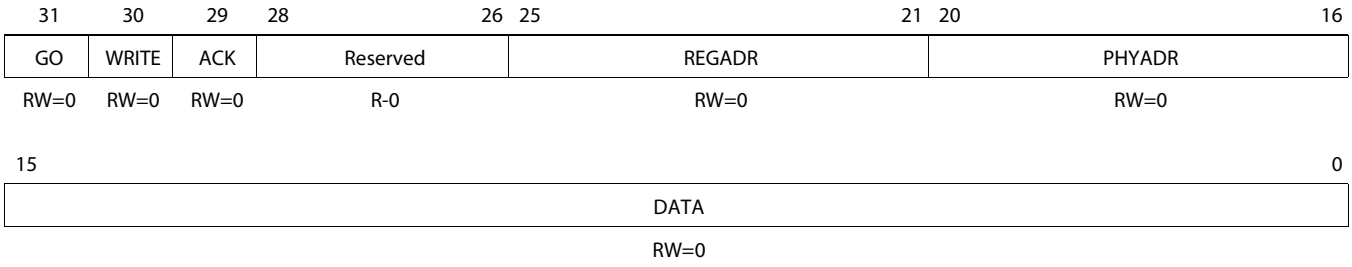
Table 3-26 MDIO User Command Complete Interrupt Mask Clear Register (USERINTMASKCLEAR) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1-0	USERINTMASKCLEAR	MDIO user command complete interrupt mask clear for USERINTMASKED[1-0], respectively. Setting a bit to 1 will disable further user command complete interrupts for that particular USERACCESS register. Writing a 0 to this register has no effect.
End of Table 3-26		

3.4.11 MDIO User Access Register 0 (USERACCESS0)

The MDIO user access register is shown in Figure 3-21 and described in Table 3-27.

Figure 3-21 MDIO User Access Register 0 (USERACCESS0)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

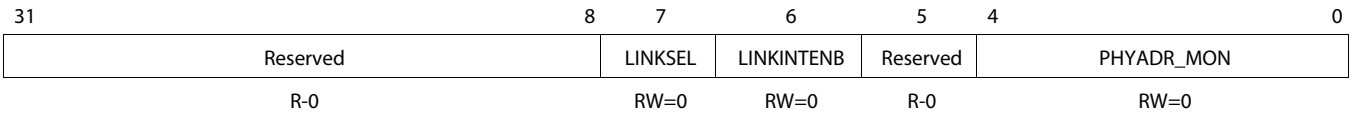
Table 3-27 MDIO User Access Register 0 (USERACCESS0) Field Descriptions

Bits	Field	Description
31	GO	Go bit. Writing a 1 to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so--this is not an instantaneous process. Writing a 0 to this bit has no effect. This bit can be written only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the USERACCESS0 register are blocked when the GO bit is 1.
30	WRITE	Write enable bit. Setting this bit to 1 causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	Acknowledge bit. This bit is set if the PHY acknowledged the read transaction.
28-26	Reserved	Reserved
25-21	REGADR	Register address bits. This field specifies the PHY register to be accessed for this transaction.
20-16	PHYADR	PHY address bits. This field specifies the PHY to be accessed for this transaction.
15-0	DATA	User data bits. These bits specify the data value read from or to be written to the specified PHY register.
End of Table 3-27		

3.4.12 MDIO User PHY Select Register 0 (USERPHYSEL0)

The MDIO user PHY select register 0 is shown in Figure 3-22 and described in Table 3-28.

Figure 3-22 MDIO User PHY Select Register 0 (USERPHYSEL0)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-28 MDIO User PHY Select Register 0 (USERPHYSEL0) Field Descriptions

Bits	Field	Description
31-8	Reserved	Reserved
7	LINKSEL	Link status determination select bit. Default value is 0 which implies that the link status is determined by the MDIO state machine. This is the only option supported on this device.
6	LINKINTENB	Link change interrupt enable. Set to 1 to enable link change status interrupts for PHY address specified in PHYADRMON. Link change interrupts are disabled if this bit is set to 0. 0 = Link change interrupts are disabled. 1 = Link change status interrupts for PHY address specified in PHYADRMON bits are enabled.
5	Reserved	Reserved
4-0	PHYADRMON	PHY address whose link status is to be monitored.
End of Table 3-28		

3.4.13 MDIO User Access Register 1 (USERACCESS1)

The MDIO user access register 1 is shown in Figure 3-23 and described in Table 3-29.

Figure 3-23 MDIO User Access Register 1 (USERACCESS1)

31	30	29	28 26	25 21	20 16
GO	WRITE	ACK	Reserved	REGADR	PHYADR
RW=0	RW=0	RW=0	R-0	RW=0	RW=0

15 0
DATA
RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-29 MDIO User Access Register 1 (USERACCESS1) Field Descriptions

Bits	Field	Description
31	GO	Go bit. Writing a 1 to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so--this is not an instantaneous process. Writing a 0 to this bit has no effect. This bit can be written only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the USERACCESS1 register are blocked when the GO bit is 1.
30	WRITE	Write enable bit. Setting this bit to 1 causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	Acknowledge bit. This bit is set if the PHY acknowledged the read transaction.
28-26	Reserved	Reserved
25-21	REGADR	Register address bits. This field specifies the PHY register to be accessed for this transaction.
20-16	PHYADR	PHY address bits. This field specifies the PHY to be accessed for this transaction.
15-0	DATA	User data bits. These bits specify the data value read from or to be written to the specified PHY register.
End of Table 3-29		

3.4.14 MDIO User PHY Select Register 1 (USERPHYSEL1)

The MDIO user PHY select register 1 is shown in Figure 3-24 and described in Table 3-30.

Figure 3-24 MDIO User PHY Select Register 1 (USERPHYSEL1)

31 — 8	7	6	5	4 — 0
Reserved	LINKSEL	LINKINTENB	Reserved	PHYADR_MON
R-0	RW=0	RW=0	R-0	RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-30 MDIO User PHY Select Register 1 (USERPHYSEL1) Field Descriptions

Bits	Field	Description
31-8	Reserved	Reserved
7	LINKSEL	Link status determination select bit. Default value is 0 which implies that the link status is determined by the MDIO state machine. This is the only option supported on this device.
6	LINKINTENB	Link change interrupt enable. Set to 1 to enable link change status interrupts for PHY address specified in PHYADRMON. Link change interrupts are disabled if this bit is set to 0. 0 = Link change interrupts are disabled. 1 = Link change status interrupts for PHY address specified in PHYADRMON bits are enabled.
5	Reserved	Reserved
4-0	PHYADRMON	PHY address whose link status is to be monitored.
End of Table 3-30		

3.5 PCS-R Module

This section describes the registers available in the Ethernet switch sub-module PCS-R module. The register offset addresses listed in Table 3-16 are relative to the PCS-R module offset address. To determine the offset address of the PCS-R module, please see Table 3-1. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

Table 3-31 PCS-R Module Registers

00h	PCSR_TX_CTL	PCSR Transmit Control Register	Section 3.5.1
04h	PCSR_TX_STATUS	PCSR Transmit Status Register	Section 3.5.2
08h	PCSR_RX_CTL	PCSR1 Receive Control Register	Section 3.5.3
0Ch	PCSR_RX_STATUS	PCSR Receive Status Register	Section 3.5.4
10h	PCSR_SEED_A_LO	PCSR Seed A Low Register	Section 3.5.5
14h	PCSR_SEED_A_HI	PCSR Seed A High Register	Section 3.5.6
18h	PCSR_SEED_B_LO	PCSR Seed B Low Register	Section 3.5.7
1Ch	PCSR_SEED_B_HI	PCSR Seed B High Register	Section 3.5.8
20h	PCSR_FEC	PCSR Seed A High Register	Section 3.5.9
24h	PCSR_CTL	PCSR Control Register	Section 3.5.10
28h	PCSR_RX_FEC_CNT	PCSR Receive FEC Count Register	Section 3.5.11
2Ch	PCSR_RX_ERR_FIFO	PCSR Receive Error FIFO Register	Section 3.5.12
End of Table 3-31			

3.5.1 PCSR Transmit Control Register (PCSR_TX_CTL)

PCSR Transmit Control Register is shown in Figure 3-26 and described in Table 3-32.

Figure 3-25 PCSR Transmit Control Register (PCSR_TX_CTL)

31 8	7	6	5
Reserved	TX_SCR_BYPASS	TX_TEST_EN	TX_TEST_SEL
R-0	RW-0	RW-0	RW-0

4	3	2	1	0
TX_TEST_DAT_SEL	TX_PRBS31_EN	TX_PRBS9_EN	TX_LOOPBACK_EN	TX_SCR_LOOPBACK_EN
RW-0	RW-0	RW-0	RW-0	RW-0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-32 PCSR Transmit Control Register (PCSR_TX_CTL)

Bits	Field	Description
31-8	Reserved	TBD
7	tx_scr_bypass	TBD
6	tx_test_en	TBD
5	tx_test_sel	TBD
4	tx_test_dat_sel	TBD
3	tx_prbs31_en	TBD
2	tx_prbs9_en	TBD
1	tx_loopback_en	TBD
0	tx_scr_loopback-en	TBD
End of Table 3-32		

3.5.2 PCSR Transmit Status Register (PCSR_Tx_Status)

PCSR Transmit Status Register is shown in Figure 3-27 and described in Table 3-33.

Figure 3-26 PCSR Transmit Status Register (PCSR_Tx_Status)

31 1	0
Reserved	TX_FAULT
R-0h	R-0h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-33 PCSR Transmit Status Register (PCSR_Tx_Status)

Bits	Field	Description
31-1	Reserved	TBD
0	tx_fault	TBD
End of Table 3-33		

3.5.3 PCSR Receive Control Register (PCSR_Rx_Ctl)

PCSR Receive Control Register is shown in Figure 3-28 and described in Table 3-34.

Figure 3-27 PCSR Receive Control Register (PCSR_Rx_Ctl)

31 8	7	6	5
Reserved	RX_TEST_EN	RX_TEST_DAT_SEL	RX_PRBS31_EN
R-0	RW-0	RW-0	RW-0

4	3	2	1	0
RX_ERR_BLK_CNT_RST	RX_BER_CNT_RST	RX_TEST_CNT_PRE	RX_TEST_CNT_125US	RX_TPTER_CNT_RST
RW-0	RW-0	RW-0	RW-0	RW-0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-34 PCSR Receive Control Register (PCSR_Rx_Ctl)

Bits	Field	Description
31-8	Reserved	TBD
7	rx_test_en	TBD
6	rx_test_dat_sel	TBD
5	rx_prbs31_en	TBD
4	rx_err_blk_cnt_rst	TBD
3	rx_ber_cnt_rst	TBD
2	rx_test_cnt_pre	TBD
1	rx_test_cnt_125us	TBD
0	rx_tpter_cnt_rst	TBD
End of Table 3-34		

3.5.4 PCSR Receive Status Register (PCSR_Rx_Status)

PCSR Receive Status Register is shown in Figure 3-29 and described in Table 3-35.

Figure 3-28 PCSR Receive Status Register (PCSR_Rx_Status)

31	30	29 24	23 16	15 0
RX_HI_BER	RX_BLOCK_LOCK	RX_BER_COUNT	RX_ERR_BLK_CNT	RX_TPT_ERR_CNT
R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

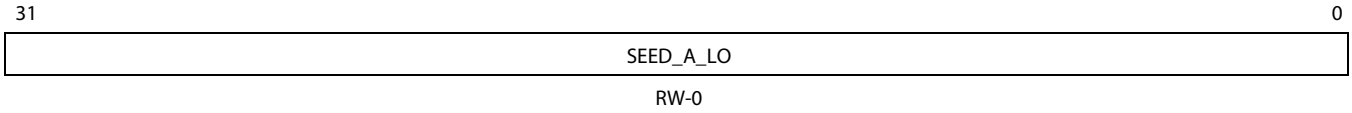
Table 3-35 PCSR Receive Status Register (PCSR_Rx_Status)

Bits	Field	Description
31	rx_hi_ber	TBD
30	rx_block_lock	TBD
29-24	rx_ber_count	TBD
23-16	rx_err_blk_cnt	TBD
15-0	rx_tpt_err_cnt	TBD
End of Table 3-35		

3.5.5 PCSR Seed A Low Register (PCSR_Seed_A_LO)

PCSR Seed A Low Register is shown in and Figure 3-30 described in Table 3-36.

Figure 3-29 PCSR Seed A Low Register (PCSR_Seed_A_LO)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

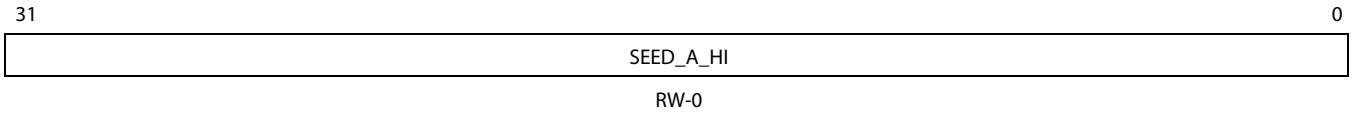
Table 3-36 PCSR Seed A Low Register (PCSR_Seed_A_LO)

Bits	Field	Description
31-0	seed_a_lo	TBD
End of Table 3-36		

3.5.6 PCSR Seed A Hi Register (PCSR_Seed_A_Hi)

PCSR Seed A Hi Register is shown in and Figure 3-30 described in Table 3-37.

Figure 3-30 PCSR Seed A Hi Register (PCSR_Seed_A_Hi)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

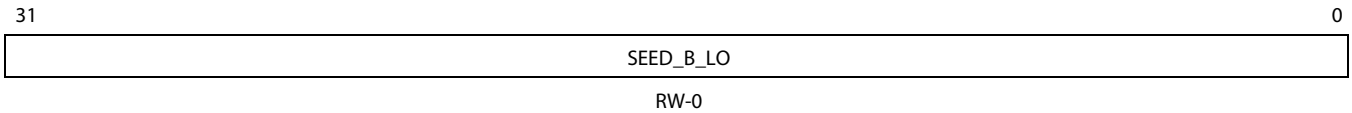
Table 3-37 PCSR Seed A Hi Register (PCSR_Seed_A_Hi)

Bits	Field	Description
31-0	seed_a_hi	TBD
End of Table 3-37		

3.5.7 PCSR Seed B Low Register (PCSR_Seed_B_LO)

PCSR Seed B Low Register is shown in and Figure 3-31 described in Table 3-38.

Figure 3-31 PCSR Seed B Low Register (PCSR_Seed_B_LO)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

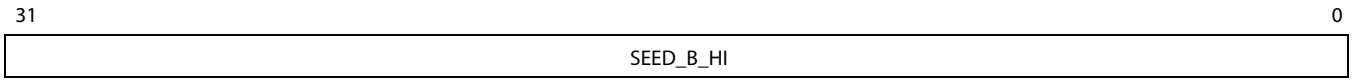
Table 3-38 PCSR Seed B Low Register (PCSR_Seed_B_LO)

Bits	Field	Description
31-0	seed_a_hi	TBD
End of Table 3-38		

3.5.8 PCSR Seed B Hi Register (PCSR_Seed_B_Hi)

PCSR Seed B Hi Register is shown in Figure 3-32 and described in Table 3-39.

Figure 3-32 PCSR Seed B Hi Register (PCSR_Seed_B_Hi)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

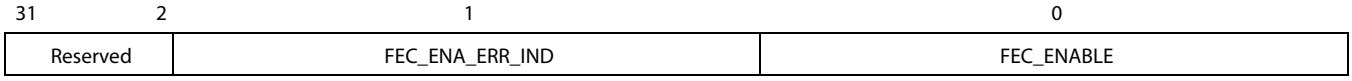
Table 3-39 PCSR Seed B Hi Register (PCSR_Seed_B_Hi)

Bits	Field	Description
31-0	seed_b_hi	TBD
End of Table 3-39		

3.5.9 PCSR Forward Error Correction Register (PCSR_FEC)

PCSR Forward Error Correction Register is shown in Figure 3-33 and described in Table 3-40.

Figure 3-33 PCSR Forward Error Correction Register (PCSR_FEC)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

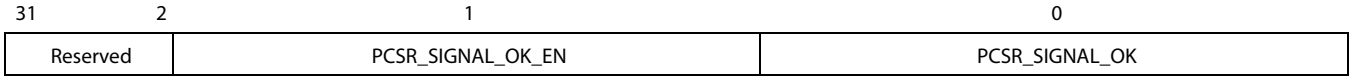
Table 3-40 PCSR Forward Error Correction Register (PCSR_FEC)

Bits	Field	Description
31-2	Reserved	TBD
1	fec_ena_err_ind	TBD
0	fec_enable	TBD
End of Table 3-40		

3.5.10 PCSR Control Register (PCSR_CTL)

PCSR Control Register is shown in Figure 3-34 and described in Table 3-41.

Figure 3-34 PCSR Control Register (PCSR_CTL)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-41 PCSR Control Register (PCSR_CTL) (Part 1 of 2)

Bits	Field	Description
31-2	Reserved	TBD

Table 3-41 PCSR Control Register (PCSR_CTL) (Part 2 of 2)

Bits	Field	Description
1	pcsr_signal_ok_en	TBD
0	pcsr_signal_ok	This bit is input to PCSR1 signal_ok when signal_ok_en is set to one. The serdes !losdet output is used when signal_ok_en is cleared to zero.
End of Table 3-41		

3.5.11 PCSR FEC Count Register (PCSR_FEC_CNT)

PCSR FEC Count Register is shown in Figure 3-35 and described in Table 3-42.

Figure 3-35 PCSR FEC Count Register (PCSR_FEC_CNT)

31 2	1	0
Reserved	RX_FEC_CORR	RX_FEC_UNCORR
	RW-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-42 PCSR FEC Count Register (PCSR_FEC_CNT)

Bits	Field	Description
31-2	Reserved	TBD
1	rx_fec_corr	TBD
0	rx_fec_uncorr	TBD
End of Table 3-42		

3.5.12 PCSR Error FIFO Register (PCSR_ERR_FIFO)

PCSR Error FIFO Register is shown in Figure 3-36 and described in Table 3-43.

Figure 3-36 PCSR Error FIFO Register (PCSR_ERR_FIFO)

31 1	0
Reserved	RX_ERR_FIFO_CTC
R-0h	R-0h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-43 PCSR Error FIFO Register (PCSR_ERR_FIFO)

Bits	Field	Description
31-1	Reserved	TBD
0	rx_err_fifo_ctc	Receive Error FIFO CTC – This bit will be set to one and held until cleared when the PCSR rx_err_fifo_ctc output is set to one. This bit is cleared to zero by writing a one.
End of Table 3-43		

3.6 10 Gigabit Ethernet Switch

This section describes the registers available in the Ethernet switch module. The submodule offset addresses listed in Table 3-44 are relative to the Ethernet switch module offset address. To determine the offset address of the Ethernet switch module, please see Table 3-1. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

Table 3-44 shows the submodules contained in the Ethernet switch module.

Table 3-44 10Gigabit Ethernet switch submodules

Offset Address [1]	Acronym	Submodule Name	Section
000h	10GbE Switch	10Gigabit Ethernet Switch	Section 3.6.1
100h	EMAC1	Port 1 Ethernet MAC submodule	Section 3.6.2
140h	EMAC2	Port 2 Ethernet MAC submodule	Section 3.6.2
300h	CPTS	Time Sync submodule	Section 3.6.4
400h	ALE	Address lookup engine submodule	Section 3.6.5
500h	STATS0	10Gigabit Ethernet statistics 0 submodule	Section 3.6.3
600h	STATS1	10Gigabit Ethernet statistics 1 submodule	Section 3.6.3
700h	STATS2	10Gigabit Ethernet statistics 2 submodule	Section 3.6.3
End of Table 3-44			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.6.1 10Gigabit Ethernet (10GbE) Switch

This section describes the registers available in the Ethernet switch submodule. The register offset addresses listed in Table 3-45 are relative to the Ethernet switch module offset address. To determine the offset address of the Ethernet switch module, please see Table 3-1. For convenience, a complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-45 10Gigabit Ethernet Switch Registers (Part 1 of 2)

Offset Address[1]	Acronym	Description	Section
000h	CPSW_IDVER	10GbE switch identification and version register	Section 3.6.1.1
004h	CPSW_CONTROL	10GbE switch Control Register	Section 3.6.1.2
008h	CPSW_EMCONTROL	10GbE switch Emulation Control Register	Section 3.6.1.3
00Ch	CPSW_STAT_PORT_EN	10GbE switch Statistics Port Enable Register	Section 3.6.1.4
010h	CPSW_PTYPE	10GbE switch Transmit Priority Type Register	Section 3.6.1.5
014h	CPSW_SOFT_IDLE	10GbE switch Software Idle Register	Section 3.6.1.6
018h	CPSW_THRU_RATE	10GbE switch Thru Rate Register	Section 3.6.1.7
01Ch	CPSW_GAP_THRESH	Transmit FIFO Short Gap Threshold Register	Section 3.6.1.8
020h	CPSW_TX_START_WDS	Transmit FIFO Start Words Register	Section 3.6.1.9
024h	CPSW_FLOW_CONTROL	Flow Control Register	Section 3.6.1.10
028h	CPSW_CPPI_THRESH	CPPI Threshold Register	Section 3.6.1.11
02Ch-030h	Reserved		

Table 3-45 10Gigabit Ethernet Switch Registers (Part 2 of 2)

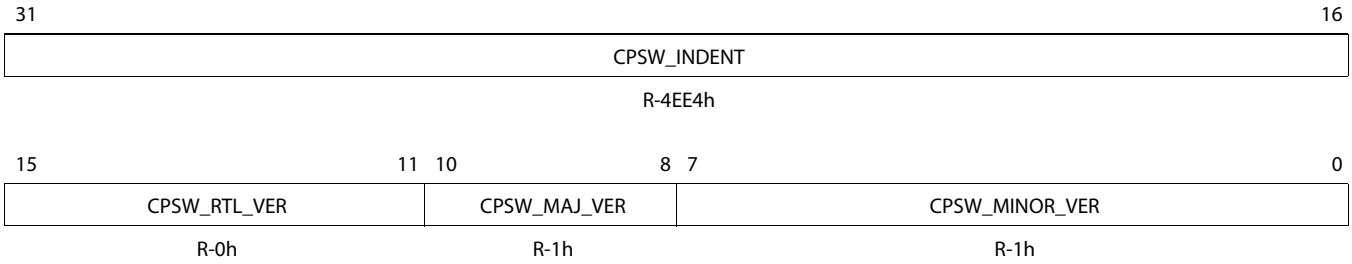
Offset Address[1]	Acronym	Description	Section
034h	P0_BLK_CNT	Port 0 Source ID Register	Section 3.6.1.15
038h	P0_PORT_VLAN	Port 0 VLAN Register	Section 3.6.1.13
03Ch	P0_Tx_Pri_Map	Port 0 Transmit Packet Priority to Header Priority Mapping Register	Section 3.6.1.20
040h	P0_SRC_ID	Port 0 Receive Frame Max Length Register	Section 3.6.1.17
044h	P0_Rx_Pri_Map	Port 0 RX Packet Priority to Header Priority Mapping Register	Section 3.6.1.16
048h	P0_Rx_Maxlen	Port 0 Receive Frame Max Length Register	Section 3.6.1.17
04C-060h	Reserved		
064h	P1_BLK_CNT	Port 1 FIFO Block Usage Count	Section 3.6.1.18
068h	P1_PORT_VLAN	Port 1 VLAN Register	Section 3.6.1.19
06Ch	P1_TX_PRI_MAP	Port 1 Tx Header Priority to switch Queue Mapping Reg	Section 3.6.1.20
070h	MAC1_SA_LO	MAC1 Source Address Low Register	Section 3.6.1.21
074h	MAC1_SA_HI	MAC1 Source Address High Register	Section 3.6.1.22
078h	P1_TS_CTL	Port 1 Time Sync Control Register	Reserved
07Ch	P1_TS_SEQ_LTYPE	Port 1 Time Sync LTYPE (and SEQ_ID_OFFSET)	Section 3.6.1.26
080h	P1_TS_VLAN	Port 1 Time Sync VLAN2 and VLAN2 Register	Section 3.6.1.25
084h	P1_TS_CTL_LTYPE2	Port 1 Time Sync Control and LTYPE2 Register	Section 3.6.1.23
088h	P1_TS_CTL2	Port 1 Time Sync Control 2 Register	Section 3.6.1.26
08Ch	P1_Control	Port 1 Control Register	Section 3.6.1.28
090h	Reserved		
094h	P2_BLK_CNT	Port 2 FIFO Block Usage Count	Section 3.6.1.29
098h	P2_PORT_VLAN	Port 2 VLAN Register	Section 3.6.1.30
09Ch	P2_TX_PRI_MAP	Port 2 Tx Header Priority to switch Queue Mapping Register	Section 3.6.1.31
0A0h	MAC2_SA_LO	MAC2 Source Address Low Register	Section 3.6.1.32
0A4h	MAC2_SA_HI	MAC2 Source Address High Register	Section 3.6.1.33
0A8h	P2_TS_CTL	Port 2 Time Sync Control Register	Section 3.6.1.34
0ACh	P2_TS_SEQ_LTYPE	Port 2 Time Sync LTYPE (and SEQ_ID_OFFSET)	Section 3.6.1.35
0B0h	P2_TS_VLAN	Port 2 Time Sync VLAN2 and VLAN2 Register	Section 3.6.1.36
0B4h	P2_TS_CTL_LTYPE2	Port 2 Time Sync Control and LTYPE2 Register	Section 3.6.1.37
0B8h	P2_TS_CTL2	Port 2 Time Sync Control 2 Register	Section 3.6.1.38
0BCh	P2_Control	Port 2 Control Register	Section 3.6.1.39
End of Table 3-45			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.6.1.1 10GbE switch Identification and Version Register (CPSW_IDVER)

The GbE switch identification and version register is shown in Figure 3-37 and described in Table 3-46.

Figure 3-37 GbE switch Identification and Version Register (CPSW_IDVER)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

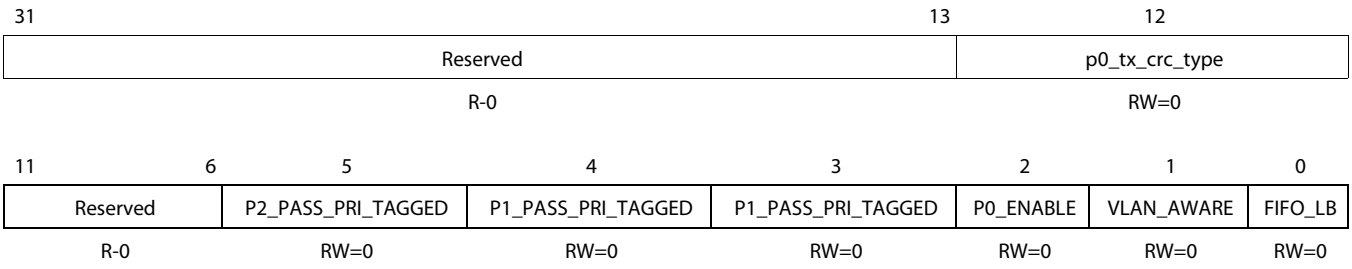
Table 3-46 GbE switch Identification and Version Register (CPSW_IDVER) Field Descriptions

Bits	Field	Description
31-16	CPSW_IDENT	Identification Value
15-11	CPSW_RTL_VER	RTL Version Value
10-8	CPSW_MAJ_VER	Major Version Value
7-0	CPSW_MINOR_VERS	CPSW_3GF Minor Version Value
End of Table 3-46		

3.6.1.2 10 GbE switch Control Register (CPSW_CONTROL)

The GbE switch control register is shown in Figure 3-38 and described in Table 3-47.

Figure 3-38 10GbE switch Control Register (CPSW_CONTROL)



Legend: R = Read only; W = Write only; -*n* = value after reset

Table 3-47 GbE switch Control Register (CPSW_CONTROL) Field Descriptions (Part 1 of 2)

Bits	Field	Description
31-13	Reserved	Reserved
12	p0_tx_crc_type	Port 0 Transmit CRC type – The type of CRC on all Port 0 transmit packet (egress), regardless of the CRC type of in ingress Ethernet port. 0 – Ethernet CRC on Port 0 Transmit 1 – Castagnoli CRC on Port 0 Transmit
11-6	Reserved	Reserved

Table 3-47 GbE switch Control Register (CPSW_CONTROL) Field Descriptions (Part 2 of 2)

Bits	Field	Description
5	P2_PASS_PRI_TAG	Port 2 Pass Priority Tagged. 0 = Priority tagged packets have the zero VID replaced with the input port P2_PORT_VLAN[11-0] on ingress. 1 = Priority tagged packets are processed unchanged.
4	P1_PASS_PRI_TAG	Port 1 Pass Priority Tagged. 0 = Priority tagged packets have the zero VID replaced with the input port P1_PORT_VLAN[11-0] on ingress. 1 = Priority tagged packets are processed unchanged.
3	P0_PASS_PRI_TAG	Port 0 Pass Priority Tagged. 0 = Priority tagged packets have the zero VID replaced with the input port P0_PORT_VLAN[11-0] on ingress. 1 = Priority tagged packets are processed unchanged.
2	P0_ENABLE	Port 0 Enable. 0 = Port 0 packet operations are disabled. 1 = Port 0 packet operations are enabled.
1	VLAN_AWARE	VLAN Aware Mode. 0 = 10GbE switch is in the VLAN unaware mode. 1 = CPSW_3GF is in the VLAN aware mode.
0	FIFO_LB	FIFO Loopback Mode. 0 = Loopback is disabled 1 = FIFO Loopback mode enabled. Each packet received is turned around and sent out on the same port's transmit path. RXSOFOVERRUN will increment for each loopback mode packet.
End of Table 3-47		

3.6.1.3 Emulation Control Register (EM_CONTROL)

The emulation control register is shown in Figure 3-39 and described in Table 3-48.

Figure 3-39 Emulation Control Register (EM_CONTROL)

31	2	1	0
Reserved		SOFT	FREE
R-0		RW=0	RW=0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-48 Emulation Control Register (EM_CONTROL) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1	SOFT	Emulation Soft Bit
0	FREE	Emulation Free Bit
End of Table 3-48		

3.6.1.4 Statistics Port Enable (STAT_PORT_EN)

The statistics port enable register is shown in Figure 3-40 and described in Table 3-49.

Figure 3-40 Statistics Port Enable (STAT_PORT_EN)

31	3	2	1	0
Reserved		P2_STAT_EN	P1_STAT_EN	P0_STAT_EN
R-0		RW=0	RW=0	RW=0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-49 Statistics Port Enable (STAT_PORT_EN) Field Descriptions

Bits	Field	Description
31-3	Reserved	Reserved
2	P2_STAT_EN	Port 2 Statistics Enable 0 – Port 2 statistics are not enabled 1 – Port 2 statistics are enabled.
1	P1_STAT_EN	Port 1 Statistics Enable 0 – Port 1 statistics are not enabled 1 – Port 1 statistics are enabled.
0	P0_STAT_EN	Port 0 Statistics Enable 0 – Port 0 statistics are not enabled 1 – Port 0 statistics are enabled.
End of Table 3-49		

3.6.1.5 Priority Type Register (PTYPE)

The priority type register is shown in Figure 3-41 and described in Table 3-50.

Figure 3-41 Priority Type Register (PTYPE)

31	11	10	9	8
Reserved		P2_PTYPE_ESC	P1_PTYPE_ESC	P0_PTYPE_ESC
R-0		RW=0	RW=0	RW=0

7	5	4	0
Reserved		ESC_PRI_LD_VAL	
R-0		RW=0	

Legend: R = Read only; W = Write only; -*n* = value after reset

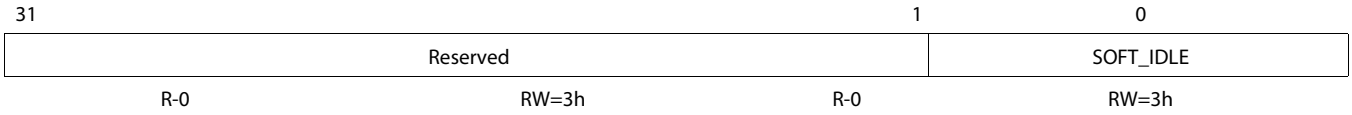
Table 3-50 Priority Type Register (PTYPE) Field Descriptions

Bits	Field	Description
31-11	Reserved	Reserved
10	P2_PTYPE_ESC	Port 2 Priority Type Escalate. 0 = Port 2 priority type fixed. 1 = Port 2 priority type escalate.
9	P1_PTYPE_ESC	Port 1 Priority Type Escalate. 0 = Port 1 priority type fixed. 1 = Port 1 priority type escalate.
8	P0_PTYPE_ESC	Port 0 Priority Type Escalate. 0 = Port 0 priority type fixed. 1 = Port 0 priority type escalate.
7-5	Reserved	Reserved
4-0	ESC_PRI_LD_VAL	Escalate Priority Load Value. When a port is in escalate priority, this is the number of higher priority packets sent before the next lower priority is allowed to send a packet. Escalate priority allows lower priority packets to be sent at a fixed rate relative to the next higher priority.
End of Table 3-50		

3.6.1.6 10GbE switch Software Idle Register (CPSW_SOFT_IDLE)

The Software Idle Register is shown in Figure 3-42 and described in Table 3-51.

Figure 3-42 Software Idle Register (CPSW_SOFT_IDLE)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

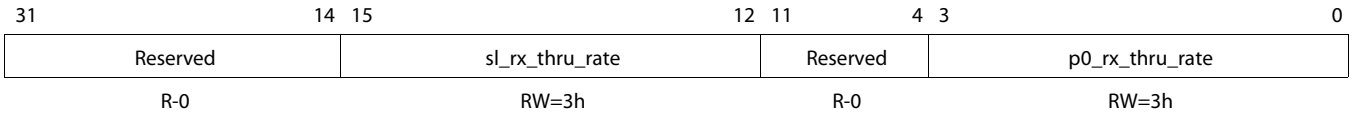
Table 3-51 Software Idle Register (CPSW_SOFT_IDLE)

Bits	Field	Description
31-1	Reserved	
0	soft_idle	Software Idle 0 – not in idle. 1 – Command a CPSW_3XF software idle. When set, no packets will be started to be unloaded from ports 0 through 4 receive unload. Packets that are currently being unloaded are unaffected.
End of Table 3-51		

3.6.1.7 10GbE switch Thru Rate Register (THRU_RATE)

The Thru Rate register is shown in Figure 3-43 and described in Table 3-52.

Figure 3-43 THRU_RATE – Through Rate Register



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

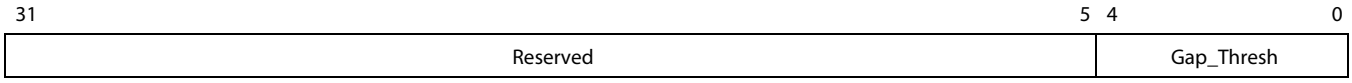
Table 3-52 THRU_RATE – Through Rate Register Field Descriptions

Bits	Field	Description
31-14	Reserved	Reserved
15-12	sl_rx_thru_rate	MAC Ports FIFO receive through rate. This register value is the maximum throughput of the Ethernet ports to the crossbar SCR. The default is one 8-byte word for every 3 VBUSP_GCLK periods maximum. The minimum value is 2. This is not a field that is intended to be changed by a user.
11-4	Reserved	Reserved
3-0	p0_rx_thru_rate	Port 0 receive through rate. This register value is the maximum throughput of the Port 0 into the CPSW_3XF. This field is not intended to be changed by the user.
End of Table 3-52		

3.6.1.8 MAC Short Gap Threshold Register (GAP_THRESH)

The MAC short gap threshold register is shown in Figure 3-44 and described in Table 3-53.

Figure 3-44 MAC Short Gap Threshold Register (GAP_THRESH)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

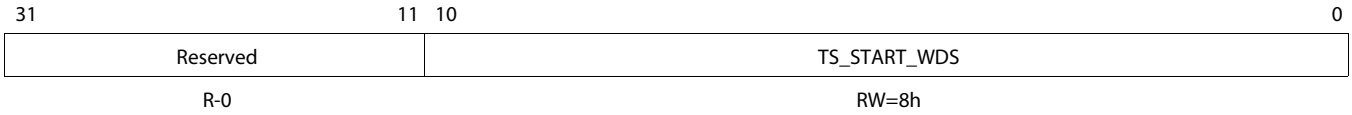
Table 3-53 MAC Short Gap Threshold Register (GAP_THRESH) Field Descriptions

Bits	Field	Description
31-5	Reserved	Reserved
4-0	Gap_Thresh	MAC Short Gap Threshold. This is the MAC associated FIFO transmit block usage value for triggering TX_SHORT_GAP.
End of Table 3-53		

3.6.1.9 Transmit FIFO Start Words Register (TX_START_WDS)

The transmit FIFO start words register is shown in Figure 3-45 and described in Table 3-54.

Figure 3-45 Transmit FIFO Start Words Register (TX_START_WDS)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-54 Transmit FIFO Start Words Register (TX_START_WDS) Field Descriptions

Bits	Field	Description
31-11	Reserved	Reserved
10-0	TX_START_WDS	FIFO Packet Transmit (egress) Start Words. This value is the number of required packet words in the transmit FIFO before the packet egress will begin. This value is non-zero to preclude underrun. Decimal 8 is the recommended value. It should not be increased unnecessarily to prevent adding to the switch latency.
End of Table 3-54		

3.6.1.10 Flow Control Register (FLOW_CONTROL)

The flow control register is shown in Figure 3-46 and described in Table 3-55.

Figure 3-46 Flow Control Register (FLOW_CONTROL)

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-55 Flow Control Register (FLOW_CONTROL) Field Descriptions

Bits	Field	Description
31-3	Reserved	Reserved
2	P2_FLOW_EN	Port 2 Receive flow control enable.
1	P1_FLOW_EN	Port 1 Receive flow control enable.
0	P0_FLOW_EN	Port 0 Receive flow control enable.
End of Table 3-55		

3.6.1.11 CPPI Threshold

The CPPI threshold register is shown in Figure 3-47 and described in Table 3-56.

Figure 3-47 CPPI Threshold

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

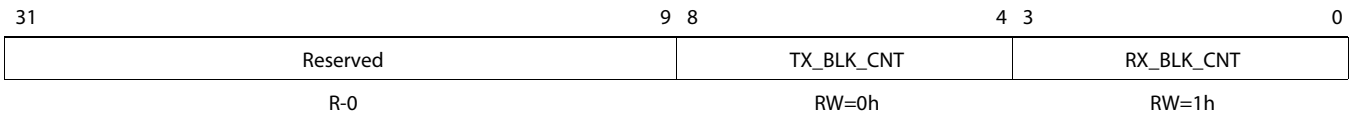
Table 3-56 CPPI Threshold Field Descriptions

Bits	Field	Description
31-10	Reserved	Reserved
9 - 0	cppi_thresh	This is the number of 16-byte words required to be in the TXST output buffer before an egress transfer will begin (if there is not at least one complete packet in the FIFO). TXSTn_THREAD_MREADY is not asserted until the number of 16-byte words (or a complete packet) in the output buffer reaches this value (plus 2).
End of Table 3-56		

3.6.1.12 Port0 Block Count (P0_BLK_CNT)

The port 0 source identification register is shown in Figure 3-48 and described in Table 3-57.

Figure 3-48 Port0 Block Count Register (P0_BLK_CNT)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

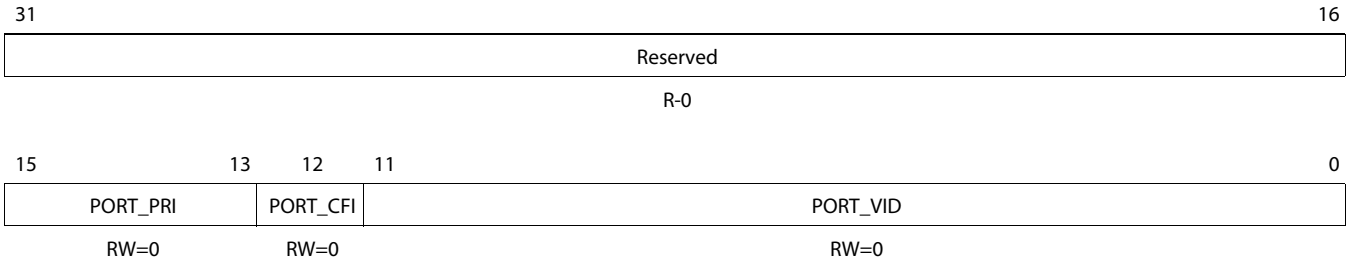
Table 3-57 Port 0 Block Count Register (P0_BLK_CNT) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-8	TX_BLK_CNT	Port 0 Transmit Block Count Usage – This value is the number of blocks allocated to the FIFO logical transmit queues.
7-0	RX_BLK_CNT	Port 0 Receive Block Count Usage – This value is the number of blocks allocated to the FIFO logical receive queues.
End of Table 3-57		

3.6.1.13 Port 0 VLAN Register (P0_PORT_VLAN)

The port 0 VLAN register is shown in Figure 3-49 and described in Table 3-58.

Figure 3-49 Port 0 VLAN Register (P0_PORT_VLAN)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

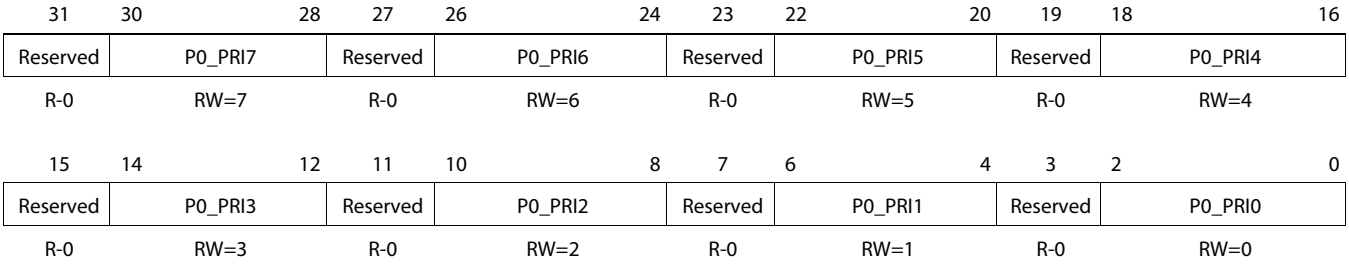
Table 3-58 Port 0 VLAN Register (P0_PORT_VLAN) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-13	PORT_PRI	Port VLAN Priority (7 is highest priority).
12	PORT _CFI	Port CFI bit.
11-0	PORT _VID	Port VLAN ID.
End of Table 3-58		

3.6.1.14 Port 0 TX Header Priority to Switch Priority Mapping Register (P0_TX_PRI_MAP)

The port 0 receive packet priority to header priority mapping register is shown in Figure 3-50 and described in Table 3-59.

Figure 3-50 Port 0 TX Header Priority to Switch Priority Mapping Register (P0_TX_PRI_MAP)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-59 Port 0 TX Header Priority to Switch Priority Mapping Register (P0_TX_PRI_MAP) Field Descriptions (Part 1 of 2)

Bits	Field	Description
31	Reserved	Reserved
30-8	P0_PRI7	Port 0 Priority 7. A packet header priority of 0x7 is given this switch queue priority
27	Reserved	Reserved
26-24	P0_PRI6	Port 0 Priority 6. A packet header priority of 0x6 is given this switch queue priority
23	Reserved	Reserved
22-20	P0_PRI5	Port 0 Priority 5. A packet header priority of 0x5 is given this switch queue priority
19	Reserved	Reserved
18-16	P0_PRI4	Port 0 Priority 4. A packet header priority of 0x4 is given this switch queue priority.

Table 3-59 Port 0 TX Header Priority to Switch Priority Mapping Register (P0_TX_PRI_MAP) Field Descriptions (Part 2 of 2)

Bits	Field	Description
15	Reserved	Reserved
14-12	P0_PRI3	Port 0 Priority 3. A packet header priority of 0x3 is given this switch queue priority.
11	Reserved	Reserved
10-8	P0_PRI2	Port 0 Priority 2. A packet header priority of 0x2 is given this switch queue priority.
7	Reserved	Reserved
6-4	P0_PRI1	Port 0 Priority 1. A packet header priority of 0x1 is given this switch queue priority.
3	Reserved	Reserved
2-0	P0_PRI0	Port 0 Priority 0. A packet header priority of 0x0 is given this switch queue priority.
End of Table 3-59		

3.6.1.15 Port0 Source Identification Register (P0_CPPI_SRC_ID)

The port 0 source identification register is shown in Figure 3-51 and described in Table 3-60.

Figure 3-51 Port0 Source Identification Register (P0_CPPI_SRC_ID)

31 16	15 8	7 0
Reserved	TXB_SCR_ID	TXA_SRC_ID
R-0	RW=2h	RW=1h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-60 Port 0 Source Identification Register (P0_CPPI_SRC_ID) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-8	TXB_SRC_ID	CPPI Info Word0 Source ID Value on TXB. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 2 (which go to CPPI TXB).
7-0	TXA_SRC_ID	CPPI Info Word0 Source ID Value on TXA. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 1 (which go to CPPI TXA).
End of Table 3-60		

3.6.1.16 Port 0 Receive Packet Priority to Header Priority Mapping Register (P0_RX_PRI_MAP)

The port 0 receive packet priority to header priority mapping register is shown in Figure 3-52 and described in Table 3-61.

Figure 3-52 Port 0 Receive Packet Priority to Header Priority Mapping Register (P0_RX_PRI_MAP)

31	30 28	27	26 24	23	22 20	19	18 16
Reserved	P0_PRI7	Reserved	P0_PRI6	Reserved	P0_PRI5	Reserved	P0_PRI4
R-0	RW=7	R-0	RW=6	R-0	RW=5	R-0	RW=4

15	14 12	11	10 8	7	6 4	3	2 0
Reserved	P0_PRI3	Reserved	P0_PRI2	Reserved	P0_PRI1	Reserved	P0_PRI0
R-0	RW=3	R-0	RW=2	R-0	RW=1	R-0	RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-61 Port 0 Receive Packet Priority to Header Priority Mapping Register (P0_RX_PRI_MAP) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-8	P0_PRI7	Port 0 Priority 7. A packet priority of 7h is mapped (changed) to this header packet priority.
27	Reserved	Reserved
26-24	P0_PRI6	Port 0 Priority 6. A packet priority of 6h is mapped (changed) to this header packet priority.
23	Reserved	Reserved
22-20	P0_PRI5	Port 0 Priority 5. A packet priority of 5h is mapped (changed) to this header packet priority.
19	Reserved	Reserved
18-16	P0_PRI4	Port 0 Priority 4. A packet priority of 4h is mapped (changed) to this header packet priority.
15	Reserved	Reserved
14-12	P0_PRI3	Port 0 Priority 3. A packet priority of 3h is mapped (changed) to this header packet priority.
11	Reserved	Reserved
10-8	P0_PRI2	Port 0 Priority 2. A packet priority of 2h is mapped (changed) to this header packet priority.
7	Reserved	Reserved
6-4	P0_PRI1	Port 0 Priority 1. A packet priority of 1h is mapped (changed) to this header packet priority.
3	Reserved	Reserved
2-0	P0_PRI0	Port 0 Priority 0. A packet priority of 0h is mapped (changed) to this header packet priority.
End of Table 3-61		

3.6.1.17 Port 0 Receive Maximum Length Register (P0_RX_MAXLEN)

The port 0 receive maximum length register is shown in Figure 3-53 and described in Table 3-62.

Figure 3-53 Port 0 RX Maximum Length Register (P0_RX_MAXLEN)

31	14	13	0
Reserved		RX_MAXLEN	
R-0		RW=5EEh	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

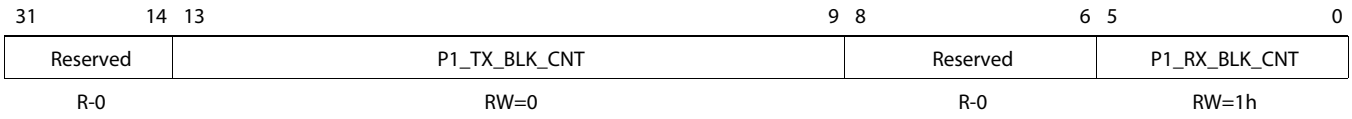
Table 3-62 Port 0 RX Maximum Length Register (P0_RX_MAXLEN) Field Descriptions

Bits	Field	Description
31-14	Reserved	Reserved
13-0	RX_MAXLEN	Receive Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than **RX_MAXLEN** are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN).
End of Table 3-62		

3.6.1.18 Port 1 Block Count Register (P1_BLK_CNT)

The port 1 block count register is shown in Figure 3-53 and described in Table 3-62.

Figure 3-54 Port 1 Block Count Register (P1_BLK_CNT)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

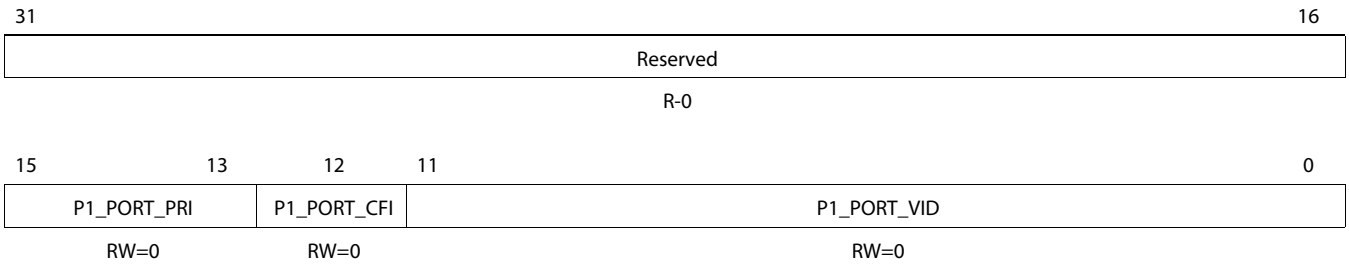
Table 3-63 Port 1 Block Count Register (P1_BLK_CNT) Field Descriptions

Bits	Field	Description
31-14	Reserved	Reserved
13-9	P1_TX_BLK_CNT	Port 1 Transmit Block Count Usage. This value is the number of blocks allocated to the FIFO logical transmit queues.
8-6	Reserved	Reserved
5-0	P1_RX_BLK_CNT	Port 1 Receive Block Count Usage. This value is the number of blocks allocated to the FIFO logical receive queues.
End of Table 3-63		

3.6.1.19 Port 1 VLAN Register (P1_PORT_VLAN)

The port 1 VLAN register is shown in Figure 3-55 and described in Table 3-64.

Figure 3-55 Port 1 VLAN Register (P1_PORT_VLAN)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-64 Port 1 VLAN Register (P1_PORT_VLAN) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-13	P1_PORT_PRI	Port VLAN Priority (7 is highest priority)
12	P1_PORT_CFI	Port CFI bit
11-0	P1_PORT_VID	Port VLAN ID
End of Table 3-64		

3.6.1.20 Port 1 Transmit Header Priority to switch Priority Mapping Register (P1_TX_PRI_MAP)

The port 1 transmit header priority to switch priority mapping register is shown in Figure 3-56 and described in Table 3-65.

Figure 3-56 Port 1 Transmit Header Priority to switch Priority Mapping Register (P1_TX_PRI_MAP)

31	30–28	27	26–24	23	22–20	19	18–16
Reserved	P1_PRI7	Reserved	P1_PRI6	Reserved	P1_PRI5	Reserved	P1_PRI4
R-0	RW=3h	R-0	RW=3h	R-0	RW=2h	R-0	RW=2h

15	14–12	11	10–8	7	6–4	3	2–0
Reserved	P1_PRI3	Reserved	P1_PRI2	Reserved	P1_PRI1	Reserved	P1_PRI0
R-0	RW=1h	R-0	RW=0	R-0	RW=0	R-0	RW=1h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

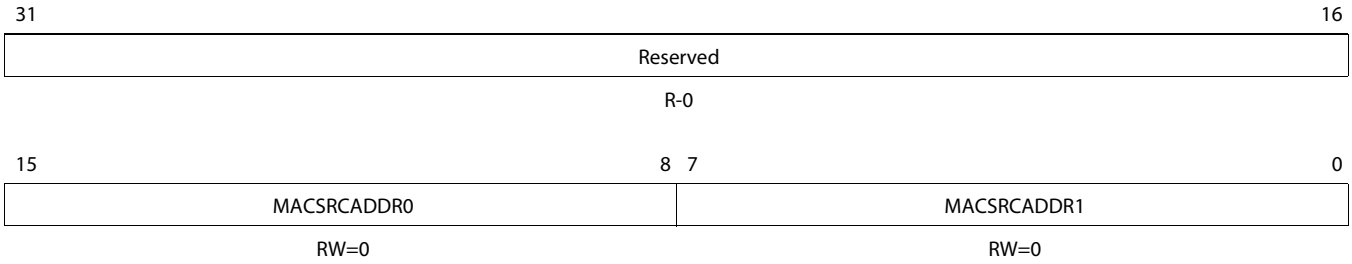
Table 3-65 P1 Transmit Header Priority to switch Priority Mapping Register (P1_TX_PRI_MAP) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	P1_PRI7	Port 1 Priority 7. A packet header priority of 7h is given this switch queue priority.
27	Reserved	Reserved
26-24	P1_PRI6	Port 1 Priority 6. A packet header priority of 6h is given this switch queue priority.
23	Reserved	Reserved
22-20	P1_PRI5	Port 1 Priority 5. A packet header priority of 5h is given this switch queue priority.
19	Reserved	Reserved
18-16	P1_PRI4	Port 1 Priority 4. A packet header priority of 4h is given this switch queue priority.
15	Reserved	Reserved
14-12	P1_PRI3	Port 1 Priority 3. A packet header priority of 3h is given this switch queue priority.
11	Reserved	Reserved
10-8	P1_PRI2	Port 1 Priority 2. A packet header priority of 2h is given this switch queue priority.
7	Reserved	Reserved
6-4	P1_PRI1	Port 1 Priority 1. A packet header priority of 1h is given this switch queue priority.
3	Reserved	Reserved
2-0	P1_PRI0	Port 1 Priority 0. A packet header priority of 0h is given this switch queue priority.
End of Table 3-65		

3.6.1.21 MAC1 Source Address Low Register (MAC1_SA_LO)

The MAC1 source address low register is shown in Figure 3-57 and described in Table 3-66.

Figure 3-57 MAC1 Source Address Low Register (MAC1_SA_LO)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

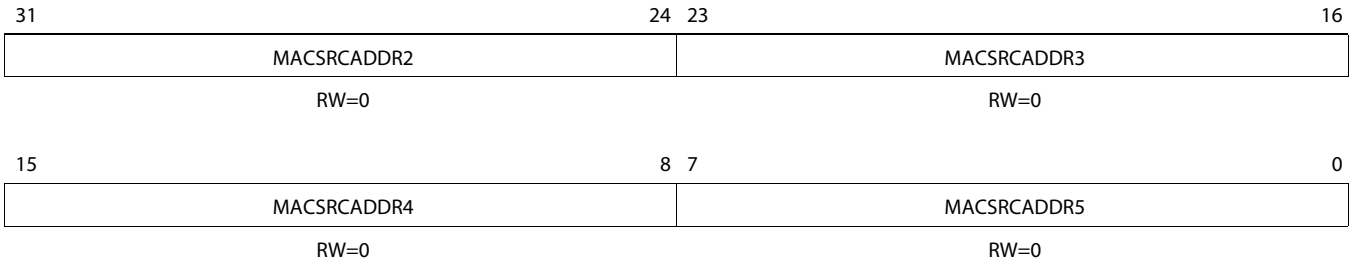
Table 3-66 MAC1 Source Address Low Register (MAC1_SA_LO) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-8	MACSRCADDR0	Source address bits 7-0 (byte 0).
7-0	MACSRCADDR1	Source Address bits 15-8(byte 1).
End of Table 3-66		

3.6.1.22 MAC1 Source Address High Register (MAC1_SA_HI)

The MAC1 source address high register is shown in Figure 3-58 and described in Table 3-67.

Figure 3-58 MAC1 Source Address High Register (MAC1_SA_HI)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-67 MAC1 Source Address High Register (MAC1_SA_HI) Field Descriptions

Bits	Field	Description
31-24	MACSRCADDR2	Source Address bits 23-16 (byte 2)
23-16	MACSRCADDR3	Source Address bits 31-24 (byte 3)
15-8	MACSRCADDR4	Source Address bits 39-32 (byte 4)
7-0	MACSRCADDR5	Source Address bits 47-40 (byte 5)
End of Table 3-67		

3.6.1.23 Port 1 Time Sync Control Register (P1_TS_CTL)

The port 1 time sync control register is shown in Figure 3-59 and described in Table 3-68.

Figure 3-59 Port 1 Time Sync Control Register (P1_TS_CTL)

31–16	15–11	10	9	8	7	6
TX_MSG_TYPE_EN	Reserved	TX_ANNEX_E_EN	RX_ANNEX_E_EN	LTYPE2_EN	TX_ANNEX_D_EN	TX_VLAN_LTYPE2_EN
RW=0				R-0		RW=0

5	4	3	2	1	0
TX_VLAN_LTYPE1_EN	TX_ANNEX_F_EN	RX_ANNEX_D_EN	RX_VLAN_LTYPE2_EN	TX_VLAN_LTYPE1_EN	RX_ANNEX_F_EN
RW=0		RW=0	R-0	RW=0	RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-68 Port 1 Time Sync Control Register (P1_TS_CTL) Field Descriptions

Bits	Field	Description
31-16	TX_MSG_TYPE_EN	Port 1 Time Sync Message Type Enable. Each bit in this field enables the corresponding message type in receive and transmit time sync messages (Bit 0 enables message type 0 etc.).
15-11	Reserved	Reserved
10	TX_ANNEX_E_EN	Port 1 Time Sync Transmit Annex E enable
9	RX_ANNEX_E_EN	Port 1 Time Sync Receive Annex E enable
8	LTYPE2_EN	Port 1 Time Sync LTYPE 2 enable (transmit and receive)
7	TX_ANNEX_D_EN	Port 1 Time Sync Transmit Annex D enable
6	TX_VLAN_LTYPE2_EN	Port 1 Time Sync Transmit VLAN LTYPE 2 enable.
5	TX_VLAN_LTYPE1_EN	Port 1 Time Sync Transmit VLAN LTYPE 1 enable.
4	TX_ANNEX_F_EN	Port 1 Time Sync Transmit Annex F Enable.
3	RX_ANNEX_D_EN	Port 1 Time Sync Receive Annex D enable
2	RX_VLAN_LTYPE2_EN	Port 1 Time Sync Receive VLAN LTYPE 2 enable.
1	TX_VLAN_LTYPE1_EN	Port 1 Time Sync Receive VLAN LTYPE 1 enable.
0	RX_ANNEX_F_EN	Port 1 Time Sync Receive Annex F Enable.
End of Table 3-68		

3.6.1.24 Port 1 Time Sync Sequence ID and LTYPE Register (P1_TS_SEQ_LTYPE)

The port 1 time sync sequence ID and LTYPE register is shown in Figure 3-60 and described in Table 3-69.

Figure 3-60 Port 1 Time Sync Sequence ID and LTYPE Register (P1_TS_SEQ_LTYPE)

31–22	21–16	15–0
Reserved	P1_TS_SEQ_ID_OFFSET	P1_TS_LTYPE
R-0	RW=1Eh	RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

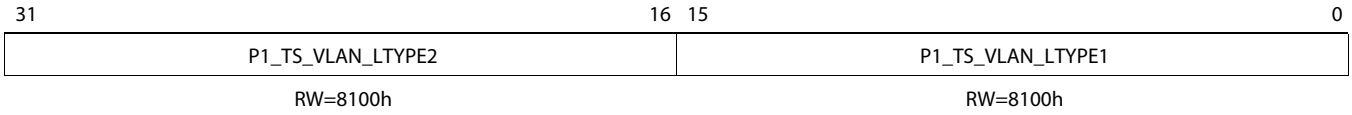
Table 3-69 Port 1 Time Sync Sequence ID and LTYPE Register (P1_TS_SEQ_LTYPE) Field Descriptions

Bits	Field	Description
31-22	Reserved	Reserved
21-16	P1_TS_SEQ_ID_OFFSET	Port 1 Time Sync Sequence ID Offset. This is the number of octets that the sequence ID is offset in the transmit and receive time sync message header. The minimum value is 6.
15-0	P1_TS_LTYPE	Port 1 Time Sync LTYPE. This is the LTYPE value to match for transmit and receive time sync messages.
End of Table 3-69		

3.6.1.25 Port 1 Time Sync VLAN LTYPE Register (P1_TS_VLAN_LTYPE)

The port 1 time sync VLAN LTYPE register is shown in Figure 3-61 and described in Table 3-70.

Figure 3-61 Port 1 Time Sync VLAN LTYPE Register (P1_TS_VLAN_LTYPE)



Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

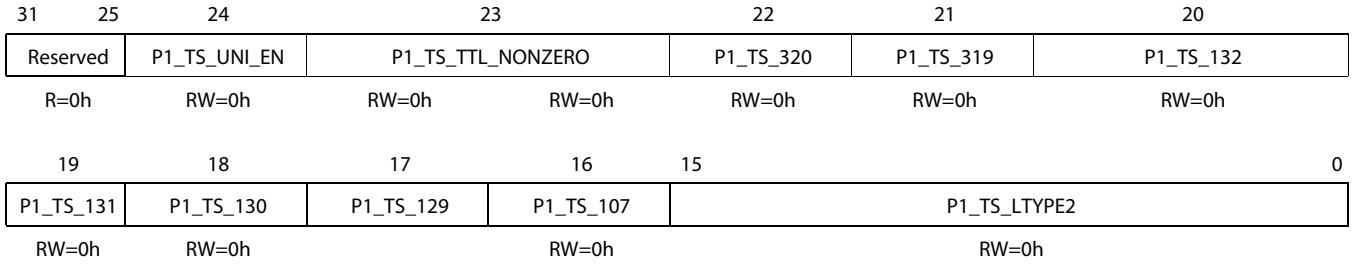
Table 3-70 Port 1 Time Sync VLAN LTYPE Register (P1_TS_VLAN_LTYPE) Field Descriptions

Bits	Field	Description
31-16	P1_TS_VLAN_LTYPE2	Port 1 Time Sync VLAN LTYPE2. This VLAN LTYPE value is used for port 1 transmit and receive time sync decode.
15-0	P1_TS_VLAN_LTYPE1	Port 1 Time Sync VLAN LTYPE1. This VLAN LTYPE value is used for port 1 transmit and receive time sync decode.
End of Table 3-70		

3.6.1.26 Port 1 Time Sync Control LTYPE2 Register (P1_TS_CTL_LTYPE2)

The port 1 time sync control LTYPE2 register is shown in Figure 3-62 and described in Table 3-71.

Figure 3-62 Port Time Sync Control LTYPE2 Register (P1_TS_CTL_LTYPE2)



Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-71 Port Time Sync Control LTYPE2 Register (P1_TS_CTL_LTYPE2) Field Descriptions

Bits	Field	Description
31-25	Reserved	Reserved
24	P1_TS_UNI_EN	Port 1 Time Sync Unicast Enable 0 – Unicast disabled 1 – Unicast enabled
23	P1_TS_TTL_NONZERO	Port 1 Time Sync Time to Live Non-zero enable 0 – TTL must be zero 1 – TTL may be non-zero
22	P1_TS_320	Port 1 Time Sync Destination Port Number 320 enable 0 – disabled 1 – destination port number (dec) 320 is enabled.
21	P1_TS_319	Port 1 Time Sync Destination Port Number 319 enable 0 – disabled 1 – destination port number (dec) 319 is enabled.
20	P1_TS_132	Port 1 Time Sync Destination IP Address 132 enable 0 – disabled 1 – destination IP address (dec) 224.0.1.132 is enabled.
19	P1_TS_131	Port 1 Time Sync Destination IP Address 131 enable 0 – disabled 1 – destination IP address (dec) 224.0.1.131 is enabled.
18	P1_TS_130	Port 1 Time Sync Destination IP Address 130 enable 0 – disabled 1 – destination IP address (dec) 224.0.1.130 is enabled.
17	P1_TS_129	Port 1 Time Sync Destination IP Address 129 enable 0 – disabled 1 – destination IP address (dec) 224.0.1.129 is enabled.
16	P1_TS_107	Port 1 Time Sync Destination IP Address 107 enable 0 – disabled 1 – destination IP address (dec) 224.0.0.107 is enabled.
15-0	P1_TS_LTYPE2	Port 1 Time Sync LTYPE2 This is the time sync LTYPE2 value for port 1.
End of Table 3-71		

3.6.1.27 Port 1 Time Sync Control 2 Register (P1_TS_CTL2)

The port 1 Time Sync Control 2 register is shown in Figure 3-63 and described in Table 3-72.

Figure 3-63 Port 1 Time Sync Control 2 Register (P1_TS_CTL2)

31 9	8 4	3 0
Reserved	P1_DOMAIN_OFFSET	P1_TS_MCAST_TYPE_EN
R-0	RW=4h	RW=0h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-72 Port 1 Time Sync Control 2 Register (P1_TS_CTL2) Field Descriptions

Bits	Field	Description
31-16	P1_DOMAIN_OFFSET	Domain offset value
15-0	P1_TS_MCAST_TYPE_EN	Multicast Type Enable
End of Table 3-72		

3.6.1.28 Port 1 Control Register (P1_CTL)

The port 1 Time Sync Control 2 register is shown in Figure 3-64 and described in Table 3-73

Figure 3-64 Port 1 Control Register (P1_CTL)

31 9	8	7	6
Reserved	P1_MACSEC_VLAN_PRI_EN	P1_MACSEC_VLAN_EN	P1_MACSEC_DEBUG
R-0	RW=0h	RW=0h	RW=0h

5	4	3 0
P1_MACSEC_CEF	P1_MACSEC_BYPASS_N	Reserved
RW=0h	RW=0h	R-0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-73 Port 1 Control Register (P1_CTL)

Bits	Field	Description
31-9	Reserved	Reserved
8	P1_MACSEC_VLAN_PRI_EN	Port 1 MACSEC VLAN Priority enable
7	P1_MACSEC_VLAN_EN	Port 1 MACSEC VLAN enable
6	P1_MACSEC_DEBUG	Port 1 MACSEC DEBUG – When set all packets from this port will be designated as MACSEC debug packets. Routing will depend on specified ALE modes.
5	P1_MACSEC_CEF	Port 1 MACSEC Copy Error Frames – when set, frames with MACSEC errors are copied to the host
4	P1_MACSEC_BYPASS_N	Port 1 MACSEC Bypass (asserted low) when set, MACSEC is bypassed on this port. When clear macsec_controlled will be set for all packet from this port. When set macsec_controlled is determined by the MACSEC lookup.
3-0	Reserved	Reserved
End of Table 3-73		

3.6.1.29 Port 2 Block Count Register (P2_BLK_CNT)

The port 2 block count register is shown in Figure 3-65 and described in Table 3-74.

Figure 3-65 Port 2 Block Count Register (P2_BLK_CNT)

31 14	13 9	8 6	5 0
Reserved	P2_TX_BLK_CNT	Reserved	P2_RX_BLK_CNT
R-0	RW=0	R-0	RW=1h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

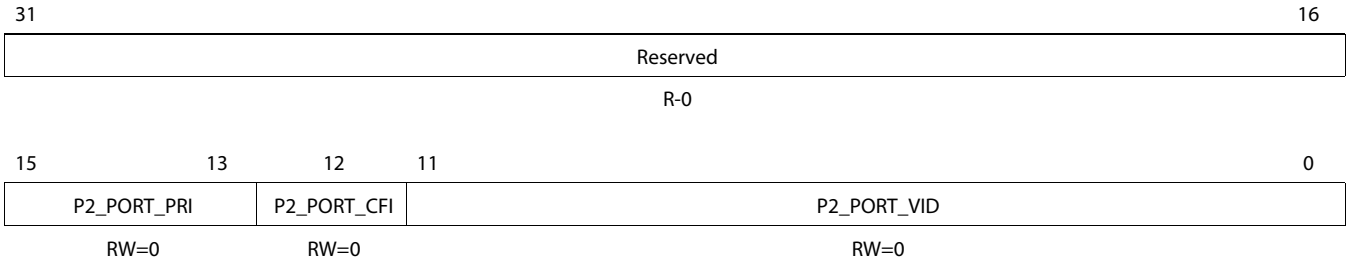
Table 3-74 Port 2 Block Count Register (P2_BLK_CNT) Field Descriptions

Bits	Field	Description
31-14	Reserved	Reserved
13-9	P2_TX_BLK_CNT	Port 2 Transmit Block Count Usage. This value is the number of blocks allocated to the FIFO logical transmit queues.
8-6	Reserved	Reserved
5-0	P2_RX_BLK_CNT	Port 2 Receive Block Count Usage. This value is the number of blocks allocated to the FIFO logical receive queues.
End of Table 3-74		

3.6.1.30 Port 2 VLAN Register (P2_PORT_VLAN)

The port 2 VLAN register is shown in Figure 3-66 and described in Table 3-75.

Figure 3-66 Port 2 VLAN Register (P2_PORT_VLAN)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

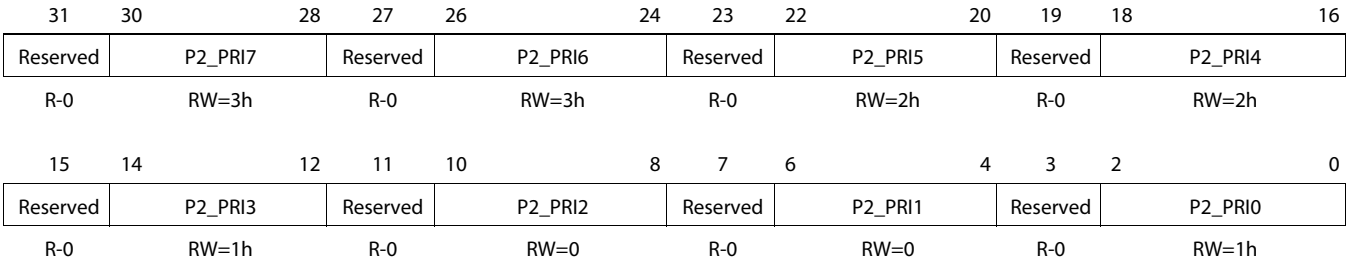
Table 3-75 Port 2 VLAN Register (P2_PORT_VLAN) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-13	P2_PORT_PRI	Port VLAN Priority (7 is highest priority)
12	P2_PORT_CFI	Port CFI bit
11-0	P2_PORT_VID	Port VLAN ID
End of Table 3-75		

3.6.1.31 Port 2 Transmit Header Priority to switch Priority Mapping Register (P2_TX_PRI_MAP)

The port 2 transmit header priority to switch priority mapping register is shown in Figure 3-67 and described in Table 3-76.

Figure 3-67 Port 2 Transmit Header Priority to switch Priority Mapping Register (P2_TX_PRI_MAP)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

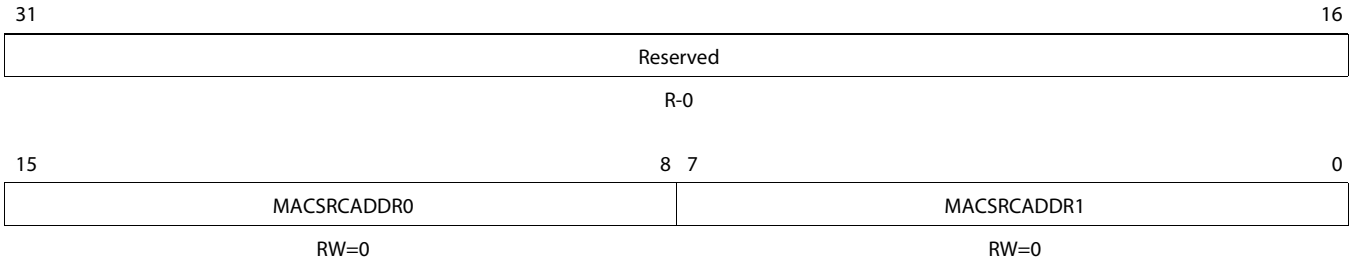
Table 3-76 P2 Transmit Header Priority to switch Priority Mapping Register (P2_TX_PRI_MAP) Field Descriptions

Bits	Field	Description
31	Reserved	Reserved
30-28	P2_PRI7	Port 2 Priority 7. A packet header priority of 7h is given this switch queue priority.
27	Reserved	Reserved
26-24	P2_PRI6	Port 2 Priority 6. A packet header priority of 6h is given this switch queue priority.
23	Reserved	Reserved
22-20	P2_PRI5	Port 2 Priority 5. A packet header priority of 5h is given this switch queue priority.
19	Reserved	Reserved
18-16	P2_PRI4	Port 2 Priority 4. A packet header priority of 4h is given this switch queue priority.
15	Reserved	Reserved
14-12	P2_PRI3	Port 2 Priority 3. A packet header priority of 3h is given this switch queue priority.
11	Reserved	Reserved
10-8	P2_PRI2	Port 2 Priority 2. A packet header priority of 2h is given this switch queue priority.
7	Reserved	Reserved
6-4	P2_PRI1	Port 2 Priority 1. A packet header priority of 1h is given this switch queue priority.
3	Reserved	Reserved
2-0	P2_PRI0	Port 2 Priority 0. A packet header priority of 0h is given this switch queue priority.
End of Table 3-76		

3.6.1.32 MAC2 Source Address Low Register (MAC2_SA_LO)

The MAC2 source address low register is shown in Figure 3-68 and described in Table 3-77.

Figure 3-68 MAC2 Source Address Low Register (MAC2_SA_LO)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-77 MAC2 Source Address Low Register (MAC2_SA_LO) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-8	MACSRCADDR0	Source address bits 7-0 (byte 0).
7-0	MACSRCADDR1	Source Address bits 15-8(byte 1).
End of Table 3-77		

3.6.1.33 MAC2 Source Address High Register (MAC2_SA_HI)

The MAC2 source address high register is shown in Figure 3-69 and described in Table 3-78.

Figure 3-69 MAC2 Source Address High Register (MAC2_SA_HI)

31 — 24	23 — 16
MACSRCADDR2	MACSRCADDR3
RW=0	RW=0

15 — 8	7 — 0
MACSRCADDR4	MACSRCADDR5
RW=0	RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-78 MAC2 Source Address High Register (MAC2_SA_HI) Field Descriptions

Bits	Field	Description
31-24	MACSRCADDR2	Source Address bits 23-16 (byte 2)
23-16	MACSRCADDR3	Source Address bits 31-24 (byte 3)
15-8	MACSRCADDR4	Source Address bits 39-32 (byte 4)
7-0	MACSRCADDR5	Source Address bits 47-40 (byte 5)
End of Table 3-78		

3.6.1.34 Port 2 Time Sync Control Register (P2_TS_CTL)

The port 2 time sync control register is shown in Figure 3-70 and described in Table 3-79.

Figure 3-70 Port 2 Time Sync Control Register (P2_TS_CTL)

31 — 16	15 — 11	10	9	8	7	6
TX_MSG_TYPE_EN	Reserved	TX_ANNEX_E_EN	RX_ANNEX_E_EN	LTYPE2_EN	TX_ANNEX_D_EN	TX_VLAN_LTYPE2_EN
RW=0				R-0		RW=0

5	4	3	2	1	0
TX_VLAN_LTYPE1_EN	TX_ANNEX_F_EN	RX_ANNEX_D_EN	RX_VLAN_LTYPE2_EN	TX_VLAN_LTYPE1_EN	RX_ANNEX_F_EN
RW=0		RW=0	R-0	RW=0	RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-79 Port 2 Time Sync Control Register (P2_TS_CTL) Field Descriptions (Part 1 of 2)

Bits	Field	Description
31-16	TX_MSG_TYPE_EN	Port 2 Time Sync Message Type Enable. Each bit in this field enables the corresponding message type in receive and transmit time sync messages (Bit 0 enables message type 0 etc.).
15-11	Reserved	Reserved
10	TX_ANNEX_E_EN	Port 2 Time Sync Transmit Annex E enable
9	RX_ANNEX_E_EN	Port 2 Time Sync Receive Annex E enable

Table 3-79 Port 2 Time Sync Control Register (P2_TS_CTL) Field Descriptions (Part 2 of 2)

Bits	Field	Description
8	LTYPE2_EN	Port 2 Time Sync LTYPE 2 enable (transmit and receive)
7	TX_ANNEX_D_EN	Port 2 Time Sync Transmit Annex D enable
6	TX_VLAN_LTYPE2_EN	Port 2 Time Sync Transmit VLAN LTYPE 2 enable.
5	TX_VLAN_LTYPE1_EN	Port 2 Time Sync Transmit VLAN LTYPE 1 enable.
4	TX_ANNEX_F_EN	Port 2 Time Sync Transmit Annex F Enable.
3	RX_ANNEX_D_EN	Port 2 Time Sync Receive Annex D enable
2	RX_VLAN_LTYPE2_EN	Port 2 Time Sync Receive VLAN LTYPE 2 enable.
1	TX_VLAN_LTYPE1_EN	Port 2 Time Sync Receive VLAN LTYPE 1 enable.
0	RX_ANNEX_F_EN	Port 2 Time Sync Receive Annex F Enable.
End of Table 3-79		

3.6.1.35 Port 2 Time Sync Sequence ID and LTYPE Register (P2_TS_SEQ_LTYPE)

The port 2 time sync sequence ID and LTYPE register is shown in Figure 3-71 and described in Table 3-80.

Figure 3-71 Port 2 Time Sync Sequence ID and LTYPE Register (P2_TS_SEQ_LTYPE)

31 22	21 16	15 0
Reserved	P2_TS_SEQ_ID_OFFSET	P2_TS_LTYPE
R-0	RW=1Eh	RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-80 Port 2 Time Sync Sequence ID and LTYPE Register (P2_TS_SEQ_LTYPE) Field Descriptions

Bits	Field	Description
31-22	Reserved	Reserved
21-16	P2_TS_SEQ_ID_OFFSET	Port 2 Time Sync Sequence ID Offset. This is the number of octets that the sequence ID is offset in the transmit and receive time sync message header. The minimum value is 6.
15-0	P2_TS_LTYPE	Port 2 Time Sync LTYPE. This is the LTYPE value to match for transmit and receive time sync messages.
End of Table 3-80		

3.6.1.36 Port 2 Time Sync VLAN LTYPE Register (P2_TS_VLAN_LTYPE)

The port 2 time sync VLAN LTYPE register is shown in Figure 3-72 and described in Table 3-81.

Figure 3-72 Port 2 Time Sync VLAN LTYPE Register (P2_TS_VLAN_LTYPE)

31 16	15 0
P2_TS_VLAN_LTYPE2	P2_TS_VLAN_LTYPE1
RW=8100h	RW=8100h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-81 Port 2 Time Sync VLAN LTYPE Register (P2_TS_VLAN_LTYPE) Field Descriptions

Bits	Field	Description
31-16	P2_TS_VLAN_LTYPE2	Port 2 Time Sync VLAN LTYPE2. This VLAN LTYPE value is used for port 2 transmit and receive time sync decode.
15-0	P2_TS_VLAN_LTYPE1	Port 2 Time Sync VLAN LTYPE1. This VLAN LTYPE value is used for port 2 transmit and receive time sync decode.
End of Table 3-81		

3.6.1.37 Port 2 Time Sync Control LTYPE2 Register (P2_TS_CTL_LTYPE2)

The port 2 time sync control LTYPE2 register is shown in Figure 3-73 and described in Table 3-82.

Figure 3-73 Port 2Time Sync Control LTYPE2 Register (P2_TS_CTL_LTYPE2)

31 25	24	23	22	21	20
Reserved	P2_TS_UNI_EN	P2_TS_TTL_NONZERO	P2_TS_320	P2_TS_319	P2_TS_132
R=0h	RW=0h	RW=0h RW=0h	RW=0h	RW=0h	RW=0h

19	18	17	16	15 0
P2_TS_131	P2_TS_130	P2_TS_129	P2_TS_107	P2_TS_LTYPE2
RW=0h	RW=0h	RW=0h		RW=0h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-82 Port 2 Time Sync Control LTYPE2 Register (P2_TS_CTL_LTYPE2) Field Descriptions (Part 1 of 2)

Bits	Field	Description
31-25	Reserved	Reserved
24	P2_TS_UNI_EN	Port 2 Time Sync Unicast Enable 0 – Unicast disabled 1 – Unicast enabled
23	P2_TS_TTL_NONZERO	Port 2 Time Sync Time to Live Non-zero enable 0 – TTL must be zero 1 – TTL may be non-zero
22	P2_TS_320	Port 2 Time Sync Destination Port Number 320 enable 0 – disabled 1 – destination port number (dec) 320 is enabled.
21	P2_TS_319	Port 2 Time Sync Destination Port Number 319 enable 0 – disabled 1 – destination port number (dec) 319 is enabled.
20	P2_TS_132	Port 2 Time Sync Destination IP Address 132 enable 0 – disabled 1 – destination IP address (dec) 224.0.1.132 is enabled.
19	P2_TS_131	Port 2 Time Sync Destination IP Address 131 enable 0 – disabled 1 – destination IP address (dec) 224.0.1.131 is enabled.
18	P2_TS_130	Port 2 Time Sync Destination IP Address 130 enable 0 – disabled 1 – destination IP address (dec) 224.0.1.130 is enabled.

Table 3-82 Port 2 Time Sync Control LTYPE2 Register (P2_TS_CTL_LTYPE2) Field Descriptions (Part 2 of 2)

Bits	Field	Description
17	P2_TS_129	Port 2 Time Sync Destination IP Address 129 enable 0 – disabled 1 – destination IP address (dec) 224.0.1.129 is enabled.
16	P2_TS_107	Port 2 Time Sync Destination IP Address 107 enable 0 – disabled 1 – destination IP address (dec) 224.0.0.107 is enabled.
15-0	P2_TS_LTYPE2	Port 2 Time Sync LTYPE2 This is the time sync LTYPE2 value for port 2.
End of Table 3-82		

3.6.1.38 Port 2 TIme Sync Control 2 Register (P2_TS_CTL2)

The port 2 Time Sync Control 2 register is shown in Figure 3-74 and described in Table 3-83.

Figure 3-74 Port 2 Time Sync Control 2 Register (P2_TS_CTL2)

31 9	8 4	3 0
Reserved	P2_DOMAIN_OFFSET	P2_TS_MCAST_TYPE_EN
R-0	RW=4h	RW=0h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-83 Port 2 Time Sync Control 2 Register (P2_TS_CTL2) Field Descriptions

Bits	Field	Description
31-16	P2_DOMAIN_OFFSET	Domain offset value
15-0	P2_TS_MCAST_TYPE_EN	Multicast Type Enable
End of Table 3-83		

3.6.1.39 Port 2 Control Register (P2_CTL)

The port 2 Time Sync Control 2 register is shown in Figure 3-75 and described in Table 3-84

Figure 3-75 Port 2 Control Register (P2_CTL)

31 9	8	7	6
Reserved	P2_MACSEC_VLAN_PRI_EN	P2_MACSEC_VLAN_EN	P2_MACSEC_DEBUG
R-0	RW=0h	RW=0h	RW=0h

5	4	3 0
P2_MACSEC_CEF	P2_MACSEC_BYPASS_N	Reserved
RW=0h	RW=0h	R-0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-84 Port 2 Control Register (P2_CTL)

Bits	Field	Description
31-9	Reserved	Reserved
8	P2_MACSEC_VLAN_PRI_EN	Port 2 MACSEC VLAN Priority enable
7	P2_MACSEC_VLAN_EN	Port 2 MACSEC VLAN enable
6	P2_MACSEC_DEBUG	Port 2 MACSEC DEBUG – When set all packets from this port will be designated as MACSEC debug packets. Routing will depend on specified ALE modes.
5	P2_MACSEC_CEF	Port 2 MACSEC Copy Error Frames – when set, frames with MACSEC errors are copied to the host
4	P2_MACSEC_BYPASS_N	Port 2 MACSEC Bypass (asserted low) when set, MACSEC is bypassed on this port. When clear macsec_controlled will be set for all packet from this port. When set macsec_controlled is determined by the MACSEC lookup.
3-0	Reserved	Reserved
End of Table 3-84		

3.6.2 Ethernet Media Access Controller (EMAC) submodule

This section describes the registers available in the Ethernet Media Access Controller (EMAC) modules. There are two EMAC modules in the Ethernet switch. EMAC1 is used with switch Port 1 and EMAC2 is used with Port 2. The EMAC1 and EMAC2 modules each have identical registers. The memory offset addresses listed in this section in Table 3-85 are relative to the EMAC module. To determine the starting address offset of each EMAC module, please see Table 3-44. For convenience, a complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-85 lists the registers in the Ethernet Media Access Controller (EMAC) module and the corresponding offset address for each register.

Table 3-85 EMAC Registers

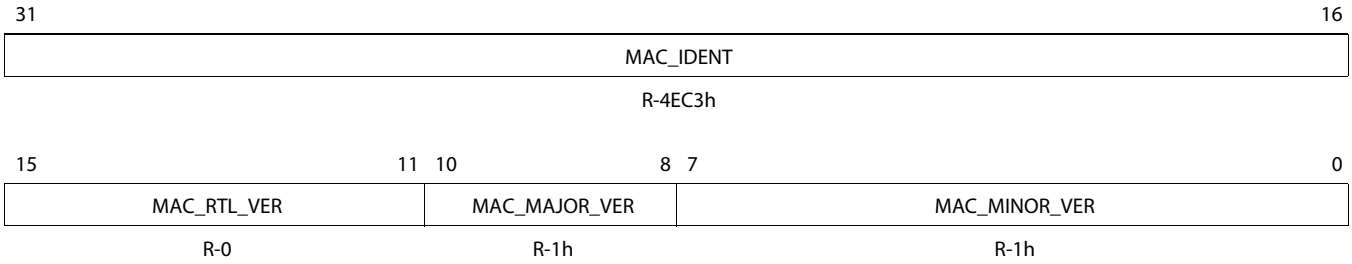
Offset Address[1]	Acronym	Register Name	Section
000h	MAC_IDVER	MAC Identification and Version Register	Section 3.6.2.1
004h	MAC_MAC_CTL	MAC Control Register	Section 3.6.2.3
008h	MAC_MAC_STATUS	MAC Status Register	Section 3.6.2.3
00Ch	MAC_SOFT_RESET	Soft Reset Register	Section 3.6.2.4
010h	MAC_RX_MAXLEN	RX Maximum Length Register	Section 3.6.2.5
014h	Reserved	Reserved	Reserved
018h	MAC_RX_PAUSE	Receive Pause Timer Register	Section 3.6.2.6
01Ch	MAC_TX_PAUSE	Transmit Pause Timer Register	Section 3.6.2.7
020h	MAC_EM_CTL	Emulation Control	Section 3.6.2.8
024h	Reserved	Reserved	Reserved
028h	MAC_TX_GAP	TX Inter-Packet Gap Register	Section 3.6.2.9
02Ch-0FCh	Reserved	Reserved	Reserved
End of Table 3-85			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.6.2.1 MAC Identification and Version Register (MAC_IDVER)

The MAC identification and version register is shown in Figure 3-76 and described in Table 3-86.

Figure 3-76 MAC Identification and Version Register (MAC_IDVER)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

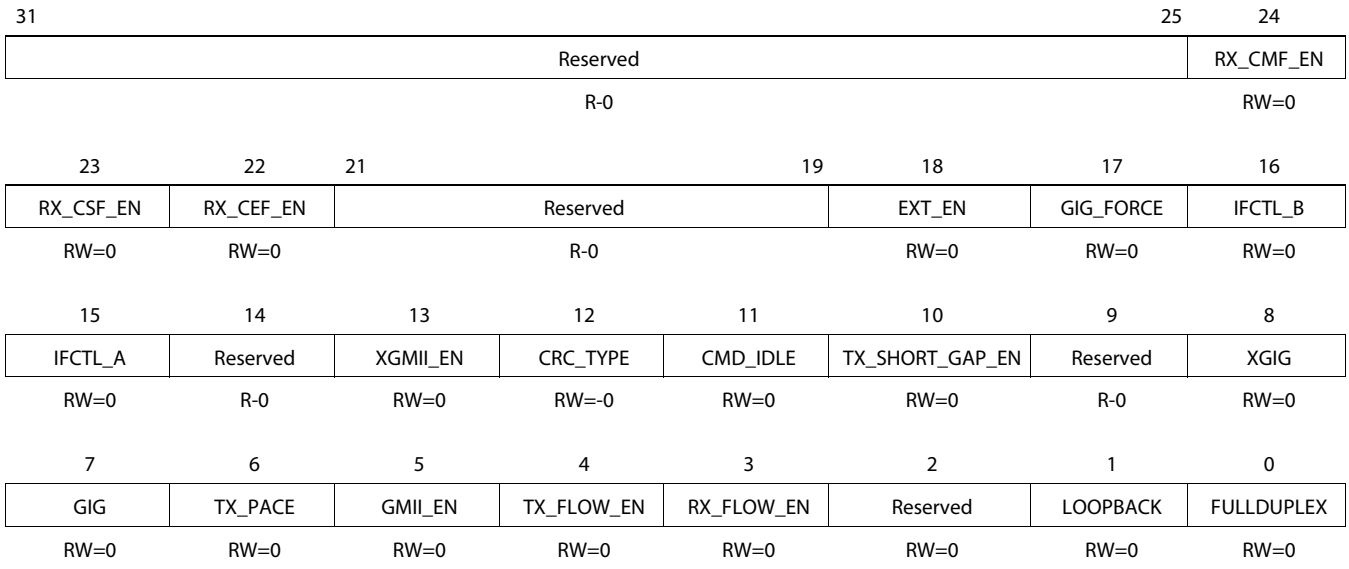
Table 3-86 MAC Identification and Version Register (MAC_IDVER) Field Descriptions

Bits	Field	Description
31-16	MAC_IDENT	Identification Value
15-11	MAC_RTL_VER	RTL Version Value
10-8	MAC_MAJOR_VER	Major Version Value
7-0	MAC_MINOR_VER	Minor Version Value
End of Table 3-86		

3.6.2.2 MAC Control Register (MAC_CONTROL)

The MAC control register is shown in Figure 3-77 and described in Table 3-87.

Figure 3-77 MAC Control Register (MAC_CONTROL)



Legend: R = Read only; W = Write only; -*n* = value after reset

Table 3-87 MAC Control Register (MAC_CONTROL) Field Descriptions (Part 1 of 2)

Bits	Field	Description
31-25	Reserved	Reserved
24	RX_CMF_EN	Receive Copy MAC Control Frames Enable. Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied to memory. MAC control frames that are pause frames will be acted upon if enabled in the MAC_CTL register, regardless of the value of RX_CMF_EN. Frames transferred to memory due to RX_CMF_EN will have the CONTROL bit set in their EOP buffer descriptor. 0 = MAC control frames are filtered (but acted upon if enabled). 1 = MAC control frames are transferred to memory.
23	RX_CSF_EN	RX Copy Short Frames Enable – Enables frames or fragments shorter than 64 bytes to be copied to memory. Frames transferred to memory due to RX_CSF_EN will have the FRAGMENT or UNDERSIZED bit set in their receive footer. Fragments are short frames that contain CRC/align/code errors and undersized are short frames without errors. 0 = Short frames are filtered. 1 = Short frames are transferred to memory.
22	RX_CEF_EN	RX Copy Error Frames Enable – Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive footer. Frames containing errors will be filtered when RX_CEF_EN is not set. 0 = Frames containing errors are filtered. 1 = Frames containing errors are transferred to memory.
21-19	Reserved	Reserved
18	EXT_EN	Control Enable. Enables the fullduplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the FULLDUPLEX and GIG bits in this register. The FULLDUPLEX_MODE bit reflects the actual fullduplex mode selected.
17	GIG_FORCE	Gigabit Mode Force. This bit is used to force the MAC into gigabit mode if the input GMII_MTCLK has been stopped by the PHY.
16	IFCTL_B	Interface Control B. Intended as a general purpose output bit to be used to control external gaskets associated with the GMII (GMII to RGMII etc.).
15	IFCTL_A	Interface Control A. Intended as a general purpose output bit to be used to control external gaskets associated with the GMII (GMII to RGMII etc.).
14	Reserved	Reserved
13	XGMII_EN	XGMII Enable – 0 – XGMII RX and TX held in reset. 1 – XGMII RX and TX released from reset.
12	CRC_TYPE	Port CRC Type 0 – Ethernet CRC 1 – Castagnoli CRC
11	CMD_IDLE	Command Idle. 0 = Idle not commanded. 1 = Idle Commanded (read IDLE in MACSTATUS).
10	TX_SHORT_GAP_EN	Transmit Short Gap Enable. 0 = Transmit with a short IPG is disabled. 1 = Transmit with a short IPG (when TX_SHORT_GAP input is asserted) is enabled.
9	Reserved	Reserved
8	XGIG	10 Gigabit Mode 0 – 10/100/1G mode as determined by gig 1 – 10 Gigabit mode
7	GIG	Gigabit Mode. The GIG_OUT output is the value of this bit. 0 = 10/100 mode. 1 = Gigabit mode (full duplex only).
6	TX_PACE	Transmit Pacing Enable. 0 = Transmit Pacing Disabled. 1 = Transmit Pacing Enabled.

Table 3-87 MAC Control Register (MAC_CONTROL) Field Descriptions (Part 2 of 2)

Bits	Field	Description
5	GMII_EN	GMII Enable. 0 = GMII receive and transmit held in reset. 1 = GMII receive and transmit released from reset.
4	TX_FLOW_EN	Transmit Flow Control Enable. Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_ENABLE bits determine whether or not received pause frames are transferred to memory. 0 = Transmit Flow Control Disabled. Full-duplex mode – Incoming pause frames are not acted upon. 1 = Transmit Flow Control Enabled. Full-duplex mode – Incoming pause frames are acted upon.
3	RX_FLOW_EN	Receive Flow Control Enable. 0 = Receive Flow Control Disabled Half-duplex mode – No flow control generated collisions are sent. Full-duplex mode – No outgoing pause frames are sent. 1 = Receive Flow Control Enabled Half-duplex mode – Collisions are initiated when receive flow control is triggered. Full-duplex mode - Outgoing pause frames are sent when receive flow control is triggered.
2	Reserved	Reserved
1	LOOPBACK	Loop Back Mode. Loopback mode forces internal fullduplex mode regardless of whether the FULLDUPLEX bit is set or not. The LOOPBACK bit should be changed only when GMII_EN is deasserted. 0 = Not looped back. 1 = Loop Back Mode enabled.
0	FULLDUPLEX	Full Duplex mode. Gigabit mode forces fullduplex mode regardless of whether the FULLDUPLEX bit is set or not. The FULLDUPLEX_OUT output is the value of this register bit. 0 = half duplex mode. 1 = full duplex mode.
End of Table 3-87		

3.6.2.3 MAC Status Register (MACSTATUS)

The MAC control register is shown in Figure 3-78 and described in Table 3-88.

Figure 3-78 MAC Status Register (MACSTATUS)

31	30 5	4	3	2	1	0
IDLE	Reserved	EXT_GIG	EXT_FD	Reserved	RX_FLOW_ACT	TX_FLOW_ACT
R-1h	R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-88 MAC Status Register (MACSTATUS) Field Descriptions (Part 1 of 2)

Bits	Field	Description
31	IDLE	IDLE – The MAC is in the idle state (valid after an idle command). 0 = The MAC is not in the idle state. 1 = The MAC is in the idle state.
30-5	Reserved	Reserved
4	EXT_GIG	External GIG. This is the value of the EXT_GIG input bit.
3	EXT_FD	External Fullduplex. This is the value of the EXT_FULLDUPLEX input bit.

Table 3-88 MAC Status Register (MACSTATUS) Field Descriptions (Part 2 of 2)

Bits	Field	Description
21	RX_FLOW_ACT	Receive Flow Control Active. When asserted, indicates that receive flow control is enabled and triggered.
0	TX_FLOW_ACT	Transmit Flow Control Active. When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete.
End of Table 3-88		

3.6.2.4 Software Reset Register (SOFT_RESET)

The software reset register is shown in Figure 3-79 and described in Table 3-89.

Figure 3-79 Software Reset Register (SOFT_RESET)

31	1	0
Reserved		SOFT_RESET
R-0		RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-89 Software Reset Register (SOFT_RESET) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	SOFT_RESET	Software reset. Writing a one to this bit causes the MAC logic to be reset. After writing a one to this bit, it may be polled to determine if the reset has occurred. If a one is read, the reset has not yet occurred. If a zero is read then reset has occurred.
End of Table 3-89		

3.6.2.5 Receive Maximum Length Register (RX_MAXLEN)

The receive maximum length register is shown in Figure 3-80 and described in Table 3-90.

Figure 3-80 Receive Maximum Length Register (RX_MAXLEN)

31	14	13	0
Reserved		RX_MAXLEN	
R-0		RW=5EEh	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-90 Receive Maximum Length Register (RX_MAXLEN) Field Descriptions

Bits	Field	Description
31-14	Reserved	Reserved
13-0	RX_MAXLEN	Reserved Maximum Frame Length. This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than RX_MAXLEN are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 16,383.
End of Table 3-90		

3.6.2.6 Receive Pause Timer Register (RX_PAUSE)

The receive pause timer register is shown in Figure 3-81 and described in Table 3-91.

Figure 3-81 Receive Pause Timer Register (RX_PAUSE)

31	16	15	0
Reserved		RX_PAUSETIMER	
R-0		R=0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-91 Receive Pause Timer Register (RX_PAUSE) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	RX_PAUSETIMER	Receive Pause Timer Value. This field allows the contents of the receive pause timer to be observed. The receive pause timer is loaded with FF00h when the MAC sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated.
End of Table 3-91		

3.6.2.7 Transmit Pause Timer Register (TX_PAUSE)

The transmit pause timer register is shown in Figure 3-82 and described in Table 3-92.

Figure 3-82 Transmit Pause Timer Register (TX_PAUSE)

31	16	15	0
Reserved		TX_PAUSETIMER	
R-0		R=0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-92 Receive Pause Timer Register (TX_PAUSE) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_PAUSETIMER	Transmit Pause Timer Value. This field allows the contents of the transmit pause timer to be observed. The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slot time intervals, down to zero at which time MAC transmit frames are again enabled.
End of Table 3-92		

3.6.2.8 Emulation Control Register (EM_CONTROL)

The emulation control register is shown in Figure 3-83 and described in Table 3-93.

Figure 3-83 Emulation Control Register (EM_CONTROL)

31	2	1	0
Reserved		SOFT	FREE
R-0		RW=0	RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-93 Emulation Control Register (EM_CONTROL) Field Descriptions

Bits	Field	Description
31-2	Reserved	Reserved
1	SOFT	Emulation Soft Bit.
0	FREE	Emulation Free Bit.
End of Table 3-93		

3.6.2.9 TX Inter-Packet Gap Register (MAC_TX_GAP)

The tx inter-packet gap register is shown in Figure 3-84 and described in Table 3-94.

Figure 3-84 Receive Packet Priority to Header Priority Mapping Register (MAC_RX_PRI_MAP)

31	16	15	0
Reserved		TX_GAP	
R-0		RW-Ch	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-94 Receive Packet Priority to Header Priority Mapping Register (MAC_RX_PRI_MAP) Field Descriptions

Bits	Field	Description
31-16	Reserved	Reserved
15-0	TX_GAP	Transmit Inter-Packet Gap GMII modes – This is the default gap value and only bits 8:0 are used. This can be increased from 12 to increase the gap between packets. XGMII mode – In 10 gigabit mode this is the short gap rate and should be changed to 5000 (0x1388) to get approximately 200ppm faster when short gap is triggered and enabled
End of Table 3-94		

3.6.3 Statistics (STATS) Submodule

This section describes the registers available in the Statistics (STATS) modules. There are three STATS modules in the Ethernet switch, one for each port (0,1 & 2). Port 1 and Port 2 have identical modules. Port 0 has only a sub-set of the registers listed in this section. To see which registers are not present in Port 0's module please see Table 3-2. The memory address offsets listed in this section in Table 3-95 are relative to the STATS module. To determine the starting address offset of each STATS module, please see Table 3-44. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

Table 3-95 lists the registers in the Statistics (STATS) module and the corresponding offset address for each register.

Table 3-95 STATS Registers (Part 1 of 2)

Offset Address [1]	Acronym	Register Name	Section
00h	RXGOODFRAMES	Total number of good frames received	3.6.3.1
04h	RXBROADCASTFRAMES	Total number of good broadcast frames received	3.6.3.2
08h	RXMULTICASTFRAMES	Total number of good multicast frames received	3.6.3.3
0Ch	RXPAUSEFRAMES	Total number of pause frames received	3.6.3.4
10h	RXCRCERRORS	Total number of CRC errors frames received	3.6.3.5
14h	RXALIGNCODEERRORS	Total number of alignment/code errors received	3.6.3.6
18h	RXOVERSIZEDFRAMES	Total number of oversized frames received	3.6.3.7

Table 3-95 STATS Registers (Part 2 of 2)

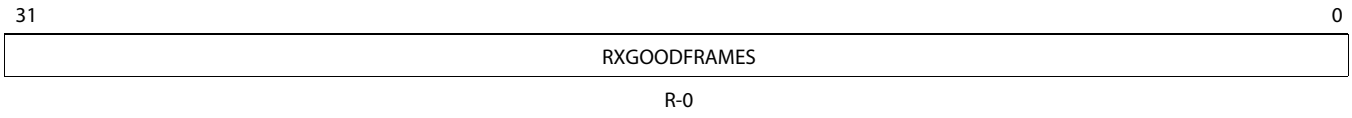
Offset Address [1]	Acronym	Register Name	Section
1Ch	RXJABBERFRAMES	Total number of jabber frames received	3.6.3.8
20h	RXUNDERSIZEDFRAMES	Total number of undersized frames received	3.6.3.9
24h	RXFRAGMENTS	Total number of fragment frames received	3.6.3.10
28h	Overrun Type 4	Type 4 Overrun	3.6.3.11
2Ch	Overrun Type 5	Type 5 Overrun	3.6.3.12
30h	RXOCTETS	Total number of received bytes in good frames	3.6.3.13
34h	TXGOODFRAMES	Total number of good frames transmitted	3.6.3.14
38h	TXBROADCASTFRAMES	Total number of good broadcast frames transmitted	3.6.3.15
3Ch	TXMULTICASTFRAMES	Total number of good multicast frames transmitted	3.6.3.16
40h	TXPAUSEFRAMES	Total number of pause frames transmitted	3.6.3.17
44h	TXDEFERREDFRAMES	Total number of frames deferred	3.6.3.18
48h	TXCOLLISIONFRAMES	Total number of collisions	3.6.3.19
4Ch	TXSINGLECOLLFRAMES	Total number of single collision transmit frames	3.6.3.20
50h	TXMULTCOLLFRAMES	Total number of multiple collision transmit frames	3.6.3.21
54h	TXEXCESSIVECOLLISIONS	Total number of transmit frames aborted due to excessive collisions	3.6.3.22
58h	TXLATECOLLISIONS	Total number of late collisions	3.6.3.23
5Ch	IPGERR	Receive Inter Packet Gap Error (10G only)	3.6.3.24
60h	TXCARRIERSENSEERRORS	Total number of carrier sense errors	3.6.3.25
64h	TXOCTETS	Total number of octets transmitted	3.6.3.26
68h	64OCTETFRAMES	Total number of 64 octet frames transmitted	3.6.3.27
6Ch	65T127OCTETFRAMES	Total number of 65-127 octet frames transmitted	3.6.3.28
70h	128T255OCTETFRAMES	Total number of 128-255 octet frames transmitted	3.6.3.29
74h	256T511OCTETFRAMES	Total number of 256-511 octet frames transmitted	3.6.3.30
78h	512T1023OCTETFRAMES	Total number of 512-1023 octet frames transmitted	3.6.3.31
7Ch	1024TUPOCTETFRAMES	Total number of 1023-1518 octet frames transmitted	3.6.3.32
80h	NETOCTETS	Total number of net octets	3.6.3.33
84h	RXSOFOVERRUNS	Total number of receive FIFO or DMA start of frame overruns	3.6.3.34
88h	RXMOFOVERRUNS	Total number of receive FIFO or DMA middle of frame overruns	3.6.3.35
8Ch	RXDMAOVERRUNS	Total number of receive DMA start of frame and middle of frame overruns	3.6.3.36
90h-FFh	Reserved	Reserved	Reserved
End of Table 3-95			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.6.3.1 Good Receive Frames Register (RXGOODFRAMES)

The good receive frames register is shown in Figure 3-85 and described in Table 3-96.

Figure 3-85 Good Receive Frames Register (RXGOODFRAMES)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-96 Good Receive Frames Register (RXGOODFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXGOODFRAMES	The total number of good frames received on the port. A frame must match all of the following criteria to be considered a good frame: • The frame was a data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.
End of Table 3-96		

3.6.3.2 Broadcast Receive Frames Register (RXBROADCASTFRAMES)

The broadcast receive frames register is shown in Figure 3-86 and described in Table 3-97.

Figure 3-86 Broadcast Receive Frames Register (RXBROADCASTFRAMES)

31	0
RXBROADCASTFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-97 Broadcast Receive Frames Register (RXBROADCASTFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXBROADCASTFRAMES	The total number of good broadcast frames received on the port. A frame must match all of the following criteria to be considered a good broadcast frame: • The frame was a data or MAC control frame which was destined for address FFFFFFFFFFFFh • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.
End of Table 3-97		

3.6.3.3 Multicast Receive Frames Register (RXMULTICASTFRAMES)

The multicast receive frames register is shown in Figure 3-87 and described in Table 3-98.

Figure 3-87 Multicast Receive Frames Register (RXMULTICASTFRAMES)

31	0
RXMULTICASTFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-98 Multicast Receive Frames Register (RXMULTICASTFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXMULTICASTFRAMES	The total number of good multicast frames received on the port. A frame must match all of the following criteria to be considered a good multicast frame: • The frame was a data or MAC control frame which was destined for any multicast address other than FFFFFFFFFFFFh • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.
End of Table 3-98		

3.6.3.4 Pause Receive Frames Register (RXPAUSEFRAMES)

The pause receive frames register is shown in Figure 3-88 and described in Table 3-99.

Figure 3-88 Pause Receive Frames Register (RXPAUSEFRAMES)

31	0
RXPAUSEFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-99 Pause Receive Frames Register (RXPAUSEFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXPAUSEFRAMES	The total number of IEEE 802.3X pause frames received on the port. A frame must match all of the following criteria to be considered a pause frame: • The frame contained a unicast, broadcast, or multicast address • The frame contains the length/type field value 88.08h and the opcode 0001h • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have a CRC error, alignment error or code error • Pause-frames were enabled on the port (TX_FLOW_EN = 1). The port could have been in half or full-duplex mode. Overruns have no effect on this statistic.
End of Table 3-99		

3.6.3.5 Receive CRC Errors Register (RXCRCERRORS)

The CRC errors receive frames register is shown in Figure 3-89 and described in Table 3-100.

Figure 3-89 Receive CRC Errors Register (RXCRCERRORS)

31	0
RXCRCERRORS	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-100 Receive CRC Errors Register (RXCRCERRORS) Field Descriptions

Bits	Field	Description
31-0	RXCRCERRORS	The total number of frames received on the port that experienced a CRC error. A frame must match all of the following criteria to be considered a CRC error frame: • The frame was a data or MAC control frame which matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have an alignment error or code error • The frame had a CRC error A CRC error must meet the following two conditions: • A frame that contains an even number of nibbles • A frame that fails the Frame Check Sequence test Overruns have no effect on this statistic.
End of Table 3-100		

3.6.3.6 Receive Align/Code Errors Register (RXALIGNCODEERRORS)

The receive align/code errors register is shown in Figure 3-90 and described in Table 3-101.

Figure 3-90 Receive Align/Code Errors Register (RXALIGNCODEERRORS)

31	0
RXALIGNCODEERRORS	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

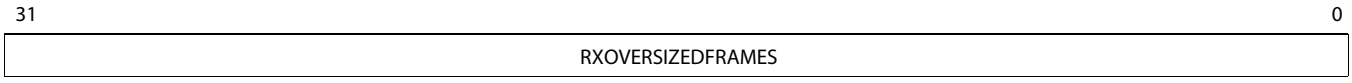
Table 3-101 Receive Align/Code Errors Register (RXALIGNCODEERRORS) Field Descriptions

Bits	Field	Description
31-0	RXALIGNCODEERRORS	The total number of frames received on the port that experienced an alignment error or code error. A frame must match all of the following criteria to be considered an alignment or code error frame: • The frame was a data or MAC control frame which matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame had an alignment error or code error An alignment error must meet the following two conditions: • A frame that contains an odd number of nibbles • A frame that fails the Frame Check Sequence test if the final nibble is ignored A code error must meet the following condition: • A frame that has been discarded because the port's MRXER pin driven with a 1 for at least one bit-time's duration at any point during the frame's reception Overruns have no effect on this statistic.
End of Table 3-101		

3.6.3.7 Oversize Receive Frames Register (RXOVERSIZEDFRAMES)

The oversize receive frames register is shown in Figure 3-91 and described in Table 3-102.

Figure 3-91 Oversize Receive Frames Register (RXOVERSIZEDFRAMES)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

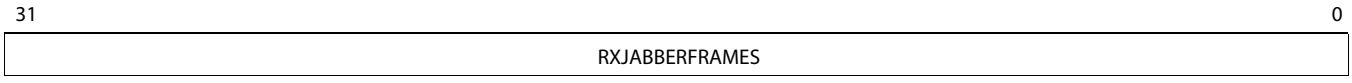
Table 3-102 Oversized Receive Frames Register (RXOVERSIZEDFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXOVERSIZEDFRAMES	The total number of oversized frames received on the port. A frame must match all of the following criteria to be considered an oversized frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was greater than RX_MAXLEN bytes • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.
End of Table 3-102		

3.6.3.8 Receive Jabber Frames Register (RXJABBERFRAMES)

The receive jabber frames register is shown in Figure 3-92 and described in Table 3-103.

Figure 3-92 Receive Jabber Frames Register (RXJABBERFRAMES)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-103 Receive Jabber Frames Register (RXJABBERFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXJABBERFRAMES	The total number of jabber frames received on the port. A frame must match all of the following criteria to be considered a jabber frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was greater than RX_MAXLEN bytes • The frame did had a CRC error, alignment error, or code error Overruns have no effect on this statistic.
End of Table 3-103		

3.6.3.9 Undersize (Short) Receive Frames Register (RXUNDERSIZEDFRAMES)

The undersize (short) receive frames register is shown in Figure 3-93 and described in Table 3-104.

Figure 3-93 Undersize (Short) Receive Frames Register (RXUNDERSIZEDFRAMES)

31	0
RXUNDERSIZEDFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-104 Undersized (Short) Receive Frames Register (RXUNDERSIZEDFRAMES) Field Descriptions

Bits	Field	Description
31-0	RXUNDERSIZEDFRAMES	The total number of undersized frames received on the port. A frame must match all of the following criteria to be considered an undersized frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was less than 64 bytes • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.
End of Table 3-104		

3.6.3.10 Receive Fragment Register (RXFRAGMENTS)

The receive fragment frames register is shown in Figure 3-94 and described in Table 3-105.

Figure 3-94 Receive Fragment Register (RXFRAGMENTS)

31	0
RXFRAGMENTS	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

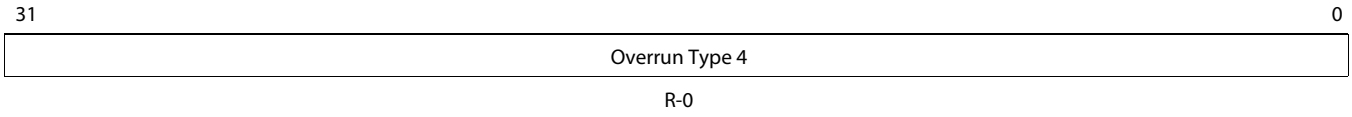
Table 3-105 Receive Fragment Frames Register (RXFRAGMENTS) Field Descriptions

Bits	Field	Description
31-0	RXFRAGMENTS	The total number of frame fragments received on the port. A frame fragment must match all of the following criteria to be considered a frame fragment: • The frame was a data frame (address matching does not matter) • The frame was less than 64 bytes • The frame had a CRC error, alignment error, or code error • The frame was not the result of a collision caused by half duplex, collision based flow control Overruns have no effect on this statistic.
End of Table 3-105		

3.6.3.11 Overrun Type 4

The overrun type 4 register is shown in Figure 3-95 and described in Table 3-106.

Figure 3-95 Overrun Type 4



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

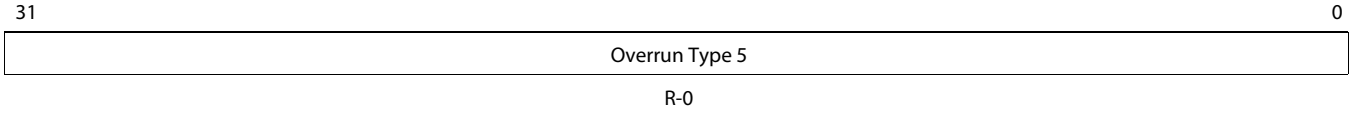
Table 3-106 Overrun Type 4

Bits	Field	Description
31-0	Overrun Type 4	The total number of frames received on a port such that the destination port was not equal to the source port but the frame was not forwarded to any port. • was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and • was any length (including <64 bytes and > rx_maxlen bytes), and • the destination port was not equal to the source port and had a zero port_mask
End of Table 3-106		

3.6.3.12 Overrun Type 5

The overrun type 5register is shown in Figure 3-96 and described in Table 3-107.

Figure 3-96 Overrun Type 5



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

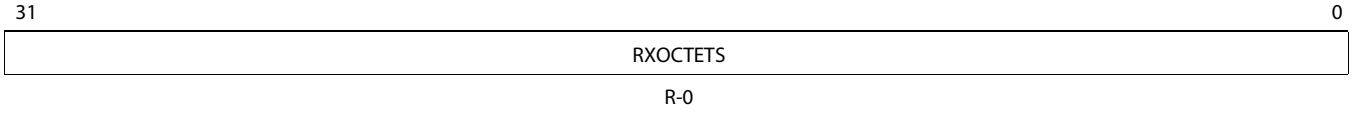
Table 3-107 Overrun Type 5

Bits	Field	Description
31-0	Overrun Type 5	The total number of frames received on a port that were dropped (zero port_mask) due to exceeding the maximum ALE lookup rate (Port 0 should have no type 5 overruns). • was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode, and • was any length (including <64 bytes and > rx_maxlen bytes), and • the maximum ALE lookup rate was exceeded so the lookup was aborted and the packet was dropped.
End of Table 3-107		

3.6.3.13 Receive Octets Register (RXOCTETS)

The receive octets frames register is shown in Figure 3-97 and described in Table 3-108.

Figure 3-97 Receive Octets Register (RXOCTETS)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-108 Receive Octets Register (RXOCTETS) Field Descriptions

Bits	Field	Description
31-0	RXOCTETS	The total number of bytes in all good frames received on the port. A frame must match all of the following criteria to be considered a good frame: • The frame was a data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode • The frame was of length 64 to RX_MAXLEN bytes inclusive • The frame did not have a CRC error, alignment error, or code error Overruns have no effect on this statistic.
End of Table 3-108		

3.6.3.14 Good Transmit Frames Register (TXGOODFRAMES)

The good transmit frames register is shown in Figure 3-98 and described in Table 3-109.

Figure 3-98 Good Transmit Frames Register (TXGOODFRAMES)

31	0
TXGOODFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-109 Good Transmit Frames Register (TXGOODFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXGOODFRAMES	The total number of good frames transmitted on the port. A frame must match all of the following criteria to be considered a good frame: • The frame was a data or MAC control frame which was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have late or excessive collisions, no carrier loss, and no underrun
End of Table 3-109		

3.6.3.15 Broadcast Transmit Frames Register (TXBROADCASTFRAMES)

The broadcast transmit frames register is shown in Figure 3-99 and described in Table 3-110.

Figure 3-99 Broadcast Transmit Frames Register (TXBROADCASTFRAMES)

31	0
TXBROADCASTFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-110 Broadcast Transmit Frames Register (TXBROADCASTFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXBROADCASTFRAMES	The total number of good broadcast frames transmitted on the port. A frame must match all of the following criteria to be considered a good broadcast frame: • The frame was a data or MAC control frame which was destined for address FFFFFFFFFFFFh • The frame was of any length • The frame did not have late or excessive collisions, no carrier loss, and no underrun
End of Table 3-110		

3.6.3.16 Multicast Transmit Frames (TXMULTICASTFRAMES)

The multicast transmit frames register is shown in Figure 3-100 and described in Table 3-111.

Figure 3-100 Multicast Transmit Frames (TXMULTICASTFRAMES)

31	0
TXMULTICASTFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-111 Multicast Transmit Frames Register (TXMULTICASTFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXMULTICASTFRAMES	The total number of good multicast frames transmitted on the port. A frame must match all of the following criteria to be considered a good multicast frame: • The frame was a data or MAC control frame which was destined for any multicast address other than FFFFFFFFFFFFh • The frame was of any length • The frame did not have late or excessive collisions, no carrier loss, and no underrun
End of Table 3-111		

3.6.3.17 Pause Transmit Frames (TXPAUSEFRAMES)

The pause transmit frames register is shown in Figure 3-101 and described in Table 3-112.

Figure 3-101 Pause Transmit Frames (TXPAUSEFRAMES)

31	0
TXPAUSEFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-112 Pause Transmit Frames Register (TXPAUSEFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXPAUSEFRAMES	The total number of IEEE 802.3X pause frames transmitted on the port. Pause frames cannot underrun or contain a CRC error because they are created in the transmitting MAC, so these error conditions have no effect on the statistic. Pause frames sent by software will not be included in this count. Since pause frames are only transmitted in full duplex mode, carrier loss and collisions have no effect on this statistic. Transmitted pause frames are always 64 byte multicast frames, so these frames will appear in the TXMULTICASTFRAMES and 64OCTECTFRAMES statistics.
End of Table 3-112		

3.6.3.18 Deferred Transmit Frames Register (TXDEFERREDFRAMES)

The deferred transmit frames register is shown in Figure 3-102 and described in Table 3-113.

Figure 3-102 Deferred Transmit Frames Register (TXDEFERREDFRAMES)

31	0
TXDEFERREDFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-113 Deferred Transmit Frames Register (TXDEFERREDFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXDEFERREDFRAMES	The total number of frames transmitted on the port that first experienced deferment. A frame must match all of the following criteria to be considered a deferred frame: • The frame was a data or MAC control frame which was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have carrier loss or underrun • The frame did not experience any collisions before being successfully transmitted • The frame found the medium busy when transmission was first attempted, so had to wait CRC errors have no effect on this statistic.
End of Table 3-113		

3.6.3.19 Transmit Frames Collision Register (TXCOLLISIONFRAMES)

The transmit frames collision register is shown in Figure 3-103 and described in Table 3-114.

Figure 3-103 Transmit Frames Collision Register (TXCOLLISIONFRAMES)

31	0
TXCOLLISIONFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-114 Transmit Frames Collision Register (TXCOLLISIONFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXCOLLISIONFRAMES	This statistic records the total number of times that this port has experienced a collision. Collisions occur under two circumstances: 1. When all of the following conditions are true for a transmit data or MAC control frame: – The frame was destined for any unicast, broadcast or multicast address – The frame was of any size – The frame had no carrier loss and no underrun – The frame experienced a collision. A jam sequence is sent for every non-late collision, so this statistic will increment on each occasion if a frame experiences multiple collisions (and increments on late collisions). CRC errors have no effect on this statistic. 2. When the port is in half-duplex mode, flow control is active, and a frame reception begins.
End of Table 3-114		

3.6.3.20 Transmit Frames Single Collision Register (TXSINGLECOLLFRAMES)

The transmit frames single collision register is shown in Figure 3-104 and described in Table 3-115.

Figure 3-104 Transmit Frames Single Collision Register (TXSINGLECOLLFRAMES)

31	0
TXSINGLECOLLFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-115 Transmit Frames Single Collision Register (TXSINGLECOLLFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXSINGLECOLLFRAMES	The total number of frames transmitted on the port that experience exactly one collision. A frame must match all of the following criteria to be considered a single collision frame: • The frame was a data or MAC control frame which was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have carrier loss or underrun • The frame experience one collision before successful transmission, and the collision was not late CRC errors have no effect on this statistic.
End of Table 3-115		

3.6.3.21 Transmit Frames Multiple Collision Register (TXMULTCOLLFRAMES)

The transmit frames multiple collision register is shown in Figure 3-105 and described in Table 3-116.

Figure 3-105 Transmit Frames Multiple Collision Register (TXMULTCOLLFRAMES)

31	0
TXMULTCOLLFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-116 Transmit Frames Multiple Collision Register (TXMULTCOLLFRAMES) Field Descriptions

Bits	Field	Description
31-0	TXMULTCOLLFRAMES	The total number of frames transmitted on the port that experience multiple collisions. A frame must match all of the following criteria to be considered a multiple collision frame: • The frame was a data or MAC control frame which was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have carrier loss or underrun • The frame experienced 2-15 collisions before successful transmission, and none of the collisions were late CRC errors have no effect on this statistic.
End of Table 3-116		

3.6.3.22 Excessive Collision Register (TXEXCESSIVECOLLISIONS)

The excessive collision register is shown in Figure 3-106 and described in Table 3-117.

Figure 3-106 Excessive Collision Register (TXEXCESSIVECOLLISIONS)

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-117 Excessive Collisions Register (TXECESSIVECOLLISIONS) Field Descriptions

Bits	Field	Description
31-0	TXEXCESSIVECOLLISIONS	The total number of frames on the port where transmission was abandoned due to excessive collisions. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame which was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have carrier loss or underrun • The frame experienced 16 collisions before abandoning all attempts at transmitting the frame, and none of the collisions were late CRC errors have no effect on this statistic.
End of Table 3-117		

3.6.3.23 Late Collisions Register (TXLATECOLLISIONS)

The transmit frames multiple collision register is shown in Figure 3-107 and described in Table 3-118.

Figure 3-107 Late Collisions Register (TXLATECOLLISIONS)

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

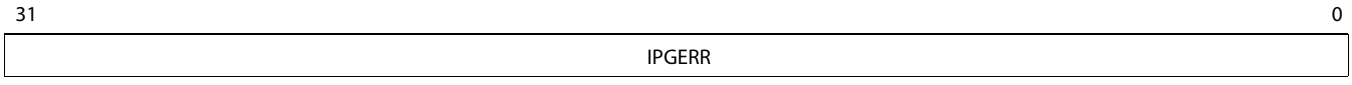
Table 3-118 Late Collisions Register (TXLATECOLLISIONS) Field Descriptions

Bits	Field	Description
31-0	TXLATECOLLISIONS	The total number of frames on the port where transmission was abandoned due to a late collision. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame which was destined for a unicast, broadcast or multicast address • The frame was of any length • The frame did not have carrier loss or underrun • The frame experienced a collision later than 512 bit-times into the transmission. There may have been up to 15 previous (non-late) collisions which had previously required the transmission to be re-attempted. The Late Collisions statistic dominates over the single, multiple and excessive Collisions statistics - if a late collision occurs the frame will not be counted in any of these other three statistics. CRC errors, carrier loss, and underrun have no effect on this statistic.
End of Table 3-118		

3.6.3.24 Inter-Packet Gap Register (IPGERR)

The transmit frames multiple collision register is shown in Figure 3-108 and described in Table 3-119.

Figure 3-108 Inter-Packet Gap Error (IPGERR)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

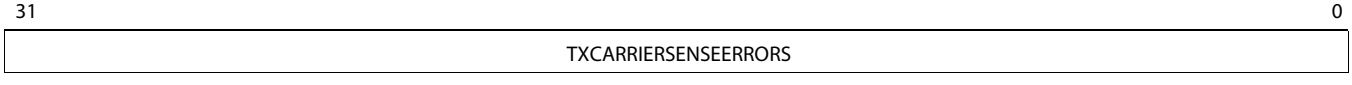
Table 3-119 Inter-Packet Gap Error (IPGERR)

Bits	Field	Description
31-0	IPGERR	The total number of 10G frames received on a port that had a correct preamble but did not have at least five bytes of IDLE preceding the frame. This does not indicate if the frame with the IPG error was kept or ignored
End of Table 3-119		

3.6.3.25 Carrier Sense Errors Register (TXCARRIERSENSEERRORS)

The carrier sense errors register is shown in Figure 3-109 and described in Table 3-120.

Figure 3-109 Carrier Sense Errors Register (TXCARRIERSENSEERRORS)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-120 Carrier Sense Errors Register (TXCARRIERSENSEERRORS) Field Descriptions

Bits	Field	Description
31-0	TXCARRIERSENSEERRORS	The total number of frames on the port that experience carrier loss. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame which was destined for a unicast, broadcast or multicast address • The frame was of any length • The carrier sense condition was lost or never asserted when transmitting the frame (the frame is not retransmitted). This is a transmit only statistic. Carrier Sense is a don't care for received frames. Transmit frames with carrier sense errors are sent until completion and are not aborted. CRC errors and underrun have no effect on this statistic.
End of Table 3-120		

3.6.3.26 Transmit Octets Register (TXOCTETS)

The transmit octets register is shown in Figure 3-110 and described in Table 3-121.

Figure 3-110 Transmit Octets Register (TXOCTETS)

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-121 Transmit Octets Register (TXOCTETS) Field Descriptions

Bits	Field	Description
31-0	TXOCTETS	The total number of bytes in all good frames transmitted on the port. A frame must match all of the following criteria to be considered a good frame: • The frame was a data or MAC control frame which was destined for any unicast, broadcast or multicast address • The frame was any size • The frame had no late or excessive collisions, no carrier loss, and no underrun
End of Table 3-121		

3.6.3.27 Receive and Transmit 64 Octet Frames Register (64OCTETFRAMES)

The receive and transmit 64 octet frames register is shown in Figure 3-111 and described in Table 3-122.

Figure 3-111 Receive and Transmit 64 Octet Frames Register (64OCTETFRAMES)

31	0
64OCTETFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-122 Receive and Transmit 64 Octet Frames Register (64OCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	64OCTETFRAMES	The total number of 64-byte frames received and transmitted on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame which was destined for any unicast, broadcast or multicast address • The frame did not experience late collisions, excessive collisions, or carrier sense error, and • The frame was exactly 64 bytes long. (If the frame was being transmitted and experienced carrier loss that resulted in a frame of this size being transmitted, then the frame will be recorded in this statistic). CRC errors, code/align errors, and overruns do not affect the recording of frames in this statistic.
End of Table 3-122		

3.6.3.28 Receive and Transmit 65-127 Octet Frames Register (65T127OCTETFRAMES)

The receive and transmit 65-127 octet frames register is shown in Figure 3-112 and described in Table 3-123.

Figure 3-112 Receive and Transmit 65-127 Octet Frames Register (65T127OCTETFRAMES)

31	0
65T127OCTETFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-123 Receive and Transmit 65-127 Octet Frames Register (65T127OCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	65T127OCTETFRAMES	The total number of frames of size 65 to 127 bytes received and transmitted on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame which was destined for any unicast, broadcast or multicast address • The frame was did not experience late collisions, excessive collisions, or carrier sense error • The frame was 65 to 127 bytes long CRC errors, code/align errors, underruns, and overruns do not affect the recording of frames in this statistic.
End of Table 3-123		

3.6.3.29 Receive and Transmit 128-255 Octet Frames Register (128T255OCTETFRAMES)

The receive and transmit 128-255 octet frames register is shown in Figure 3-113 and described in Table 3-124.

Figure 3-113 Receive and Transmit 128-255 Octet Frames Register (128T255OCTETFRAMES)

31	0
128T255OCTETFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-124 Receive and Transmit 128-255 Octet Frames Register (128T255OCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	128T255OCTETFRAMES	The total number of frames of size 128 to 255 bytes received and transmitted on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame which was destined for any unicast, broadcast or multicast address • The frame did not experience late collisions, excessive collisions, or carrier sense error • The frame was 128 to 255 bytes long CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.
End of Table 3-124		

3.6.3.30 Receive and Transmit 256-511 Octet Frames Register (256T511OCTETFRAMES)

The receive and transmit 256-511 octet frames register is shown in Figure 3-114 and described in Table 3-125.

Figure 3-114 Receive and Transmit 256-511 Octet Frames Register (256T511OCTETFRAMES)

31	0
256T511OCTETFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-125 Receive and Transmit 256-511 Octet Frames Register (256T511OCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	256T511OCTETFRAMES	The total number of frames of size 256 to 511 bytes received and transmitted on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame which was destined for any unicast, broadcast or multicast address • The frame did not experience late collisions, excessive collisions, or carrier sense error • The frame was 256 to 511 bytes long CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.
End of Table 3-125		

3.6.3.31 Receive and Transmit 512-1023 Octet Frames Register (512T1023OCTETFRAMES)

The receive and transmit 64 octet frames register is shown in Figure 3-115 and described in Table 3-126.

Figure 3-115 Receive and Transmit 512-1023 Octet Frames Register (512T1023OCTETFRAMES)

31	0
512T1023OCTETFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-126 Receive and Transmit 512-1023 Octet Frames Register (512T1023OCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	512T1023OCTETFRAMES	The total number of frames of size 512 to 1023 bytes received and transmitted on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame which was destined for any unicast, broadcast or multicast address • The frame did not experience late collisions, excessive collisions, or carrier sense error • The frame was 512 to 1023 bytes long CRC errors, code/align errors and overruns do not affect the recording of frames in this statistic.
End of Table 3-126		

3.6.3.32 Receive and Transmit 1024 and Up Octet Frames Register (1024TUPOCTETFRAMES)

The receive and transmit 1024 and up octet frames register is shown in Figure 3-116 and described in Table 3-127.

Figure 3-116 Receive and Transmit 1024 and Up Octet Frames Register (1024TUPOCTETFRAMES)

31	0
1024TUPOCTETFRAMES	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-127 Receive and Transmit 1024 and Up Octet Frames Register (1024TUPOCTETFRAMES) Field Descriptions

Bits	Field	Description
31-0	1024TUPOCTETFRAMES	The total number of frames of size 1024 to RX_MAXLEN bytes for receive or 1024 up for transmit on the port. Such a frame must match all of the following criteria: • The frame was a data or MAC control frame which was destined for any unicast, broadcast or multicast address • The frame did not experience late collisions, excessive collisions, or carrier sense error • The frame was 1024 to RX_MAXLEN bytes long on receive, or any size on transmit CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.
End of Table 3-127		

3.6.3.33 Net Octets Register (NETOCTETS)

The net octets register is shown in Figure 3-117 and described in Table 3-128.

Figure 3-117 Net Octets Register (NETOCTETS)

31	0
NETOCTETS	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-128 Net Octets Register (NETOCTETS) Field Descriptions

Bits	Field	Description
31-0	NETOCTETS	The total number of bytes of frame data received and transmitted on the port. Each frame must match all of the following criteria to be counted: • The frame was a data or MAC control frame destined for any unicast, broadcast, or multicast address (address match does not matter) • The frame was of any length, including a length of less than 64 bytes or greater than RX_MAXLEN bytes This statistic also counts: • Every byte transmitted before a carrier-loss was experienced • Every byte transmitted before each collision was experienced (i.e. multiple retries are counted each time) • Every byte received if the port is in half-duplex mode until a jam sequence was transmitted to initiate flow control. (The jam sequence was not counted to prevent double-counting). Error conditions such as alignment errors, CRC errors, code errors, overruns, and underruns do not affect the recording of bytes by this statistic. The objective of this statistic is to give a reasonable indication of Ethernet utilization.
End of Table 3-128		

3.6.3.34 Receive Start of Frame Overruns Register (RXSOFOVERRUNS)

The receive start of frame overruns register is shown in Figure 3-118 and described in Table 3-129.

Figure 3-118 Receive Start of Frame Overruns Register (RXSOFOVERRUNS)

31	0
RXSOFOVERRUNS	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-129 Receive Start of Frame Overrun Register (RXSOFOVERRUNS) Field Descriptions

Bits	Field	Description
31-0	RXSOFOVERRUNS	The total number of frames received on the port that had a start of frame (SOF) overrun or were dropped due to FIFO resource limitations. A frame must match all of the following criteria to be considered a SOF overrun frame: • The frame was a data or MAC control frame that matched a unicast, broadcast, or multicast address, or matched due to promiscuous mode • The frame was any length, including length less than 64 bytes or greater than RX_MAXLEN bytes • The packet was dropped due to FIFO resource limitations
End of Table 3-129		

3.6.3.35 Receive Middle of Frame Overruns Register (RXMOFOVERRUNS)

The receive middle of frame overruns register is shown in Figure 3-119 and described in Table 3-130.

Figure 3-119 Receive Middle of Frame Overruns Register (RXMOFOVERRUNS)

31	0
RXMOFOVERRUNS	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-130 Receive Middle of Frame Overrun Register (RXMOFOVERRUNS) Field Descriptions

Bits	Field	Description
31-0	RXMOFOVERRUNS	This statistic should always be zero.
End of Table 3-130		

3.6.3.36 Receive DMA Overruns Register (RXDMAOVERRUNS)

The receive DMA overruns register is shown in Figure 3-120 and described in Table 3-131.

Figure 3-120 Receive DMA Overruns Register (RXDMAOVERRUNS)

31	0
RXDMAOVERRUNS	
R-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-131 Receive DMA Overrun Register (RXDMAOVERRUNS) Field Descriptions

Bits	Field	Description
31-0	RXDMAOVERRUNS	This statistic should always be zero.
End of Table 3-131		

3.6.4 Time Synchronization (CPTS) submodule

This section describes the registers available in the Time Synchronization (CPTS) submodule. There is one CPTS submodule in the Ethernet switch module for time synchronization. The register offset addresses listed in this section in Table 3-132 are relative to the CPTS submodule. To determine the starting address offset of the CPTS submodule, please see Table 3-44. For convenience, a complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-132 lists the registers in the CPTS submodule and the corresponding offset address for each register.

Table 3-132 CPTS Registers

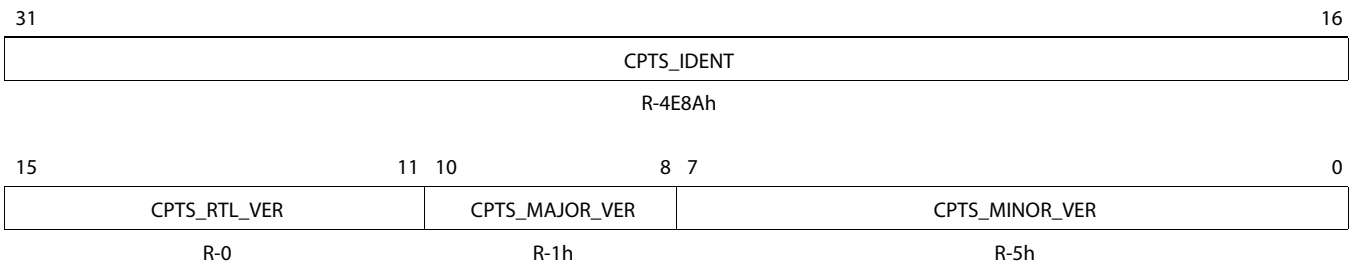
Offset Address[1]	Acronym	Register Name	Section
00	CPTS_IDVER	Identification and Version Register	Section 3.6.4.1
04	TS_CTL	Time Sync Control Register	Section 3.6.4.2
08	CPTS_RFTCLK_SEL	Reference Clock Select Register	Section 3.6.4.3
0C	TS_PUSH	Time Stamp Event Push Register	Section 3.6.4.4
10h	TS_Load_Val	Time Stamp Load Value Register	Section 3.6.4.5
14h	TS_Load_En	Time Stamp Load Enable Register	Section 3.6.4.6
18h	TS_Comp_Val	Time Stamp Comparison Value Register	Section 3.6.4.7
1Ch	TS_Comp_Length	Time Stamp Comparison Length Register	Section 3.6.4.8
20h	INTSTAT_RAW	Interrupt Status Raw Register	Section 3.6.4.9
24h	INTSTAT_MASKED	Interrupt Status Masked Register	Section 3.6.4.10
28h	INT_ENABLE	Interrupt Enable Register	Section 3.6.4.11
2Ch	Reserved		
30h	EVENT_POP	Event Interrupt Pop Register	Section 3.6.4.12
34h	EVENT_LOW	Lower 32-bits of the event value	Section 3.6.4.13
38h	EVENT_MID	Mid 32-bits of the event value	Section 3.6.4.14
3Ch	EVENT_HIGH	Upper 32-bits of the event value	Section 3.6.4.15

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.6.4.1 CPTS Identification and Version Register (CPTS_IDVER)

The CPTS identification and version register is shown in Figure 3-121 and described in Table 3-133.

Figure 3-121 CPTS Identification and Version Register (CPTS_IDVER)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-133 CPTS Identification and Version Register (CPTS_IDVER) Field Descriptions

Bits	Field	Description
31-16	CPTS_IDENT	CPTS Identification Value
15-11	CPTS_RTL_VER	RTL Version Value
10-8	CPTS_MAJOR_VER	Major Version Value
7-0	CPTS_MINOR_VER	Minor Version Value
End of Table 3-133		

3.6.4.2 Time Sync Control Register (TS_CTL)

The time sync control register is shown in Figure 3-122 and described in Table 3-134.

Figure 3-122 Time Sync Control Register (TS_CTL)

31	1	0
Reserved		CPTS_EN
R-0		RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-134 Time Sync Control Register (TS_CTL) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	CPTS_EN	Time Sync Enable. When disabled (cleared to zero), the RCLK domain is held in reset. 0 = Time Sync Disabled 1 = Time Sync Enabled
End of Table 3-134		

3.6.4.3 RFTCLK Select Register (CPTS_RFTCLK_SEL)

The CPTS_RFTCLK_SEL select register is shown in Figure 3-123 and described in Table 3-135.

Figure 3-123 RFTCLK Select Register (CPTS_RFTCLK_SEL)

31	5	4	0
Reserved		CPTS_RFTCLK_SEL	
R-0		RW=0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

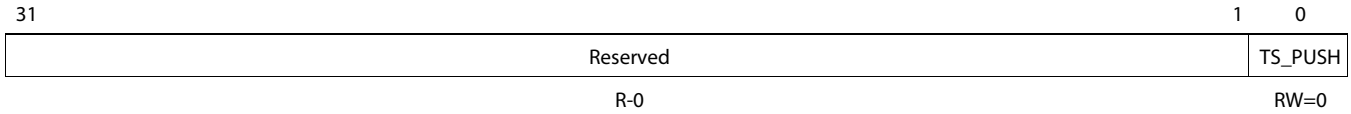
Table 3-135 RFTCLK Select Register (CPTS_RFTCLK_SEL) Field Descriptions

Bits	Field	Description
31-5	Reserved	Reserved
4-0	CPTS_RFTCLK_SEL	Reference Clock Select. This signal is used to control an external multiplexer that selects one of up to 32 clocks for time sync reference (RFTCLK). This CPTS_RFTCLK_SEL value can be written only when the CPTS_EN bit is cleared to zero in the TS_CTL register. For more information on the clock sources for this module, please see the device specific data manual.
End of Table 3-135		

3.6.4.4 Time Stamp Event Push Register (TS_PUSH)

The time stamp event push register is shown in Figure 3-124 and described in Table 3-136.

Figure 3-124 Time Stamp Event Push Register (TS_PUSH)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

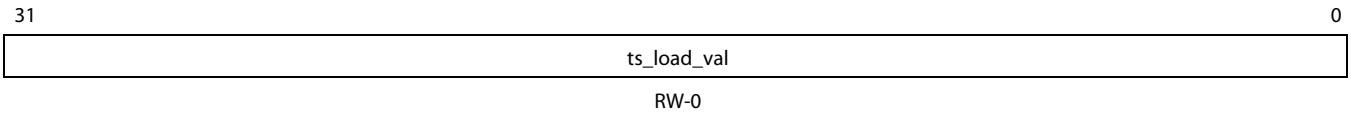
Table 3-136 Time Stamp Event Push Register (TS_PUSH) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	TS_PUSH	Time stamp event push. When a logic high is written to this bit a time stamp event is pushed onto the event FIFO. The time stamp value is the time of the write of this register, not the time of the event read. The time stamp value can then be read on interrupt via the event registers. Software should not push a second time stamp event onto the event FIFO until the first time stamp value has been read from the event FIFO (there should be only one time stamp event in the event FIFO at any given time). This bit is write only and always reads zero.
End of Table 3-136		

3.6.4.5 Time Stamp Load Value Register (TS_Load_Val)

The time stamp load value register is shown Figure 3-125 in and described in Table 3-137.

Figure 3-125 Time Stamp Load Value Register (TS_Load_Val)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

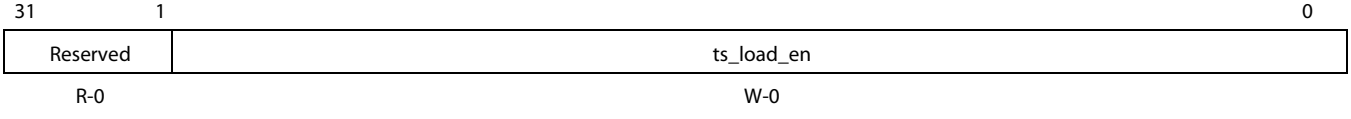
Table 3-137 Time Stamp Load Value Register (TS_Load_Val)

Bits	Field	Description
31-0	ts_load_val	Time Stamp Load Value – Writing the ts_load_en bit causes the value contained in this register to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register.
End of Table 3-137		

3.6.4.6 Time Stamp Load Enable Register (TS_Load_En)

The Time Stamp Load Enable Register is shown in Figure 3-126 and described in Table 3-138.

Figure 3-126 Time Stamp Load Enable Register (TS_Load_En)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-138 Time Stamp Load Enable Register (TS_Load_En)

Bits	Field	Description
31-1	Reserved	
0	ts_load_en	Time Stamp Load – Writing a one to this bit enables the time stamp value to be written via the ts_load_val[31:0] register. This bit is write only and will be cleared by the hardware after one clock.
End of Table 3-138		

3.6.4.7 Time Stamp Comparison Value Register (TS_Comp_Val)

Time Stamp Comparison Value Register is shown in Figure 3-127 and described in Table 3-139.

Figure 3-127 Time Stamp Comparison Value Register (TS_Comp_Val)

31	0
ts_comp_val	
RW-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-139 Time Stamp Comparison Value Register (TS_Comp_Val)

Bits	Field	Description
31-0	ts_comp_val	Time Stamp Comparison Value – Writing a non-zero value to the TS_Comp_Length[15:0] register causes a pulse of TS_Comp_Length RCLK periods on the TS_COMP output and a comparison event when the time_stamp counter value is equivalent to ts_comp_val.
End of Table 3-139		

3.6.4.8 Time Stamp Comparison Length Register (TS_Comp_Length)

Time stamp comparison length register is shown in Figure 3-128 and described inTable 3-140.

Figure 3-128 Time Stamp Comparison Length Register (TS_Comp_Length)

31	16	15	0
Reserved		ts_comp_length	
R-0		RW-0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

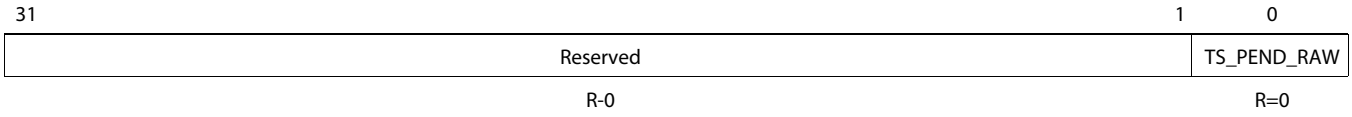
Table 3-140 Time Stamp Comparison Length Register (TS_Comp_Length)

Bits	Field	Description
31-16	Reserved	
15-0	ts_comp_length	Time Stamp Comparison Length – Writing a non-zero value to this field enables the time stamp comparison event and output. This value should be zero when the TS_Comp_Val register is written.
End of Table 3-140		

3.6.4.9 Interrupt Status Raw Register (INTSTAT_RAW)

The interrupt status raw register is shown in Figure 3-129 and described in Table 3-141.

Figure 3-129 Interrupt Status Raw Register (INTSTAT_RAW)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

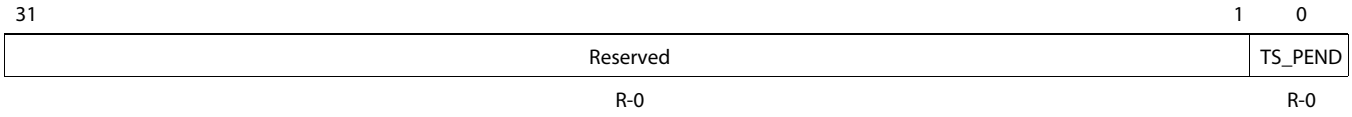
Table 3-141 Interrupt Status Raw Register (INTSTAT_RAW) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	TS_PEND_RAW	Time Sync Raw Pending Interrupt Register. A one in this bit indicates that there is one or more events in the event FIFO.
End of Table 3-141		

3.6.4.10 Interrupt Status Masked Register (INTSTAT_MASKED)

The interrupt status masked register is shown in Figure 3-130 and described in Table 3-142.

Figure 3-130 Interrupt Status Masked Register (INTSTAT_MASKED)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

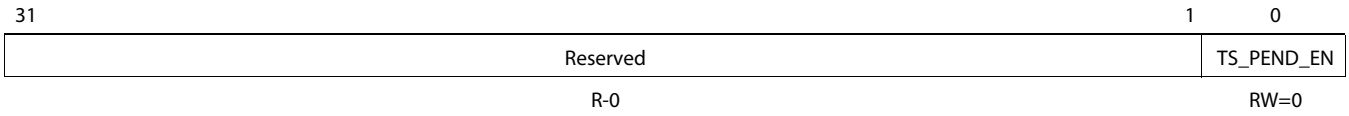
Table 3-142 Interrupt Status Masked Register (INTSTAT_MASKED) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved.
0	TS_PEND	Time Sync Masked Pending Interrupt Register. Masked interrupt read (after enable).
End of Table 3-142		

3.6.4.11 Interrupt Enable Register (INT_ENABLE)

The interrupt enable register is shown in Figure 3-131 and described in Table 3-143.

Figure 3-131 Interrupt Enable Register (INT_ENABLE)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-143 Interrupt Enable Register (INT_ENABLE) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	TS_PEND_EN	Time Sync Interrupt Enable Register. Enables time sync masked interrupts.
End of Table 3-143		

3.6.4.12 Event Pop Register (EVENT_POP)

The event pop register is shown in Figure 3-132 and described in Table 3-144.

Figure 3-132 Event Pop Register (EVENT_POP)

31	1	0
Reserved		EVENT_POP
R-0		W=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-144 Event Pop Register (EVENT_POP) Field Descriptions

Bits	Field	Description
31-1	Reserved	Reserved
0	EVENT_POP	Event Pop. When a logic high is written to this bit an event is popped off the event FIFO. The event FIFO pop occurs as part of the interrupt process after the event has been read in the EVENT_LOW and EVENT_HIGH registers. Popping an event discards the event and causes the next event, if any, to be moved to the top of the FIFO ready to be read by software on interrupt.
End of Table 3-144		

3.6.4.13 Event Low Register (EVENT_LOW)

The event low register is shown in Figure 3-133 and described in Table 3-145.

Figure 3-133 Event Low Register (EVENT_LOW)

31	0
TIME_STAMP	
R-x	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

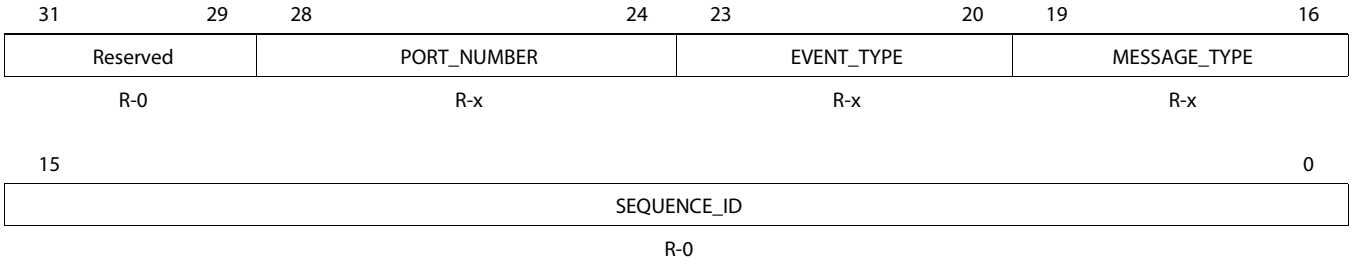
Table 3-145 Event Low Register (EVENT_LOW) Field Descriptions

Bits	Field	Description
31-0	TIME_STAMP	Time Stamp. The timestamp is valid for transmit, receive, and time stamp push event types. The timestamp value is not valid for counter roll event types.
End of Table 3-145		

3.6.4.14 Event Mid Register (EVENT_MID)

The event mid register is shown in Figure 3-135 and described in Table 3-147.

Figure 3-134 32-Bit Register



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

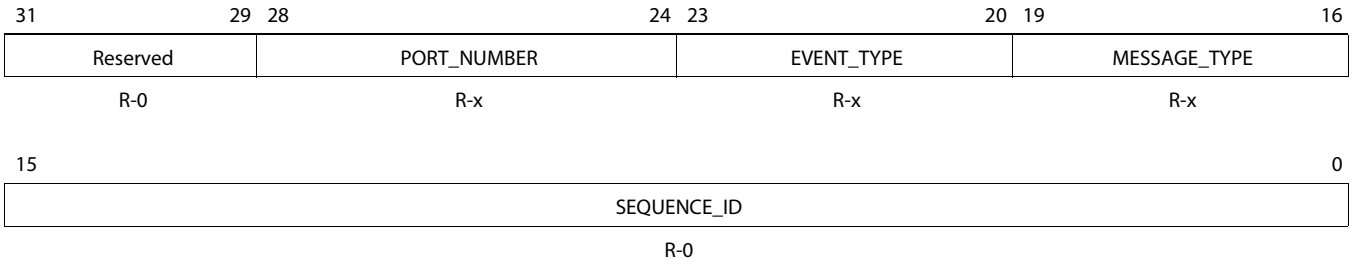
Table 3-146 Event High Register (EVENT_MID) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	PORT_NUMBER	Port Number. Indicates the port number (encoded) of an Ethernet event or the encoded hardware timestamp number.
23-20	EVENT_TYPE	Time Sync Event Type. 0000 = Time Stamp Push Event 0001 = Time Stamp Rollover Event 0010 = Time Stamp Half Rollover Event 0011 = Hardware Time Stamp Push Event 0100 = Ethernet Receive Event 0101 = Ethernet Transmit Event 0111-1111 = Reserved
19-16	MESSAGE_TYPE	Message type. The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.
15-0	SEQUENCE_ID	Sequence ID. The 16-bit sequence ID is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.
End of Table 3-146		

3.6.4.15 Event High Register (EVENT_HIGH)

The event high register is shown in Figure 3-135 and described in Table 3-147.

Figure 3-135 Event High Register (EVENT_HIGH)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-147 Event High Register (EVENT_HIGH) Field Descriptions

Bits	Field	Description
31-29	Reserved	Reserved
28-24	PORT_NUMBER	Port Number. Indicates the port number of an Ethernet event.
23-20	EVENT_TYPE	Time Sync Event Type. 0000 = Time Stamp Push Event 0001 = Time Stamp Rollover Event 0010 = Time Stamp Half Rollover Event 0011 = Reserved 0100 = Ethernet Receive Event 0101 = Ethernet Transmit Event 0111-1111 = Reserved
19-16	MESSAGE_TYPE	Message type. The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.
15-0	SEQUENCE_ID	Sequence ID. The 16-bit sequence ID is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.
End of Table 3-147		

3.6.5 Address Lookup Engine (ALE) submodule

This section describes the registers available in the Address Lookup Engine (ALE) submodule. There is one ALE submodule in the Ethernet switch module for time synchronization. The register offset addresses listed in this section in Table 3-148 are relative to the ALE submodule. To determine the starting address offset of the ALE submodule, please see Table 3-44. For convenience, a complete list of all of the registers in the GbE switch subsystem is provided in Table 3-2.

Table 3-148 lists the registers in the ALE submodule and the corresponding offset address for each register.

Table 3-148 ALE Registers

Offset Address[1]	Register Mnemonic	Register Name	Section
00h	ALE_IDVER	Address Lookup Engine ID/Version Register	Section 3.6.5.1
04h	Reserved	Reserved	Reserved
08h	ALE_CONTROL	Address Lookup Engine Control Register	Section 3.6.5.2
0Ch	Reserved	Reserved	Reserved
10h	ALE_PRESCALE	Address Lookup Engine Prescale Register	Section 3.6.5.3
14h	ALE_AGING_TIMER	ALE Aging Timer Register	Reserved
18h	ALE_UNKNOWN_VLAN	Address Lookup Engine Unknown VLAN Register	Section 3.6.5.4
1Ch	Reserved	Reserved	Reserved
20h	ALE_TBLCTL	Address Lookup Engine Table Control	Section 3.6.5.5
24h-30h	Reserved	Reserved	Reserved
34h	ALE_TBLW2	Address Lookup Engine Table Word 2 Register	Section 3.6.5.6
38h	ALE_TBLW1	Address Lookup Engine Table Word 1 Register	Section 3.6.5.7
3Ch	ALE_TBLW0	Address Lookup Engine Table Word 0 Register	Section 3.6.5.8
40h	ALE_PORTCTL0	Address Lookup Engine Port 0 Control Register	Section 3.6.5.9
44h	ALE_PORTCTL1	Address Lookup Engine Port 1 Control Register	Section 3.6.5.10
48h	ALE_PORTCTL2	Address Lookup Engine Port 2 Control Register	Section 3.6.5.11
End of Table 3-148			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.6.5.1 ALE Identification and Version Register (ALE_IDVER)

The ALE identification and version register is shown in Figure 3-136 and described in Table 3-149.

Figure 3-136 ALE Identification and Version Register (ALE_IDVER)

31	16
ALE_IDENT	
R-29h	

15	8	7	0
ALE_MAJOR_VER		ALE_MINOR_VER	
R-1h		R-3h	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-149 ALE Identification and Version Register (ALE_IDVER) Field Descriptions

Bits	Field	Description
31-16	ALE_IDENT	ALE Identification Value.
15-8	ALE_MAJ_VER	ALE Major Version Value.
7-0	ALE_MINOR_VER	ALE Minor Version Value.
End of Table 3-149		

3.6.5.2 ALE Control Register (ALE_CONTROL)

The ALE control register is shown in Figure 3-137 and described in Table 3-150.

Figure 3-137 ALE Control Register (ALE_CONTROL)

31	30	29	28	8
ENABLE_ALE	CLEAR_TABLE	AGE_OUT_NOW	Reserved	
RW=0	RW=0	RW=0	R-0	

7	6	5	4	3	2	1	0
LEARN_NO_VID	EN_VID0_MODE	EN_OUI_DENY	ALE_BYPASS	RATE_LIMIT_TX	ALE_VLAN_AWARE	EN_AUTH_MODE	EN_RATE_LIMIT
RW=0	RW=0	RW=0	RW=0	RW=0	RW=0	RW=0	RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset

Table 3-150 ALE Control Register (ALE_CONTROL) Field Descriptions

Bits	Field	Description
31	ENABLE_ALE	Enable ALE. 0 = Drop all packets. 1 = Enable ALE packet processing.
30	CLEAR_TABLE	Clear ALE address table. Setting this bit causes the ALE hardware to write all table bit values to zero. Software must perform a clear table operation as part of the ALE setup/configuration process. Setting this bit causes all ALE accesses to be held up for 64 clocks while the clear is performed. Access to all ALE registers will be blocked (wait states) until the 64 clocks have completed. This bit cannot be read as one because the read is blocked until the clear table is completed at which time this bit is cleared to zero.
29	AGE_OUT_NOW	Age Out Address Table Now. Setting this bit causes the ALE hardware to remove (free up) any ageable table entry that does not have a set touch bit. This bit is cleared when the age out process has completed. This bit may be read. The age out process takes a minimum of 4096 clock cycles (no ale packet processing during ageout) and a maximum of 66550 clock cycles.
28-8	Reserved	Reserved
7	LEARN_NO_VID	Learn No VID. 0 = VID is learned with the source address. 1 = VID is not learned with the source address (source address is not tied to VID).
6	EN_VID0_MODE	Enable VLAN ID = 0 Mode. 0 = Process the packet with VID = PORT_VLAN[11-0]. 1 = Process the packet with VID = 0.
5	EN_OUI_DENY	Enable OUI Deny Mode. When set this bit indicates that a packet with a non OUI table entry matching source address will be dropped to the host unless the destination address matches a multicast table entry with the SUPER bit set.
4	ALE_BYPASS	ALE Bypass. 0 = ALE bypass is disabled. 1 = ALE bypass is enabled. Note-packets originating from the GbE switch host port (port 0) will not bypass the ALE. To bypass the ALE for packets originating from port 0, use a directed packet.
3	RATE_LIMIT_TX	Rate Limit Transmit mode. 0 = Broadcast and multicast rate limit counters are received port based. 1 = Broadcast and multicast rate limit counters are transmit port based.
2	ALE_VLAN_AWARE	ALE VLAN Aware. Determines what is done if VLAN not found. 0 = Flood if VLAN not found. 1 = Drop packet if VLAN not found.
1	EN_AUTH_MODE	Enable MAC Authorization Mode. Mac authorization mode requires that all table entries be made by the host software. There are no learned addresses in authorization mode and the packet will be dropped if the source address is not found (and the destination address is not a multicast address with the **SUPER** table entry bit set). 0 = The ALE is not in MAC authorization mode. 1 = The ALE is in MAC authorization mode.
0	EN_RATE_LIMIT	Enable Broadcast and Multicast Rate Limit. 0 = Broadcast/Multicast rates not limited. 1 = Broadcast/Multicast packet reception limited to the port control register rate limit fields.
End of Table 3-150		

3.6.5.3 ALE Prescale Register (ALE_PRESCALE)

The ALE prescale register is shown in Figure 3-138 and described in Table 3-151.

Figure 3-138 ALE Prescale Register (ALE_PRESCALE)

31	20	19	0
Reserved		ALE_PRESCALE	
R-0		RW=0	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-151 ALE Prescale Register (ALE_PRESCALE) Field Descriptions

Bits	Field	Description
31-20	Reserved	Reserved
19-0	ALE_PRESCALE	ALE Prescale Register. The input clock is divided by this value for use in the multicast/broadcast rate limiters. The minimum operating value is 10h. The prescaler is off when the value is zero.
End of Table 3-151		

3.6.5.4 ALE Unknown VLAN Register (UNKNOWN_VLAN)

The ALE unknown VLAN register is shown in Figure 3-139 and described in Table 3-152.

Figure 3-139 ALE Unknown VLAN Register (UNKNOWN_VLAN)

31 30	29 24	23 22	21 16
Reserved	UNKNOWN_FORCE_UNTAGGED_EGRESS	Reserved	UNKNOWN_REG_MCAST_FLOOD_MASK
R-0	RW=0	R-0	RW=0

15 14	13 8	7 6	5 0
Reserved	UNKNOWN_MCAST_FLOOD_MASK	Reserved	UNKNOWN_VLAN_MEMBER_LIST
R-0	RW=0	R-0	RW=0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-152 ALE Unknown VLAN Register (UNKNOWN_VLAN) Field Descriptions

Bits	Field	Description
31-30	Reserved	Reserved
29-24	UNKNOWN_FORCE_UNTAGGED_EGRESS	Unknown VLAN Force Untagged Egress.
23-22	Reserved	Reserved
21-16	UNKNOWN_REG_MCAST_FLOOD_MASK	Unknown VLAN Registered Multicast Flood Mask.
15-14	Reserved	Reserved
13-8	UNKNOWN_MCAST_FLOOD_MASK	Unknown VLAN Multicast Flood Mask.
7-6	Reserved	Reserved
5-0	UNKNOWN_VLAN_MEMBER_LIST	Unknown VLAN Member List.
End of Table 3-152		

3.6.5.5 ALE Table Control Register (ALE_TBLCTL)

The ALE table control register is shown in Figure 3-140 and described in Table 3-153.

Figure 3-140 ALE Table Control Register (ALE_TBLCTL)

31	30 16
WRITE_RDZ	Reserved
RW=0	

15 10	9 0
Reserved	ENTRY_POINTER
R-0	RW=0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-153 ALE Table Control Register (ALE_TBLCTL) Field Descriptions

Bits	Field	Description
31	WRITE_RDZ	Write Bit. Writing a 1 to this bit causes the three table word register values to be written to the ENTRY_POINTER location in the address table. Writing a 0 to this bit causes the three table word register values to be loaded from the ENTRY_POINTER location in the address table so that they may be subsequently read. A read of any ALE address location will be stalled until the read or write has completed. This bit is always read as zero.
30-10	Reserved	Reserved
9-0	ENTRY_POINTER	Table Entry Pointer. The ENTRY_POINTER contains the table entry value that will be read/written with accesses to the table word registers.
End of Table 3-153		

3.6.5.6 ALE Table Word 2 Register (ALE_TBLW2)

The ALE table word 2 register is shown in Figure 3-141 and described in Table 3-154.

Figure 3-141 ALE Table Word 2 Register (ALE_TBLW2)

31	8	7	0
Reserved		ENTRY2	
R-0		RW=x	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-154 ALE Table Word 2 Register (ALE_TBLW2) Field Descriptions

Bits	Field	Description
31-8	Reserved	Reserved
7-0	ENTRY2	Table entry bits 71-64
End of Table 3-154		

3.6.5.7 ALE Table Word 1 Register (ALE_TBLW1)

The ALE table word 1 register is shown in Figure 3-142 and described in Table 3-155.

Figure 3-142 ALE Table Word 1 Register (ALE_TBLW1)

31	0
ENTRY1	
RW=x	

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-155 ALE Table Word 1 Register (ALE_TBLW2) Field Descriptions

Bits	Field	Description
31-0	ENTRY1	Table entry bits 63-32
End of Table 3-155		

3.6.5.8 ALE Table Word 0 Register (ALE_TBLW0)

The ALE table word 0 register is shown in Figure 3-143 and described in Table 3-156.

Figure 3-143 ALE Table Word 0 Register (ALE_TBLW0)

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

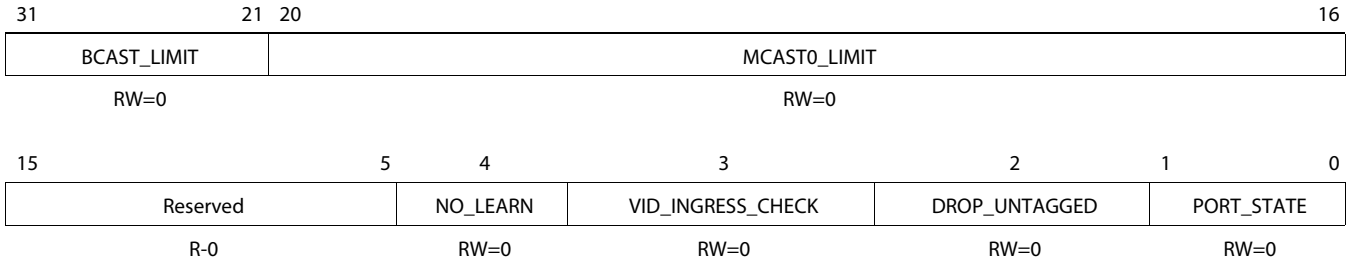
Table 3-156 ALE Table Word 0 Register (ALE_TBLW0) Field Descriptions

Bits	Field	Description
31-0	ENTRY0	Table entry bits 31-0
End of Table 3-156		

3.6.5.9 ALE Port Control Register 0 (ALE_PORTCTL0)

The ALE port control register 0 is shown in Figure 3-144 and described in Table 3-157.

Figure 3-144 ALE Port Control Register 0 (ALE_PORTCTL0)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-157 ALE Port Control Register 0 (ALE_PORTCTL0) Field Descriptions (Part 1 of 2)

Bits	Field	Description
31-21	BCAST_LIMIT	Broadcast Packet Rate Limit. Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
20-16	MCAST0_LIMIT	Multicast Packet Rate Limit. Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field.
15-5	Reserved	Reserved
4	NO_LEARN	No Learn Mode. When set the port is disabled from learning new source addresses; however, currently existing addresses will still update.
3	VID_INGRESS_CHECK	VLAN ID Ingress Check. If VLAN not found then drop the packet. Packets with an unknown (default) VLAN will be dropped.

Table 3-157 ALE Port Control Register 0 (ALE_PORTCTL0) Field Descriptions (Part 2 of 2)

Bits	Field	Description
2	DROP_UNTAGGED	Drop Untagged Packets. Drop non-VLAN tagged ingress packets.
1-0	PORT_STATE	Port State. 0 = Disabled 1 = Blocked 2 = Learn 3 = Forward
End of Table 3-157		

3.6.5.10 ALE Port Control Register 1 (ALE_PORTCTL1)

The ALE port control register 1 is shown in Figure 3-145 and described in Table 3-158.

Figure 3-145 ALE Port Control Register 1 (ALE_PORTCTL1)

31 21	20 16
BCAST_LIMIT	MCAST1_LIMIT
RW=0	RW=0

15 5	4	3	2	1 0
Reserved	NO_LEARN	VID_INGRESS_CHECK	DROP_UNTAGGED	PORT_STATE
R-0	RW=0	RW=0	RW=0	RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

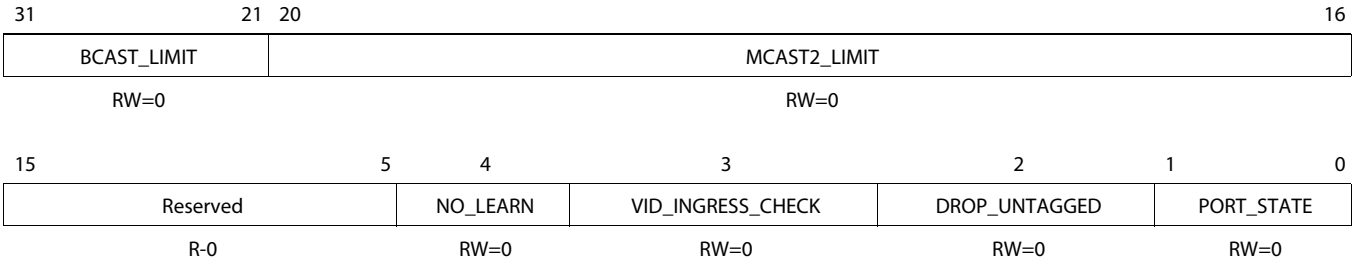
Table 3-158 ALE Port Control Register 1 (ALE_PORTCTL1) Field Descriptions

Bits	Field	Description
31-21	BCAST_LIMIT	Broadcast Packet Rate Limit. Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
20-16	MCAST1_LIMIT	Multicast Packet Rate Limit. Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field.
15-5	Reserved	Reserved
4	NO_LEARN	No Learn Mode. When set the port is disabled from learning or updating source addresses.
3	VID_INGRESS_CHECK	VLAN ID Ingress Check. If VLAN not found then drop the packet. Packets with an unknown (default) VLAN will be dropped.
2	DROP_UNTAGGED	Drop Untagged Packets. Drop non-VLAN tagged ingress packets.
1-0	PORT_STATE	Port State. 0 = Disabled 1 = Blocked 2 = Learn 3 = Forward
End of Table 3-158		

3.6.5.11 ALE Port Control Register 2 (ALE_PORTCTL2)

The ALE port control register 2 is shown in Figure 3-146 and described in Table 3-159.

Figure 3-146 ALE Port Control Register 2 (ALE_PORTCTL2)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-159 ALE Port Control Register 2 (ALE_PORTCTL2) Field Descriptions

Bits	Field	Description
31-21	BCAST_LIMIT	Broadcast Packet Rate Limit. Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
20-16	MCAST2_LIMIT	Multicast Packet Rate Limit. Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field.
15-5	Reserved	Reserved
4	NO_LEARN	No Learn Mode. When set the port is disabled from learning or updating source addresses.
3	VID_INGRESS_CHECK	VLAN ID Ingress Check. If VLAN not found then drop the packet. Packets with an unknown (default) VLAN will be dropped.
2	DROP_UNTAGGED	Drop Untagged Packets. Drop non-VLAN tagged ingress packets.
1-0	PORT_STATE	Port State. 0 = Disabled 1 = Blocked 2 = Learn 3 = Forward
End of Table 3-159		

3.7 MACSEC Module

This section describes the registers available in the MACSEC module. Each MACSEC module have two set of registers: Egress and Ingress. Unless noted otherwise, all egress and ingress registers are identical. Therefore, only one description is given per register. The submodule offset addresses listed in Table 3-160 are relative to the Ethernet switch module offset address. To determine the offset address of the Ethernet switch module, please see Table 3-1. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

Table 3-160 shows the submodules contained in the MACSEC module.

Table 3-160 MACSEC Module

Offset Address [1]	Acronym	Submodule Name	Section
20000h – 23FFFh	XFORMREC	Transform records area	Section 3.7.1
24000h – 26FFFh	SAMPARMS	SA match parameter sets	Section 3.7.2
27000h – 277FFh	FLOWCTRLWRDS	Flow control words for frames that matched an SA parameter set	Section 3.7.3
27800h - 27FFFh	Reserved		
28000h – 2C7FFh	SECURITYSTATS	Security statistics counters of 40 bits each	Section 3.7.4
2C800h – 2CFFFh	SECOUNTERDBG	Security statistics counter control and debug	Section 3.7.5
2E000h – 2EFFFh	CCPARAM	Consistency check parameter sets control bits and debug status	Section 3.7.6
2F100h – 2F123h	VLANCHECKCTRL	9 MTU check control words for VLAN packets and non-VLAN pkts	Section 3.7.7
2F124h – 2F3FFh	PKTENGINESECFAIL	Security fail control masks and debug registers for Packet Engine	Section 3.7.8
2F400h – 2F7FFh	PKTENGINEREGS	Access space for Packet Engine	Section 3.7.9
2F800h – 2FFFFh	Reserved		
End of Table 3-160			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.7.1 Transform Records Area

This section describes the registers available in the Transform Records Area of the MACSEC module. The are offset addresses listed in Table 3-161 are relative to the MACSEC module offset address. To determine the offset address of the MACSEC module, please see Table 3-1. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

Table 3-161 shows the submodules contained in the Transform Records Area.

Table 3-161 Transform Records Area

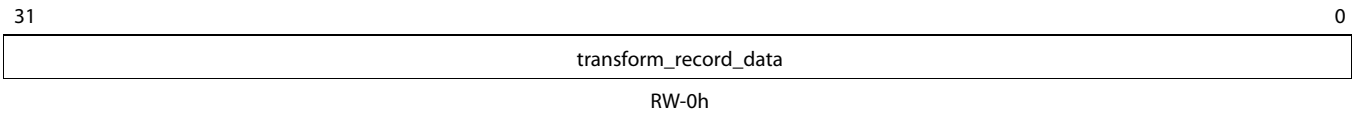
Offset Address [1]	Acronym	Submodule Name	Section
0x0000h-0x003Fh	XFORMREC_0	Transform record 0	Section 3.7.1.1
0x0040h-0x007Fh	XFORMREC_1	Transform record 1	Section 3.7.1.1
0x0080h-0x03FFh	XFORMREC_2...XFORMREC_15	Transform record 2 till 15	Section 3.7.1.1
0x0400h-0x07FFh	XFORMREC_16...XFORMREC_31	Transform record 16 till 31	Section 3.7.1.1
0x0800h-0x0FFFh	XFORMREC_32...XFORMREC_63	Transform record 32 till 63	Section 3.7.1.1
End of Table 3-161			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.7.1.1 Transform Record N (offset 0x0000 + (n*64))

Transform context records (each 16 words of 32 bits long) are stored in a RAM, with one record for each SA match entry. For 16 SA match entries, the total size is 256 words of 32 bits (1KByte); for 32 SA match entries – 512 words of 32 bits (2Kbyte) and for 64 SA – 1024 words of 32 bits (4Kbyte).

Figure 3-147 Transform Record N



Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-162 Transform Record N

Bits	Field	Description
31-0	transform_record_data	Transform record data, split into records of 64 Bytes each (number of records corresponds to the number of SA supported by the hardware configuration)
End of Table 3-162		

3.7.2 SA Match Parameter Sets

This section describes the registers available in the SA MATCH Parameters Sets registers area of the MACSEC module. The offset addresses listed in Table 3-163 are relative to the MACSEC module offset address. To determine the offset address of the MACSEC module, please see Table 3-1. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

Table 3-161 shows the submodules contained in the Transform Records Area.

Table 3-163 SA MATCH Parameter Sets (Part 1 of 2)

Offset Address [1]	Acronym	Submodule Name	Section
0x4000h	SAM_MAC_SA_MATCH_LO_0	SA Match Parameter 0	Section 3.7.2.1
0x4004h	SAM_MAC_SA_MATCH_HI_0	SA Match Parameter 0	Section
0x4008h	SAM_MAC_DA_MATCH_LO_0	SA Match Parameter 0	Section 3.7.2.3
0x400Ch	SAM_MAC_DA_MATCH_HI_0	SA Match Parameter 0	Section 3.7.2.4
0x4010h	SAM_MISC_MATCH_0	SA Match Parameter 0	Section 3.7.2.5
0x4014h	SAM_SCI_MATCH_LO_0	SA Match Parameter 0	Section 3.7.2.6
0x4018h	SAM_SCI_MATCH_HI_0	SA Match Parameter 0	Section 3.7.2.7
0x401Ch	SAM_MASK_0	SA Match Parameter 0	Section 3.7.2.8
0x4020h-0x403Fh	Reserved		
0x4040h-0x407Fh	SAM_MAC_SA_MATCH_LO_1 .. SAM_MASK_1	SA Match Parameter 1	Section 3.7.2.1 - Section 3.7.2.8
0x4080h-0x43FFh	SAM_MAC_SA_MATCH_LO_2 .. SAM_MASK_2 SAM_MAC_SA_MATCH_LO_15 .. SAM_MASK_15	SA Match Parameter 2 till 15	Section 3.7.2.1 - Section 3.7.2.8
0x4400h-0x47FFh	SAM_MAC_SA_MATCH_LO_16 .. SAM_MASK_16 SAM_MAC_SA_MATCH_LO_31 .. SAM_MASK_31	SA Match Parameter 16 till 31	Section 3.7.2.1 - Section 3.7.2.8
0x4800h-0x4FFFh	SAM_MAC_SA_MATCH_LO_32 .. SAM_MASK_32 SAM_MAC_SA_MATCH_LO_63 .. SAM_MASK_63	SA Match Parameter 32 till 63	Section 3.7.2.1 - Section 3.7.2.8
0x5000h-0x5FFFh	Reserved		

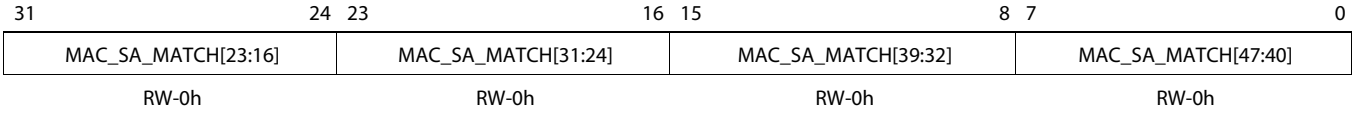
Table 3-163 SA MATCH Parameter Sets (Part 2 of 2)

Offset Address [1]	Acronym	Submodule Name	Section
0x6000h	SAM_ENTRY_ENABLE1	SA Match entry enable control registers	Section 3.7.2.9
0x6004h	SAM_ENTRY_ENABLE2		Section 3.7.2.10
0x6010h	SAM_ENTRY_TOGGLE1		Section 3.7.2.11
0x6014h	SAM_ENTRY_TOGGLE2		Section 3.7.2.12
0x6020h	SAM_ENTRY_SET1		Section 3.7.2.13
0x6024h	SAM_ENTRY_SET2		Section 3.7.2.14
0x6030h	SAM_ENTRY_CLEAR1		Section 3.7.2.15
0x6034h	SAM_ENTRY_CLEAR2		Section 3.7.2.16
0x6040h	SAM_IN_FLIGHT		Section 3.7.2.17
0x6044h-0x6FFFh	Reserved		
End of Table 3-163			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.7.2.1 SAM_MAC_SA_MATCH_LO_N (offset 0x4000 + (n*64))

Figure 3-148 SAM_MAC_SA_MATCH_LO_N



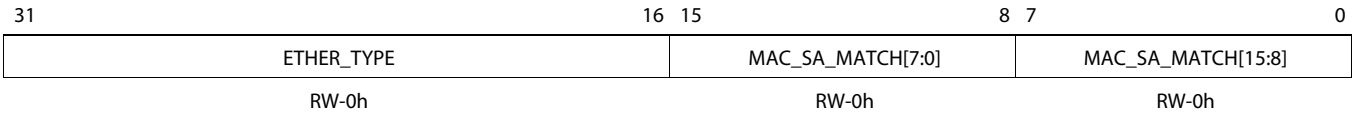
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-164 SAM_MAC_SA_MATCH_LO_N

Bits	Field	Description
31-24	mac_sa_match[23:16]	bits [[23:16] of one mac_sa compare value (compare_enabled per byte)
23-16	mac_sa_match[31:24]	bits [31:24] of one mac_sa compare value (compare_enabled per byte)
15-8	mac_sa_match[39:32]	bits [39:32] of one mac_sa compare value (compare_enabled per byte)
7-0	mac_sa_match[47:40]	bits [47:40] of one mac_sa compare value (compare_enabled per byte), first byte received.
End of Table 3-164		

3.7.2.2 SAM_MAC_SA_MATCH_HI_N (offset 0x4004 + (n*64))

Figure 3-149 SAM_MAC_SA_MATCH_HI_N



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-165 SAM_MAC_SA_MATCH_HI_N (Part 1 of 2)

Bits	Field	Description
31-16	ether_type	Parsed Ether -type compared value (stored big endian)

Table 3-165 SAM_MAC_SA_MATCH_HI_N (Part 2 of 2)

Bits	Field	Description
15-8	mac_sa_match[7:0]	bits [7:0] of one mac_sa compare value (compare_enabled per byte), last byte received
7-0	mac_sa_match[15:8]	bits [15:8] of one mac_sa compare value (compare_enabled per byte)
End of Table 3-165		

3.7.2.3 SAM_MAC_DA_MATCH_LO_N (offset 0x4008 + (n*64))

Figure 3-150 SAM_MAC_DA_MATCH_LO_N

31 24	23 16	15 8	7 0
MAC_DA_MATCH[23:16]	MAC_DA_MATCH[31:24]	MAC_DA_MATCH[39:32]	MAC_DA_MATCH[47:40]
RW-0h	RW-0h	RW-0h	RW-0h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-166 SAM_MAC_DA_MATCH_LO_N

Bits	Field	Description
31-24	mac_da_match[23:16]	bits [[23:16] of one mac_da compare value (compare_enabled per byte)
23-16	mac_da_match[31:24]	bits [31:24] of one mac_da compare value (compare_enabled per byte)
15-8	mac_da_match[39:32]	bits [39:32] of one mac_da compare value (compare_enabled per byte)
7-0	mac_da_match[47:40]	bits [47:40] of one mac_da compare value (compare_enabled per byte), first byte received.
End of Table 3-166		

3.7.2.4 SAM_MAC_DA_MATCH_HI_N (offset 0x400C + (n*64))

Figure 3-151 SAM_MAC_DA_MATCH_HI_N

31 16	15 8	7 0
VLAN_ID	MAC_DA_MATCH[7:0]	MAC_DA_MATCH[15:8]
RW-0h	RW-0h	RW-0h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-167 SAM_MAC_DA_MATCH_HI_N

Bits	Field	Description
31-16	vlan_id	Parsed VLAN_ID compared value
15-8	mac_da_match[7:0]	bits [7:0] of one mac_da compare value (compare_enabled per byte), last byte received
7-0	mac_da_match[15:8]	bits [15:8] of one mac_da compare value (compare_enabled per byte)
End of Table 3-167		

3.7.2.5 SAM_MISC_MATCH_N (offset 0x4010 + (n*64))

Figure 3-152 SAM_MISC_MATCH_N

31–24	23–20	19–16	15–14	13–12	11	10	9
MACSEC_TCI_AN	Reserved	MATCH_PRI	Reserved	SOURCE_PORT	KEY_TAG	BAD_TAG	TAGGED
RW=0	R=0	RW=0	R=0	RW=0	RW=0	RW=0	RW=0

8	7	6–4	3	2	1	0
UNTAGGED	CONTROL_PKT	VLAN_UP	QTAG_VALID	STAG_VALID	Reserved	VLAN_VALID
RW=0	RW=0	RW=0	RW=0	RW=0	R=0	RW=0

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-168 SAM_MISC_MATCH_N

Bits	Field	Description
31-24	macsec_tci_an	MACsec TCI/AN byte compare value, bits are individually masked for comparing. The TCI bits are in bits [31:26] while the AN bits reside in bits [25:24]. These bits are Reserved for an egress-only (-e) core.
23-20	Reserved	
19-16	match_pri	Priority of this entry for determining the actual transform used on a match when multiple entries match, 0 = lowest, 15 = highest. In case of identical priorities, the lowest numbered entry takes precedence.
15-14	Reserved	
13-12	source_port	Source port compare value (00b = Common port, 01b = Reserved port, 10b = Controlled port, 11b = Uncontrolled port)
11	key_tag	1b = allow packets with a MACsec tag indicating KaY handling to be done to match (MACsec tag classification logic output)
10	bad_tag	1b = allow packets with an invalid MACsec tag to match (MACsec tag classification logic output)
9	tagged	1b = allow packets with a standard and valid MACsec tag to match (MACsec tag classification logic output)
8	untagged	1b = allow packets without a MACsec tag to match (MACsec tag classification logic output)
7	control_pkt	Packet is control packet (as pre-decoded) compare value
6-4	vlan_up	Parsed VLAN User Priority compare value
3	qtag_valid	Parsed QTAG valid flag compare value
2	stag_valid	Parsed STAG valid flag compare value
1	Reserved	
0	vlan_valid	Parsed VLAN valid flag compare value
End of Table 3-168		

3.7.2.6 SAM_SCI_MATCH_LO_N (offset 0x4014 + (n*64))

Figure 3-153 SAM_SCI_MATCH_LO_N

31 24	23 16	15 8	7 0
MACSEC_SCI_MATCH[39:32]	MACSEC_SCI_MATCH[47:40]	MACSEC_SCI_MATCH[55:48]	MACSEC_SCI_MATCH[63:56]
RW-0h	RW-0h	RW-0h	RW-0h

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-169 SAM_SCI_MATCH_LO_N

Bits	Field	Description
31-24	macsec_sci_match[39:32]	Bits [39:32] of one MACsec SCI compare value
23-16	macsec_sci_match[47:40]	Bits [47:40] of one MACsec SCI compare value
15-8	macsec_sci_match[55:48]	Bits [55:48] of one MACsec SCI compare value
7-0	macsec_sci_match[63:56]	Bits [63:56] of one MACsec SCI compare value, first byte received.
End of Table 3-169		

3.7.2.7 SAM_SCI_MATCH_HI_N (offset 0x4018 + (n*64))

Figure 3-154 SAM_SCI_MATCH_HI_N

31 24	23 16	15 8	7 0
MACSEC_SCI_MATCH[7:0]	MACSEC_SCI_MATCH[15:8]	MACSEC_SCI_MATCH[23:16]	MACSEC_SCI_MATCH[31:24]
RW-0h	RW-0h	RW-0h	RW-0h

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-170 SAM_SCI_MATCH_HI_N

Bits	Field	Description
31-24	macsec_sci_match[7:0]	Bits [7:0] of one MACsec SCI compare value, last byte received
23-16	macsec_sci_match[15:8]	Bits [15:8] of one MACsec SCI compare value
15-8	macsec_sci_match[23:16]	Bits [23:16] of one MACsec SCI compare value
7-0	macsec_sci_match[31:24]	Bits [31:24] of one MACsec SCI compare value
End of Table 3-170		

3.7.2.8 SAM_MASK_N (offset 0x401C + (n*64))

Figure 3-155 SAM_MASK_N

31 24	23	22 21	20	19	18	17	16	15
TCI_AN_MASK	MACSEC_SCI_MASK	Reserved	CTRL_PKT_MASK	SRC_PORT_MASK	VLAN_ID_MASK	VLAN_UP_MASK	QTAG_VLD_MASK	STAG_VLD_MASK
RW=0	R=0	R=0	R=0	RW=0	RW=0	RW=0	RW=0	RW=0

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	VLAN_VLD_MASK	MAC_ETYPE_MASK	MAC_DA_5_MASK	mac_da_4_mask	MAC_DA_3_MASK	MAC_DA_2_MASK	MAC_DA_1_MASK	MAC_DA_0_MASK	MAC_SA_5_MASK	MAC_SA_4_MASK	MAC_SA_3_MASK	MAC_SA_2_MASK	MAC_SA_1_MASK	MAC_SA_0_MASK
R=0	RW=0	RW=0	RW=0	RW=0	RW=0	RW=0	RW=0	RW=0	RW=0	RW=0	RW=0	RW=0	RW=0	RW=0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-171 SAM_MASK_N

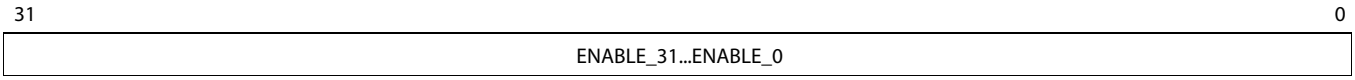
Bits	Field	Description
31-24	tci_an_mask	Separate compare enable bits for the macsec_tci_an field in the SAM_MISC_MATCH_x register – should only be set to non-zero for an actual MACsec packet. The TCI bits are in bits [31:26] while the AN bits reside in bits [25:24]. These bits are Reserved for an egress-only (-e) core.
23	macsec_sci_mask	1b = Enable MACsec header SCI value compare with 64 bits SCI value in the SAM_SCI_MATCH_LO/HI_x registers – should only be set to 1b for an actual MACsec packet This bit is Reserved for an egress-only (-e) core.
22-21	Reserved	
20	ctrl_packet_mask	1b = Enable control packet status compare with control_packet bit in the SAM_MISC_MATCH_x register
19	source_port_mask	1b = Enable source port compare with source_port field in the SAM_MISC_MATCH_x register
18	vlan_id_mask	1b = Enable parsed VLAN ID value compare with vlan_id field in the SAM_MAC_DA_MATCH_HI_x register
17	vlan_up_mask	1b = Enable parsed VLAN User Priority value compare with vlan_up field in the SAM_MISC_MATCH_x register
16	qtag_vld_mask	1b = Enable parsed QTAG valid flag compare with qtag_valid bit in the SAM_MISC_MATCH_x register
15	stag_vld_mask	1b = Enable parsed STAG valid flag compare with stag_valid bit in the SAM_MISC_MATCH_x register
14	Reserved	
13	vlan_vld_mask	1b = Enable parsed VLAN valid flag compare with vlan_valid bit in the SAM_MISC_MATCH_x register
12	mac_etype_mask	1b = Enable parsed Ether-type field compare with ether_type field in the SAM_MAC_DA_MATCH_LO_x register
11	mac_da_5_mask	1b = Enable MAC_DA bits [47:40] (first byte received) compare with bits [7:0] in the SAM_MAC_DA_MATCH_LO_x register
10	mac_da_4_mask	1b = Enable MAC_DA bits [39:32] compare with bits [15:8] in the SAM_MAC_DA_MATCH_LO_x register
9	mac_da_3_mask	1b = Enable MAC_DA bits [31:24] compare with bits [23:16] in the SAM_MAC_DA_MATCH_LO_x register
8	mac_da_2_mask	1b = Enable MAC_DA bits [23:16] compare with bits [31:24] in the SAM_MAC_DA_MATCH_LO_x register
7	mac_da_1_mask	1b = Enable MAC_DA bits [15:8] compare with bits [7:0] in the SAM_MAC_DA_MATCH_HI_x register
6	mac_da_0_mask	1b = Enable MAC_DA bits [7:0] (last byte received) compare with bits [15:8] in the SAM_MAC_DA_MATCH_HI_x register
5	mac_sa_5_mask	1b = Enable MAC_SA bits [47:40] (first byte received) compare with bits [7:0] in the SAM_MAC_SA_MATCH_LO_x register

Table 3-171 SAM_MASK_N

Bits	Field	Description
4	mac_sa_4_mask	1b = Enable MAC_SA bits [39:32] compare with bits [15:8] in the SAM_MAC_SA_MATCH_LO_x register
3	mac_sa_3_mask	1b = Enable MAC_SA bits [31:24] compare with bits [23:16] in the SAM_MAC_SA_MATCH_LO_x register
2	mac_sa_2_mask	1b = Enable MAC_SA bits [23:16] compare with bits [31:24] in the SAM_MAC_SA_MATCH_LO_x register
1	mac_sa_1_mask	1b = Enable MAC_SA bits [15:8] compare with bits [7:0] in the SAM_MAC_SA_MATCH_HI_x register
0	mac_sa_0_mask	1b = Enable MAC_SA bits [7:0] (last byte received) compare with bits [15:8] in the SAM_MAC_SA_MATCH_HI_x register
End of Table 3-171		

3.7.2.9 SAM_ENTRY_ENABLE1

Figure 3-156 SAM_ENTRY_ENABLE1



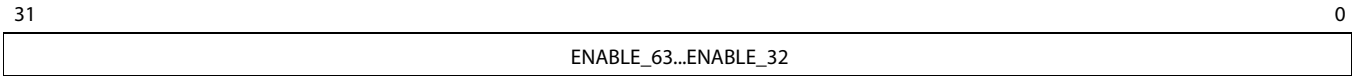
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-172 SAM_ENTRY_ENABLE1

Bits	Field	Description
31-24	enable_31...enable_0	1b = Enable SA match the corresponding entry (in SAM_..._x registers)
End of Table 3-172		

3.7.2.10 SAM_ENTRY_ENABLE2

Figure 3-157 SAM_ENTRY_ENABLE2



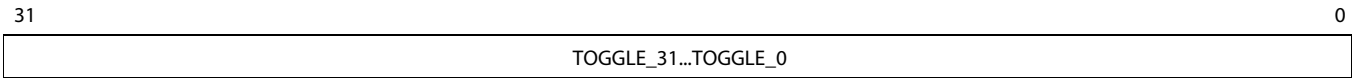
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-173 SAM_ENTRY_ENABLE2

Bits	Field	Description
31-24	enable_63...enable_32	1b = Enable SA match the corresponding entry (in SAM_..._x registers)
End of Table 3-173		

3.7.2.11 SAM_ENTRY_TOGGLE1

Figure 3-158 SAM_ENTRY_TOGGLE1



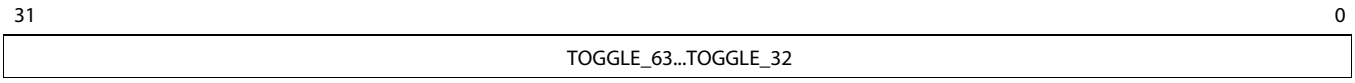
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-174 SAM_ENTRY_TOGGLE1

Bits	Field	Description
31-24	TOGGLE_13...TOGGLE_0	1b = Toggle enable_n bit in SAM_ENTRY_ENABLE1 register, writing 0b has no effect
End of Table 3-174		

3.7.2.12 SAM_ENTRY_TOGGLE2

Figure 3-159 SAM_ENTRY_TOGGLE2



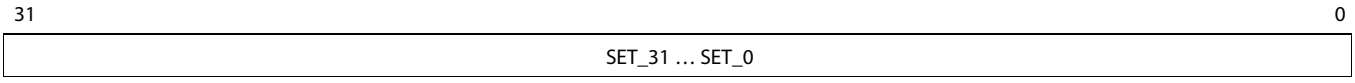
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-175 SAM_ENTRY_TOGGLE2

Bits	Field	Description
31-24	TOGGLE_13...TOGGLE_0	1b = Toggle enable_n bit in SAM_ENTRY_ENABLE2 register, writing 0b has no effect
End of Table 3-175		

3.7.2.13 SAM_ENTRY_SET1

Figure 3-160 SAM_ENTRY_SET1



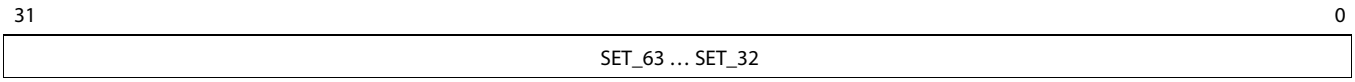
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-176 SAM_ENTRY_SET1

Bits	Field	Description
31-24	set_31 … set_0	1b = Set enable_n bit in SAM_ENTRY_ENABLE_1 register, writing 0b has no effect
End of Table 3-176		

3.7.2.14 SAM_ENTRY_SET2

Figure 3-161 SAM_ENTRY_SET2



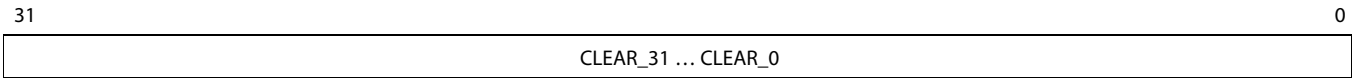
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-177 SAM_ENTRY_SET2

Bits	Field	Description
31-24	set_63 … set_32	1b = Set enable_n bit in SAM_ENTRY_ENABLE2 register, writing 0b has no effect
End of Table 3-177		

3.7.2.15 SAM_ENTRY_CLEAR1

Figure 3-162 SAM_ENTRY_CLEAR1



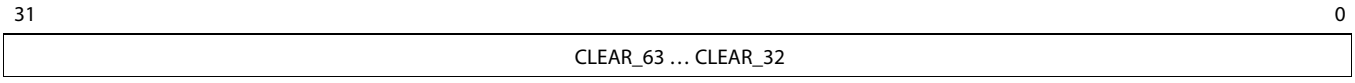
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-178 SAM_ENTRY_CLEAR1

Bits	Field	Description
31-24	clear_31 … clear_0	1b = Clear enable_n bit in SAM_ENTRY_ENABLE1 register, writing 0b has no effect
End of Table 3-178		

3.7.2.16 SAM_ENTRY_CLEAR2

Figure 3-163 SAM_ENTRY_CLEAR2



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-179 SAM_ENTRY_CLEAR2

Bits	Field	Description
31-24	clear_63 … clear_32	1b = Clear enable_n bit in SAM_ENTRY_ENABLE2 register, writing 0b has no effect
End of Table 3-179		

3.7.2.17 SAM_IN_FLIGHT

Figure 3-164 SAM_IN_FLIGHT

31				0
LOAD_UNSAFE	Reserved	IN_FLIGHT	Reserved	UNSAFE
	R-0h	RW-0h	R-0h	RW-0h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-180 SAM_IN_FLIGHT

Bits	Field	Description
31	load_unsafe	Debug functionality: 1b = Load unsafe field in this register with contents of in_flight field of that same register to start counting down just like when disabling an SA match entry, writing 0b has no effect.
30-14	reserved	
13-8	in_flight	Read-only, number of packets in the EIP-160 pipeline at this time. This counter increments on every packet entering the pipeline for classification and decrements on every packet that has been handled by the statistics counters module (this includes packets that are officially dropped).
7-6	reserved	
5-0	unsafe	Read-only, number of packets in the EIP-160 pipeline that might want to use an SA that has been disabled. This counter is copied from the in_flight counter when any of the enable_X bits drops from 1b to 0b and then decrements towards zero on every packet that has been handled by the statistics counters module (this includes packets that are officially dropped). After disabling an SA, Host software should wait until this field is zero before final readout of the SA statistics and re-using the transform record.
End of Table 3-180		

3.7.3 Flow Control Words for frames that matched an SA parameter set

This section describes the registers available in the Flow Control Registers area of the MACSEC module. The register has two versions: Ingress version & Egress version. The offset addresses listed in Table 3-181 are relative to the MACSEC module offset address. To determine the offset address of the MACSEC module, please see Table 3-1. Please note the ingress and egress offsets for each MACSEC instance since it is relevant for this register area. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

- 3.7.3.1 "SAM_FLOW_CTRL_N (Ingress) Byte Address Offset 0x7000 + (n * 4)" on page 3-109
- 3.7.3.2 "SAM_FLOW_CTRL_N (Egress) Byte Address Offset 0x7000 + (n * 4)" on page 3-109

Table 3-181 shows the submodules contained in the Transform Records Area.

Table 3-181 Flow Control Words for frames that matched an SA parameter set

Offset Address [1]	Acronym	Submodule Name	Section
0x7000 – 0x703F	SAM_FLOW_CTRL_0 … SAM_FLOW_CTRL_15	flow control words for SA 0 till 15 matched packets (per SA match):	Section 3.7.3.1 & Section 3.7.3.2
0x7040 – 0x707F	SAM_FLOW_CTRL_16 … SAM_FLOW_CTRL_31	flow control words for SA 16 till 31 matched packets (per SA match)	Section 3.7.3.1 & Section 3.7.3.2
0x7080 – 0x70FF	SAM_FLOW_CTRL_32 … SAM_FLOW_CTRL_63	flow control words for SA 32 till 63 matched packets (per SA match)	Section 3.7.3.1 & Section 3.7.3.2
End of Table 3-181			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.7.3.1 SAM_FLOW_CTRL_N (Ingress) Byte Address Offset 0x7000 + (n * 4)

Figure 3-165 SAM_FLOW_CTRL_N (Ingress)

31	30 24	23 21	20 19	18	17
Reserved	CONFIDENTIALITY_OFFSET	Reserved	VALIDATE_FRAMES	Reserved	SA_IN_USE
R=0	RW=0	R=0	RW=0	R=0	RW=0

16	15 8	7 6	5	4	3 2	1 0
REPLAY_PROTECT	Reserved	DROP_ACTION	Reserved	DROP_NON_RESERVED	DEST_PORT	FLOW_TYPE
RW=0	R=0	RW=0	R=0	RW=0	RW=0	RW=0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-182 SAM_FLOW_CTRL_N (Ingress)

Bits	Field	Description
31	reserved	
30-24	confidentiality_offset	The number of bytes (in the range of 0-64) that are be authenticated but not encrypted following the SecTag in the encrypted MACsec packet. Values 65-127 are reserved and should not be used
23-21	reserved	
20-19	validate_frames	Frame validation level, 00b = disabled, 01b = check, 10b = strict, 11b = Reserved This function is used for MACsec ingress processing only (flow_type = 10b)
18	reserved	
17	sa_in_use	1b = MACsec SA inUse for the looked-up SA
16	replay_protec	1b = enable replay protection, 0b = disable replay protection This function is used for MACsec ingress processing only (flow_type = 10b)
15-8	reserved	
7-6	drop_action	Defines the way the drop operation is performed: 00b = bypass with CRC corruption signaling, 01b = bypass with bad packet indicator, 10b = internal drop by crypto-core (packet is not seen outside), 11b = do not drop (for debugging only).
5	reserved	
4	drop_non_reserved	Perform drop_action if packet is not from the reserved port This bit is Reserved for an egress-only (-e) configuration.
3-2	dest_port	Destination port: 00b = Common port, 01b = Reserved port, 10b = Controlled Port, 11b = Uncontrolled port
1-0	flow_type	Flow type (action type): 00b = bypass, 01b = perform drop_action, 10b = MACsec ingress , 11b = MACsec egress. The static_bypass bit in the MISC_CONTROL register can disable the MACsec crypto-core, forcing the MACsec operation to "bypass" – the contents of this field are not influenced by this overruling.
End of Table 3-182		

3.7.3.2 SAM_FLOW_CTRL_N (Egress) Byte Address Offset 0x7000 + (n * 4)

Figure 3-166 SAM_FLOW_CTRL_N (Egress)

31	30 24	23 21	20 19	18	18	17
CONF_PROTECT	CONFIDENTIALITY_OFFSET	Reserved	USE_SCB	USE_ES	INCLUDE_SCI	SA_IN_USE
R=0	RW=0	R=0	RW=0			RW=0

16	15 8	7 6	5	4	3 2	1 0
PROTECT_FRAME	Reserved	DROP_ACTION	Reserved	DROP_NON_RESERVED	DEST_PORT	FLOW_TYPE
RW=0	R=0	RW=0	R=0	RW=0	RW=0	RW=0

Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-183 SAM_FLOW_CTRL_N (Egress)

Bits	Field	Description
31	conf_protect	1b = enable confidentiality protection, 0b = disable confidentiality protection This function is used for MACsec egress processing only (flow_type = 11b)
30-24	confidentiality_offset	The number of bytes (in the range of 0-64) that are be authenticated but not encrypted following the SecTag in the encrypted MACsec packet. Values 65-127 are reserved and should not be used
23-21	reserved	
20	use_scb	1b = set SCB („Single Copy Broadcast?) bit in TCI field, 0b = clear SCB bit in TCI field This function is used for MACsec egress processing only (flow_type = 11b)
19	use_es	1b = set ES („End Station?) bit in TCI field, 0b = clear ES bit in TCI field This function is used for MACsec egress processing only (flow_type = 11b)
18	include_sci	1b = include explicit SCI in packet, 0b = use implicit SCI (not transmitted in packet) This function is used for MACsec egress processing only (flow_type = 11b)
17	sa_in_use	1b = MACsec SA inUse for the looked-up SA
16	protect_frame	1b = enable frame protection, 0b = bypass frame through crypto-core This function is used for MACsec egress processing only (flow_type = 11b)
15-8	reserved	
7-6	drop_action	Defines the way the drop operation is performed: 00b = bypass with CRC corruption signaling, 01b = bypass with bad packet indicator, 10b = internal drop by crypto-core (packet is not seen outside), 11b = do not drop (for debugging only).
5	reserved	
4	drop_non_reserved	Perform drop_action if packet is not from the reserved port This bit is Reserved for an egress-only (-e) configuration.
3-2	dest_port	Destination port: 00b = Common port, 01b = Reserved port, 10b = Controlled Port, 11b = Uncontrolled port
1-0	flow_type	Flow type (action type): 00b = bypass, 01b = perform drop_action, 10b = MACsec ingress , 11b = MACsec egress. The static_bypass bit in the MISC_CONTROL register can disable the MACsec crypto-core, forcing the MACsec operation to "bypass" – the contents of this field are not influenced by this overruling.
End of Table 3-183		

3.7.4 Security statistics counters of 40 bits each

This section describes the registers available in the Security Statistics area of the MACSEC module. The register has two versions: Ingress version & Egress version. The offset addresses listed in Table 3-184 are relative to the MACSEC module offset address. To determine the offset address of the MACSEC module, please see Table 3-1. Please note the ingress and egress offsets for each MACSEC instance since it is relevant for this register area. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

Table 3-184 shows the submodules contained in the Security Statistics area.

Table 3-184 Security Statistics Counters of 40 Bits Each

Offset Address [1]	Acronym	Submodule Name	Section
0x8000 – 0xBFFF	SA related statistics counters	Statistics counters	Section 3.7.4.1
0xC000 – 0xC3FF	8 sets of VLAN related statistics counters		Section 3.7.4.2
0xC400 – 0xC7FF	Global statistics counters		Section 3.7.4.3
End of Table 3-184			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.7.4.1 SA related statistics counters

Table 3-185 Statistics Counters (Part 1 of 2)

SA statistics	Counter
0x8000 – 0x8004	SA 0, mask bit [0]: sa.InOctetsDecrypted/InOctetsValidated (chained, 1st counter) (ingress) SA 0, mask bit [0]: sa.OutOctetsEncrypted/OutOctetsProtected(chained, 1st counter) (egress)
0x8008 – 0x800C	SA 0, mask bit [1]: sa.InOctetsDecrypted/InOctetsValidated (chained, 2nd counter) (ingress) SA 0, mask bit [1]: sa.OutOctetsEncrypted/OutOctetsProtected (chained, 2nd counter) (egress)
0x8010 – 0x8014	SA 0, mask bit [2]: sa.InPktsUnchecked/InPktsHitDropReserved (ingress) SA 0, mask bit [2]: sa.OutPktsEncrypted/OutPktsProtected/OutPktsHitDropReserved (egress)
0x8018 – 0x801C	SA 0, mask bit [3]: sa.InPktsDelayed (ingress) SA 0, mask bit [3]: sa.OutPktsTooLong (MTU check) (egress)
0x8020 – 0x8024	SA 0, mask bit [4]: sa.InPktsLate (ingress, counter is not used for egress)
0x8028 – 0x802C	SA 0, mask bit [5]: sa.InPktsOk (ingress, counter is not used for egress)
0x8030 – 0x8034	SA 0, mask bit [6]: sa.InPktsInvalid (sum with next one gives sa.InPktsAuthFail, replay fail overrules) (ingress, counter is not used for egress)
0x8038 – 0x803C	SA 0, mask bit [7]: sa.InPktsNotValid (ingress, counter is not used for egress)
0x8040 – 0x8044	SA 0, mask bit [8]: sa.InPktsNotUsingSA (added with next one gives sa.InPktsSAMiss) (ingress, counter is not used for egress)
0x8048 – 0x804C	SA 0, mask bit [9]: sa.InPktsUnusedSA (ingress, counter is not used for egress)
0x8050 – 0x8054	SA 0, mask bit [10]: sa.InPktsUntaggedHit (ingress, counter is not used for egress)
0x8058 – 0x807C	Reserved
0x8080 – 0x80D4	SA 1: Same counters as for SA 0
0x80D8 – 0x80FC	Reserved
0x8100 – 0x8154	SA 2: Same counters as for SA 0
0x8158 – 0x817C	Reserved
0x8180 – 0x81D4	SA 3: Same counters as for SA 0
0x81D8 – 0x81FC	Reserved
0x8200 – 0x8254	SA 4: Same counters as for SA 0
0x8258 – 0x827C	Reserved
0x8280 – 0x82D4	SA 5: Same counters as for SA 0
0x82D8 – 0x82FC	Reserved
0x8300 – 0x8354	SA 6: Same counters as for SA 0
0x8358 – 0x837C	Reserved
0x8380 – 0x83D4	SA 7: Same counters as for SA 0
0x83D8 – 0x83FC	Reserved
0x8400 – 0x8454	SA 8: Same counters as for SA 0
0x8458 – 0x847C	Reserved
0x8480 – 0x84D4	SA 9: Same counters as for SA 0

Table 3-185 Statistics Counters (Part 2 of 2)

SA statistics	Counter
0x84D8 – 0x84FC	Reserved
0x8500 – 0x8554	SA 10: Same counters as for SA 0
0x8558 – 0x857C	Reserved
0x8580 – 0x85D4	SA 11: Same counters as for SA 0
0x85D8 – 0x85FC	Reserved
0x8600 – 0x8654	SA 12: Same counters as for SA 0
0x8658 – 0x867C	Reserved
0x8680 – 0x86D4	SA 13: Same counters as for SA 0
0x86D8 – 0x86FC	Reserved
0x8700 – 0x8754	SA 14: Same counters as for SA 0
0x8758 – 0x877C	Reserved
0x8780 – 0x87D4	SA 15: Same counters as for SA 0
0x87D8 – 0x87FC	Reserved
0x8800 – 0x8FFC	SA16...SA31: Same counters as for SA 0
0x9000 – 0x9FFC	SA32...SA63: Same counters as for SA 0
0xA000 – 0xBFFC	Reserved
End of Table 3-185	

3.7.4.2 8 sets of VLAN Related Statistics Counters

Table 3-186 8 Sets of VLAN Related Statistics Counters

SA statistics	Counter
0xC000 – 0xC004	VLAN UP 0, mask bit [0]: vlan.InOctetsVL (chained, 1st counter)
0xC008 – 0xC00C	VLAN UP 0, mask bit [1]: vlan.InOctetsVL (chained, 2nd counter)
0xC010 – 0xC014	VLAN UP 0, mask bit [2]: vlan.OutOctetsVL (chained, 1st counter)
0xC018 – 0xC01C	VLAN UP 0, mask bit [3]: vlan.OutOctetsVL (chained, 2nd counter)
0xC020 – 0xC024	VLAN UP 0, mask bit [4]: vlan.InPktsVL
0xC028 – 0xC02C	VLAN UP 0, mask bit [5]: vlan.InDroppedPktsVL
0xC030 – 0xC034	VLAN UP 0, mask bit [6]: vlan.InOverSizePktsVL (MTU check)
0xC038 – 0xC03C	VLAN UP 0, mask bit [7]: vlan.OutPktsVL
0xC040 – 0xC044	VLAN UP 0, mask bit [8]: vlan.OutDroppedPktsVL
0xC048 – 0xC04C	VLAN UP 0, mask bit [9]: vlan.OutOverSizePktsVL (MTU check)
0xC028 – 0xC07C	Reserved
0xC080 – 0xC0A4	VLAN UP 1: Same counters as for VLAN UP 0
0xC0A8 – 0xC0FC	Reserved
0xC100 – 0xC024	VLAN UP 2: Same counters as for VLAN UP 0
0xC128 – 0xC17C	Reserved
0xC180 – 0xC1A4	VLAN UP 3: Same counters as for VLAN UP 0
0xC1A8 – 0xC1FC	Reserved
0xC200 – 0xC224	VLAN UP 4: Same counters as for VLAN UP 0
0xC228 – 0xC27C	Reserved
0xC280 – 0xC2A4	VLAN UP 5: Same counters as for VLAN UP 0

Table 3-186 8 Sets of VLAN Related Statistics Counters

SA statistics	Counter
0xC2A8 – 0xC2FC	Reserved
0xC300 – 0xC324	VLAN UP 6: Same counters as for VLAN UP 0
0xC328 – 0xC37C	Reserved
0xC380 – 0xC3A4	VLAN UP 7: Same counters as for VLAN UP 0
0xC3A8 – 0xC3FC	Reserved
End of Table 3-186	

3.7.4.3 Global Statistics Counters

Table 3-187 Global Statistics Counters

SA statistics	Counter
0xC400 – 0xC404	Global mask bit [0]: global.TransformErrorPkts
0xC408 – 0xC40C	Global mask bit [1]: global.InPktsCtrl
0xC410 – 0xC414	Global mask bit [2]: global.InPktsNoTag
0xC418 – 0xC41C	Global mask bit [3]: global.InPktsUntagged
0xC420 – 0xC424	Global mask bit [4]: global.InPktsTagged
0xC428 – 0xC42C	Global mask bit [5]: global.InPktsBadTag
0xC430 – 0xC434	Global mask bit [6]: global.InPktsUntaggedMiss
0xC438 – 0xC43C	Global mask bit [7]: global.InPktsNoSCI (added with next one gives global.InPktsSCIMiss)
0xC440 – 0xC444	Global mask bit [8]: global.InPktsUnknownSCI
0xC448 – 0xC44C	Global mask bit [9]: global.InConsistCheckControlledNotPass
0xC450 – 0xC454	Global mask bit [10]: global.InConsistCheckUncontrolledNotPass
0xC458 – 0xC45C	Global mask bit [11]: global.InConsistCheckControlledPass
0xC460 – 0xC464	Global mask bit [12]: global.InConsistCheckUncontrolledPass
0xC468 – 0xC46C	Global mask bit [13]: global.InOverSizePkts
0xC46C – 0xC470	Global mask bit [14]: global.OutPktsCtrl
0xC470 – 0xC474	Global mask bit [15]: global.OutPktsUnknownSA
0xC474 – 0xC478	Global mask bit [16]: global.OutPktsUntagged
0xC478 – 0xC47C	Global mask bit [17]: global.OutOverSizePkts (MTU check)
0xC480 – 0xC7FC	Reserved
End of Table 3-187	

3.7.5 Security Statistics Counter Control and Debug

This section describes the registers available in the Security statistics counter control and debug area of the MACSEC module. The offset addresses listed in Table 3-184 are relative to the MACSEC module offset address. To determine the offset address of the MACSEC module, please see Table 3-1. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

Table 3-184 shows the submodules contained in the Security Statistics area.

Table 3-188 Security Statistics Counters Control and Debug

Offset Address [1]	Acronym	Submodule Name	Section
0xC800 – 0xC80C	Reserved		
0xC810	COUNT_CONTROL	Statistics counters control	Section 3.7.5.1
0xC814-0xCFFF	Reserved		
End of Table 3-188			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.7.5.1 Count Control

Figure 3-167 Count Control

31	4	3	2	1	0
Reserved		AUTO_CNTR_RESET	SATURATE_CNTRS	DEBUG_ACCESS	RESET_ALL
R-0h		RW-0h		R-0h	RW-0h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-189 Count Control

Bits	Field	Description
31-4	Reserved	
3	auto_cntr_reset	0b = Reading counters does not change them, 1b = Counters are cleared on a read access
2	saturate_cntrs	0b = Counters wrap back to zero on overflow, 1b = Counters do not increment past maximum value
1	debug_access	1b = Enable normal read/write access to the counter memory for debugging purposes (reset_all has priority). In this mode, increment operation requests (as well as test increment requests made via the COUNT_DEBUG4 register) are ignored and clear-on-read is suppressed.
0	reset_all	Set-only: 1b = Reset all statistics counters to zero (increments are ignored while doing this, reading any counter returns zeroes), automatically falls back to 0b when done. Writing 0b has no effect. Default state of 1b coming out of reset clears all counters after power-up. Writing this bit with a 1b keeps other fields in this register intact, irrespective the value written.
End of Table 3-189		

3.7.6 Consistency Check Parameters Sets Control Bits and Debug Status

This section describes the registers available in the Consistency check parameters sets control bits and debug status area of the MACSEC module. The offset addresses listed in Table 3-190 are relative to the MACSEC module offset address. To determine the offset address of the MACSEC module, please see Table 3-1. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

Table 3-190 shows the submodules contained in the Consistency check parameters sets control bits and debug status register area.

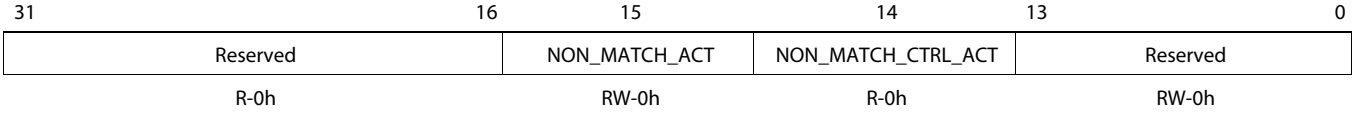
Table 3-190 Consistency Check Parameters Sets Control Bits and Debug Status

Offset Address [1]	Acronym	Submodule Name	Section
0xE000-0xE83F	Reserved		
0xE840	IG_CC_CONTROL	Ingress consistency check controll	Section 3.7.6.1
0xE844	IG_CC_TAGS		Section 3.7.6.2
0xE848-0xEFFF	Reserved		
End of Table 3-190			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.7.6.1 IG_CC _CONTROL

Figure 3-168 IG_CC_CONTROL



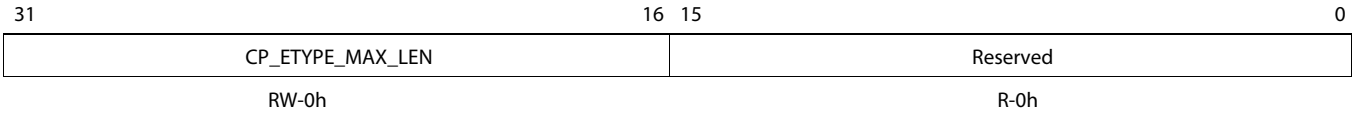
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-191 IG_CC_CONTROL

Bits	Field	Description
31-16	Reserved	
15	non_match_act	Action to perform on control packet (as defined by the control packet classification logic) when none of the entries matches, 0b = drop, 1b = pass
14	non_match_ctrl_act	Action to perform on non-control packet (as defined by the control packet classification logic) when none of the entries matches, 0b = drop, 1b = pass
13-0	Reserved	
End of Table 3-191		

3.7.6.2 IG_CC_TAGS

Figure 3-169 IG_CC_TAGS



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-192 IG_CC_TAGS

Bits	Field	Description
31-16	CP_ETYPE_MAX_LEN	Ether-type field compare value for the etype_valid comparison (global for all entries), default value 0x05FF indicates the maximum length that can be encoded in the Ether-type field, which is 1535 Bytes – as this is a length compare, this field is not swapped
15-0	Reserved	
End of Table 3-192		

3.7.7 9 MTU Check Control Words for VLAN packets and Non-VLAN Packets

This section describes the registers available in the Consistency check parameters sets control bits and debug status area of the MACSEC module. The offset addresses listed in Table 3-193 are relative to the MACSEC module offset address. To determine the offset address of the MACSEC module, please see Table 3-1. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

- 3.7.7.1 "NON_VLAN_MTU_CHECK" on page 3-116

Table 3-193 shows the submodules contained in the MTU check control words for VLAN and non-VLAN packets register area.

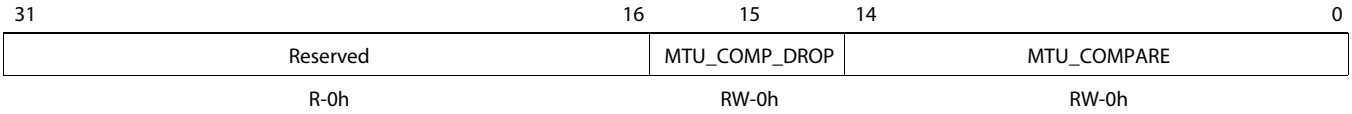
Table 3-193 9 MTU Check Control Words for VLAN Packets and Non-VLAN Packets

Offset Address [1]	Acronym	Submodule Name	Section
0xF000-0xF11F	Reserved		
0xF120	NON_VLAN_MTU_CHECK	Non-VLAN MTU setting	Section 3.7.7.1
End of Table 3-193			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.7.7.1 NON_VLAN_MTU_CHECK

Figure 3-170 NON_VLAN_MTU_CHECK



Legend: R = Read only; W = Write only; *-n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-194 NON_VLAN_MTU_CHECK

Bits	Field	Description
31-16	Reserved	
15	MTU_COMP_DROP	1b = drop (by corrupting the CRC) all non-VLAN packets that are longer than the maximum packet size defined by the mtu_compare field
14-0	MTU_COMPARE	Maximum packet size (in bytes) allowed for all non-VLAN packets. Default value 1514 (decimal, or 0x05EA) allows standard Ethernet frames (without CRC) without a VLAN tag. Packets longer than the value programmed here will be counted as „oversized? packets and can optionally be truncated and dropped under control of the mtu_comp_drop bit
End of Table 3-194		

3.7.8 Security Fail Control Masks and Debug Registers for Packet Engine

This section describes the registers available in the Security fail control masks and debug registers for Packet Engine register area of the MACSEC module. The offset addresses listed in Table 3-195 are relative to the MACSEC module offset address. To determine the offset address of the MACSEC module, please see Table 3-1. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

- 3.7.8.1 "COUNT_SECFAIL1" on page 3-117

Table 3-195 shows the submodules contained in the Security fail control masks and debug registers for Packet Engine register area.

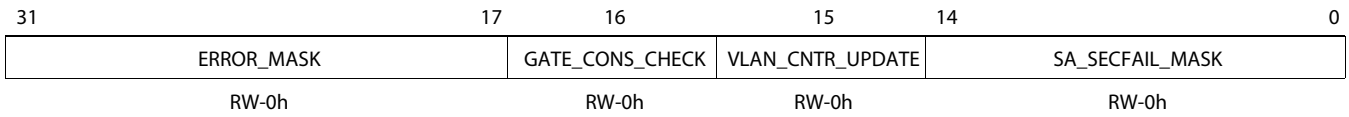
Table 3-195 Security Fail Control Masks and Debug Registers for Packet Engine

Offset Address [1]	Acronym	Submodule Name	Section
0xF124	COUNT_SECFAIL1	Security failure counter masks & post-process error mask	Section 3.7.8.1
0xF128-0xF12F	Reserved		
End of Table 3-195			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.7.8.1 COUNT_SECFAIL1

Figure 3-171 COUNT_SECFAIL1



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-196 COUNT_SECFAIL1

Bits	Field	Description
31-17	error_mask	Mask for MACsec crypto-core first result token word bits [31:17] – these are the error bits of that module?s processing. The default value selects the errors that are deemed fatal. The contents of this field should not be changed except for AuthenTec debugging.
16	gate_cons_check	0b = always use result of consistency checking module, 1b = force outputs of consistency checking module to 'non-consistent' and 'no VLAN tag found' if a MACsec packet fails integrity check,performed by the MACsec crypto core.
15	vlan_cntr_update	0b = do not update any VLAN counters for a non-VLAN packet, 1b = update VLAN counters for non-VLAN packets using the default User Priority assigned to them
14-0	sa_secfail_mask	This mask specifies which SA-related counter increments are regarded a security fail event – bit [0] is for the first 40-bits counter of an SA-related counter set. Note that the upper 40-bits counters of an octet counter should not have their mask bit set here. Note: In the –i configuration, there are 11 SA counters – bits [14:11] must be kept zero. In the –e configuration, there are 4 SA counters – bits [14:4] must be kept zero. In the –ie configuration, there are 11 SA counters – bits [14:11] must be kept zero.
End of Table 3-196		

3.7.9 Access space for Packet Engine

This section describes the registers available in the Packet Engine register area of the MACSEC module. The offset addresses listed in Table 3-197 are relative to the MACSEC module offset address. To determine the offset address of the MACSEC module, please see Table 3-1. For convenience, a complete list of all of the registers in the 10GbE switch subsystem is provided in Table 3-2.

- 3.7.9.1 "CONTEXT_CONTROL" on page 3-118
- 3.7.9.2 "BLOCK_CONTEXT_UPDATE" on page 3-118

Table 3-197 shows the submodules contained in the Packet Engine register area.

Table 3-197 Security Fail Control mMasks and Debug Registers for Packet Engine

Offset Address [1]	Acronym	Submodule Name	Section
0xF000-0xF004	Reserved		
0xF408	CONTEXT_CONTROL		Section 3.7.9.1
0xF430	BLOCK_CONTEXT_UPDATE		Section 3.7.9.2
0xF128-0xF12F	Reserved		
End of Table 3-197			

1. The actual addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.7.9.1 CONTEXT_CONTROL

Figure 3-172 CONTEXT_CONTROL

31 16	15 10	9	8	7 0
MACSEC_ETHER_TYPE	Reserved	CONTROL MODE	ADDRESS MODE	CONTEXT SIZE (DWORDS)
RW-E588h	R-0h	RW-1h	RW-0h	RW-12h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-198 CONTEXT_CONTROL

Bits	Field	Description
31-16	macsec_ether_type	This field contains the EtherType field for MACsec. This field is inserted in the SecTAG when processing a MACsec outbound token. It is reset to 0xE588 (EtherType 88-E5 represented in little endian format) and should not be changed, unless the MACsec EtherType definition in [4] changes.
15-10	reserved	
9	control mode	Selects a fetch of only relevant context fields. This bit is always one. (Read only) Refer to the next paragraph for details about the fetch modes.
8	address mode	This mode is not supported in the EIP60. This bit is always zero. (Read only)
7-0	context size (dwords)	Indicates the size (in dwords) of the context that must be fetched. This field must be programmed with the value that corresponds to the used context with the maximum size (refer to Table 19 for supported contexts). Note that the EIP60 always fetches a multiple of 16 bytes. This means that the programmed value is rounded up to the next multiple of four (32-bit words), if needed.
End of Table 3-198		

3.7.9.2 BLOCK_CONTEXT_UPDATE

Figure 3-173 BLOCK_CONTEXT_UPDATE

31 2	1 0
Reserved	BLOCK CONTEXT UPDATES
R-0h	RW-0h

Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-199 BLOCK_CONTEXT_UPDATE

Bits	Field	Description
31-2	Reserved	
1-0	block context updates	If both the bit in this register and the related input bit for a frame are set to one, the context update for that frame is blocked.
End of Table 3-199		

3.8 10 Gigabit Ethernet Subsystem Registers

This section describes the registers located at the subsystem level of the 10Gigabit Ethernet .

Table 3-200 lists the registers in the SerDes SGMII boot configuration module.

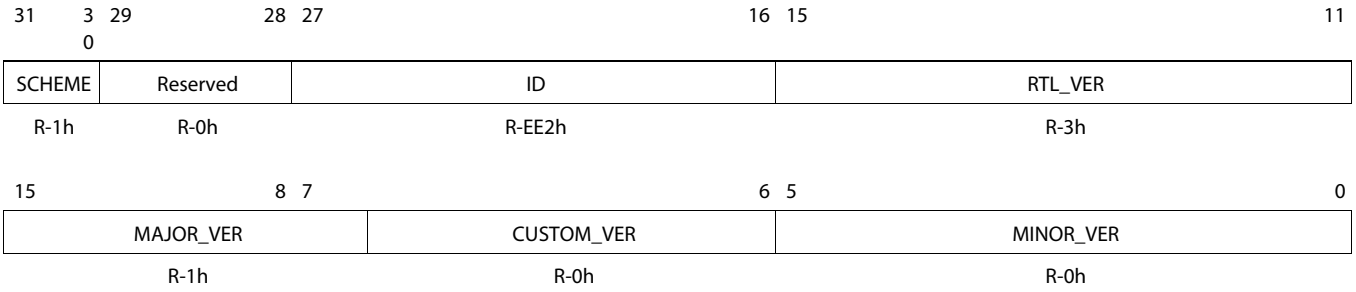
Table 3-200 10Gigabit Ethernet Subsystem Registers

Offset Address[1]	Register Mnemonic	Register Name	Section
00h	IDVER	Identification and Version Register	Section 3.8.1
04h-0Ch	Reserved		Section 3.8.2
10h	CPPI_TS	CPPI Timestamp Register	Section 3.8.3
14h	CPPI_TS_EN	CPPI Timestamp Enable Register	Section 3.8.4
18h	CPPI_TS_DIV	CPPI Timestamp Divider Register	Section 3.8.3
End of Table 3-200			

1. The addresses of these registers are device specific. See your device-specific data manual to verify the register addresses.

3.8.1 Identification and Verification Register (IDVER)

Figure 3-174 Identification and Verification Register (IDVER)



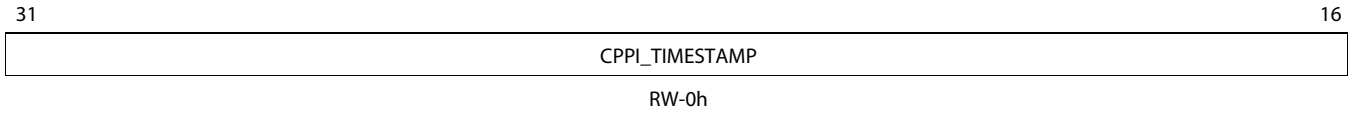
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-201 Identification and Verification Register (IDVER) Field Descriptions

Bits	Field	Description
31-30	Scheme	ID Scheme
29-28	Reserved	
27-16	ID	Module Identification value.
15-11	RTL Version	Module RTL version
10-8	Major Version	Module Major version
7-6	Custom Version	Module Custom version.
5-0	Minor Version1	Module Minor version
End of Table 3-201		

3.8.2 CPPI Timestamp Register (CPPI_TS)

Figure 3-175 CPPI Timestamp Register (CPPI_TS)



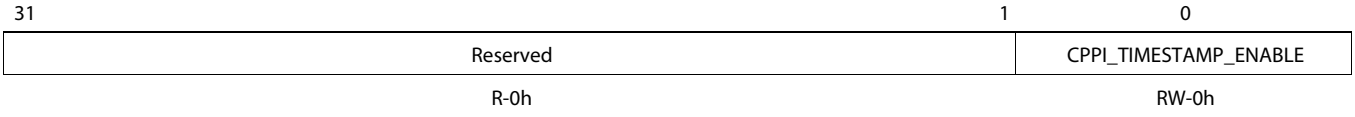
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-202 CPPI Timestamp Register (CPPI_TS)

Bits	Field	Description
31-0	CPPI TImestamp	32-bit CPPI Timestamp value. The CPPI Timestamp is a running 32-bit counter that increments every X cycles (X set by CPPI Timestamp Divider Register) if enabled by the CPPI Timestamp Enable Register. The value will roll over from 0xFFFF_FFFF to 0x0000_0000. CPPI Timestamp will hold its current value if CPPI Timestamp Enable is set to 0. You must write CPPI Timestamp to 0x0 to reset. Write to set any 32-bit value. Read to read the current CPPI Timestamp
End of Table 3-202		

3.8.3 CPPI Timestamp Enable Register (CPPI_TS_EN)

Figure 3-176 CPPI Timestamp Enable Register (CPPI_TS_EN)



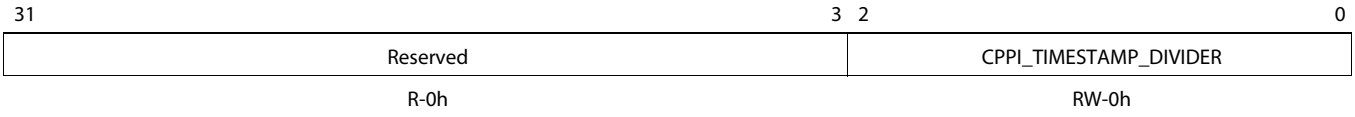
Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-203 CPPI Timestamp Enable Register (CPPI_TS_EN)

Bits	Field	Description
31-1	Reserved	Reserved
0	CPPI Timestamp Enable	Enable for CPPI Timestamp. 0 – CPPI Timestamp disabled, will not increment 1 – CPPI Timestamp enabled. CPPI Timestamp will increment by one every X cycles where X is set by the CPPI Timestamp Divider Register
End of Table 3-203		

3.8.4 CPPI Timestamp Divider Register (CPPI_TS_DIV)

Figure 3-177 CPPI Timestamp Divider Register (CPPI_TS_DIV)



Legend: R = Read only; W = Write only; -*n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 3-204 CPPI Timestamp Divider Register (CPPI_TS_DIV)

Bits	Field	Description
31-3	Reserved	
2-0	CPPI Timestamp Divider	Divider to determine how often CPPI Timestamp increments (if enabled by CPPI Timestamp Enable Register) 0 – CPPI Timestamp increments every 1 clock cycle 1 – CPPI Timestamp increments every 2 clock cycles 2 – CPPI Timestamp increments every 3 clock cycles 3 – CPPI Timestamp increments every 4 clock cycles 4 – CPPI Timestamp increments every 5 clock cycles 5 – CPPI Timestamp increments every 6 clock cycles 6 – CPPI Timestamp increments every 7 clock cycles 7 – CPPI Timestamp increments every 8 clock cycles Note that disabling the CPPI Timestamp via the CPPI Timestamp Enable register or writing a new timestamp value to the CPPI Timestamp directly will cause the internal clock counter to reset in order to avoid odd clock counting when the user wishes to reset or disable/enable the CPPI Timestamp. For example, if the divider is set to increment CPPI Timestamp every 8 clock cycles, and 6 cycles after the previous increment a new value is written to CPPI timestamp, the internal counter will not increment until 8 cycles after the write.
End of Table 3-204		

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