Technical Article

What's Not in the Power MOSFET Data Sheet, Part 1: Temperature Dependency

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Power metal-oxide semiconductor field-effect transistor (MOSFET) data sheets provide useful information such as key specifications, ratings and characteristics to help you confirm that the device will operate as intended. You may have questions about how a parameter varies, however, so in this article I'll explain not just what's in the data sheet but more importantly, what's not.

MOSFET data-sheet review

Let's use the TI CSD17576Q5B NexFET™ data sheet as an example. The first page, shown in Figure 1, summarizes of the device capabilities and is divided into features, applications and description sections, including a schematic illustration of the FET package.

The first page also includes product summary, ordering information and absolute maximum ratings tables. The product summary table is a snapshot of typical parameters so that you can pick the right FET for your application. Ordering information is self-explanatory. The absolute maximum ratings table lists the boundaries for safe operation, outside of which the MOSFET could be permanently damaged. Unless otherwise noted, the specifications and ratings in these tables are all at an ambient temperature, T_A = 25°C. In addition, typical performance plots of $R_{DS(on)}$ vs. V_{GS} (at case temperatures of T_C = 25°C and 125°C) and gate charge are also part of the first page.

TEXAS INSTRUMENTS

CSD17576Q5B

SLPS497A – JUNE 2014 – REVISED MAY 2017

CSD17576Q5B 30 V N-Channel NexFET™ Power MOSFET

1 Features

- Low Q_g and Q_{gd}
- Low $R_{DS(on)}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

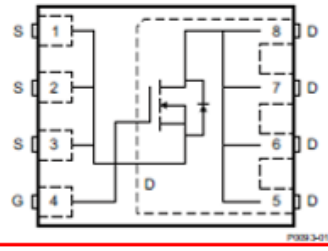
2 Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Synchronous FET Applications

3 Description

This 30 V, 1.7 mΩ, SON 5 x 6-mm NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



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Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain -to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	25		nC
Q_{gd}	Gate Charge Gate-to-Drain	5.4		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5 V	2.4	mΩ
		V_{GS} = 10 V	1.7	mΩ
$V_{GS(th)}$	Threshold Voltage	1.4		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD17576Q5B	2500	13-Inch Reel	SON 5 × 6 mm Plastic Package	Tape and Reel
CSD17576Q5BT	250	7-Inch Reel		

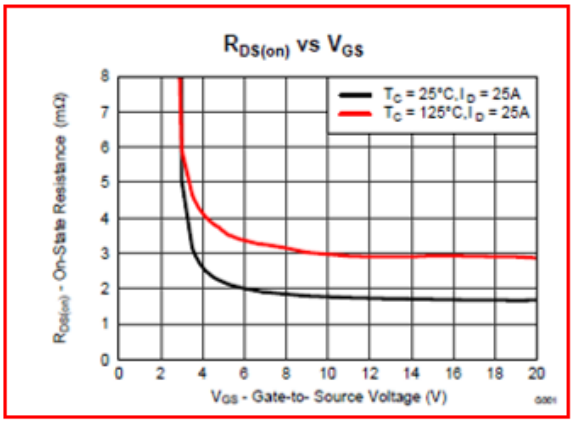
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	184	
	Continuous Drain Current(1)	30	
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	400	A
P_D	Power Dissipation(1)	3.1	W
	Power Dissipation, T_C = 25°C	125	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 48, L = 0.1 mH, R_G = 25 Ω	115	mJ

(1) Typical $R_{\theta JA}$ = 40°C/W on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1.3°C/W, Pulse duration ≤100 µs, duty cycle ≤1%.



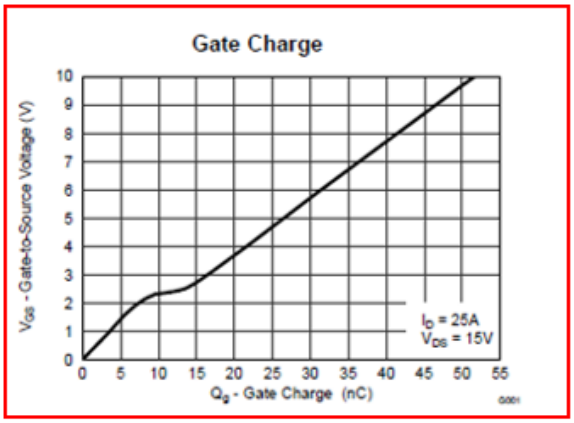


Figure 1. First page of the CSD17576Q5B NexFET™ data sheet

The second page of the data sheet includes the table of contents and the revision history. Next are the specifications tables, electrical characteristics and thermal information, followed by graphs displaying the typical MOSFET characteristics. Then there is a section on device and documentation support. The data sheet includes the mechanical, packaging and orderable information in its final section. Unless otherwise noted, all specifications and ratings are at an ambient temperature, T_A = 25°C.

Temperature dependence

Some of the FET specifications in the absolute maximum ratings table are temperature-dependent, including the drain-to-source voltage (V_{DS}), continuous drain current (I_D), pulsed drain current (I_{DM}) and power dissipation (P_D). The maximum V_{GS} ratings guarantee that there is no gate-oxide breakdown during operation and is temperature-independent. Avalanche energy (E_{AS}) is tested at case temperatures of T_C = 25°C and T_C = 125°C, with a corresponding graph in the typical MOSFET characteristics graph showing a reduction in E_{AS} at elevated temperatures.

Static characteristics

The electrical characteristics table is broken down into static, dynamic and diode characteristics, as shown in Figure 2. Let's look at the temperature-dependent FET parameters in the static characteristics section: the temperature variation of drain-to-source breakdown voltage (BV_{DSS}), drain-to-source leakage current (I_{DSS}), gate-to-source leakage current (I_{GSS}) and transconductance (g_{fs}) are not included in the data-sheet graphs. The typical MOSFET characteristics graph does include the threshold voltage, ($V_{GS(th)}$) and on-resistance ($R_{DS(on)}$) vs. temperature. The threshold voltage has a negative temperature coefficient and the on-resistance has a positive temperature coefficient.

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.1	1.4	1.8	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5 V, I_D = 25 A		2.4	2.9	mΩ
		V_{GS} = 10 V, I_D = 25 A		1.7	2.0	mΩ
g_{fs}	Transconductance	V_{DS} = 3 V, I_D = 25 A		120		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 15 V, f = 1 MHz		3410	4430	pF
C_{oss}	Output Capacitance			389	506	pF
C_{rss}	Reverse Transfer Capacitance			151	196	pF
R_G	Series Gate Resistance			1.0	2.0	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 15 V, I_D = 25 A		25	32	nC
Q_g	Gate Charge Total (10 V)			53	68	nC
Q_{gd}	Gate Charge Gate to Drain			5.4		nC
Q_{gs}	Gate Charge Gate to Source			8.9		nC
$Q_{g(th)}$	Gate Charge at Vth			4.7		nC
Q_{oss}	Output Charge	V_{DS} = 30 V, V_{GS} = 0 V		12.3		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 10 V, I_{DS} = 25 A, R_G = 0 Ω		5		ns
t_r	Rise Time			16		ns
$t_{d(off)}$	Turn Off Delay Time			23		ns
t_f	Fall Time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 25 A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 15 V, I_F = 25 A, di/dt = 300 A/µs		14.7		nC
t_{rr}	Reverse Recovery Time			14		ns

Figure 2. The electrical characteristics table in the CSD17576Q5B NexFET™ data sheet

Figure 3 is the temperature variation of BV_{DSS} for two power MOSFETs: the CSD17576Q5B 30-V trench FET and the CSD19532Q5B 100-V superjunction device; the curves in Figure 3 show the temperature dependence for BV_{DSS} as well as I_{DSS} and I_{GS}. As the temperature increases, the breakdown voltage for both increases nearly linearly. The slope of the line is the positive temperature coefficient of BV_{DSS} and will differ based on the FET's process technology and voltage rating. Notice that the positive temperature coefficient is less for the CSD19532Q5B than for the CSD17576Q5B.

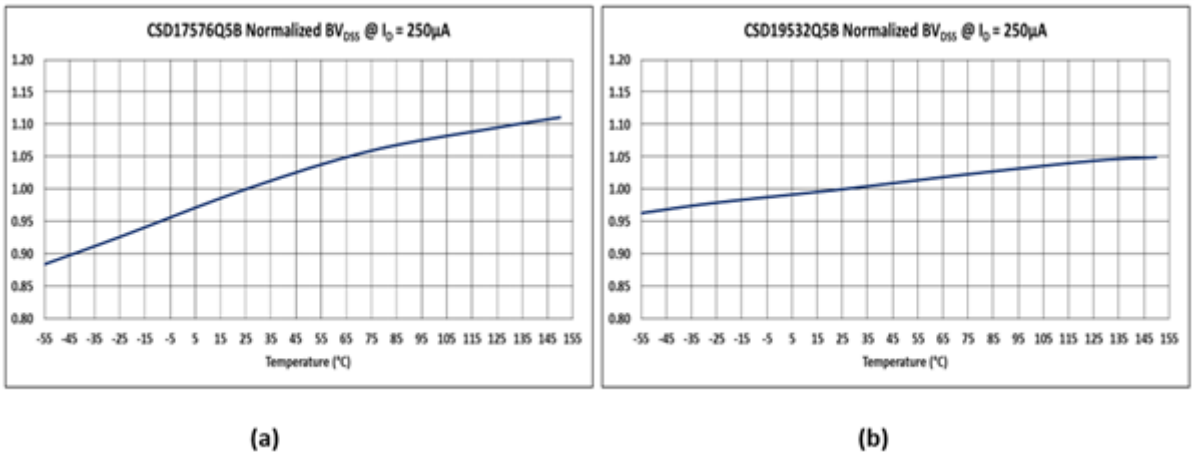


Figure 3. Normalized BV_{DSS} vs. temperature: CSD17576Q5B (a); CSD19532Q5B (b)

Figure 4 shows the temperature dependence of I_{DSS} for the CSD17576Q5B and CSD19532Q5B. The lower-voltage FET, the CSD17576Q5B, displays more variation over the temperature range from -55°C to 150°C. For both devices, the plots tend to flatten out at low temperatures. This is not actual behavior but a test measurement system limitation at the very small currents being measures. The device physics dictate a continual downward trend at low temperatures.

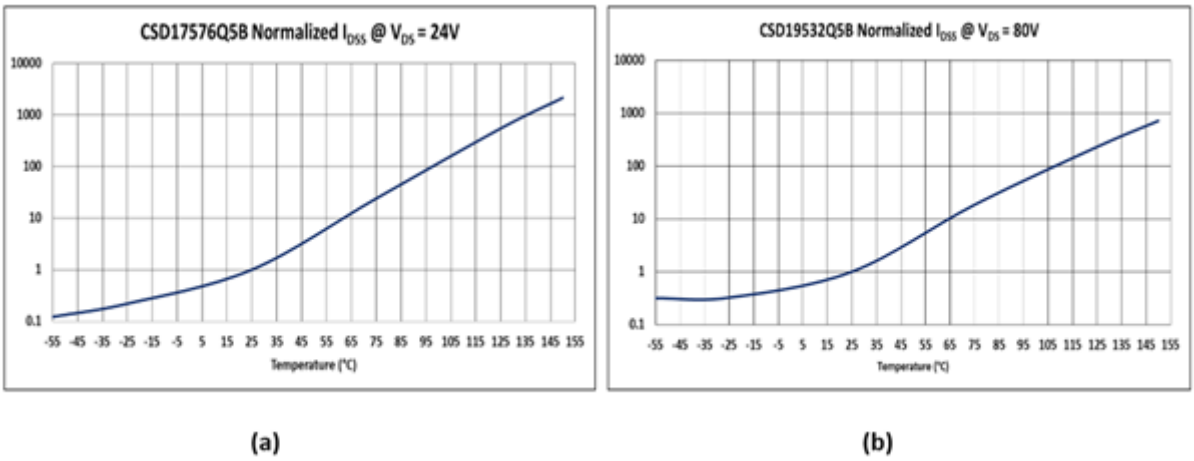


Figure 4. Normalized I_{DSS} vs. temperature: CSD17576Q5B (a); CSD19532Q5B (b)

As shown in Figure 5 for the CD17576Q5B and CSD19532Q5B, I_{GSS} also has a positive temperature variation. The relative increase in I_{GSS} is greater for the CSD19532Q5B over the temperature range from -55°C to 150°C. Again, the flattening of the curves at low temperatures is caused by the resolution of the test measurement system.

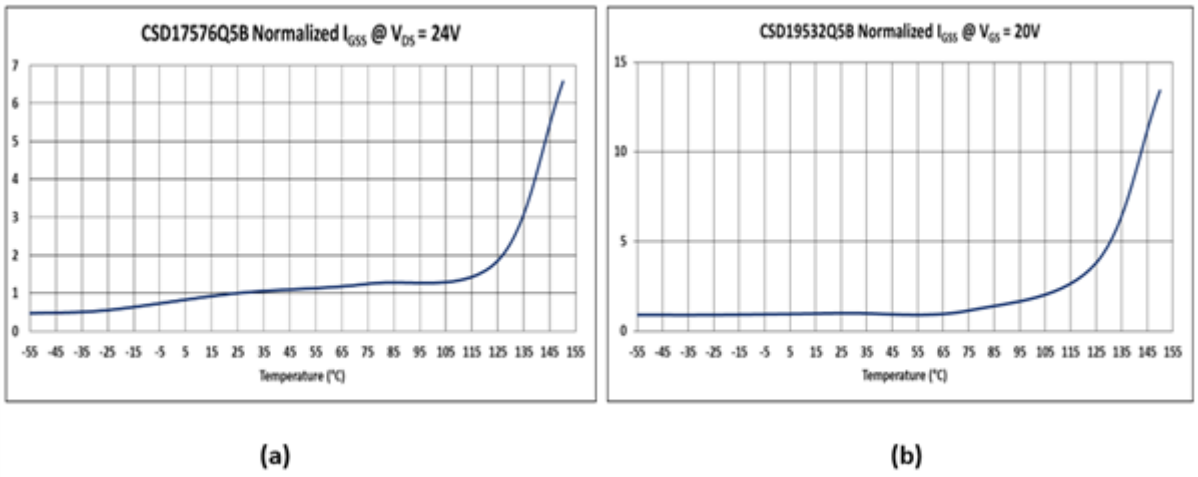


Figure 5. Normalized I_{GSS} vs. temperature: CSD17576Q5B (a); CSD19532Q5B (b)

The last parameter, g_{fs}, is also temperature-dependent. You can use the transfer curves from the CSD17576Q5B and CSD19532Q5B data sheets as shown in Figure 6 to estimate g_{fs} using Equation 1:

$$g_{fs} = \Delta I_{DS}/\Delta V_{GS} \quad (1)$$

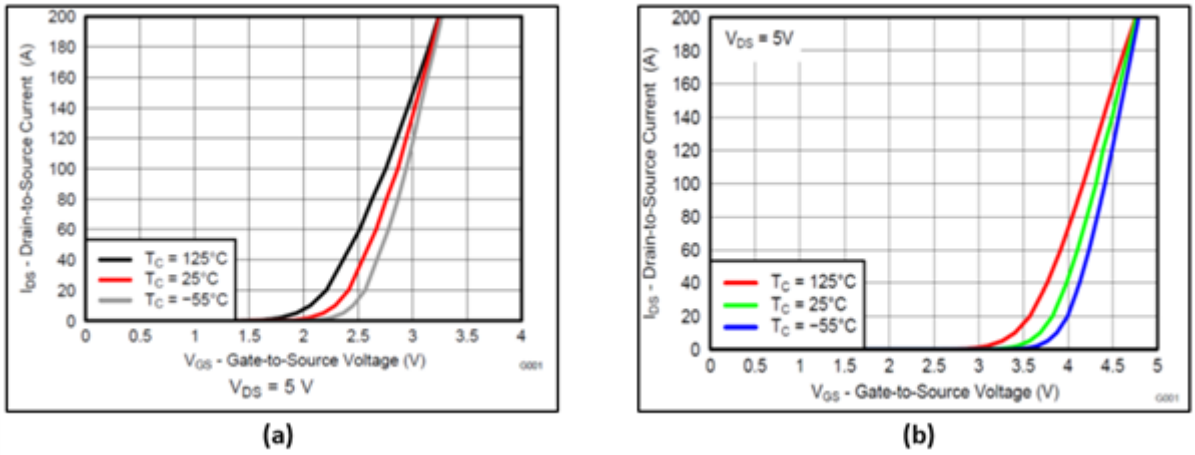


Figure 6. Transfer characteristics: CSD17576Q5B (a); CSD19532Q5B (b)

Picking data points from the data-sheet curves, Table 1 lists the estimated values for g_{fs}. You can see that transconductance has a negative temperature coefficient.

Temperature	-55°C		25°C		125°C	
	V_{GS} (V)	I_{DS} (A)	V_{GS} (V)	I_{DS} (A)	V_{GS} (V)	I_{DS} (A)
	2.6	20	2.4	20	2.2	20
	2.8	60	2.7	60	2.5	60
g_{fs}	186.9		158.1		130.7	
	2.9	80	2.8	80	2.6	80
	2.9	100	2.9	100	2.8	100
g_{fs}	266.7		190.5		158.7	

Table 1: Estimated g_{fs} values for the CSD17576Q5B

You can make the same g_{fs} estimates using the transfer characteristics for the CSD19532Q5B, as listed in Table 2.

Temperature	-55°C		25°C		125°C	
	V_{GS} (V)	I_{DS} (A)	V_{GS} (V)	I_{DS} (A)	V_{GS} (V)	I_{DS} (A)
	4.0	20	3.8	20	3.6	20
	4.1	40	4.0	40	3.8	40
g_{fs}	149.3		127.4		103.1	
	4.3	80	4.2	80	4.0	80
	4.4	100	4.3	100	4.2	100
g_{fs}	227.3		194.2		161.3	

Table 2: Estimated gfs values for the CSD19532Q5B

Dynamic characteristics

Parameters in the dynamic characteristics section are an indication of the MOSFET's switching speed. These include the parasitic capacitances (C_{ISS}, C_{OSS} and C_{RSS}), the internal series gate resistance (R_G) and the charge parameters (Q_G, Q_{GD}, Q_{GS} and Q_{OSS}). These parameters, along with the external gate-drive circuit, determine the typical switching times ($t_{d(on)}$, t_r, $t_{d(off)}$ and t_f). There is minimal temperature variation of the parasitic capacitances and charge parameters. R_G varies with temperature but is typically swamped out by an external gate resistor and the output impedance of the gate driver, resulting in some minor deviation of the switching times specified in the data sheet. Figure 7 shows a MOSFET with the parasitic capacitances and internal series gate resistance.

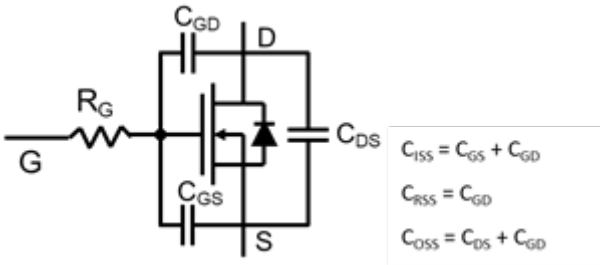


Figure 7. MOSFET model with parasitic elements

Diode characteristics

The last section of the electrical characteristics table is the drain-to-source body-diode specifications. The diode forward voltage (V_{SD}) has a negative temperature characteristic, as shown in typical MOSFET characteristics. Reverse-recovery charge (Q_{rr}) and reverse-recovery time (t_{rr}) both increase at elevated temperatures. Because of this, reverse-recovery losses also increase at elevated temperatures.

Figure 8 shows the reverse-recovery behavior with temperature for two non-TI FETs. Q_{rr} is the area enclosed by the drain current and t_{rr} is the time it takes for the current to return to zero. You can expect similar behavior from TI NexFET devices over temperature.

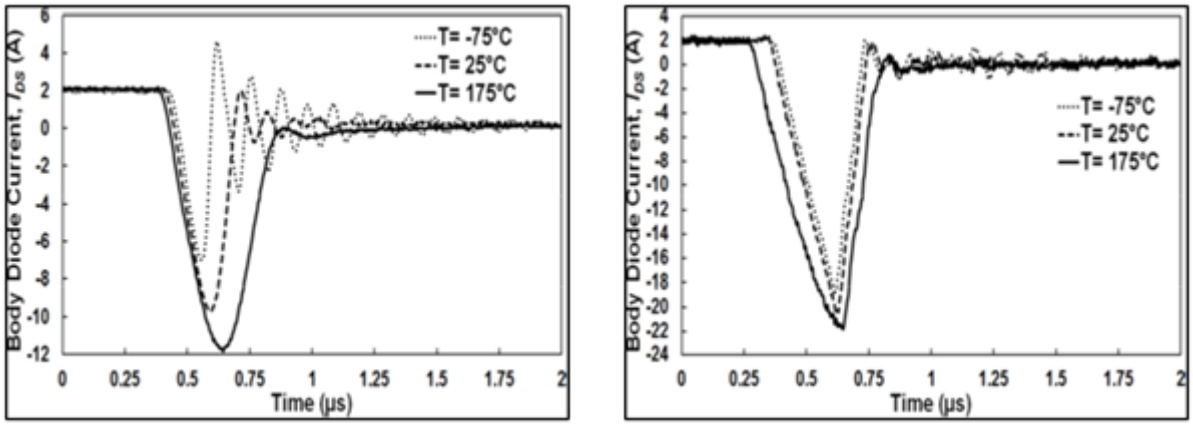


Figure 8. Reverse-recovery current vs. temperature for two FETs

Safe operating area

Engineers often ask me how to derate for temperature from the safe operating area (SOA) curves in a MOSFET data sheet. Figure 9 shows the SOA curves at T_A = 25°C for the CSD17576Q5B and CSD19532Q5B.

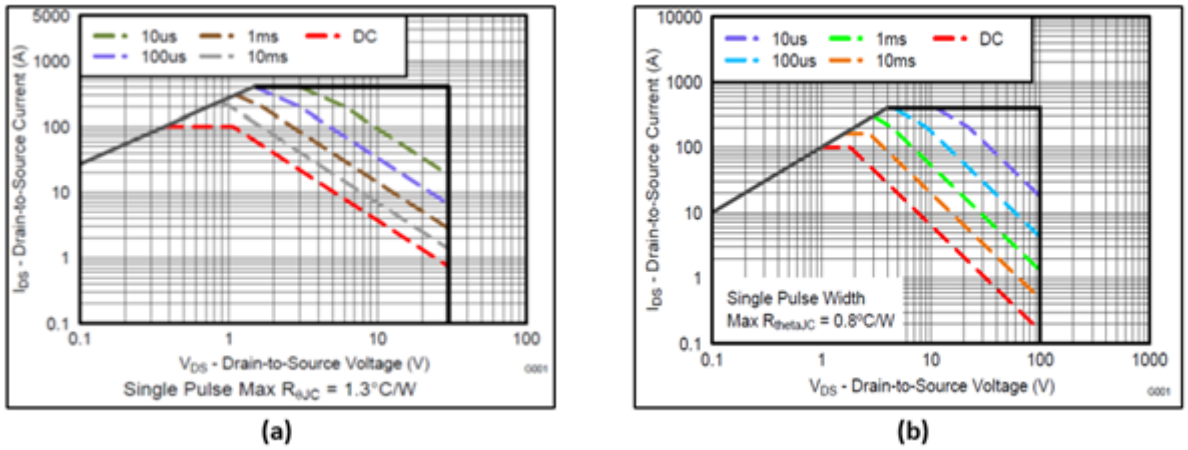


Figure 9. Maximum safe operating area at T_A = 25°C: CSD17576Q5B (a); and CSD19532Q5B (b)

The easiest approach is to use a linear derating factor. From the graph, determine the SOA current, $I_{DS(SOA)}$, at the voltage, $V_{DS(SOA)}$ and the pulse width of interest. Equation 2 calculates the SOA current at temperature T (°C) as:

$$I_{DS(SOA@T)} = I_{DS(SOA)} \times (T_{Jmax} - T)/(T_{Jmax} - 25°C) \quad (2)$$

Equation 2 yields 0 current when T = T_{Jmax}, specified in the data sheet.

Conclusion

In this technical article, I reviewed a TI NexFET data sheet, what's in it and what's not. I explored specifications that have a temperature dependency not included in the data sheet and provided typical curves and data showing how these specifications may vary with temperature. The examples used in this article were for two specific TI NexFET devices and showed the general trends versus temperature.

The typical curves presented in this article are to help you understand how these parameters vary with temperature, but they are no guarantee of actual performance. Always use the data-sheet limits when designing with TI FETs. If you don't see certain specifications in the data sheet, please request them from TI in the E2E forum.

Additional resources

- Check out these technical articles:
- "Understanding MOSFET data sheets, Part 1 – UIS/avalanche ratings."
- "Understanding MOSFET data sheets, Part 5 – Switching Parameters."
  - Visit the TI MOSFET support and training center.
  - Read the white paper, "Novel Thermally Enhanced Power Package."
  - Review the application report, "3D packaging advancements drive performance, power and density in power devices."

Reference

1. Jahdi, Saeed, Olayiwola Alatise, Roozbeh Bonyadi, Petros Alexakis, Craig Fisher, Jose A. Ortiz Gonzalez, Li Ran, and Philip Mawby "An Analysis of the Switching Performance and Robustness of Power MOSFETs Body Diodes: A Technology Evaluation." *IEEE Transactions on Power Electronics* 30, no. 5 (May 2015): pp. 2383-2394.

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