

# Optimizing Flip-chip IC Thermal Performance in Automotive Designs



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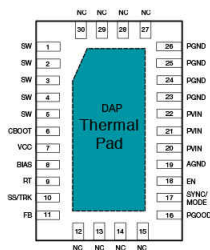
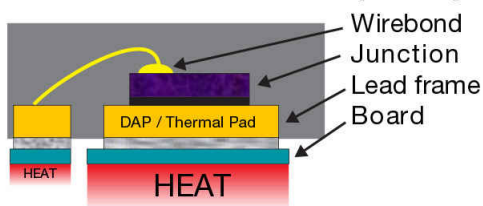
Significant decreases in the size of power integrated circuits (ICs) have enabled system designers to achieve reductions in power-supply solution size and cost, which is imperative to furthering the development of advanced systems in the automotive industry. However, one challenge that arises from this trend is impaired thermal performance. Without a thoughtful printed circuit board layout to spread the heat, using smaller ICs in a design might result in a significant temperature rise, which is especially concerning for automotive applications.

One common small-size package is a flip-chip IC. Flip-chip packages have enabled ICs to become even smaller, making them a preferred choice for engineers designing tiny power-supply solutions. This size reduction has further impacted thermal performance, however, and made thermal mitigation even more challenging. In this article, I'll review the considerations and guidelines for achieving optimal thermal performance with small flip-chip ICs.

## The difference between standard wire-bond QFN and flip-chip packages

A typical package like a wire-bond quad flat no-lead (QFN) has a junction/die that typically connects to a thermal pad for heat dissipation, as shown in Figure 1. The junction has bond wires to connect the junction to the pins. The bond wires are very thin and do not conduct heat very well, resulting in most of the heat escaping from the thermal pad.

### Standard wirebond QFN package

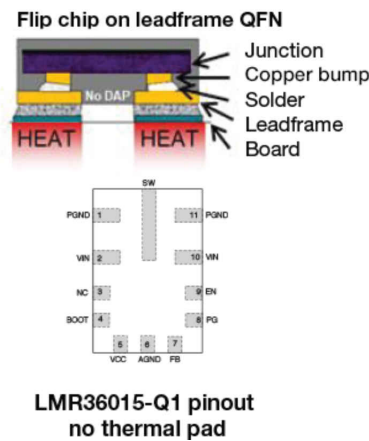


LM73606-Q1 Pinout  
Showing thermal pad

Figure 1. Junction connections to pins and thermal pad in a standard wire-bond QFN package

Flip-chip technology flips the chip/junction so that the copper bumps are upside down and soldered directly to the lead frame, as shown in Figure 2. This results in reduced parasitic impedances from the pin to the junction,

improving efficiency, size, switch ringing and overall performance for a given specification. The flipped chip, however, prohibits the die from connecting directly to a thermal pad – there is no thermal pad on typical flip-chip devices. Fortunately, the elimination of the bond wires facilitates paths of high thermal conductivity from the die, through the pins and into the board. This results in good thermal conduction between the die and the board, thus removing heat from the IC.



**Figure 2. Junction connections to pins for flip-chip devices**

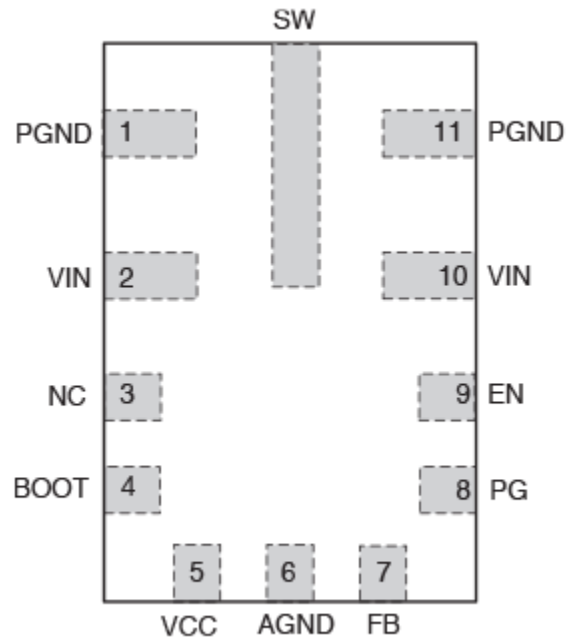
### Using pins to optimize heat distribution

Power-supply designers can achieve very good thermal performance with flip-chip ICs by connecting and using flip-chip pins for heat distribution. Connecting the pins to large copper traces and polygon pours reduces the thermal resistance and pulls more heat out of the package.

The power ground (PGND) pin is often used to extract heat from the IC. PGND also requires higher current capability; therefore, the copper bump connecting the junction to the PGND pin is typically larger than the copper bump of a signal pin. This larger copper bump allows more heat to flow from the PGND pin(s). On the system side, PGND is electrically quiet, so a large copper surface area will not impact electromagnetic interference (EMI) levels – an important requirement in automotive systems.

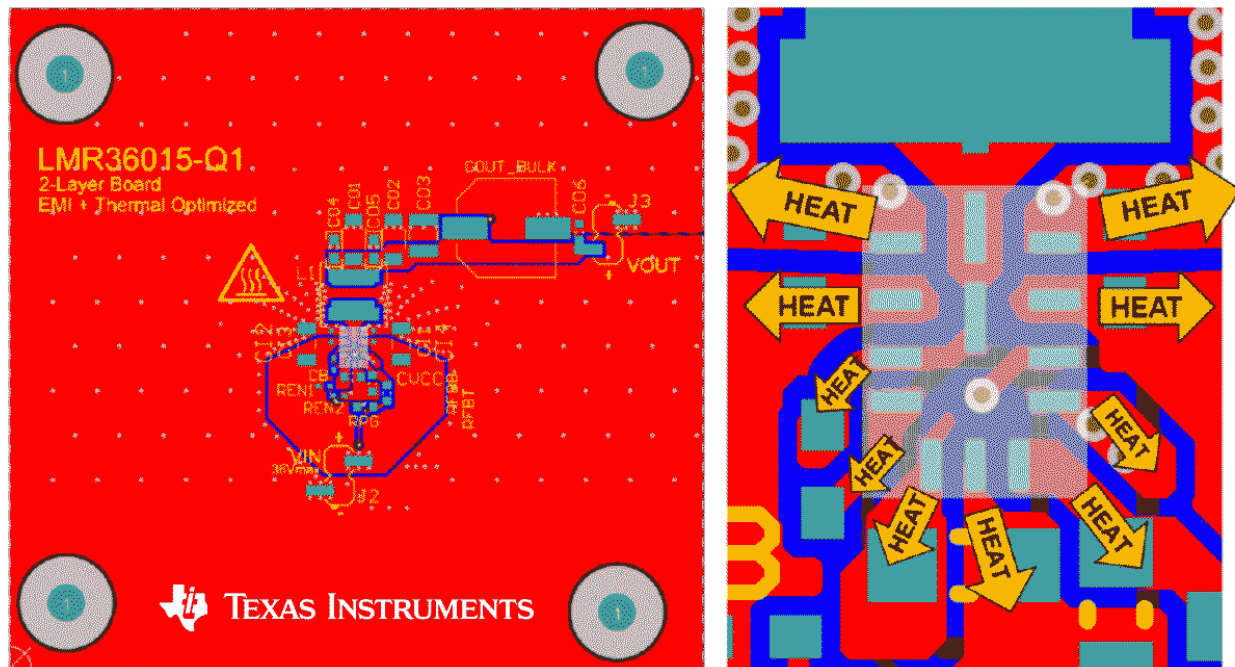
You can use other pins for improved thermal performance, but take care not to increase the surface area of noisy nodes such as the switch node and the bootstrap pin, as this can impact EMI performance and may cause violations of EMI test limits.

Let's test these strategies using the [LMR36015-Q1](#), a 150°C-rated, 60-V<sub>IN</sub>, 1.5-A<sub>OUT</sub> flip-chip buck converter. [Figure 3](#) shows the pinout of the [LMR36015-Q1](#).



**Figure 3. Pinout for the LMR36015-Q1**

Figure 4 shows a thermally optimized layout of the LMR36015-Q1. Pins 1 and 11 are PGND pins connecting to a large ground plane, which provides good heat distribution. The layout also uses thermal vias on the ground plane, harnessing the inner layers for even more heat distribution. Pin 6 is analog ground, which also has a large ground plane and thermal vias. Pins 2 and 10 are the input voltage ( $V_{IN}$ ) pins, which like the PGND pins have large internal copper bumps for increased current capacity and improved thermal conductivity for better heat dissipation. The input voltage on a buck is inherently noisy, however, so watch the size of the  $V_{IN}$  plane in order to not push EMI levels past acceptable limits. The switch node and bootstrap pin are noisy due to fast changes in voltage, so it is important to keep those nodes as small as possible.



Full board - top layer

Zoomed further showing heat flow

**Figure 4. Sample layout for the LMR36015-Q1 flip-chip IC**

The [LMR36015-Q1](#) board measures 2.2 by 2.3 inches (5.6 cm by 5.8 cm) and only has two layers: top and bottom. Typical boards are larger and contain four or more layers, so the size and number of layers increases the thermal challenge. The thermally optimized layout allows the [LMR36015-Q1](#) to operate at 12  $V_{IN}$ , 5  $V_{OUT}$  at a full load of 1.5  $A_{OUT}$ , switching at 400 kHz with a temperature rise of only 28°C in a 22°C still-air environment. This layout allows the 150°C-rated IC to operate in ambient temperatures as high as 115°C, which gives 10°C of margin above the 105°C ambient requirement, which is used in some of the harshest automotive environments.

Smaller-power ICs in flip-chip packages do not necessarily result in poor thermal performance. When compared to wire-bond packages, it is possible to achieve equivalent thermal performance by following the guidance presented in this article.

#### Additional resources

- Deep dive into a video about [LMR36015-Q1 on a 2-layer board thermals](#).
- Learn about [EMI considerations on a 2-layer board](#).
- Check out the [flip-chip vs QFN performance comparison](#).

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