Technical Article

LDO Basics: Dropout

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The quintessential characteristic of a low-dropout (LDO) linear voltage regulator has to be dropout. After all, that is the source of its name and acronym.

At the most basic level, dropout describes the minimum delta between V_{IN} and V_{OUT} required for proper regulation. However, it quickly becomes more nuanced when you incorporate variables. Dropout, as you'll see, is essential to obtaining efficient operation and generating voltage rails with limited headroom.

What Is Dropout?

Dropout voltage, V_{DO}, refers to the minimum voltage differential that the input voltage, V_{IN}, must maintain above the desired output voltage, $V_{OUT(nom)}$, for proper regulation. See Equation 1:

$$V_{IN} \geq V_{OUT(nom)} + V_{DO} \tag{1}$$

Should V_{IN} fall below this value, the linear regulator will enter dropout operation and no longer regulate the desired output voltage. In this case, the output voltage, $V_{OUT(dropout)}$, will track V_{IN} minus the dropout voltage (Equation 2):

$$V_{OUT(dropout)} = V_{IN} - V_{DO} \tag{2}$$

As an example, consider an LDO like the TPS799 regulating 3.3V. When sourcing 200mA, the TPS799's maximum dropout voltage is specified at 175mV. As long as the input voltage is 3.475V or greater, regulation is not affected. However, dropping the input voltage to 3.375V will cause the LDO to enter dropout operation and cease regulation, as shown in Figure 1.

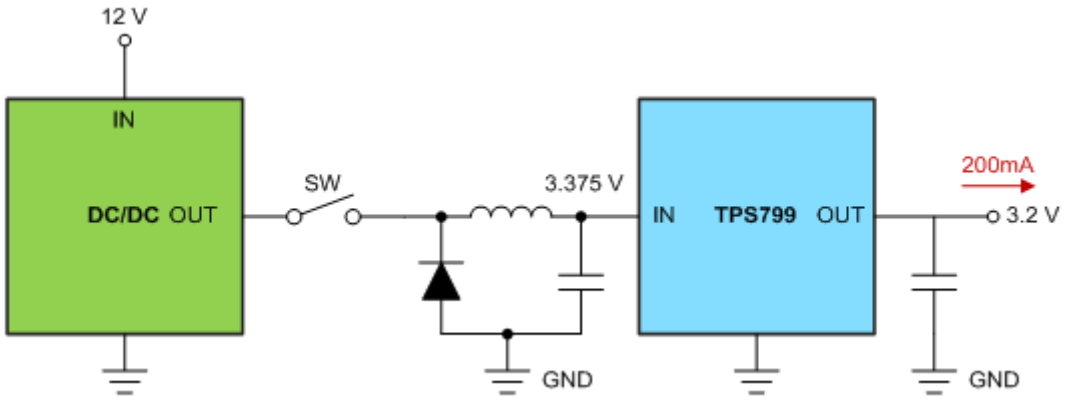

Figure 1. The TPS799 Operating in Dropout

Although it's supposed to regulate 3.3V, the TPS799 does not have the headroom required to maintain regulation. As a result, the output voltage begins to track the input voltage.

What Determines Dropout?

The architecture of the LDO primarily determines dropout. To see why, let's look at PMOS and NMOS LDOs and compare their operation.

PMOS LDO

Figure 2 shows a PMOS LDO architecture. In order to regulate the desired output voltage, the feedback loop controls the drain-to-source resistance, or R_{DS}. As V_{IN} approaches $V_{OUT(nom)}$, the error amplifier will drive the gate-to-source voltage, or V_{GS}, more negative in order to lower R_{DS} and maintain regulation.

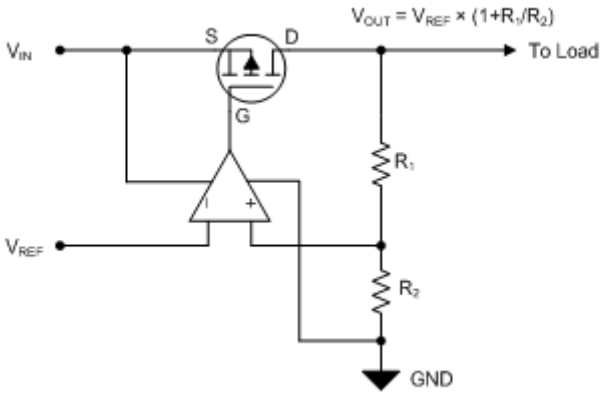

Figure 2. A PMOS LDO

At a certain point, however, the error-amplifier output will saturate at ground and cannot drive V_{GS} more negative. R_{DS} has reached its minimum value. Multiplying this R_{DS} value against the output current, or I_{OUT}, will yield the dropout voltage.

Bear in mind that the more negative the value of V_{GS}, the lower R_{DS} achieved. By increasing the input voltage, you can achieve a more negative V_{GS}. Therefore, PMOS architectures will have lower dropout at higher output voltages. Figure 3 illustrates this behavior.

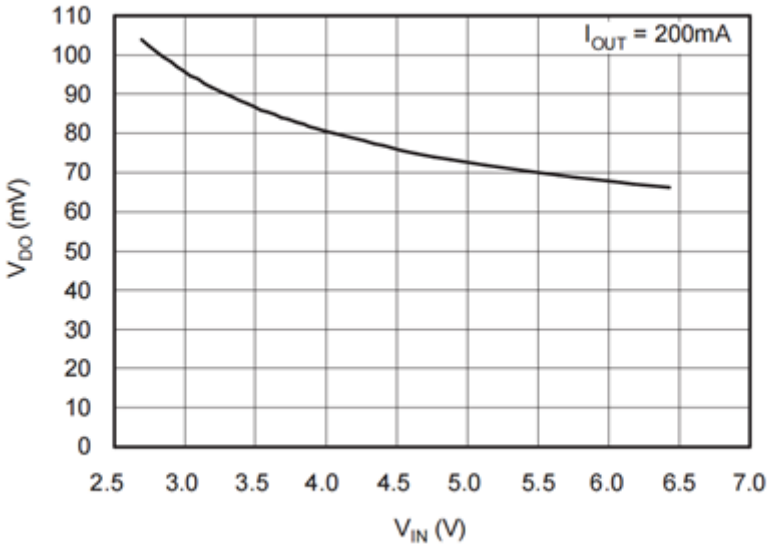

Figure 3. Dropout Voltage vs. Input Voltage for the TPS799

As shown in Figure 3, the TPS799 has a lower dropout voltage as the input voltage (and output voltage, for that matter) increases. That is because a higher input voltage yields a more negative V_{GS}.

Nmos Ldo

In the case of an NMOS architecture, as shown in Figure 4, the feedback loop still controls R_{DS}. As V_{IN} approaches $V_{OUT(nom)}$, however, the error amplifier will **increase** V_{GS} in order to lower the R_{DS} and maintain regulation.

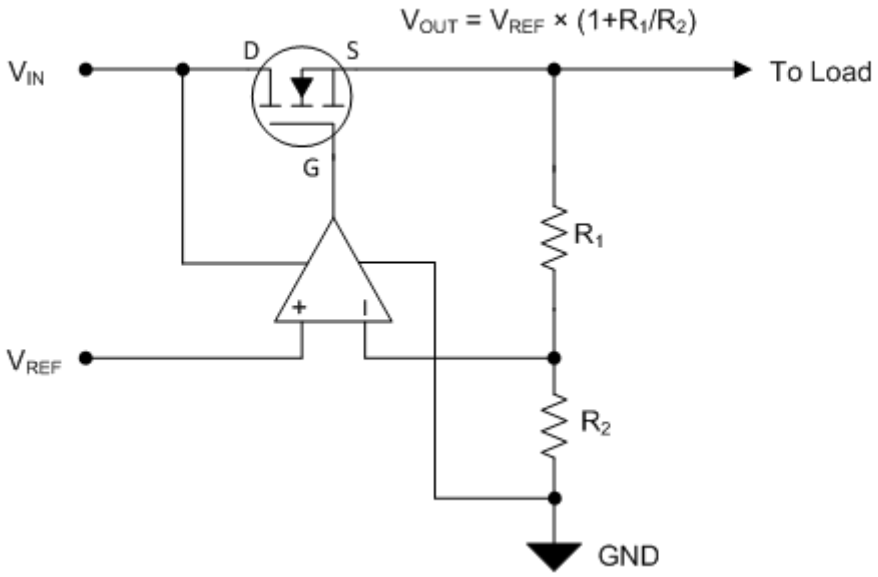

Figure 4. An Nmos Ldo

At a certain point, V_{GS} cannot increase any more, since the error-amplifier output will saturate at the supply voltage, or V_{IN}. When this condition is met, R_{DS} is at its minimum value. Multiplying this value against the output current, or I_{OUT}, derives the dropout voltage.

This presents a problem though, because as V_{IN} approaches $V_{OUT(nom)}$, V_{GS} will also decrease, since the error-amplifier output saturates at V_{IN}. This prevents ultra-low dropout.

Biasing the LDO

Many NMOS LDOs employ an auxiliary rail known as a bias voltage, or $V_{BIAS,}$ as shown in Figure 5.

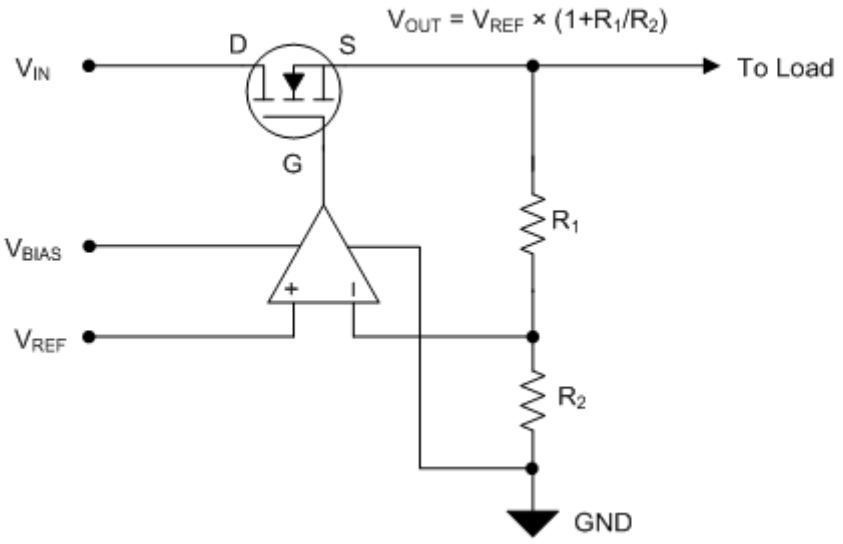

Figure 5. An NMOS LDO with a Bias Rail

This rail serves as the positive supply rail for the error amplifier and allows its output to swing all the way up to V_{BIAS}, which is higher than V_{IN}. This type of configuration enables the LDO to maintain a high V_{GS}, and therefore achieve ultra-low dropout at low output voltages.

Sometimes an auxiliary rail is not available but low dropout at a low output voltage is still desired. In such a situation, an internal charge pump can be substituted in place of V_{BIAS}, as shown in Figure 6.

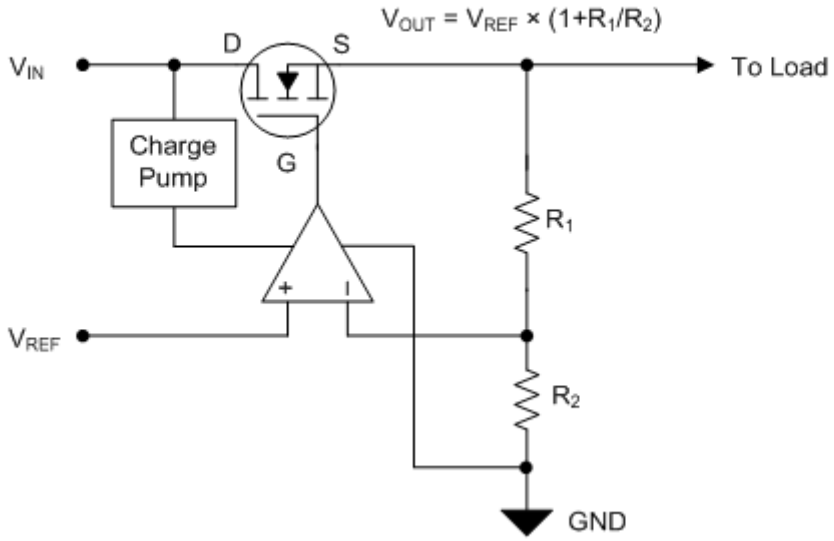

Figure 6. An NMOS LDO with an Internal Charge Pump

The charge pump will boost V_{IN} so that the error amplifier may generate a larger V_{GS} value despite the lack of an external V_{BIAS} rail.

Other Variables

In addition to architecture, dropout is also affected by a few other variables, as outlined in Table 1.

Table 1. Variables Affecting Dropout

Variable	Impact on dropout
PMOS LDO	↓V_{DO} when ↑V_{OUT}
NMOS LDO with bias	↓V_{DO} when ↓V_{OUT}
Pass element size	↓V_{DO} when ↑pass element size
Output current	↑V_{DO} when ↑I_{OUT}
Temperature	↑V_{DO} when ↑T_J
Output accuracy	↑V_{DO} when ↑tolerance

It's clear that dropout is not a static value. Rather than just complicating your LDO choice, though, these variables should help you choose the optimal LDO for your specific set of conditions. Learn more about LDO dropout in the application note, Understanding LDO Dropout.

Additional resources:

- Read more LDO blogs.

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