Level Shifting WL18xx/WL18xxMOD/WL18xxQ I/Os

1 Purpose

The purpose of this document is to provide guidelines for proper I/O-level conversion during integration of WL18xx I/Os to a host that supports I/Os with voltages greater than 1.8 V.

2 Power-up Sequence

The most crucial point during integration of the WL18xx device is following proper power-up and power-down sequences to avoid damage to the device.

2.1 WL18xx States

While either VBAT or VIO or both are deasserted, no signals at a logic high level should be driven to the device. (The only exception is the slow clock which is a fail-safe I/O.)

While VBAT, VIO, and slow clock are fed to the device but BT_EN or WL_EN are deasserted (low), the device is in shutdown state (Table 1 describes the state of the I/O). In shutdown state, all functional blocks, internal DC2DCs, clocks, and LDOs are disabled.

2.2 Power Up

To power up, do the following:

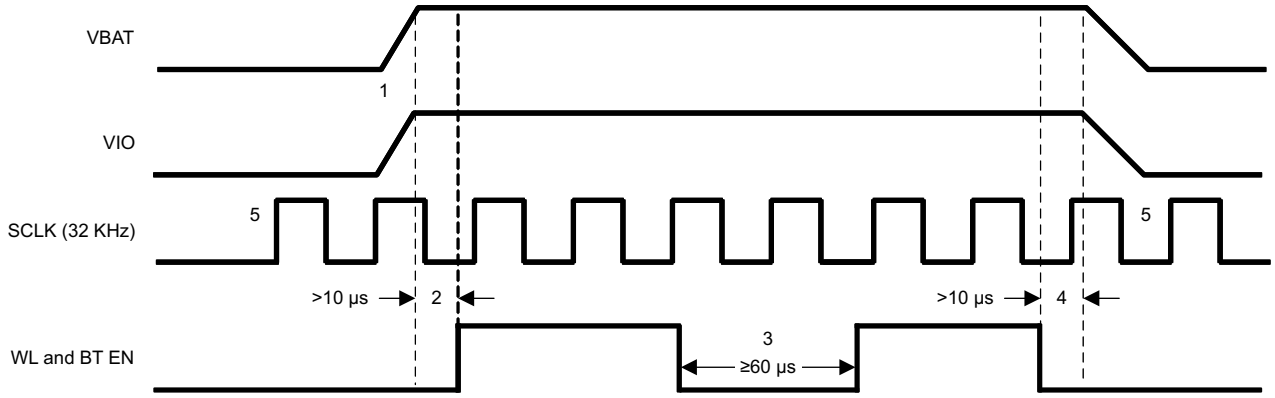
1. Ensure slow clock, VIO, and VBAT are stable.
2. Assert BT_EN or WL_EN high.

Internal DC2DCs, LDOs, and clocks start to ramp and stabilize.

2.3 Shutdown

To shutdown, do the following:

1. Ensure the supplies to the device (VBAT, VIO, and slow clock) are stable and available.
2. Deassert BT_EN or WL_EN low.
3. Deassert the supplies to the chip (VBAT and VIO). (See Figure 1.)



NOTE:

1. On system level, either VBAT and VIO can come up first.
2. VBAT supplies, VIO supplies, and slow clock (SCLK) must be stable before EN is asserted and at all times when EN is active.
3. Keep a 60-µs delay between two consecutive device enables. The device is assumed to be in a shutdown state during that period; all enables to the device are low for that minimum duration.
4. Deassert the enable line at least 10 µs before the VBAT or VIO can be lowered. (The order in which supplies are turned off after EN shutdown is immaterial.)
5. The SCLK I/O cell is a fail safe; the clock can be supplied before the VBAT and VIO supplies.

Figure 1. Power-up and Shutdown Sequences

3 Sense on Reset Configuration Pins

WiLink™ 8 has several wake-up options that are entered through sense on reset by three I/Os of the device (IRQ_WL, UART_DBG_BT, AUD_OUT_BT).

When a Bluetooth® or WLAN enable bit is set to high, the device checks the state of the lines and wakeup in a specific mode.

To avoid putting the device in an undefined state, be careful when level-shifting the three I/Os to ensure you apply only one of the two supported configurations of the device are applied.

The supported modes are as follows:

- Operational mode:
  - IRQ_WL = 0
  - UART_DBG_BT = 1
  - AUD_OUT_BT = 0

  Set operational mode by default using internal pull of WL18xx (90K typical).
- Debug mode:
  - IRQ_WL = 1
  - UART_DBG_BT = 1
  - AUD_OUT_BT = 0

  The WLAN RS232 debug interface and Jtag interface are muxed out to the WL18XX I/Os.
  To activate the debug mode a 10-k resistor pullup on the WLAN_IRQ line is required, leave the 10-k resistor pullup as a place holder (N.C.) and apply the it only if debug mode is required.

See Table 1 for the I/O states.

Table 1. I/O States

GPIO NAME	Line Debug Function	PULL UP/PULL DOWN
GPIO5	JTAG_TCK	Down
GPIO6	JTAG_TMS	Up
GPIO7	JTAG_TDI	Up
GPIO8	JTAG_TDO	Up
GPIO2	WL_RS232_RX	Up
GPIO1 (1)	WL_RS232_TX	Up

(1) GPIO1 is used on WL8 devices. GPS_EXT_LNA_EN is used on WL8Q devices.

4 18xx Interfaces

NOTE: In all cases of level shifters, apply the following guidelines:

- Control the OE or the direction signals from the host GPIO or tied to the always on signal that avoids going low which can cause the level shifter to turn off or change direction.
- TI recommends level shifters that Hi-Z the outputs when one of the supply voltages is applied unlike the examples.
- Terminate the unused inputs of the level shifter to GND or VCC.
- Use level shifters with similar performance levels.

4.1 SDIO Lines (CLK, CMD, Four Data Lines)

TI recommends connecting the SDIO lines directly to the host processor 1.8-V I/O bank because this interface is timing critical, and adding a level shifter can impact the performance. WL_IRQ is a less timing-critical signal and a separate level shifter can be used.

If level-shifting is unavoidable, connect using a bidirectional level shifter that has incorporated pullups and/or add an onboard 10-kΩ resistor on both sides of the level shifter:

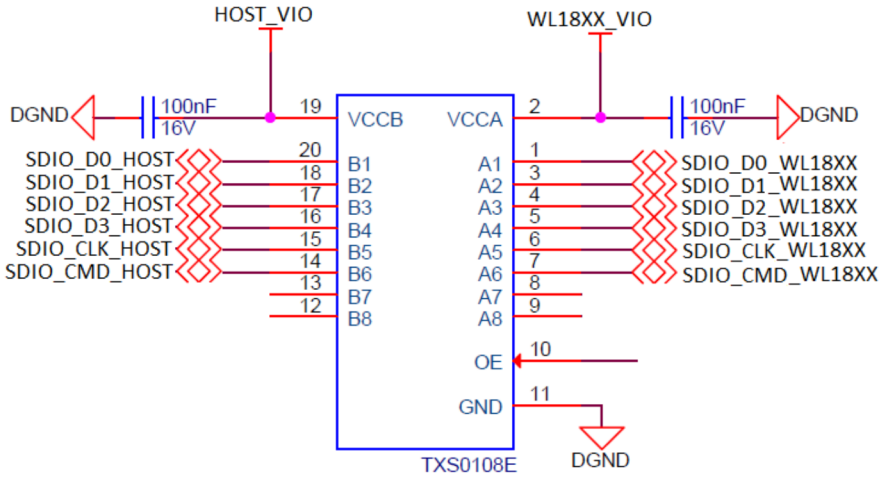


Figure 2. SDIO Lines

4.2 *WLAN and Bluetooth* Enable Signals

The lines have an internal pulldown of 200 kΩ. To comply with the WL18xx wake-up sequence, ensure that the lines are pulled down while the supplies are unstable.

If the enables are connected directly to the host 1.8-V bank or to the level shifter, ensure that there are no internal host or level-shifter pullups that can overtake the WL18xx pulldown.

TI recommends level-shifting using a resistor divider or a spare GPIO of existing level shifters for the WL18xx I/Os.

NOTE: In the resistor divider variant, an additional current of 180 µA adds to the device sleep current.

Figure 3 shows an example of 3.3-V to 1.8-V translation.

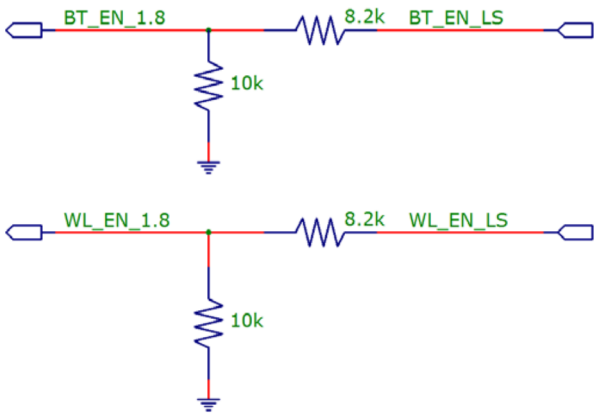


Figure 3. Enable Lines

4.3 *Bluetooth* HCI Lines

There are two input and two output lines in the interface. TI recommends using the SN74AVC4T245 device as the level shifter.

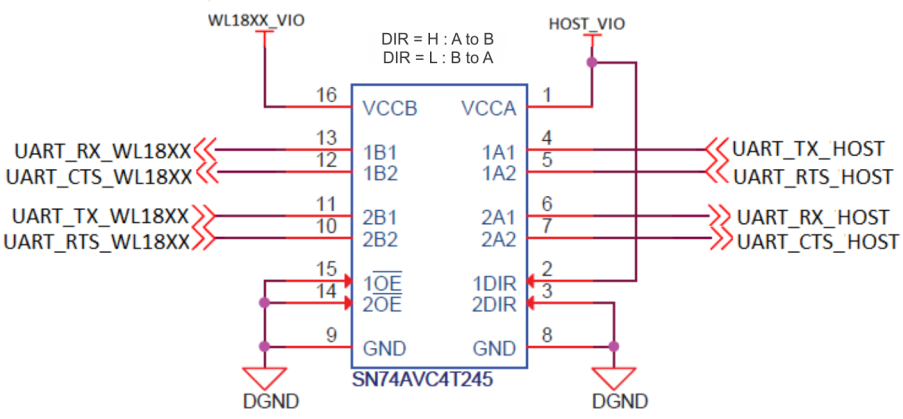


Figure 4. HCI Lines

4.4 Bluetooth PCM lines

AUD_OUT (output) and AUD_IN (input) can be bidirectional; CLK or FSYNC can support master and slave configurations.

If level-shifting is required, using one dedicated level shifter for the PCM is unavoidable. The AUD_IN line can be shared with other level shifters in the design or level shifted by using a resistor-divider configuration, which is the same configuration as the enable lines.

Usually, the PCM master or slave is a constant configuration and level shifter with onboard or controlled from the host level shifter direction line can be used.

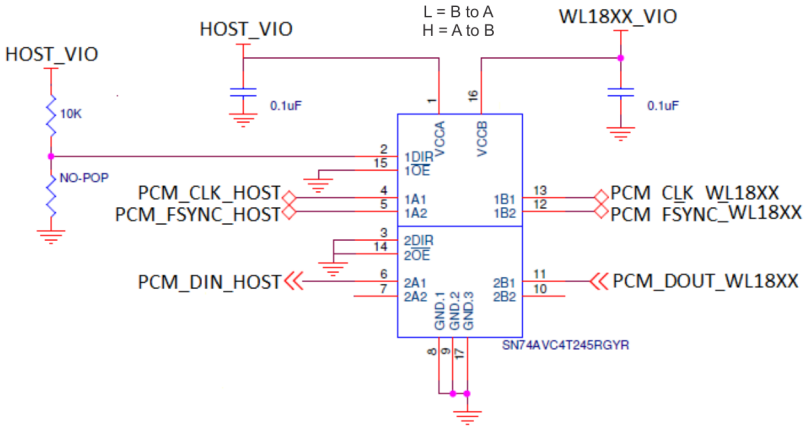


Figure 5. PCM Lines

4.5 GNSS Lines

4.5.1 EXT_LNA_EN

This line is directly connected to an external LNA, as shown in Figure 6. Depending upon the specification of the V_{IH} of the external LNA, a level shifter may be unnecessary in most cases.

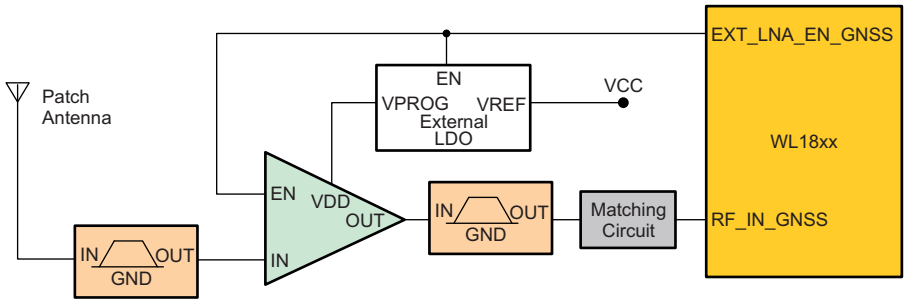


Figure 6. External LNA Powered Using External LDO (Recommended)

4.5.2 GNSS_IRQ and TIMESTAMP_GNSS

Figure 7 shows the circuit for level shifting.

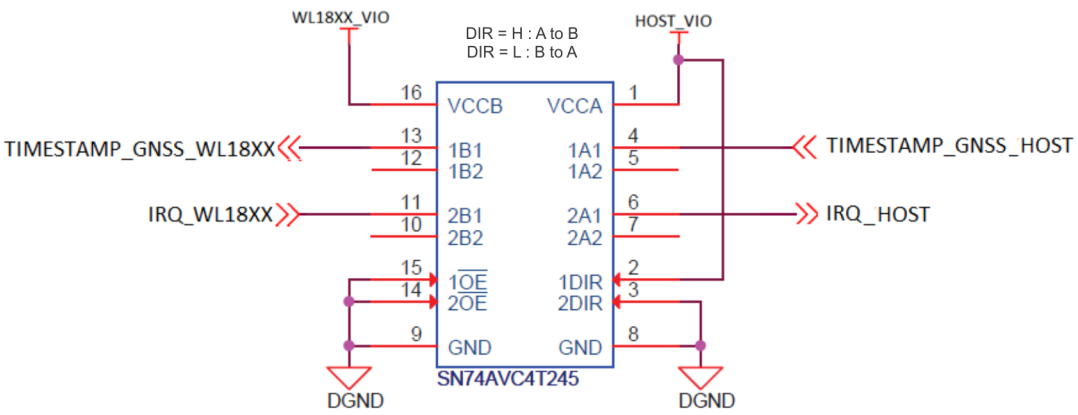


Figure 7. GNSS_IRQ and TIMESTAMP_GNSS

4.5.3 GNSS_I2C Lines

The level-shifting for the I^2C lines require a special IC and TI part PCA9306. See http://www.ti.com/product/pca9306.

Figure 8 shows a typical application of this IC.

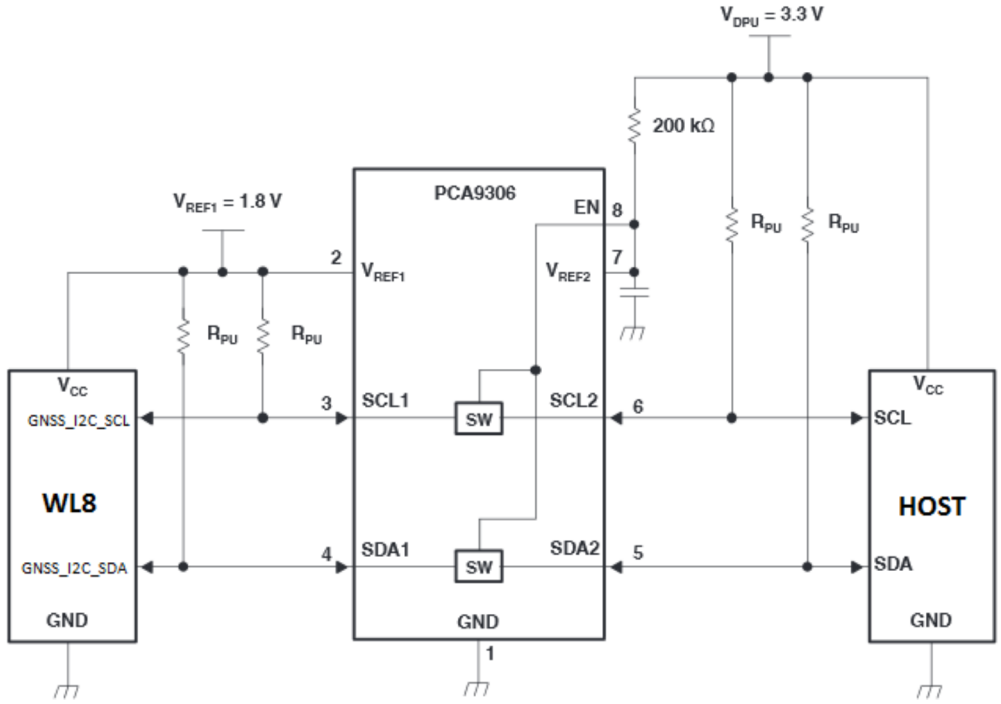


Figure 8. GNSS I^2C Application Circuit

The value of the pullup resistors are dependent upon the V_{DPU} (host I/O voltage). Table 2 helps to select this resistor.

Table 2. Pullup Resistor Values (Ω)

V_{DPU}	15 mA		10 mA		3 mA	
	Nominal	+10%	Nominal	+10%	Nominal	+10%
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532

The current that passes through the transistor is specified in Table 2 as 15 mA, 10 mA, and 3 mA. Select the appropriate value based on the sink capability of the host processor. A value of 3 mA is adequate for most applications if there are 3 to 5 slave devices on the host bus. Both the total capacitance on the bus and the speed of the I^2C bus must determine this value.

Revision History

Changes from February 1, 2014 to January 20, 2015 **Page**

- Updated content of text note 2
- Updated content and supported modes 3
- Updated content and supported modes 3

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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