EVM User's Guide: LP-EM-CC35X1

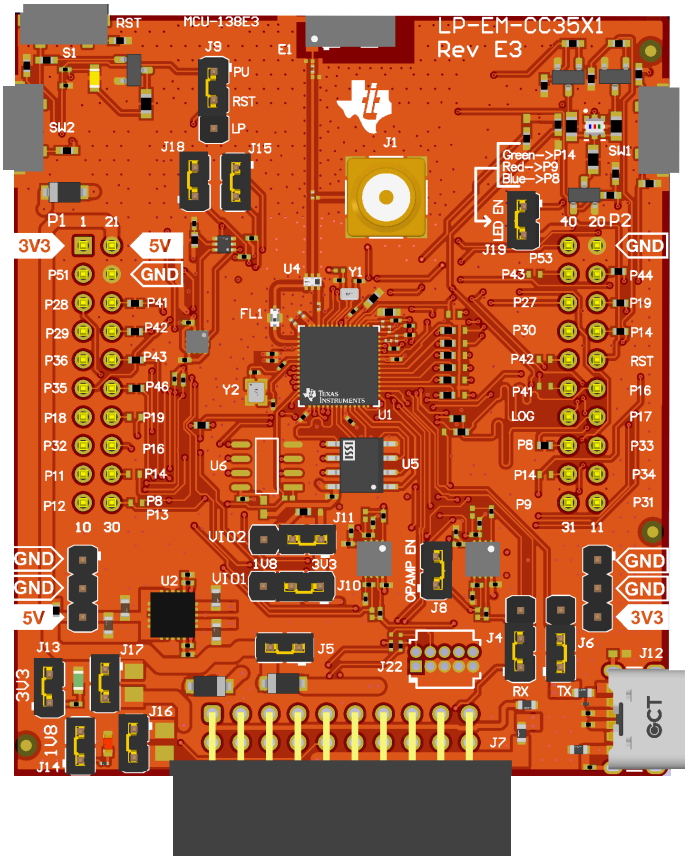
CC35xxE LaunchPad™ Development Kit for SimpleLink™ Wi-Fi 6 and Bluetooth® Low Energy Wireless MCU

Description

The SimpleLink™ CC3501E and CC3551E Wi-Fi 6 and Bluetooth® low-energy wireless MCUs enable affordable, reliable, and secure connectivity integrated with a powerful Arm® Cortex®-M33 application processor. The CC35xxE LaunchPad™ development kit (LP-EM-CC35X1) is a test and development board that features onboard sensors, buttons, and easy interface options to emulators for a full out-of-the-box experience and rapid development. **Note:** This user's guide is relevant for LP-EM-CC35X1 hardware revision E3.

Features

- CC3551E SimpleLink Wi-Fi 6 and Bluetooth low energy, Internet-on-a chip™ design with integrated MCU
- 2×20 pin stackable connectors (BoosterPack™ headers) to connect to TI LaunchPads and other BoosterPack plug-in modules
- 20-pin header for XDS110-based JTAG emulation with serial port for flash programming
- Onboard chip antenna with SMA/U.FL connector for conducted testing
- Easy access to all I/O signals with the BoosterPack plug-in module connectors
- Jumpers for current measurement on both power supplies (3.3V and 1.8V)
- Two buttons and RGB LED for user interaction
- Onboard accelerometer and temperature sensor
- USB Type-C® connector for power



1 Evaluation Module Overview

1.1 Introduction

Created for the Internet of Things (IoT), the SimpleLink Wi-Fi 6 and Bluetooth Low Energy CC3501E and CC3551E devices are single-chip microcontrollers (MCU) with built-in Wi-Fi® connectivity for the LaunchPad ecosystem, which integrates a high-performance Arm Cortex -M33 MCU and lets customers develop an entire application with one device.

No prior Wi-Fi experience is required for fast development with the CC35xxE devices to quickly enable Wi-Fi and Bluetooth Low Energy using its high-performance CP and robust security features. The CC35xxE LaunchPad kit, referred to by the part number, LP-EM-CC35X1, is a low-cost evaluation platform for Arm Cortex -M33-based MCUs. The LaunchPad design highlights the CC35xxE Internet-on-a chip design and Wi-Fi capabilities. By default the CC3551ENJARSHR is populated on the LP-EM-CC35X1, however, the board and accompanying software are designed to support the CC3500E, CC3501E, CC3550E, and CC3551E.

The CC35xxE LaunchPad also features temperature and accelerometer sensors, programmable user buttons, RGB LED for custom applications, and easy connection to emulation boards for debugging. The stackable headers of the CC35xxE LaunchPad interface demonstrate the ease to expand the functionality of the LaunchPad when interfacing with other peripherals on many existing BoosterPack add-on boards, such as graphical displays, audio codecs, antenna selection, environmental sensing, and more.

This evaluation module is specifically designed for development with the Eclipse-based Code Composer Studio™ (CCS) from Texas Instruments. More information about the LaunchPad, the supported BoosterPack modules, and the available resources can be found at the LaunchPad portal from TI. Also, visit the CC35xxE product page for design resources and example projects.

1.2 Kit Contents

- LP-EM-CC35X1—LaunchPad development tool
- USB type-C cable
- Quick Start Guide

1.3 Specification

The LP-EM-CC35X1 is a board designed to enable rapid and easy software and hardware development for the CC35xxE device. The block diagram for the LP-EM-CC35X1 is shown in Figure 1-1.

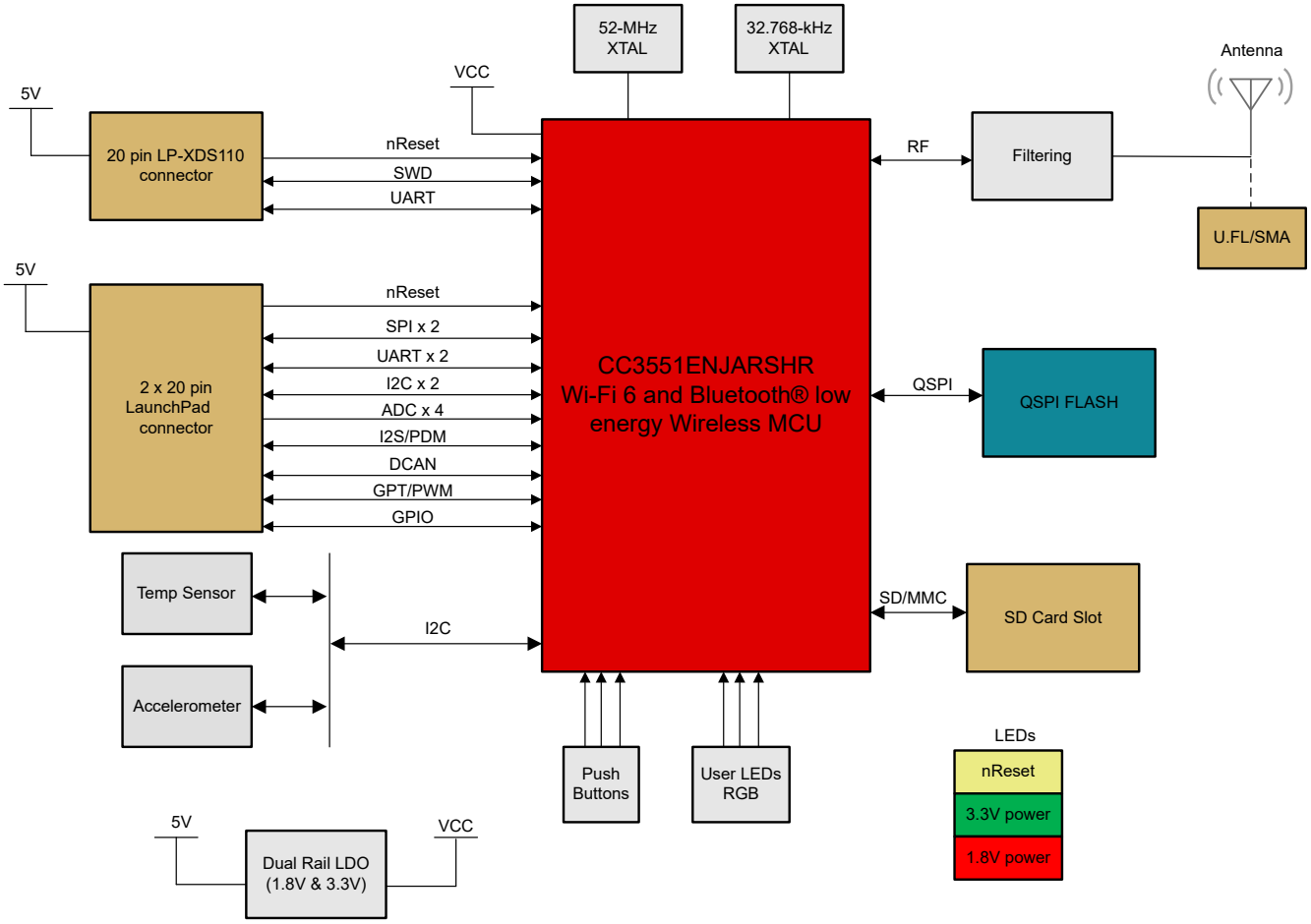


Figure 1-1. LP-EM-CC35X1 Block Diagram

1.4 Device Information

The purpose of the LP-EM-CC35X1 is to showcase the hardware and software capabilities of the CC35xxE device. The other components on the board are populated for testing and support of this main device.

2 Hardware

The overview of the LP-EM-CC35X1 is shown in Figure 2-1.

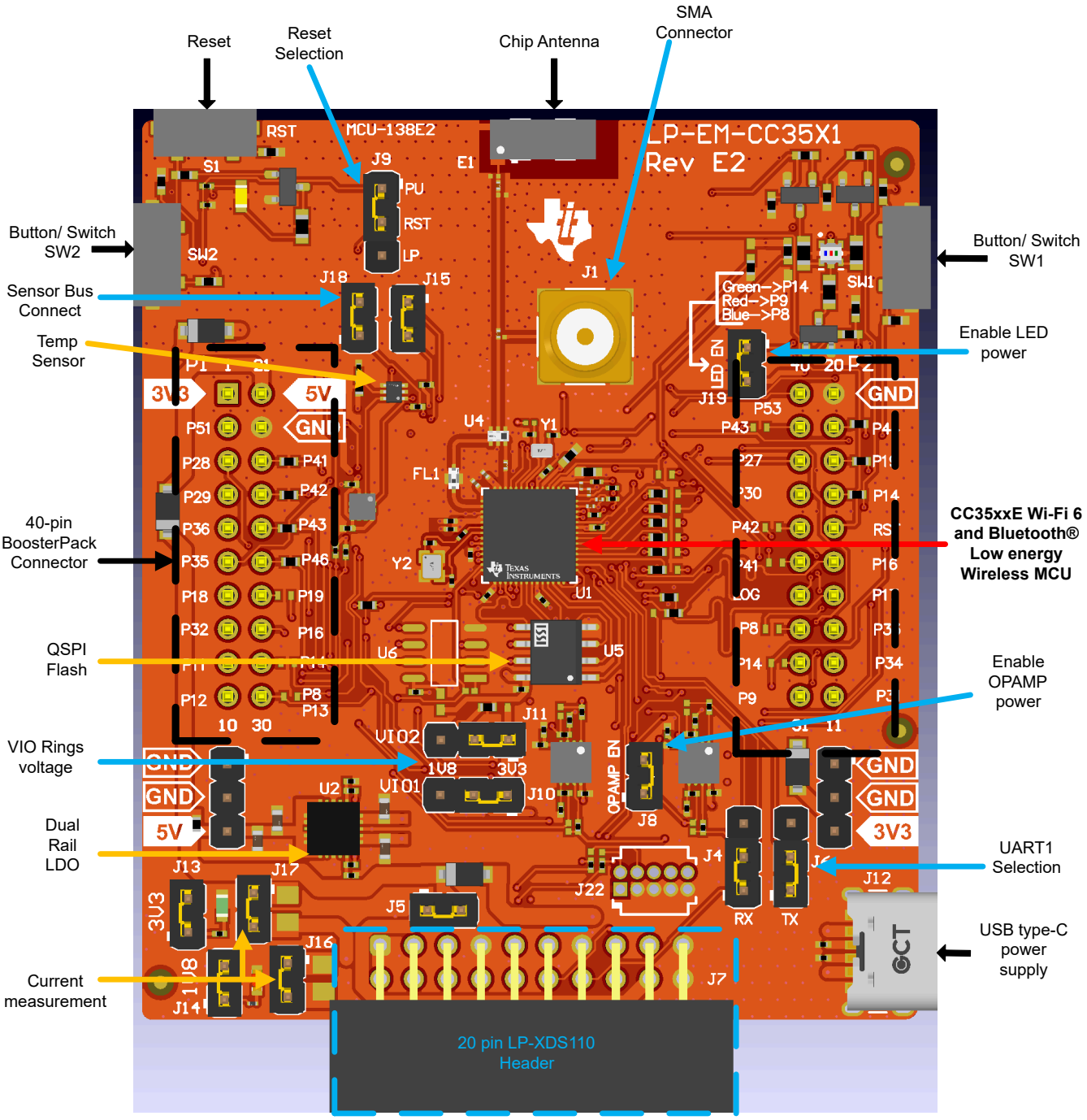


Figure 2-1. CC35xxE LaunchPad Board Overview

2.1 Wired Connections, Jumper Settings, Buttons, and LEDs

2.1.1 SWD Interface

The LP-EM-CC35X1 supports Serial Wire Debug (SWD) interface to an external XDS110 or other JTAG-based debuggers. The SWD interface to the CC35xxE device is used for flashing the device and basic debugging. The SWD lines are part of the VIO1 IO ring, the voltage of which can be controlled by shunt J10, see Section 2.2.1.

The default SWD connection is to the LP-XDS110 20-pin header on the bottom of the LP-EM-CC35X1 (J7).

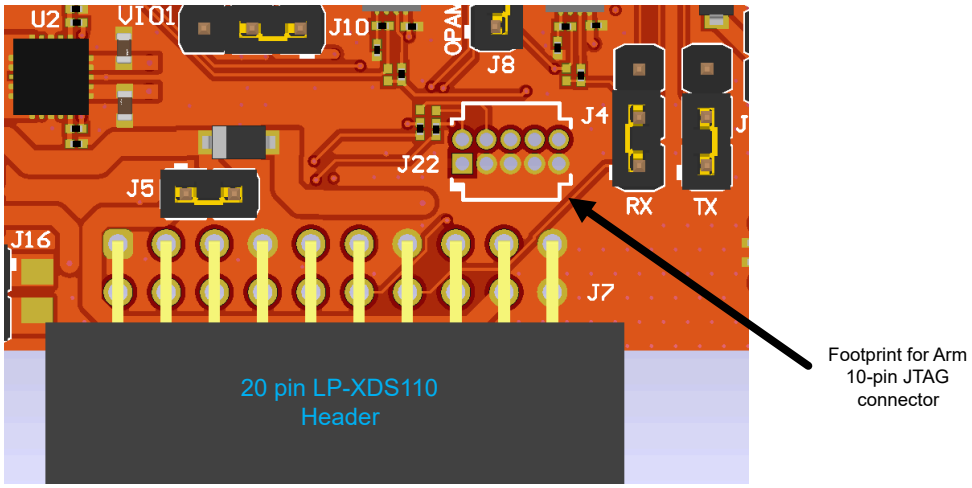


Figure 2-2. SWD Interfaces

Table 2-1. 20 pin LP-XDS110 Connector Assignment

Pin	Signal Name	Description
J7.6	SWCLK	Serial wire clock
J7.8	SWDIO	Serial wire data in/out
J7.10	XDS_RESET	nRESET (enable line to the CC3551E)
J7.12	UART1_TX_XDS	The CC3551E UART TX (from CC3551E) (can be disconnected with jumpers; see Section 2.1.3)
J7.14	UART1_RX_XDS	The CC3551E UART RX (to CC3551E) (can be disconnected with jumpers; see Section 2.1.3)
J7.16	VIO1	VIO1 supply reference voltage to connector
J7.18	VCC_BRD_5V	5V supply to LP-EM-CC35X1 from LP-XDS110
J7.1, J7.7, J7.13, J7.19, J7.20	GND	Board ground

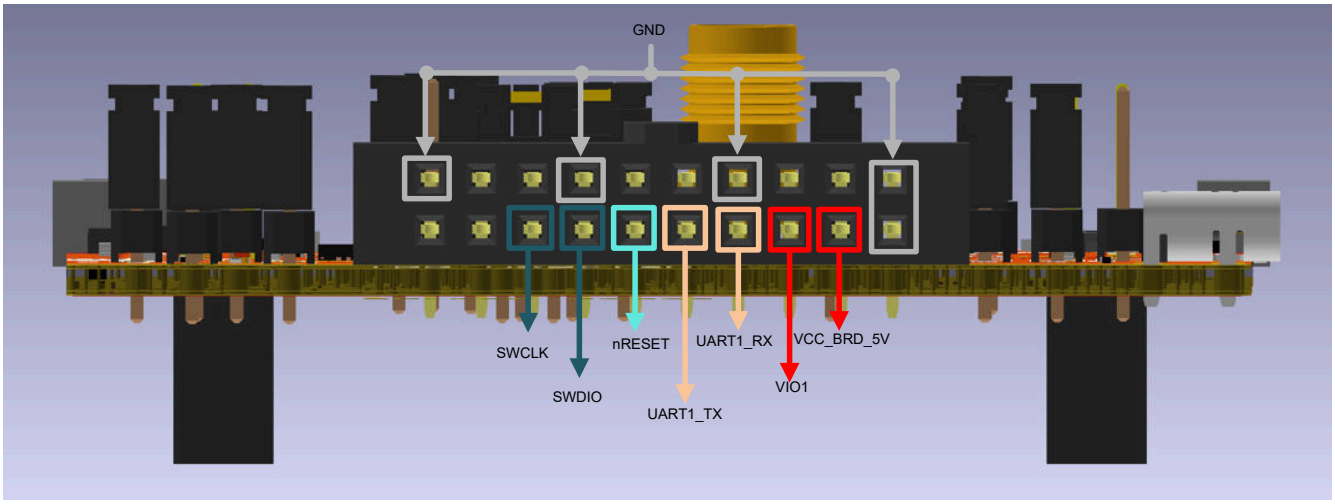


Figure 2-3. 20-Pin LP-XDS110 Connector (J7)

There is also the option to use the ARM Cortex-M 10-pin (CM10) connector for the SWD interface. This connector is not assembled by default but a CM10 header can be soldered on the J22 footprint on the LP-EM-CC35X1. For J22 footprint location, see Figure 2-2.

The pinout of the CM10 connector when assembled is shown in Figure 2-4 and Table 2-2.

Note

In addition to assembling the CM10 connector, 0 ohm resisters must change the assembly location for the SWD interface to this connector. R106 and R107 must be placed on the top two solder pads **instead** of the default bottom two solder pads, as shown in Figure 2-4.

Table 2-2. CM10 Connector (J22) Assignment

Pin	Signal Name	Description
J22.1	VIO1	VIO1 supply reference voltage to connector
J22.2	SWDIO	Serial wire data in/out (See note)
J22.4	SWCLK	Serial wire clock (See note)
J22.10	XDS_RESET	nRESET (enable line to the CC3551E)
J22.3, J22.5, J22.7, J22.9	GND	Board Ground

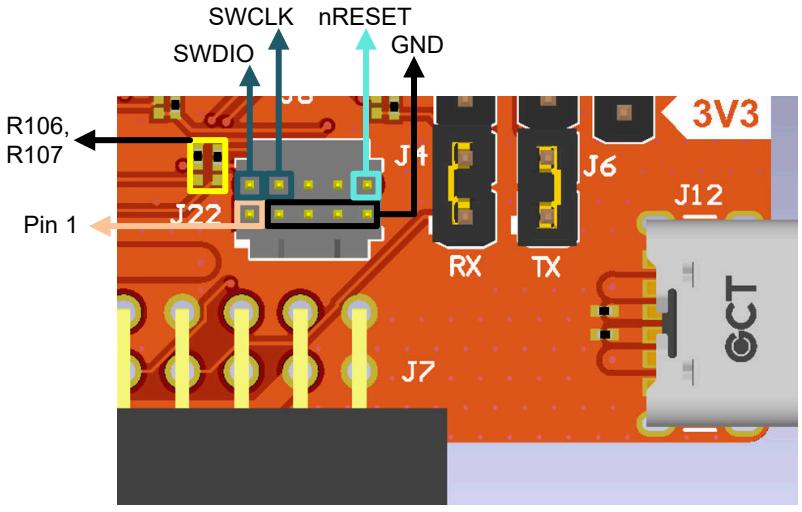


Figure 2-4. CM10 Connector (J22)

2.1.2 I²C Connections

The CC35xxE features two independent I²C peripherals, called I²C0 and I²C1. The LP-EM-CC35X1 allows you to interface to these I²C buses via the LaunchPad header pins.

The LP-EM-CC35X1 also features an accelerometer and a temperature sensor for the out-of-box demo. These features are connected to the I²C1 bus, and can be isolated using the jumpers provided (J15 and J28). By removing J15 and J18, the accelerometer and the temperature sensors are isolated from the I²C1 bus.

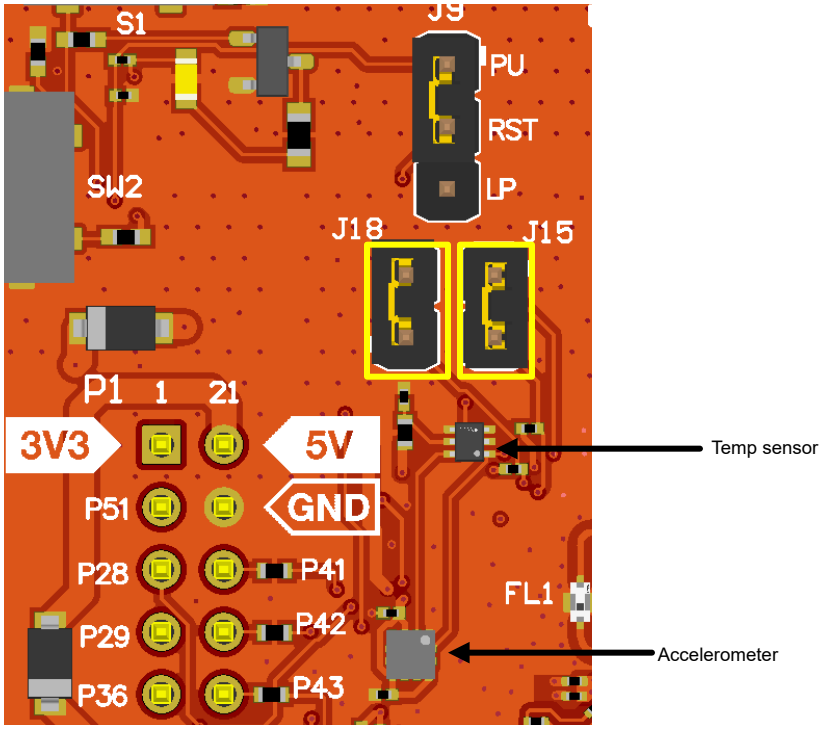


Figure 2-5. I²C Connections

Table 2-3. I2C Jumper Definitions

Reference	Use	Comments
J15	I2C1 CLK	Jumpers populated: onboard sensors connected Jumpers not populated: onboard sensors disconnected
J18	I2C1 Data	

Note

Both I²C buses have on-board pullup resistors on the data and clk lines.

2.1.2.1 Default I²C Addresses

The default I²C addresses of the onboard sensors are listed in Table 2-4.

Table 2-4. Default I²C Addresses (of Onboard Sensors)

Sensor Type	Reference Designator on LP-EM-CC35X1	Part Number (Manufacturer)	Default Target Address (Hex)
Temperature	U8	TMP1075NDRLR (TI)	0x48
Accelerometer	U9	BMA456 (BOSCH)	0x18

2.1.3 UART Signals

The CC35xxE includes two independent UART peripherals, UART0 and UART1. The LP-EM-CC35X1 allows you to interface with these UART signals through the LaunchPad header pins.

UART1 interface is by default connected to the 20-pin LP-XDS110 header (J7) for serial terminal interface (COM port) to a PC through the LP-XDS110. For more information on this header, see Section 2.1.1.

The routing selection of the UART1 TX and RX signals to header J7 or to the LaunchPad header pins is performed using onboard jumpers, J4 and J6, as seen in the figures below.

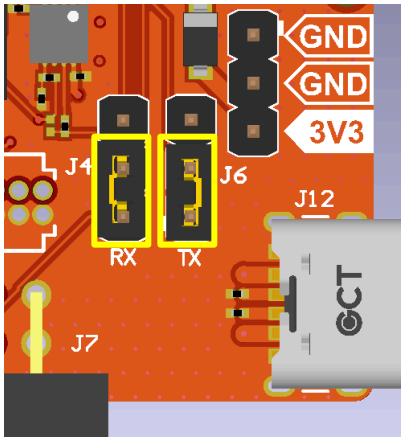


Figure 2-6. UART1 Routed to LP-XDS110

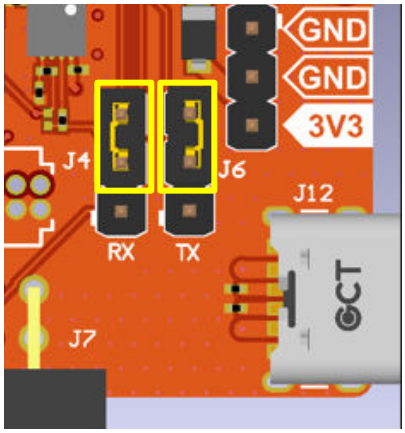


Figure 2-7. UART1 Routed To The LaunchPad Headers

Note

To allow the UART1 signals to route to the designated LaunchPad header pins, 0-ohm resistors can be placed. See Section 2.1.10.

2.1.4 SD Card Interface

The CC35xxE supports SD/MMC peripherals to write to SD memory cards. The LP-EM-CC35X1 features a footprint for an SD card slot (J3) on the back of the board.

To use the SD slot, the 693071010811 SD Slot must be assembled on the J3 footprint on the back (see Figure 2-8), and some resistors need to have the configuration changed (see Figure 2-9).

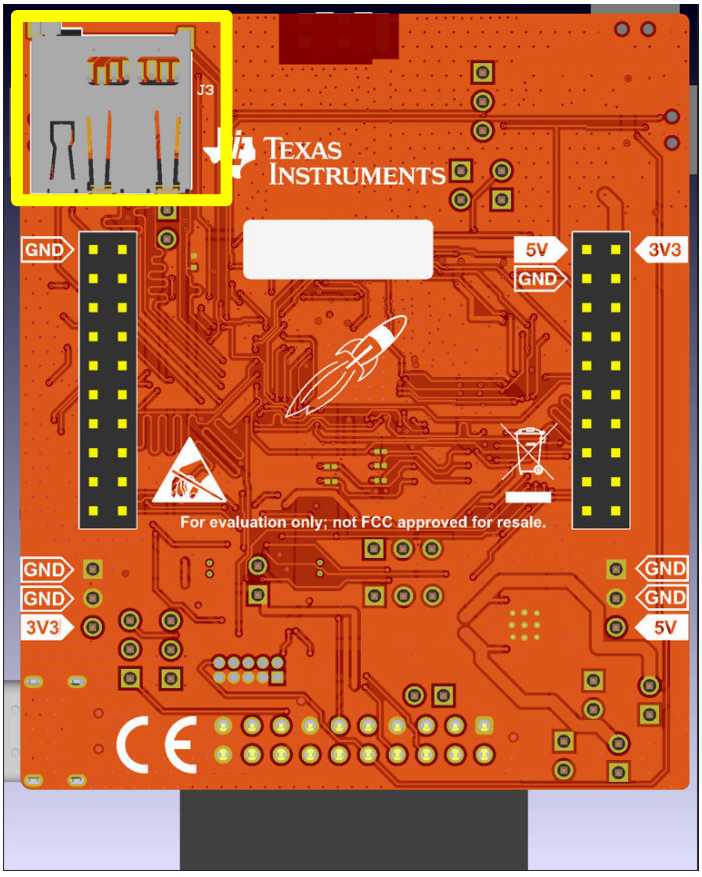


Figure 2-8. SD Card Slot

On the front side of the board, there are some resistors that need to be changed or added. See Figure 2-9.

- R34 footprint needs to have a 0-ohm resistor (0402) assembled.
- R29-R33, and R67 need to be placed on the right 2 solder pads instead of the default left two pads.

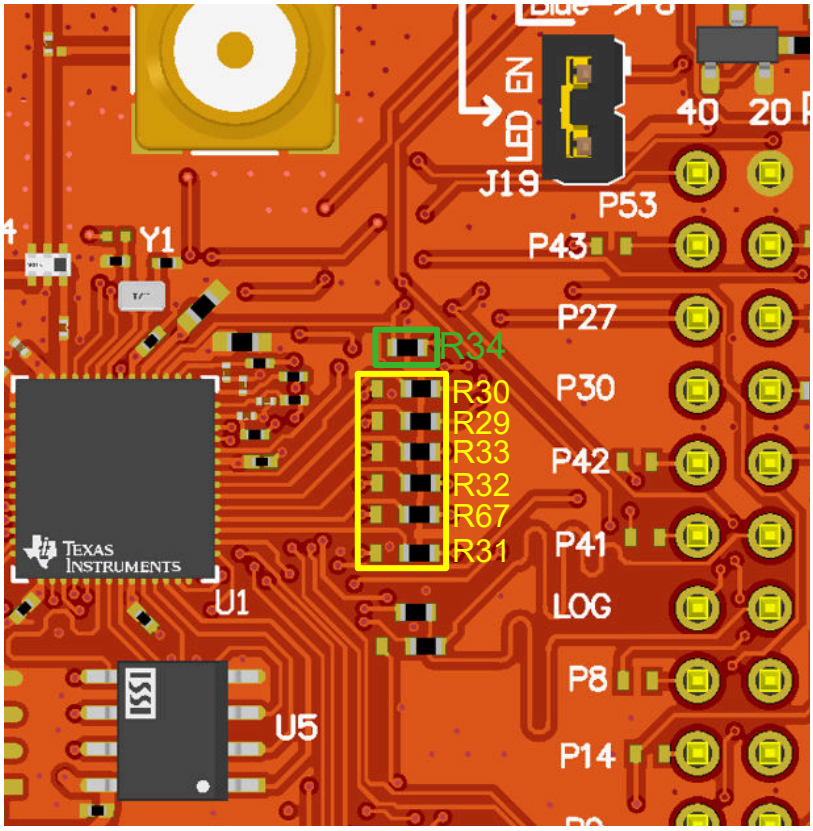


Figure 2-9. SD Slot Resistor Change

Note

Conventional SD memory cards normally require a 3.3V interface. Verify that the corresponding VIO ring for these SDMMC lines (VIO1) from the CC35xx is set to 3.3V using the appropriate VIO jumper. For details on this jumper, see Section 2.2.1.

2.1.5 External Memory Interface

The CC35xxE requires xSPI external flash memory for execution code. The LP-EM-CC35X1 features an onboard external flash (U5).

The xSPI signals from the CC35xxE are part of the VDDSF IO ring, and this voltage can be defined as either 1.8V or 3.3V, depending on the external flash used. The default voltage of VDDSF on the LP-EM-CC35X1 is 1.8V. This voltage provides the reference voltage for the xSPI lines from the CC35xxE and supply voltage to the external flash.

If users want to use a flash that interfaces at 3.3V instead, then R42 can be assembled on the right two solder pads instead of the left (left pads = 1.8V, right pads = 3.3V). The R42 is on the left solder pads, therefore, the VDDSF voltage is 1.8V, as shown in Figure 2-19.

2.1.6 ADC Interface

The CC35xxE features a 12-bit ADC with 8 channels. The LP-EM-CC35X1 enables use of 4 ADC channels with onboard buffers for impedance controlling. The two OPA2211 dual-channel operational amplifiers (U7, U10), which are configured as impedance buffers for four ADC channels can be seen in Figure 2-10.

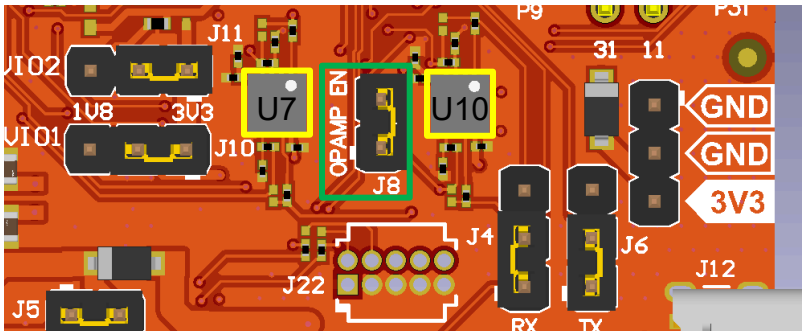


Figure 2-10. ADC Buffers

The four ADC channels available on the LP-EM-CC35X1 are ADC2, ADC3, ADC4, and ADC5. A jumper is also provided to disconnect the power to U7 and U10 for current measurements of the CC35xx.

If users want to use the corresponding GPIOs which are used as the ADC channels without the buffers, then there is the possibility to route around the buffers by removing and placing certain 0-ohm resistors.

The GPIO configuration of the ADC channels and which resistors need to be changed for buffer reroute can be seen in Table 2-5.

Table 2-5. ADC GPIO Configuration

ADC Channel	GPIO # (CC35xx)	LaunchPad Header Pin #	Needed Configuration For Unbuffered GPIO Use
ADC2	GPIO6	23	**remove:** R44, R52 **place:** R71
ADC3	GPIO5	24	**remove:** R73, R75 **place:** R79
ADC4	GPIO4	25	**remove:** R41, R50 **place:** R70
ADC5	GPIO3	26	**remove:** R72, R74 **place:** R78

The locations of the resistors mentioned in Table 2-5 can be seen in Figure 2-11.

As an example, if users want to use GPIO4 unbuffered, which is connected to LaunchPad header pin 26 on the LP-EM-CC35X1, then the following resistors need to be changed:

- Remove R41 and R50
- Place 0-ohm resistor (0201) R70

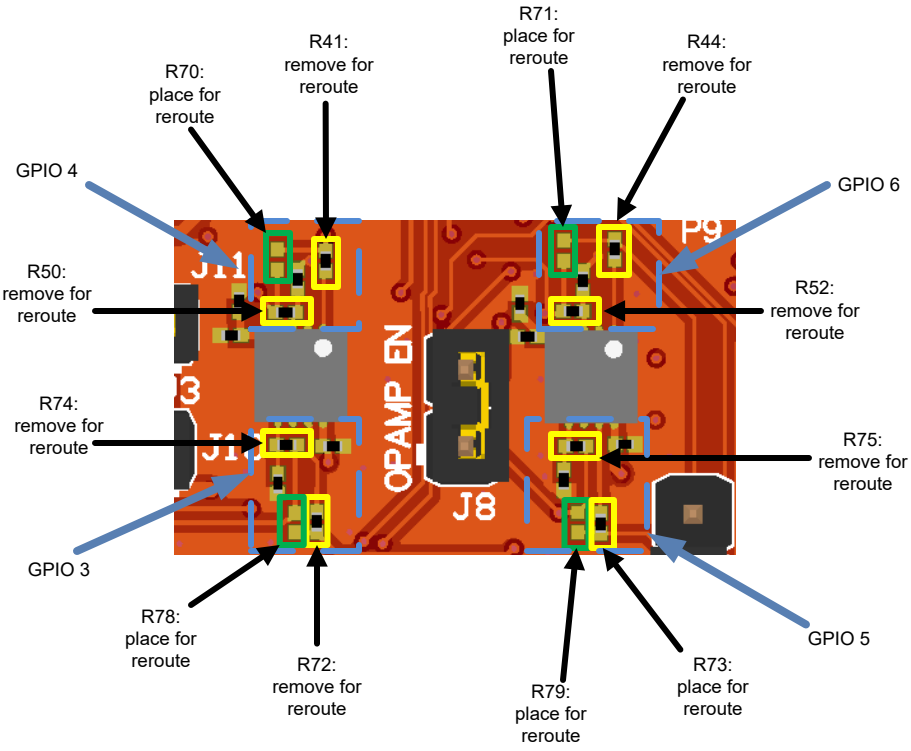


Figure 2-11. ADC Buffer Reroute Configuration

The area of the LP-EM-CC35X1 schematic which encompasses the ADC buffers is shown in Figure 2-12.

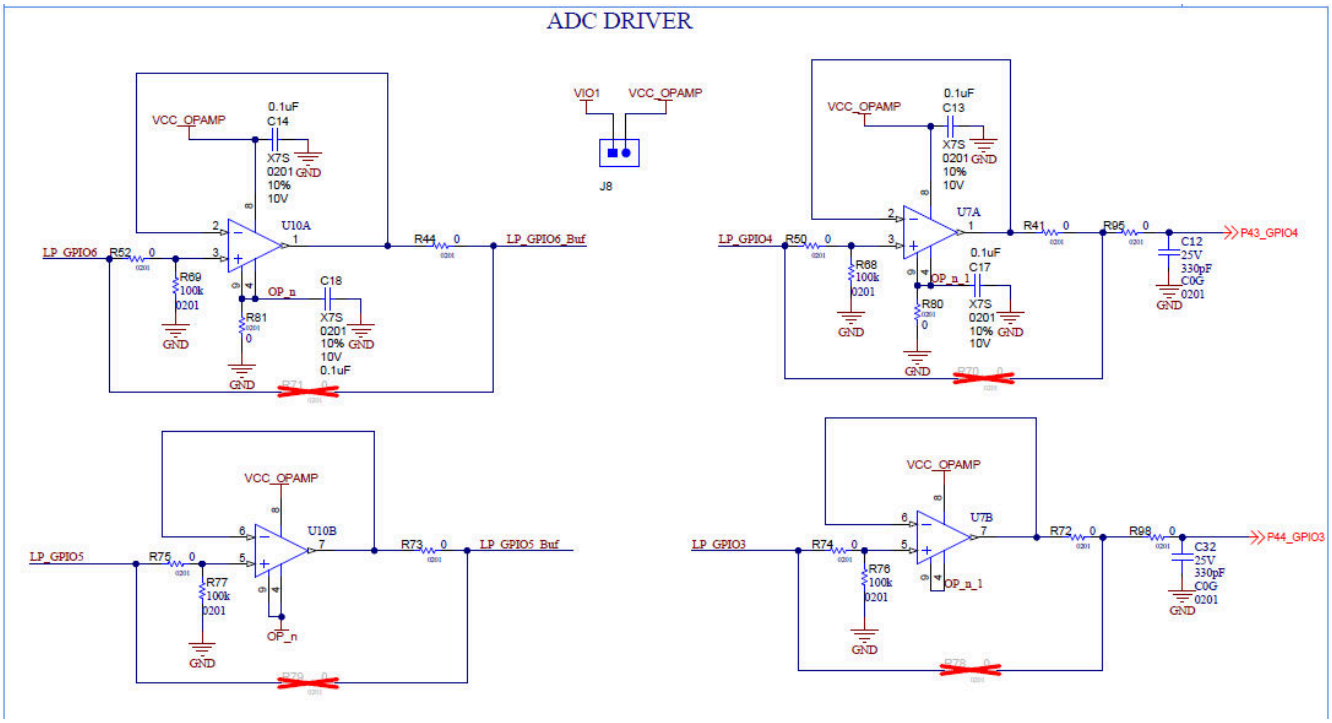


Figure 2-12. ADC Buffers Schematic

2.1.7 Reset Pullup Jumper

To enable the CC35xxE device, the nRESET line must be pulled high externally. On the LP-EM-CC35X1, the nRESET line is pulled up by default, therefore, the CC35xxE device is enabled when power is provided to the board.

The LP-EM-CC35X1 gives the option to route the Reset line to the LaunchPad header (pin 16) to control the reset line externally. To route the nRESET line to the LaunchPad header pin instead of the default pullup, jumper J9 needs to be placed on the bottom two pins. J9 is in the pullup (PU) configuration, therefore, the nRESET line is pulled up when power is supplied to the board, as shown in.Figure 2-13.

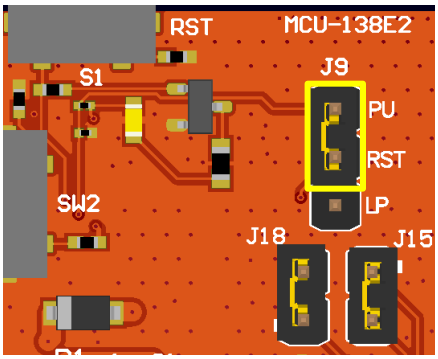


Figure 2-13. nReset Pullup

2.1.8 Push Buttons

The push-button definitions are shown in Table 2-6.

Table 2-6. Push Button Definitions

Reference	Use	Comments
S1	RESET	This signal is used to reset the CC35xxE device.
SW1	GPIO2	When pushed, GPIO2 is pulled to 3.3V.
SW2	GPIO36	When pushed, GPIO36 is pulled to 3.3V.

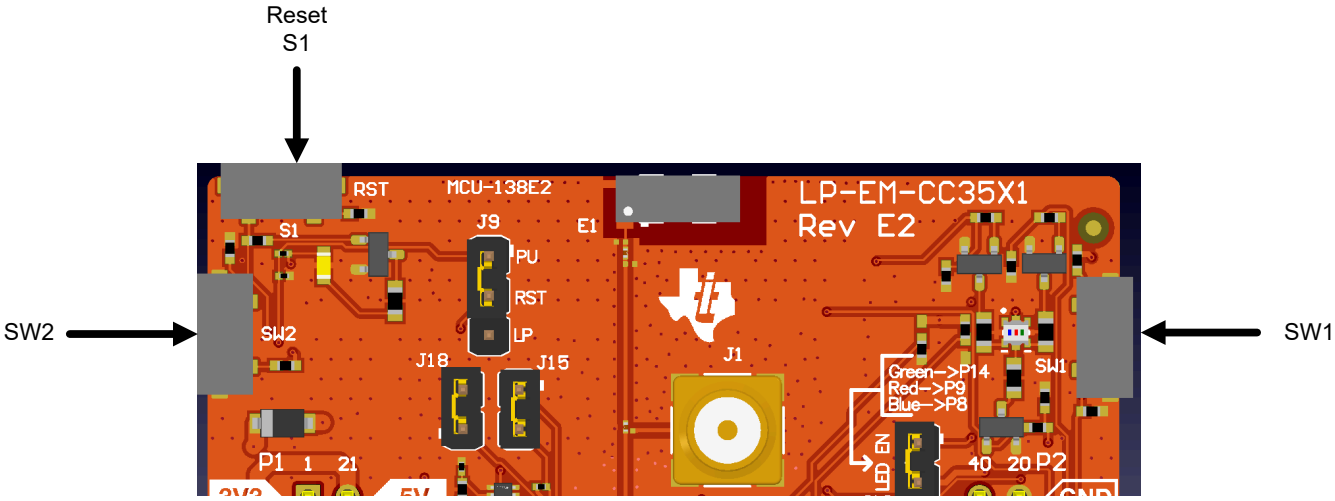


Figure 2-14. Push Buttons

2.1.9 LED Indicators

The LED indicators are listed in Table 2-7.

Table 2-7. LED Indicators

Reference	Color	Use	Comments
D2	Yellow	nRESET	Indicates the state of the nRESET pin. If this LED is on, the device is functional.
D4	RGB	Green - GPIO30 Red - GPIO34 Blue - GPO35	On when the GPIOx is logic-1. (1)
D9	Green	3.3V power indication	On: 3.3V power rail is up. Off: no 3.3V power supplied.
D10	Red	1.8V power indication	On: 1.8V power rail is up. Off: no 1.8V power supplied

(1) The RGB LEDs can be disconnected from the power supply by removing jumper J19 (LED EN). This can be used when measuring current to the CC35xxE.

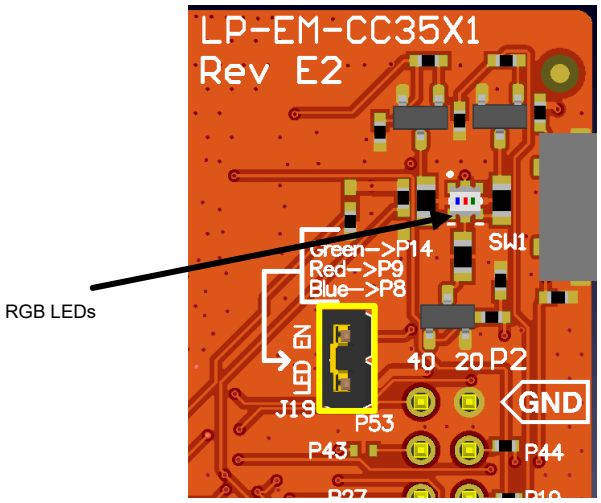


Figure 2-15. RGB LEDs

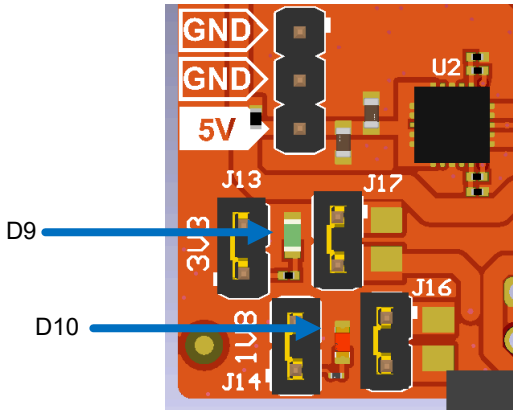


Figure 2-16. Power LEDs

2.1.10 LaunchPad™ Header Pin Assignment

The LP-EM-CC35X1 features 2 × 20-pin connectors that provide access to many of the CC35xxE pins and features. The LaunchPad header pinout is standard in TI, allowing easy stacking of other TI BoosterPacks on the LP-EM-CC35xx for quick interface with peripheral boards.

The CC35xxE LaunchPad follows this standard. For CC35xxE pin-mapping assignments and functions, see Figure 2-17.

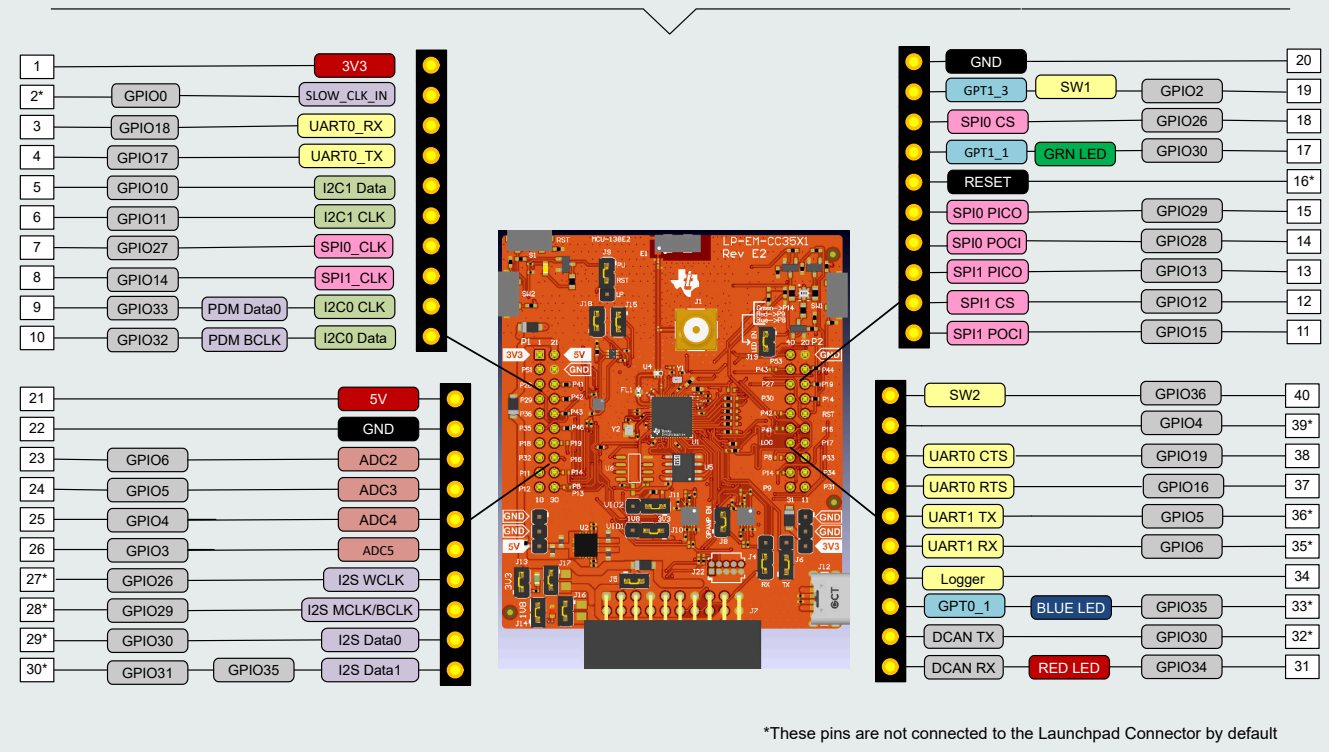


Figure 2-17. CC35xxE LaunchPad Header Pin Assignments

All the signals are referred to by the GPIOx in the SDK. The default mappings are shown in Figure 2-17. Some of the pins are repeated across the connector. For example, GPIO4 is available on header pin 25 and pin 39, but only pin 25 is connected by default. The signal on LaunchPad header pin 39 is marked with an asterisk (*) to signify that the signal is not connected by default. The signal can be routed to the pin by using a 0Ω resistor in the path.

Note

The LP-EM-CC35X1 has two jumpers, which can control the voltage of VIO1 and VIO2. The jumpers provide reference voltage for the various CC3551E IOs, and can be configured to 3.3V or 1.8V. When using the GPIOs connected to the LaunchPad header pins, knowing what VIO the jumpers correspond to, and how to configure them to be either 3.3V or 1.8V is important. For more information, refer to Section 2.2.1.

2.2 Power

The LP-EM-CC35X1 is designed to accept power from a connected LP-XDS110 and an external USB-C power connection together.

> **WARNING**
> To verify the proper functioning of the board, the LP-XDS110 and USB-C power cable from the LP-EM-CC35X1 must be connected to the same computer. Do not connect the USB-C cable to a wall outlet or a different computer.

The use of Schottky diodes makes sure that load sharing occurs between the USB connectors on the LaunchPad kit and the BoosterPack module without any board modifications. The jumpers labeled J14 (1.8V) and J13 (3.3V) can be used to measure the total current consumption of the board from the onboard LDO.

2.2.1 VIO Selection

The CC35xxE device features three Voltage IO rings (VIOs) for choosing the reference voltage of the various IOs. These three VIOs are VIO1, VIO2, and VDDSF. Each one of the IO rings can be set to 1.8V or 3.3V independently of each other.

The LP-EM-CC35X1 features 2 jumpers (J10, J11) for easy voltage configuration for VIO1 and VIO2, either to 1.8V or 3.3V. By default both are set to 3.3V; see Figure 2-18.

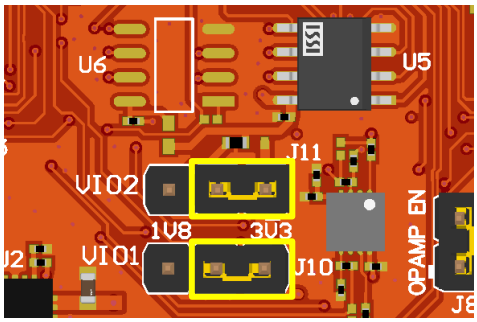


Figure 2-18. VIO Jumpers

To set either VIO to 1.8V instead of 3.3V, place the jumper on the left two header pins. For example, VIO1 is set to 1.8V and VIO2 is set to 3.3V as shown in Figure 2-19.

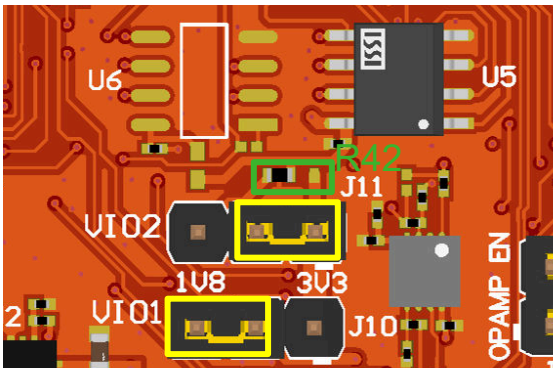


Figure 2-19. VIO Selection Example

VDDSF IO ring controls the reference voltage of the xSPI signals to the external flash. For more information on VDDSF, see Section 2.1.5.

For the VIO selection of each GPIO, see Table 2-8.

Table 2-8. GPIO VIO Selection

LaunchPad Header Pin #	Default Setting on LP-EM-CC35X1	CC35xx GPIO #	IO Ring
1	3.3V	N/A	N/A
2	SLOW_CLK_IN	GPIO0	VIO1
3	UART0 RX	GPIO18	VIO1
4	UART0 TX	GPIO17	VIO1
5	I2C1 Data	GPIO10	VIO1
6	I2C1 CLK	GPIO11	VIO1
7	SPI0 CLK	GPIO27	VIO2
8	SPI1 CLK	GPIO14	VIO1
9	I2C0 CLK, PDM Data0	GPIO33	VIO2
10	I2C0 Data, PDM BCLK	GPIO32	VIO2
11	SPI1 POCI	GPIO15	VIO1
12	SPI1 CS	GPIO12	VIO1
13	SPI1 PICO	GPIO13	VIO1
14	SPI0 POCI	GPIO28	VIO2
15	SPI0 PICO	GPIO29	VIO2
16	Reset	N/A	N/A
17	GPT1_1	GPIO30	VIO2
18	SPI0 CS	GPIO26	VIO2
19	GPT1_3	GPIO2	VIO1
20	GND	N/A	N/A
21	5V	N/A	N/A
22	GND	N/A	N/A
23	ADC2	GPIO6	VIO1
24	ADC3	GPIO5	VIO1
25	ADC4	GPIO4	VIO1
26	ADC5	GPIO3	VIO1
27	I2S WCLK	GPIO26	VIO2
28	I2S MCLK/BCLK	GPIO29	VIO2
29	I2S Data0	GPIO30	VIO2
30	I2S Data1	GPIO31, GPIO35	VIO2
31	DCAN RX	GPIO34	VIO2
32	DCAN TX	GPIO30	VIO2
33	GPT0_1	GPIO35	VIO2
34	Logger	N/A	N/A
35	UART1 RX	GPIO6	VIO1
36	UART1 TX	GPIO5	VIO1
37	UART0 RTS	GPIO16	VIO1
38	UART0 CTS	GPIO19	VIO1
39	GPIO	GPIO4	VIO1
40	N/A	GPIO36	VIO1

2.2.2 Measure the CC35xxE Current Draw

2.2.2.1 Low Current Measurement (LPDS)

To measure the current draw of the CC35xxE device for both power supplies (3.3V or 1.8V), a jumper labeled J17 (for 3.3V supply) and a jumper labeled J16 (for 1.8V supply) is provided on the board. By removing J16, users can place an ammeter into this path to observe the current on the 1.8V supply. The same process can be used for observing the current on the 3.3V supply with J17. TI recommends this method for measuring the LPDS.

Note

The current measured on the 3.3V and 1.8V jumpers is the total current that goes to the CC35xxE, not including VIO1, VIO2, and VDDSF. These supplies provide a reference voltage for all of the IOs and some of the peripherals on the LP-EM-CC35X1 (ADC buffers, sensors, and so forth).

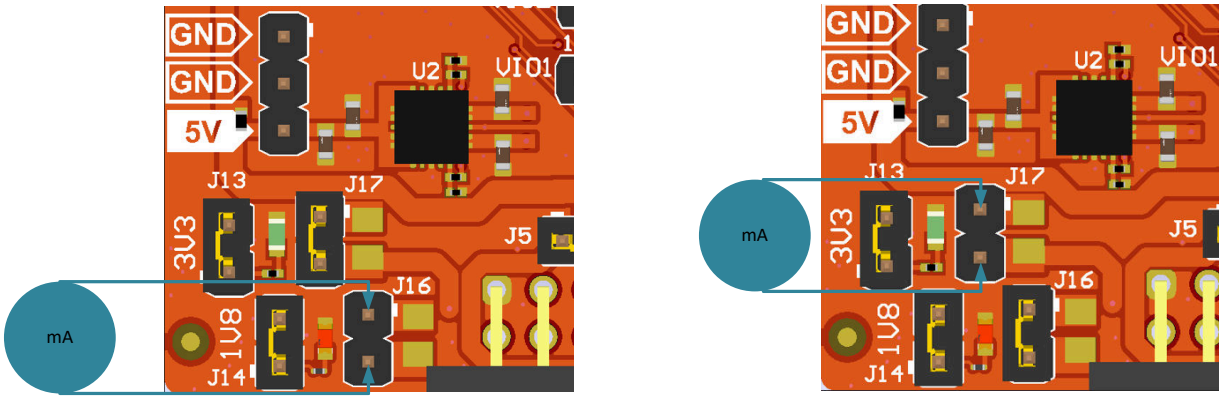


Figure 2-20. Low Current Measurement

2.2.2.2 Active Current Measurement

To measure the active current of the CC35xxE device in a profile form, TI recommends using a 0.1Ω 1% 0603 resistor on the board and measuring the differential voltage across the resistor. This can be done using a voltmeter or an oscilloscope to measure the current profile for both power supplies (3.3V or 1.8V).

Jumper J16 shunt is removed and a 0.01 resistor is populated in parallel to measure the active currents on the 1.8V supply; see Figure 2-21. Perform a similar operation with J17 and 3.3V supply.

Note

The current measured on the 3.3V and 1.8V jumpers is the total current that goes to the CC35xxE, not including VIO1, VIO2, and VDDSF. These supplies provide a reference voltage for all of the IOs and some of the peripherals on the LP-EM-CC35X1 (ADC buffers, sensors, and so forth).

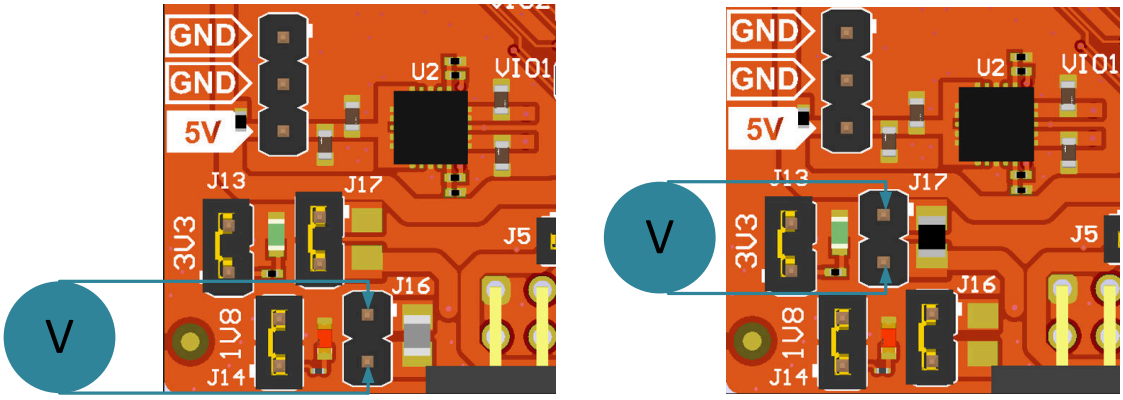


Figure 2-21. Active Current Measurement

2.3 Clocking

The LP-EM-CC35X1 provides two clock inputs to the CC35xxE device:

- Y2 is a 52MHz crystal for fast clock input.
- Y1 is a 32.768kHz XTAL for slow clock input.

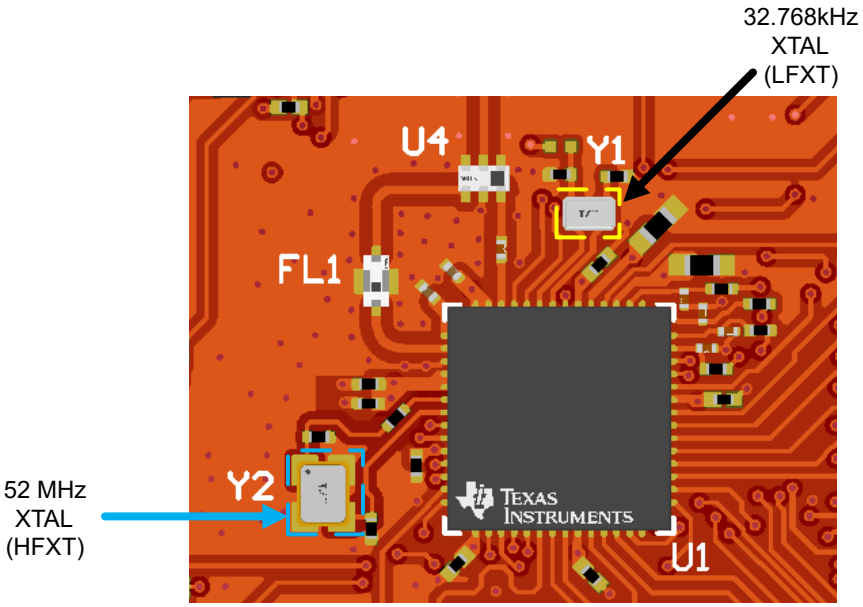


Figure 2-22. Clocks

The slow clock can be generated by an external oscillator instead of the XTAL, or generated internally by the CC35xxE.

If the user wants to provide an external slow clock through LaunchPad header pin (pin 2), then:

- Remove Y1 XTAL .
- Populate 0-ohm resistor (0201) on the R5 pad.
- Remove C6 capacitor .

See Figure 2-23.

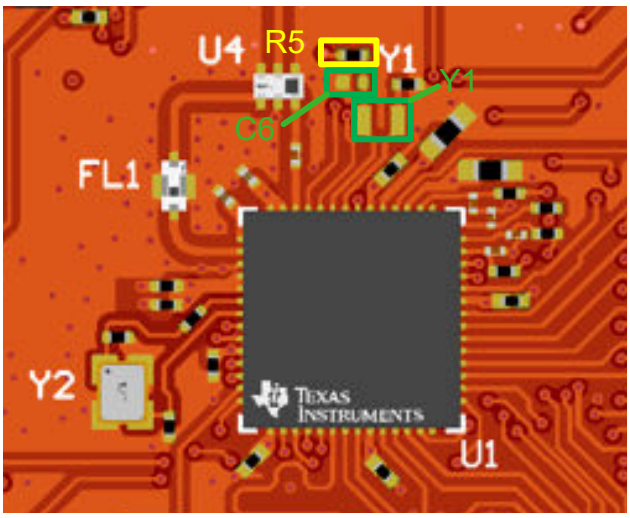


Figure 2-23. External Slow Clock

To use the CC35xxE internal slow clock, leave pin 2 floating when Y1 is not placed.

2.4 Conducted RF Testing

The LP-EM-CC35X1 can be used to test RF capabilities, using Radio Tool. For more information on Radio Tool and where to download, refer to Section 2.5.1.

As seen in Figure 2-24, the LP-EM-CC35X1 has an on-board SMA connector and component antenna. The SMA connector (J1) provides a way for testing conducted RF measurements. Alternately, a track pad for a U.FL connector (J2) is provided on-board to replace the SMA connector and provide a way to test in the lab using a compatible cable (see Figure 2-24). A rework is needed before using the connector on J1/J2. This involves swapping the position of the existing 3.9pF capacitor to lead the transmission line on the desired connection (see Figure 2-24).

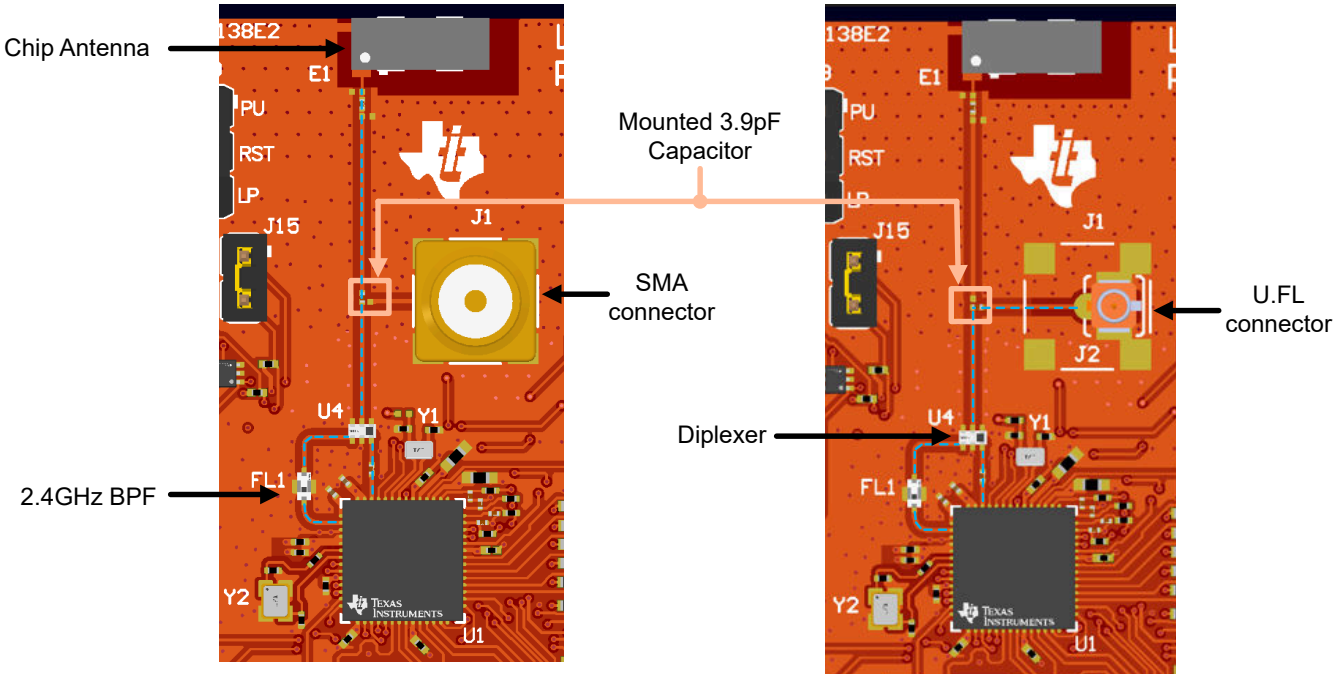


Figure 2-24. RF path on LP-EM-CC35X1

2.5 Evaluation Setup

The CC35xxE Launchpad is designed to work primarily with the LP-XDS110, which provides SWD and UART interface to external PC. The SWD interface is used for flashing the compiled image to the CC35xxE and basic debugging, while the UART is used for serial terminal access.

The LP-XDS110 or LP-XDS110ET can easily integrate with the LP-EM-CC35X1 by connecting the 20-pin LP-XDS110 connector (J7) to the corresponding connector on the LP-XDS110 (see Figure 2-25). Make sure that the jumper on the LP-XDS110 (labeled TGT VDD) is in the EXT. configuration, as shown in Figure 2-25. This verifies that the target voltage for the JTAG signals is sourced from the LP-EM-CC35X1 (which is controlled by VIO1) instead of the default LP-XDS110 target voltage (3.3V).

WARNING

To verify the proper functioning of the board, the LP-XDS110 and USB-C power cable from the LP-EM-CC35X1 must be connected to the same computer. Do not connect the USB-C cable to a wall outlet or a different computer.

To properly interface UART signals for the serial terminal interface, verify that jumpers J4 and J6 are placed in the correct configuration. See Section 2.1.3.

For more information on the 20-pin LP-XDS110 connector and the available pinout, see Section 2.1.1.

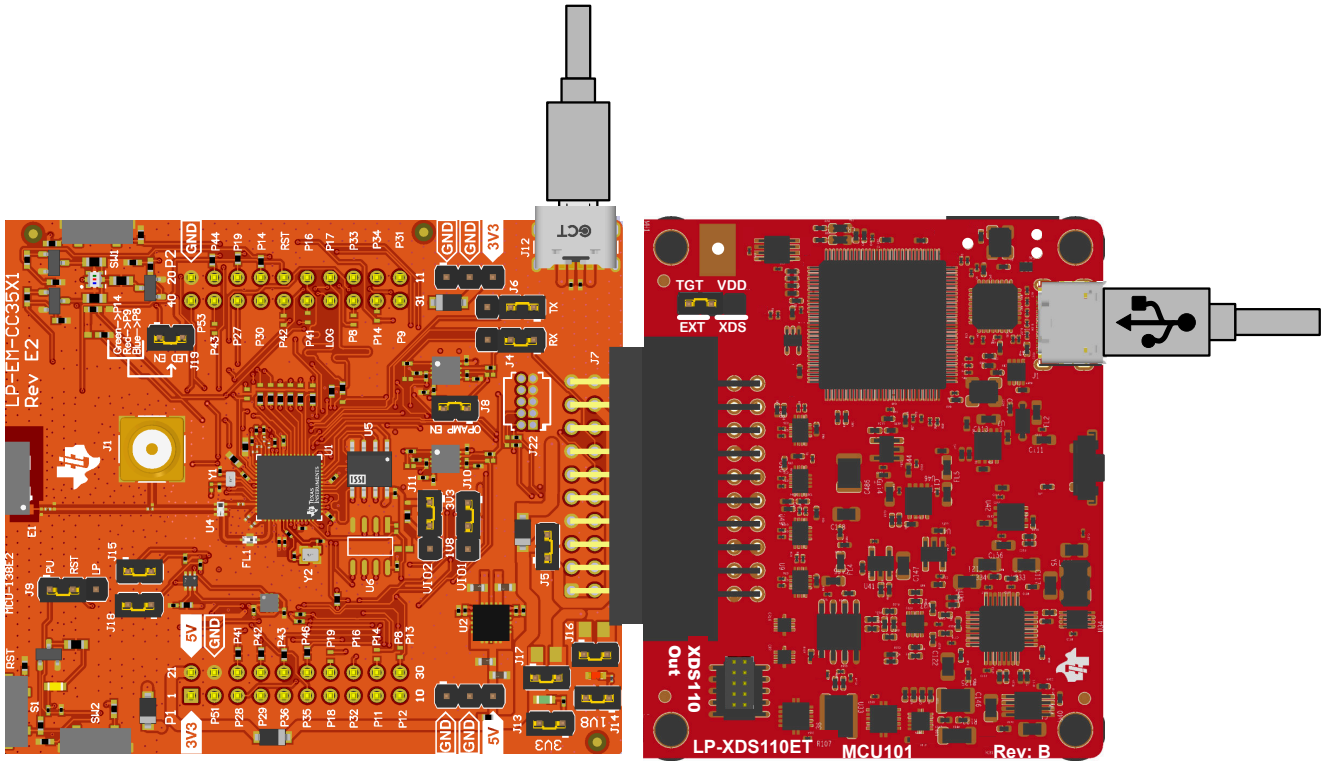


Figure 2-25. LP-EM-CC35X1 Connected to LP-XDS110(ET)

2.5.1 Wi-Fi Toolbox LP-EM-CC35X1 Hardware Setup

SimpleLink Wi-Fi toolbox is a GUI-based tool for the evaluation, programming, and testing of CC35xx designs during development and certification. Radio Tool is one of the tools included in the toolbox that allows for RF testing. The tool enables low-level radio testing capabilities by manually setting the radio into transmit or receive modes. Usage of the tool requires familiarity and knowledge of radio circuit theory and radio test methods. To perform conducted RF testing on the LP-EM-CC35X1, refer to Section 2.4. Note that a rework can be needed.

The user can download this tool from the CC35xx product page on ti.com.

HW Prerequisites

- Windows 10 64bit/ Ubuntu 18 (or higher) 64bit operation system
- Latest Chrome web browser
- Installation of Simplelink Wi-Fi Toolbox
- LP-EM-CC35X1
- LP-XDS110 or LP-XDS110ET debugger for SWD communication

The LP-XDS110 enables direct communication to the CC35xx device via the SWD interface. This allows external tools, such as the Radio Tool, to send commands directly to the device without the use of flashing the application image.

3 Hardware Design Files

3.1 Schematics

To access the schematics for the LP-EM-CC35X1, users can submit a request on the CC3551E tool folder under the *Request More Information* section.

3.2 PCB Layouts

To access the layout files for the LP-EM-CC35X1, users can submit a request on CC3551E tool folder under the *Request More Information* section.

3.3 Bill of Materials (BOM)

To access the BOM for the LP-EM-CC35X1, users can submit a request on the CC3551E tool folder under *Request More Information* section.

4 Additional Information

4.1 Trademarks

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from January 9, 2024 to January 1, 2025 (from Revision * (September 2024) to Revision A (February 2025)) **Page**

- Updated for hardware revision E3 1

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