

Errata

**IWR1443 Device Silicon Errata  
Silicon Revisions 1.0, 2.0, and 3.0**



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## 1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (IWR1443).

## 2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / mmWave sensor devices. Each of the Radar devices has one of the two prefixes: XIx or IWRx (for example: **IWR1443FQAGABL**). These prefixes represent evolutionary stages of product development from engineering prototypes (XI) through fully qualified production devices (IWR).

Device development evolutionary flow:

- XI** — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- IWR** — Production version of the silicon die that is fully qualified.

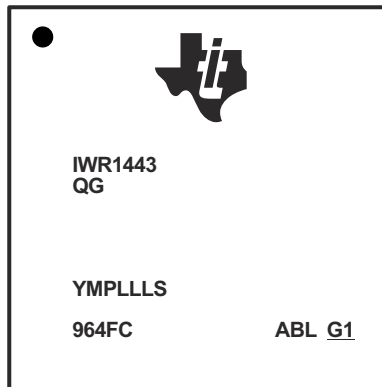
XI devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

### 3 Device Markings

Figure 3-1 shows an example of the IWR1443 Radar Device's package symbolization.



**Figure 3-1. Example of Device Part Markings**

This identifying number contains the following information:

- **Line 1:** Device Number
- **Line 2:** Temperature and Security Grade
- **Line 3:** Lot Trace Code
  - YM = Year/Month Code
  - P L L L = Assembly Lot
  - S = Assembly Site Code
- **Line 4:**
  - 964 = IWR1443 Identifier
  - D = ES2.0
  - FC = ES3.0
  - BLANK = ES1.0
  - ABL = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

## 4 Usage Notes

Usage notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These usage notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

### 4.1 MSS: SPI Speed in 3-Wire Mode Usage Note

The maximum SPI speed under 3-wire operation was only tested up to 33 MHz. This affects IWR1443 ES2.0.

### 4.2 Identification

The JTAG identification code for this device is the same as the device ICEPick Identification code.

**Table 4-1. Device Identification**

Silicon Revision	ID
ES1.0	0x0BB1F02F
ES2.0	0x1BB1F02F
ES3.0	0x3BB1F02F

## 5 Advisory to Silicon Variant / Revision Map

**Table 5-1. Advisory to Silicon Variant / Revision Map**

Advisory Number	Advisory Title	IWR1443		
		ES1.0	ES2.0	ES3.0
<b>Main Subsystem</b>				
MSS#01	Available MSS Memory (RAM) for Customer Application is Smaller by 128 KB	X	X	
MSS#03A	Incorrect Handling of "Saturation" in FFT Hardware Accelerator's Input / Output Formatter and Statistics Block	X	X	X
MSS#04A	Number of Samples (SRCACNT) Should be >3 for Correct Operation of FFT Hardware Accelerator	X	X	X
MSS#05A	Incorrect FFT Intermediate Stage Clip Status Indication	X	X	X
MSS#06	Internal Pulls on QSPI Data Lines not Enabled by the Device Bootloader	X	X	
MSS#07A	MSS interrupt Number 106 Seen as Pending by the User Application	X	X	X
MSS#08	ESM Group2 Interrupt (VIM Compare Error), Which is Mapped to FIQ Line, is Active When Control is Passed to Application	X	X	
MSS#09	ESM Group1 Interrupt (NERROR_IN_SYNC) Seen as Pending by User Application – Can Lead to Interrupt if Unmasked	X	X	
MSS#13	Incorrect Read from FFT Hardware Accelerator After Complex Multiplication Operation	X	X	X
MSS#14	Asynchronous Assertion of SoC Warm Reset may not Work Reliably When Device Operating on PLL Clock	X	X	
MSS#15	The IWR14xx ES1.0 and ES2.0 Devices Only Work With Spansion and Macronix Devices	X	X	See <sup>(1)</sup>
MSS#19	DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario	X	X	X
MSS#20	Radar Frame Stuck due to Missing Synchronizer Logic in Hardware	X	X	X
MSS#21A	Issue with HWA Input Formatter 16 bit Real Signed Format	X	X	X
MSS#22	CAN-FD: Message Transmitted With Wrong Arbitration and Control Fields	X	X	X
MSS#23	HWA Read Registers Cannot be Read Reliably When the HWA is Executing a ParamSet Instruction	X	X	X
MSS#24	Limitation With Peak Grouping Feature in Hardware Accelerator	X	X	X
MSS#25	Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs	X	X	X
MSS#26	DMA Requests Lost During Suspend Mode	X	X	X
MSS#27	MibSPI in Slave Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1	X	X	X
MSS#28	A Data Length Error is Generated Repeatedly in Slave Mode When IO Loopback is Enabled	X	X	X
MSS#29	Spurious RX DMA REQ From a Slave Mode MibSPI	X	X	X
MSS#30	MibSPI RX RAM RXEMPTY Bit Does Not Get Cleared After Reading	X	X	X
MSS#31	CPU Abort Generated on a Write to Implemented CRC Space After a Write to Unimplemented CRC Space	X	X	X
MSS#32	DMMGLBCTRL BUSY Flag Not Set When DMM Starts Receiving A Packet	X	X	X
MSS#33	MibSPI RAM ECC is Not Read Correctly in DIAG Mode	X	X	X
MSS#35	EDMA TPTC Generates an Incorrect Address on the Read Interface, Causing one or More Data Integrity Failures, Hangs, or Extra Reads	X	X	X
MSS#37B	DCC Module Frequency Comparison can Report Erroneous Results	X	X	X
MSS#38A	GPIO Glitch During Power-Up	X	X	X
MSS#39	The state of the MSS DMA is left pending and uncleared on any DMA MPU fault	X	X	X
MSS#40	Any EDMA Transfer That Spans ACCEL_MEM1 +ACCEL_MEM2 Memories of Hardware Accelerator May Result In Data Corruption Without Any Notification Of Error From The SoC	X	X	X
MSS#43A	Read-data from internal registers of PCR is not reliable. Shared PCS region protection is also not supported	X	X	X

**Table 5-1. Advisory to Silicon Variant / Revision Map (continued)**

Advisory Number	Advisory Title	IWR1443		
		ES1.0	ES2.0	ES3.0
<a href="#">MSS#44</a>	SYNC IN input pulse wider than 4usec can cause a FRC lockstep error	X	X	X
<a href="#">MSS#45</a>	Bootup failure during the serial flash busy state	X	X	X
<b>Analog / Millimeter Wave</b>				
<a href="#">ANA#01</a>	Noise Figure Degradation	X		
<a href="#">ANA#02</a>	VCO#1 [76-77GHz] Minimum Frequency Falls Short of Target	X		
<a href="#">ANA#03</a>	Spurs from LVDS Output Coupling into Synthesizer	X		
<a href="#">ANA#04</a>	Receiver Gain Range Availability	X		
<a href="#">ANA#06</a>	Return Loss Measurement on TX: S11 < -9dB, RX S11 < -6.5dB (Accepted Value of < -10dB)	X		
<a href="#">ANA#07</a>	CSI2 Activity Coupling to Clock	X	X	
<a href="#">ANA#08A</a>	Doppler Spur Observed at Certain RF Frequencies	X	X	X
<a href="#">ANA#10A</a> <sup>(1)</sup>	Unreliable Readings from Synthesizer Supply Voltage Monitor	X	X	X
<a href="#">ANA#11A</a>	TX, RX Gain Calibrations Sensitive to Large External Interference	X	X	X
<a href="#">ANA#12A</a>	Second Harmonic (HD2) Present in the Receiver	X	X	X
<a href="#">ANA#13B</a>	TX1 to TX3 Phase Mismatch Variation over Temperature is Double that of TX2/TX1 and TX3/TX2 Combinations	X	X	X
<a href="#">ANA#15</a>	Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output	X	X	X
<a href="#">ANA#16</a>	LVDS Coupling to Clock System	X	X	X
<a href="#">ANA#17A</a>	On-Board Supply Ringing Induced Spur	X	X	X
<a href="#">ANA#18B</a>	Spurs Caused due to Digital Activity Coupling to XTAL	X	X	X
<a href="#">ANA#20</a>	Occasional Failures Observed During Calibration of the Radar Subsystem	X	X	X
<a href="#">ANA#21A</a>	Out of Band Radiated Spectral Emission	X	X	X
<a href="#">ANA#22A</a>	Overshoot and Undershoot During Inter-Chirp Idle Time	X	X	X
<a href="#">ANA#24A</a>	40-MHz OSC CLKOUT Causing Spurs in 2D-FFT Spectrum	X	X	X
<a href="#">ANA#27</a>	Digital Temperature Sensor Having Higher Error	X	X	X

(1) For IWR1443 ES3.0 follow QSPI recommendations in [Flash Variants Supported by the mmWave Sensor](#).

## 6 Known Design Exceptions to Functional Specifications

### **MSS#01** *Available MSS Memory (RAM) for Customer Application is Smaller by 128 KB*

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**Revision(s)  
Affected:** IWR1443 ES1.0, and IWR1443 ES2.0

**Description:** Due to available RAM being used for Radar block development, RAM available for user application is limited to 448 KB instead of 576 KB.

**Workaround(s):** None. Silicon update will be provided by TI.

### **MSS#03A** *Incorrect Handling of "Saturation" in FFT Hardware Accelerator's Input / Output Formatter and Statistics Block*

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**Revision(s)  
Affected:** IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

- Input formatter block performs saturation based on signed or unsigned samples. However, the compute engine module always saturates the input as a 24 bit signed number.
- Output formatter block saturates the 16 bits unsigned number as signed number. This causes magnitude outputs to have a smaller max range.
- Statistics block always assumes that input is signed when checking for saturation, but the input can be unsigned in some cases.

**Workaround(s):** None, there is no planned update. The max output range must be 16 bit signed. The statistics block input should be a signed input.

### **MSS#04A** *Number of Samples (SRCACNT) Should be >3 for Correct Operation of FFT Hardware Accelerator*

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**Revision(s)  
Affected:** IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:** Logic which subtracts the compute engine pipelined delay from FFT counter wraps around incorrectly when the number of samples is less (specifically, when it is 3).

**Workaround(s):** FFT engine should not be used with FFT counter value < 4.

### **MSS#05A** *Incorrect FFT Intermediate Stage Clip Status Indication*

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**Revision(s)  
Affected:** IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:** FFT clip status register incorrectly uses all butterfly stages, even if only a few of the stages are enabled.

**Workaround(s):** Do not use the HWA FFT Intermediate Stage Clip status indication

### **MSS#06** *Internal Pulls on QSPI Data Lines not Enabled by the Device Bootloader*

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**Revision(s)  
Affected:** IWR1443 ES1.0 and IWR1443 ES2.0

**Description:** Internal Pulls on the Data lines (D2 and D3) are not enabled by the device bootloader.

**Workaround(s):** Pulls on target board required (refer to reference schematics of TI EVM).

<b>MSS#07A</b>	<b><i>MSS interrupt Number 106 Seen as Pending by the User Application</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	Due to an anomalous connection in one of the Analog blocks (which is otherwise not a concern) MSS Interrupt number 106 will always be seen as pending by the application.
<b>Workaround(s):</b>	It is recommended that this interrupt is always kept as masked by the user application.
<b>MSS#08</b>	<b><i>ESM Group2 Interrupt (VIM Compare Error), which is Mapped to FIQ Line, is Active when Control is Passed to Application</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0 and IWR1443 ES2.0
<b>Description:</b>	Compare Error is always present when the control is passed to the application due to a missing configuration in device bootloader.
<b>Workaround(s):</b>	The Application is expected to clear this error immediately on start up.
<b>MSS#09</b>	<b><i>ESM Group1 Interrupt (NERROR_IN_SYNC) Seen as Pending by User Application – Can Lead to Interrupt if Unmasked</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0 and IWR1443 ES2.0
<b>Description:</b>	ESM Group1 interrupt will be seen as pending when the control is passed to the application due to a missing configuration in device bootloader.
<b>Workaround(s):</b>	User application should keep the error masked.
<b>MSS#13</b>	<b><i>Incorrect Read from FFT Hardware Accelerator After Complex Multiplication Operation</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	Read-back from FFT hardware accelerator slave, static configuration registers, Window RAM, Param RAM, and First stage RAM gives incorrect data if the last operation performed by the accelerator was a complex multiplication.
<b>Workaround(s):</b>	None.



<b>MSS#14</b>	<b><i>Asynchronous Assertion of SoC Warm Reset may not Work Reliably When Device Operating on PLL Clock</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0 and IWR1443 ES2.0
<b>Description:</b>	Asynchronous assertion of SoC warm reset through WARM_RESET pin, SW reset, watchdog reset, or Debug reset may not reliably work and may also result in a system hang scenario.
<b>Workaround(s):</b>	MSS VCLK must be switched from PLL clock to REFCLK by following the prescribed software sequence before a warm reset is issued.
<b>MSS#15</b>	<b><i>The IWR14xx ES1.0 and ES2.0 Devices Only Work With Spansion and Macronix Devices</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0 and IWR1443 ES2.0
<b>Description:</b>	The IWR1443 ES1.0 and IWR1443 ES2.0 devices work only with Spansion and Macronix devices. In particular, the Flash variants that have been tested to work with the ROM bootloader are: <ul style="list-style-type: none"> <li>• Spansion S25FL256S, S25FL132K0XNFB010</li> <li>• Macronix MX25L3233F, MX25R1635FZNIH0 (Wide voltage part variant)</li> </ul>
<b>Workaround(s):</b>	In the next version of the Silicon ROM, the boot loader is expected to support a wide variety of flashes, with the prerequisite that Serial FLASH supports the SFDP command and responds with JEDEC compliant information regarding the capabilities and command set of the flash.
<b>MSS#19</b>	<b><i>DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	The MSS DMA generates a BER (Bus Error) interrupt when the DMA detects a bus error due to a read from unimplemented address space. This interrupt is available on VIM Interrupt Channel-70. This read from unimplemented address space results in a hang condition in the DMA infrastructure bridge that connects it to the main interconnect.  <i>Implication: A DMA read from an unimplemented address can result in a DMA hang condition. In the resulting state the DMA will not respond to any further DMA requests.</i>
<b>Workaround(s):</b>	The anomalous nERROR toggle would need to be ignored by the external monitoring circuit (if deployed).
<b>MSS#20</b>	<b><i>Radar Frame Stuck due to Missing Synchronizer Logic in Hardware</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	Radar Sub System Internal Frame Clock is triggered by rISensorStart API which starts the Radar Frame. Occasionally the rISensorStart API does not trigger the clock due to missing synchronizer logic in hardware.  <i>Implication: A DMA read from an unimplemented address can result in a DMA hang condition. In the resulting state the DMA will not respond to any further DMA requests.</i>

**Workaround(s):** The issue is frequent if FRC clock source is changed. Ensure that FRC Clock source is not changed.

**MSS#21A** *Issue with HWA Input Formatter 16 bit Real Signed Format*

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**Revision(s)  
Affected:** IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:** Wrong sign extension is implemented for 16 bit signed format in real only mode operation. Hence, signed 16-bit real format cannot be supported for input formatter.

**Workaround(s):** Don't use the 16 bit signed format in real only mode with HWA

**MSS#22**

***CAN-FD: Message Transmitted With Wrong Arbitration and Control Fields***

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**Revision(s)  
Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

Under the following conditions a message with wrong ID, format, and DLC is transmitted:

- M\_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission
- A new transmission is requested before the 3rd bit of Intermission is reached
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 Section 10.4.2.2)

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message
- The M\_CAN will start arbitration with wrong ID, format, and DLC on the next bit
- In case the ID wins arbitration, a CAN message with valid CRC is transmitted
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus, no error is detected by the transmitting M\_CAN

The erratum is limited to the case when M\_CAN is in state "Receiver" (PSR.ACT = "10") with no pending transmission and a new transmission is requested before the 3rd bit of Intermission is reached and this 3rd bit of intermission is seen dominant.

When a transmission is requested by the CPU, the Tx Message Handler performs an internal arbitration and loads the pending transmit message with the highest priority into its output buffer and then sets the transmission request for the CAN Protocol Controller. The problem occurs only when the transmission request for the CAN Protocol Controller is activated between the sample points of the 2nd and 3rd bit of Intermission and if that 3rd bit of intermission is seen dominant.

This dominant level at the 3rd bit of Intermission may result from an external disturbance or may be transmitted by another node with a significantly faster clock.

In the described case it may happen that the shift register is not loaded with arbitration and control field of the message to be transmitted. The frame is transmitted with wrong ID, format, and DLC but with the data field of the requested message. The message is transmitted in correct CAN (FD) frame format with a valid CRC.

If the message loses arbitration or is disturbed by an error, it is retransmitted with correct arbitration and control fields.

**Workaround(s):**

Request a new transmission only if another transmission is already pending or when the M\_CAN is not in state "Receiver" (when PSR.ACT ≠ "10").

Another option would be to add a checksum to the data field covering arbitration and control fields of the message to be transmitted.

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<b>MSS#23</b>	<b><i>HWA Read Registers Cannot be Read Reliably When the HWA is Executing a ParamSet Instruction</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	Any read from the HWA configuration or status registers can be corrupted, if the read access is performed when the HWA is active. Reads from the HWA registers can be performed correctly, only after the execution of the entire ParamSet (i.e., after the ACC_DONE_INTR interrupt) or when the HWA is in IDLE mode waiting for the trigger to start the execution of the next ParamSet instruction.
<b>Workaround(s):</b>	Perform the following: <ul style="list-style-type: none"><li>• Read-back of signature registers: Software needs to maintain a soft copy of the one-hot encoded signature registers and use that copy location for the EDMA programming.</li><li>• Read-back of static registers on the HWA ParamSet interrupt. There is no reliable way to read the HWA static registers, if the HWA is active.</li><li>• Read-back of Debug/status registers: The User can only read these registers when the HWA is <b>not</b> active.</li></ul>

<b>MSS#24</b>	<b><i>Limitation With Peak Grouping Feature in Hardware Accelerator</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	Peak is declared only if the cell under test is greater than its most immediate neighboring cells to its left and right. In the case where CFAR qualified peaks in the two adjacent cells happen to be equal in magnitude, enabling peak grouping can lead to the peak being lost.
<b>Workaround(s):</b>	Do not enable the peak grouping feature in the hardware accelerator.

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<b>MSS#25</b>	<b><i>Debugger May Display Unpredictable Data in the Memory Browser Window if a System Reset Occurs</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	<p>If a system reset (nRST goes low) occurs while the debugger is performing an access on the system resource using system view, a slave error should be replied to the debugger. If the access was a read, instead the response might indicate that the access completed successfully and return unpredictable data.</p> <p>This issue occurs under this condition: when a system reset is asserted (nRST low) on a specific cycle, while the debugger is completing an access on the system, using the system view. An example would be, when a debugger, like the CCS-IDE memory browser window, is refreshing content using the system view. This is not an issue for a CPU only reset and, this is not an issue during a power-on-reset (nPORRST) either.</p>
<b>Workaround(s):</b>	Avoid performing debug reads and writes while the device might be in reset.

**MSS#26**

***DMA Requests Lost During Suspend Mode***

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**Revision(s)  
Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

While the device is halted in suspend mode by the debugger, the DMA is expected to complete the remaining transfers of a block, if the DEBUG MODE bit field of the GCTRL register is configured to '01'. Instead, the DMA does not complete the remaining transfers of a block but, rather stops after two more frames of data are transferred. Subsequent DMA requests from a peripheral to trigger the remaining frames of a block can be lost.

This issue occurs only in the following conditions:

- The device is suspended by a debugger
- A peripheral continues to generate requests while the device is suspended
- The DMA is setup to continue the current block transfer during suspend mode with the DEBUG MODE bit field of the GCTRL register set to '01'
- The request transfer type TTYPE bit in the CHCTRL registers is set to frame trigger ('0')

**Workaround(s):**

**Workaround #1:**

Use TTYPE = block transfer ('1'), when the DEBUG MODE bit field is '01' (*finish current block transfer*)

**or**

**Workaround #2:**

Use the DMA DEBUG MODE = '00' (ignore suspend), when using TTYPE = frame transfer ('0') to complete the block transfer, even after suspend/halt is asserted.

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<b>MSS#27</b>	<b><i>MibSPI in Slave Mode in 3- or 4-Pin Communication Transmits Data Incorrectly for Slow SPICLK Frequencies and for Clock Phase = 1</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	<p>The MibSPI module, when configured in multibuffered slave mode with 3-functional pins (CLK, SIMO, SOMI) or 4-functional pins (CLK, SIMO, SOMI, nENA), could transmit incorrect data when all the following conditions are met:</p> <ul style="list-style-type: none"><li>• MibSPI module is configured in multibuffered mode,</li><li>• Module is configured to be a slave in the SPI communication,</li><li>• SPI communication is configured to be in 3-pin mode or 4-pin mode with nENA,</li><li>• Clock phase for SPICLK is 1, and</li><li>• SPICLK frequency is MSS_VCLK frequency / 12 or slower</li></ul>
<b>Workaround(s):</b>	<p>The issue can be avoided by setting the CSHOLD bit in the control field of the TX RAM (Multi-Buffer RAM Transmit Data Register). The nCS is not used as a functional signal in this communication; hence, setting the CSHOLD bit does not cause any other effect on the SPI communication.</p>



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<b>MSS#28</b>	<b><i>A Data Length Error is Generated Repeatedly in Slave Mode When IO Loopback is Enabled</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	When a DLEN error is created in Slave mode of the SPI using nSCS pins in IO Loopback Test mode, the SPI module re-transmits the data with the DLEN error instead of aborting the ongoing transfer and stopping. This is only an issue for an IOLPBK mode Slave in Analog Loopback configuration, when the intentional error generation feature is triggered using CTRLDLENERR (IOLPBKTSTCR.16).
<b>Workaround(s):</b>	After the DLEN_ERR interrupt is detected in IOLPBK mode, disable the transfers by clearing the SPIEN (bit 24) in the SPIGCR1 register and then, re-enable the transfers by resetting the SPIEN bit.

<b>MSS#29</b>	<b><i>Spurious RX DMA REQ From a Slave Mode MibSPI</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	<p>A spurious DMA request could be generated even when the SPI slave is not transferring data in the following condition sequence:</p> <ul style="list-style-type: none"><li>• The MIBSPI is configured in standard (non-multibuffered) SPI mode, as a slave</li><li>• The DMAREQEN bit (SPIINT0.16) is set to enable DMA requests</li><li>• The Chip Select (nSCS) pin is in an active state, but no transfers are active</li><li>• The SPI is disabled by clearing the SPIEN (SPIGCR1.24) bit from '1' to '0'</li></ul> <p>The above sequence triggers a false request pulse on the Receive DMA Request as soon as the SPIEN bit is cleared from '1' to '0'.</p>
<b>Workaround(s):</b>	Whenever disabling the SPI, by clearing the SPIEN bit (SPIGCR1.24), first clear the DMAREQEN bit (SPIINT0.16) to '0', and then, clear the SPIEN bit.

**MSS#30**

***MibSPI RX RAM RXEMPTY bit Does Not Get Cleared After Reading***

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**Revision(s)  
Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

The RXEMPTY flag may not be auto-cleared after a CPU or DMA read when the following conditions are met:

- The TXFULL flag of the latest buffer that the sequencer read out of transmit RAM for the currently active transfer group is 0,
- A higher-priority transfer group interrupts the current transfer group and the sequencer starts to read the first buffer of the new transfer group from the transmit RAM, and
- Simultaneously, the Host (CPU/DMA) is reading out a receive RAM location that contains valid received data from the previous transfers.

**Workaround(s):**

If at all possible, avoid transfer groups interrupting one another.

If dummy buffers are used in lower-priority transfer groups, select the appropriate "BUFMODE" for them (like, SKIP/DISABLED) unless, there is a specific need to use the "SUSPEND" mode.

<b>MSS#31</b>	<b><i>CPU Abort Generated on a Write to Implemented CRC Space After a Write to Unimplemented CRC Space</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	An abort could be generated on a write to a legal address in the address offset region (0x0000–0x01FF) of the CRC register space when a normal mode write to an unimplemented address region (0x0200–0xFFFF) of the CRC register space is followed by a write to a legal address region (0x0000–0x01FF) of the CRC register space.
<b>Workaround(s):</b>	None.

**MSS#32**

***DMMGLBCTRL BUSY Flag Not Set When DMM Starts Receiving A Packet***

---

**Revision(s)  
Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

The BUSY flag in the DMMGLBCTRL register should be set when the DMM starts receiving a packet or has data in its internal buffers. However, the BUSY flag (DMMGLBCTRL.24) may not get set when the DMM starts receiving a packet under the following condition:

- The BUSY bit is set only after the packet has been received, de-serialized, and written to the internal buffers. It stays active while data is still in the DMM internal buffers. If the internal buffers are empty (meaning that no data needs to be written to the destination memory) then, the BUSY bit will be cleared.

**Workaround(s):**

Wait for a number of DMMCLK cycles (for example, 95 DMMCLK cycles) beyond the longest reception and deserialization time needed for a given packet size and DMM port configuration, before checking the status of the BUSY flag, and after the DMM ON/OFF bit field (DMMGLBCTRL.[3:0]) has been programmed to OFF.

<b>MSS#33</b>	<b><i>MibSPI RAM ECC is Not Read Correctly in DIAG Mode</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	A Read operation to the ECC address space of the MibSPI RAM in DIAG mode, does not return the correct ECC value for the first 128 buffers, if the Extended Buffer support is implemented but, the Extended Mode is disabled for the particular MibSPI instance.
<b>Workaround(s):</b>	None.

**MSS#35**

***EDMA TPTC Generates an Incorrect Address on the Read Interface, Causing one or More Data Integrity Failures, Hangs, or Extra Reads***

**Revision(s) Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

Certain scenarios could lead to an incorrect read, hang, or data integrity issues in the EDMA TPTC block. [Table 6-1](#) shows the various scenarios and the resulting effects of each scenario.

A scenario happens, if *ALL* conditions listed for that scenario are satisfied (true); that is, "AND" of all conditions.

A "hang" outcome means that one or more attempts of the hang causing scenarios can progressively lead to not receiving a "transfer completion" indication from the TPTC. The last transfer attempt which does not receive the completion indication can be any transfer – any scenario transfer within this advisory or even outside of this advisory.

**Table 6-1. EDMA TPTC Scenario IDs and Condition Results**

SCENARIO ID	CONDITIONS	DATA INTEGRITY FAILURES	HANGS	EXTRA READS
1	AB-sync BCNT > 1 ACNT not in [2,4,8,16,32] (ACNT < 64) OR ((ACNT = 64) AND (SRCBIDX != ACNT)) Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers.	Yes (see <a href="#">Figure 6-4</a> )	Possible	Possible
2	AB-sync with BCNT=1 or A-sync ACNT not in [2..24, 32] ACNT <= 64 Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers.	No	Possible	Yes
3	AB-sync with BCNT=1 or A-sync ACNT in [2..24, 32] Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers.	No	No	Yes (see <a href="#">Figure 6-1</a> )
4	AB-sync BCNT > 1 ACNT in [2,4,8,16,32] SRCBIDX = ACNT ACNT * BCNT <=64 Source Addressing crossing 4-KB boundary for any of the BCNT number of ACNT transfers.	No	No	Yes (see <a href="#">Figure 6-2</a> )
5	AB-sync BCNT > 1 ACNT in [2,4,8,16,32] SRCBIDX = ACNT ACNT * BCNT <=64 Source Addressing <i>does NOT</i> cross 4-KB boundary for any of the BCNT number of ACNT transfers; that is, NOT of Source Addressing crosses 4-KB boundary for merged source array of size ACNT * BCNT.	No	No	Yes (see <a href="#">Figure 6-3</a> )

Source Addressing crossing 4-KB boundary cross **condition [1]** in [Table 6-1](#) is defined as follows:

$$[X(i) = \text{LSB}_{12\text{bits}}(\text{SRC\_ADDR} + i * \text{SRC\_BIDX})] + \text{ACNT} > 0x1000$$

where  $0 \leq i < \text{BCNT}$

Source Addressing crossing 4-KB boundary cross **condition [2]** in [Table 6-1](#) is defined as follows:

$$\text{LSB}_{12\text{bits}}(\text{SRC\_ADDR}) + (\text{ACNT} * \text{BCNT}) > 0x1000$$

For the and expressions above, note that the SRC\_ADDR is candidate source address considering the C-dimension. If CCNT > 1, then, the SRC\_ADDR would be every candidate source address for all CCNTs depending on the type of transfer and the SRCCIDX.

For each extra read in **Scenario ID #3** for which [Condition \[1\]](#) is applicable, each index i above that satisfies the condition results in extra read from starting address SRC\_ADDR + (i + 1) \* SRCBIDX and of length equal to the distance from the start address to the boundary [that is, 0x1000 – X(i)]. Note: length < ACNT.

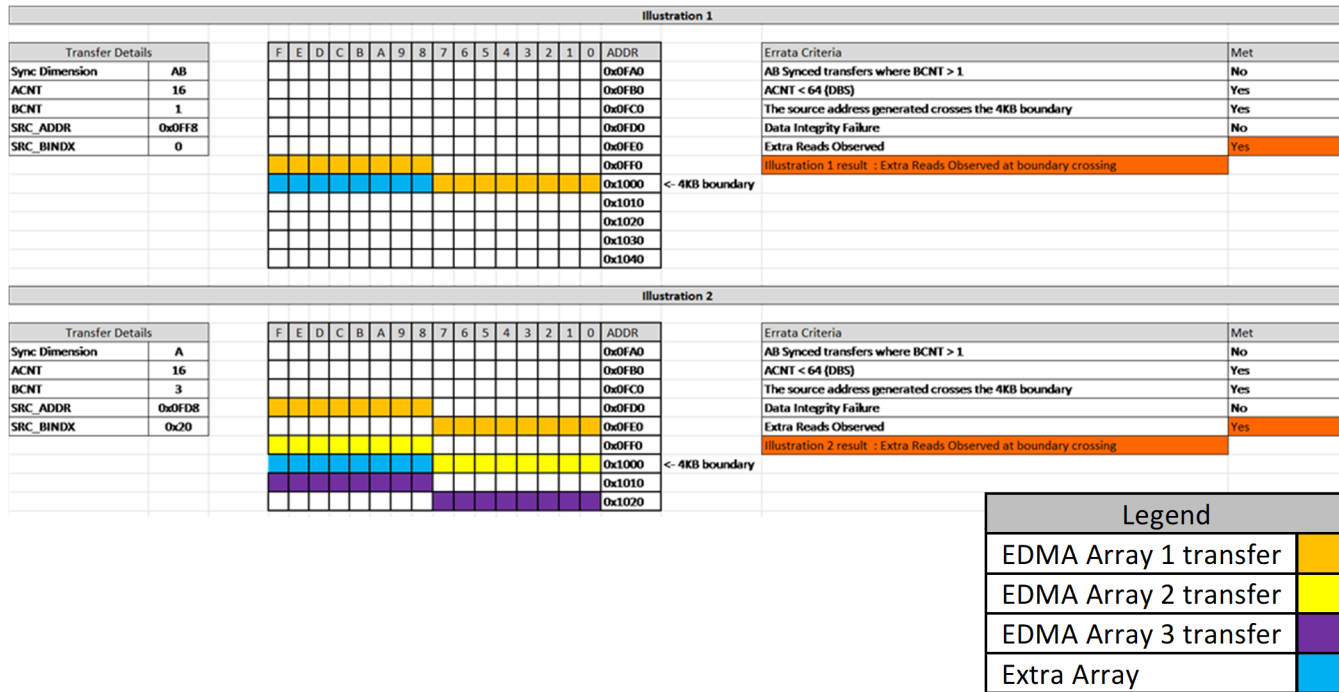


Figure 6-1. Scenario ID #3 – Extra Reads



For each extra read **Scenario ID #4** in for which **Condition [1]** is applicable, there is an extra read from starting address SRC + BCNT \* ACNT (=SRCBIDX) of length equal to the distance of the start address to the boundary [that is, length is 0x1000 – X(i)], where i is the index of one and only 4-KB boundary crossing condition. Note: length < ACNT.

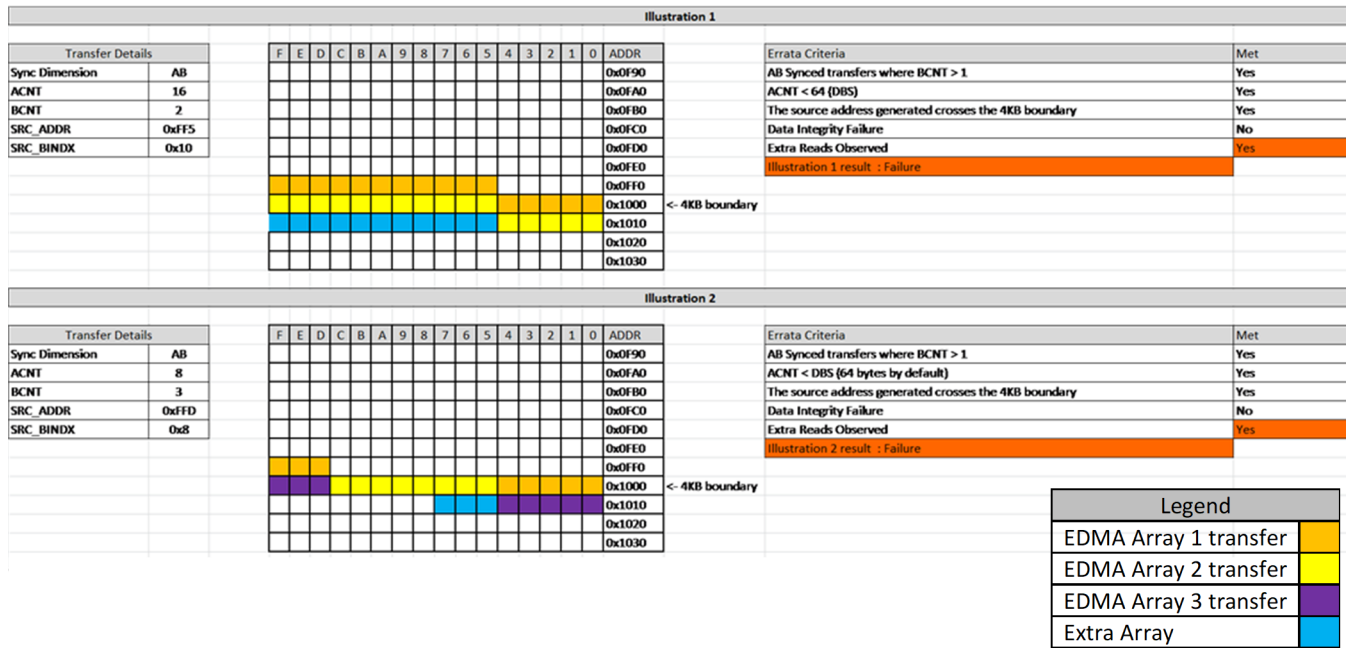


Figure 6-2. Scenario ID #4 – Extra Reads

For the extra read **Scenario ID #5** in for which **Condition [2]** is applicable, there is an extra read from starting address SRC + BCNT \* ACNT (=SRCBIDX) of length equal to the distance of the start address and is of length ACNT.

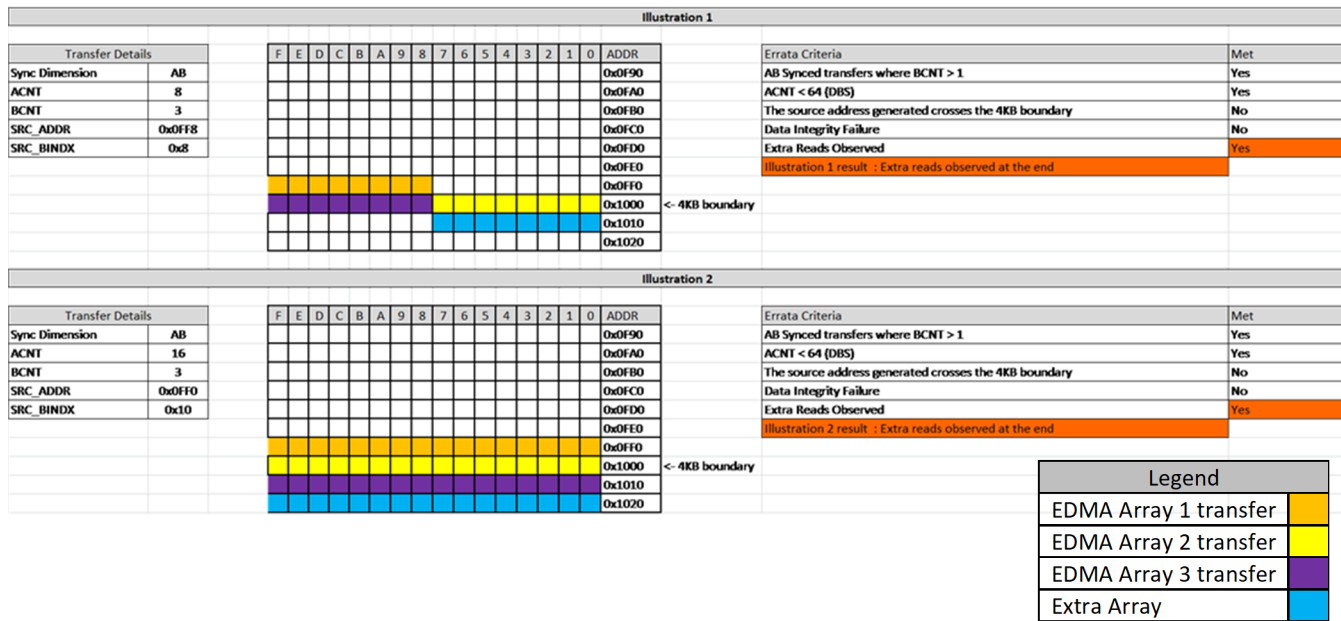


Figure 6-3. Scenario ID #5 – Extra Reads

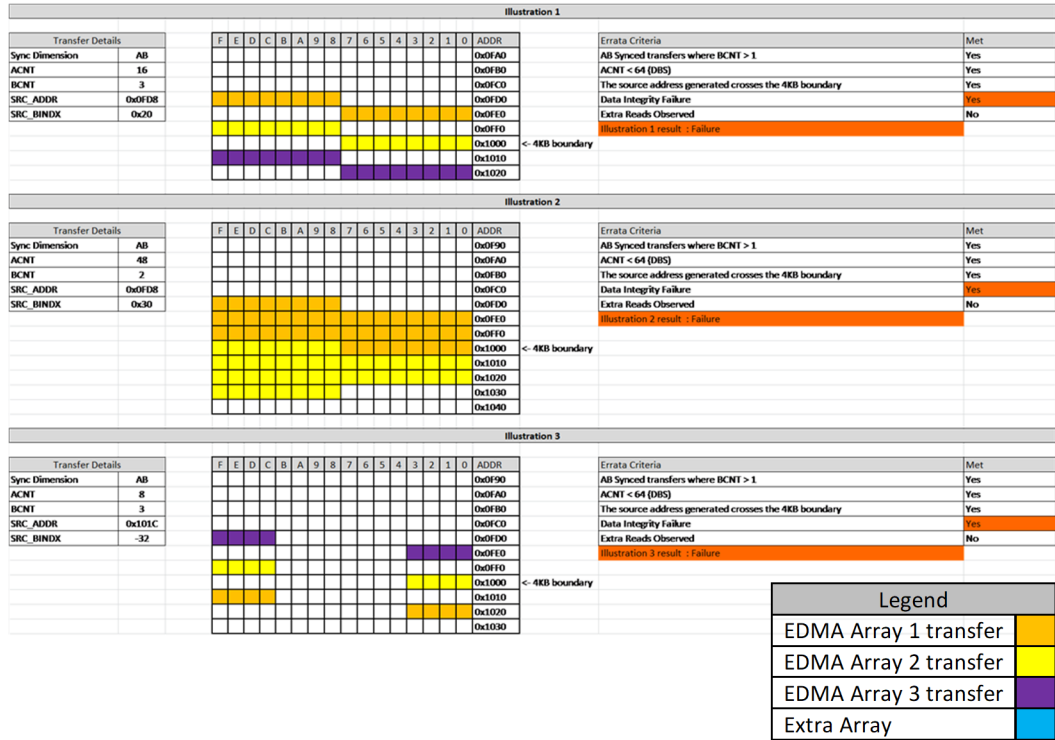


Figure 6-4. Scenario ID #1 – Data Integrity Failure

Workaround(s): **Workaround #1 - ALL SCENARIO IDs (see Table 6-1)**

Prevent one or more of the conditions necessary for the problematic scenarios to happen.

**Workaround #2 - Scenario ID #3, Scenario ID #4, and Scenario ID #5 (see Table 6-1)– EXTRA READS**

For **Scenario ID #3, Scenario ID #4, and Scenario ID #5**– EXTRA READS, another workaround besides avoiding the 4-KB boundary cross conditions, is to ensure that buffers involved in this kind of transfer are positioned so that extra reads stay within the physical memory boundaries. If the extra reads go to Reserved space or space blocked by the Memory Protection Unit (MPU), the TPTC generates a bus error interrupt to the processor.

**MSS#37B*****DCC Module Frequency Comparison can Report Erroneous Results***

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**Revision(s)  
Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

The Dual-clock Comparator module, which is used to monitor a clock frequency while comparing with a known clock reference, could stop earlier than expected, and, thus, indicating the measured clock frequency to be lower. This is due to a clock domain crossing issue causing a preset to the error detection logic to get triggered.

**Workaround(s):**

Multiple measurements can be taken for the same clock pairs and abnormal frequencies reported can be ignored

Application code, where possible, could compare the clocks using an alternate clock comparator module (CCC).

**MSS#38A**

***GPIO Glitch During Power-Up***

---

**Revision(s)  
Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

During the 3.3-V supply ramp, the GPIO outputs could possibly see a short glitch (*rising above the 0 V for a short duration*), if the 3.3V supply powers up before the 1.8V supply. This GPIO glitch cannot be avoided by just a pulldown resistor. If the GPIO glitch during boot-up is high enough, it could be falsely detected as a “high”.

**Workaround(s):**

Powering up the 1.8V supply before the 3.3V supply resolved the issue. In case that is not feasible, AND the GPIO is used for critical controls where glitch cannot be tolerated, the GPIO output should be gated by the nRESET signal of the xWR device.

Using a tri-state buffer (for example: SN74LVC1G126-Q1) externally to isolate the GPIO output from the system until the nRESET of xWR device is released. At this point, all the supplies are expected to be stable.

<b>MSS#39</b>	<b><i>The state of the MSS DMA is left pending and uncleared on any DMA MPU fault</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	<p>The state of the MSS DMA is left pending and uncleared on any DMA MPU fault. The transfer that caused this MPU fault is left pending inside the DMA IP.</p> <p>Any trigger on DMA REQ lines (could be caused by any module/IP that is hooked up to DMA in h/w) can re-trigger DMA to start executing the above pending transfer irrespective of whether that trigger is actually valid/enabled in DMA or that module/IP</p>
<b>Workaround(s):</b>	<p>For devices where the Boot ROM is executing the MSS DMA MPU Self tests. As part of application initialization, if the MSS DMA will be used, the following register field should be used to reset the MSS DMA IP so that the uncleared transfer is reset</p> <ol style="list-style-type: none"><li>1. Write MSS_RCM:SOFTTRST1[31:24] 0xAD</li><li>2. Write MSS_RCM:SOFTTRST1[31:24] 0x0</li></ol> <p>It is not recommended to use this configuration at any another instance other than that recommended here in this Errata.</p> <p>On an actual Real time MPU Error, this error should be treated as a non-recoverable error and a warm reset should be issued to recover.</p>

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**MSS#40**                    ***Any EDMA Transfer That Spans ACCEL\_MEM1 +ACCEL\_MEM2 Memories of Hardware Accelerator May Result In Data Corruption Without Any Notification Of Error From The SoC***

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**Revision(s)  
Affected:**                    IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**                    As per TPTC IP Spec, a Transfer request (TR) is supposed to access a single slave end point. ACCEL\_MEM0/ACCEL\_MEM1 memory banks of HWA are available via single slave point and ACCEL\_MEM2/ ACCEL\_MEM3 memory banks of HWA are available as another slave point (different from that of ACCEL\_MEM0/ ACCEL\_MEM1). Hence if a single TR is used to access a buffer spanning ACCEL\_MEM1 and ACCEL\_MEM2 memories of the HWA (i.e. a single buffer spanning 2 different slave points), the spec is not being adhered to. This errata is explicitly highlighting this spec requirement

**Workaround(s):**                    Split the access into 2 TRs so that a single TR does not span ACCEL\_MEM1 +ACCEL\_MEM2. The 2 TRs can be chained.

<b>MSS#43A</b>	<b><i>Read-data from internal registers of PCR is not reliable. Shared PCS region protection is also not supported</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, ES2.0 and ES3.0
<b>Description:</b>	<p>The main subsystem has PCR interconnect that manages the accesses to the peripheral registers and peripheral memories, and provides a global reset for all peripherals. The read-data from PCR is getting corrupted before handing it of to VBUSP interconnect. So any partial write to PCR-registers is not reliable. Peripheral access is blocked by writing to internal registers which is not feasible.</p> <p>Shared PCS region protection is also not supported</p>
<b>Workaround(s):</b>	No workaround



<b>MSS#44</b>	<b><i>SYNC IN input pulse wider than 4usec can cause a FRC lockstep error</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, ES2.0 and ES3.0
<b>Description:</b>	In hardware based frame triggered mode of operation, external SYNC IN pulse is provided to the radar device. If the width of the pulse is > 4usec, it could cause MSS ESM group 1 fault with FRC lockstep error.
<b>Workaround(s):</b>	The pulse width of the external SYNC IN signal should be >25nsec and < 5usec

**MSS#45*****Bootup failure during the serial flash busy state***

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**Revision(s)  
Affected:**

IWR1443 ES1.0, ES2.0 and ES3.0

**Description:**

If the radar device is rebooted internally or externally while the serial flash is busy completing a previous operation, like erase, format etc, the radar device might fail to bootup since the serial flash would not respond to the commands from the bootloader during the bootup process.

**Workaround(s):**

The user application should make sure if its triggering an internal reset due to watch dog expiry or other reasons, it should reset the serial flash to bring it to a known state or wait for completion of any pending issued commands to serial flash before it resets the XWR device.

<b>ANA#01</b>	<b>Noise Figure Degradation</b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0
<b>Description:</b>	Due to board limitation current typical Noise figure number is 18dB.
<b>Workaround(s):</b>	None. Silicon update will be provided by TI.
<b>ANA#02</b>	<b>VCO#1 [76-77GHz] Minimum Frequency Falls Short of Target</b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0
<b>Description:</b>	The supported frequency range is 77 GHz to 81 GHz (using VCO2).
<b>Workaround(s):</b>	None. Silicon update will be provided by TI.
<b>ANA#03</b>	<b>Spurs from LVDS Output Coupling into Synthesizer</b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0
<b>Description:</b>	For the characterization, the LVDS interface is used. In this mode, there is a package coupling to crystal oscillator pins causing spurs in LO (hence it comes out in IF spectrum).
<b>Workaround(s):</b>	None.

<b>ANA#04</b>	<b><i>Receiver Gain Range Availability</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0
<b>Description:</b>	The supported receiver gain range is 18dB (versus a specification target of 24dB).
<b>Workaround(s):</b>	None.
<b>ANA#06</b>	<b><i>Return Loss Measurement on TX: S11 &lt; -9dB, RX S11 &lt; -6.5dB (Accepted Value of &lt; -10dB)</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0
<b>Description:</b>	The return loss measurement on TX S11 is < -9dB and the return loss measurement on RX S11 is < -6.5dB. The accepted value is < -10dB.
<b>Workaround(s):</b>	None. TI expects to provide an update along with the next silicon revision.
<b>ANA#07</b>	<b><i>CSI2 Activity Coupling to Clock</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0 and IWR1443 ES2.0
<b>Description:</b>	The activity on the CSI lines during the state transitions at the start and at the end of CSI transfer couples into the clock leading to glitches in the TX output.
<b>Workaround(s):</b>	<p>Increase the idle time between chirps such that the "start of transfer" and "end of transfer" occur during the idle time between two chirps.</p> <ol style="list-style-type: none"> <li>The IWR1443 eDMA sends data from ADCBuffer to High Speed Peripheral. At the start of each chirp, CSI-2 changes from Low Power Mode to Standard Mode output. At the completion of the chirp, CSI-2 goes back from Standard mode to Low Power Mode output. When CSI-2 changes mode, there is a clock contamination of the ADC subsystem. In order to not contaminate the measurement, the CSI-2 data Output must be finished before the end of the idle time chirp parameter.   <math display="block">\text{Bitrate\_perChirp\_perLane} = (\text{numRxch} * \text{DFEoutrate} * (\text{numDFEsamples/chirp}) * (\text{complexmode}+1) * (\text{numbits/sample}[12,14,16]) / (\text{numLanes})</math> <math display="block">\text{perChirp\_Outperiod} = \text{Bitrate\_perChirp\_perLane} / (\text{DDC\_Clkrate} * 2)</math> <math display="block">\text{IdleTime} = \text{MAX}(\text{Synthesizer\_IdleTime}, \text{perChirp\_Outperiod})</math> <p>Note: Synthesizer_IdleTime can be calculated in the mmWave Sensing Estimator.</p> </li> <li>If the customer uses the LVDS High Speed output format, this ADC clock disturbance is not seen.</li> </ol>

**ANA#08A**

***Doppler Spur Observed at Certain RF Frequencies***

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**Revision(s)  
Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

When the instantaneous FMCW Ramp frequency nears certain specific RF frequencies, there can be coupling between the synthesizer's reference and its output, and manifest as frequency glitches or spurs in TX output spectrum.

*Implication:* In FMCW radar 2D signal processing, this can lead to spurs in a fixed Doppler bin at all range bins. This situation can occur with narrow band chirps, if the FMCW ramp includes or nears 76.8-, 77.4-, 78-, 79.2-, 80.4-, 81-GHz RF frequencies. The affected Doppler bin is a function of chirp timing and RF frequency properties.

**Workaround(s):**

Use the device's dithering features to vary idle time, RF frequency and ramp end times to spread the spurs significantly in Doppler dimension so that it does not get detected as spurious targets. Using larger chirp band widths also reduces the spur level.

**ANA#10A**

***Unreliable Readings from Synthesizer Supply Voltage Monitor***

---

**Revision(s)  
Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

During monitoring, the thresholds used to determine if the synthesizer supply voltage is within limits are much stricter than necessary for proper circuit operation. This can lead to occasional, erroneous reporting of supply failures even when there is no adverse impact on circuit or system behavior.

*Implication:* The user cannot rely on supply failure indication from the supply monitors of PM, Clock and LO subsystems. The affected field is STATUS\_SUPPLY\_PMCLKLO in the monitoring report message: AWR\_MONITOR\_PMCLKLO\_INTERNAL\_ANALOG\_SIGNALS\_REPORT\_AE\_SB.

**Workaround(s):**

Ignore the field STATUS\_SUPPLY\_PMCLKLO in the monitoring report message: AWR\_MONITOR\_PMCLKLO\_INTERNAL\_ANALOG\_SIGNALS\_REPORT\_AE\_SB.

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<b>ANA#11A</b>	<b><i>TX, RX Calibrations Sensitive to Large External Interference</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, ES2.0 and ES3.0
<b>Description:</b>	External interference present on the RX or TX pins, during the period of the device calibration at Rflnit, can lead to degraded accuracy or errors in the calibration results. If the interference changes its level while these calibrations are actively running, the calibration algorithm may interpret this as a change in signal power, leading to incorrect convergence. This applies to boot-time PD, Rx IQ mismatch calibration, Rx gain calibration, Tx power calibration, and phase-shifter calibration. It also impacts run-time Tx output power calibration in CLPC mode.
<b>Workaround(s):</b>	<b>Workaround #1:</b> <p>The incident power detector in the TX output power detector, along with the absolute level of the PA loopback used during the PA loopback monitors, are insensitive to this, and they can be used to check that the calibrations converged correctly. Calibration can be re-run if large interference was observed.</p> <b>Workaround #2:</b> <p>Another workaround is to save the boot time calibrations at production (done in a clean environment without interference) and during operation, the calibrations can be restored. For the runtime Tx output power calibrations, OLPC mode can be used instead of the CLPC mode.</p>

**ANA#12A**
***Second Harmonic (HD2) Present in the Receiver***


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**Revision(s)  
Affected:**

IWR1443 ES1.0, ES2.0 and ES3.0

**Description:**

There is a finite isolation between the RF pins/package and the FMCW synthesizer. This can create spurious tones at the synthesizer output and lead to appearance of 2nd order harmonics and inter-modulations of expected IF frequencies at RX ADC output. The amplitude of the 2nd harmonic could be as high as -55 dBc , referenced to the power level of the intended tone at the LNA input.

**Workaround(s):**

No workaround available at this time. However, in many typical radar use-cases the HD2 does not affect the system performance due to two reasons:

1. Since the HD2 comes from a coupling to the LO signal, there is an inherent suppression of the HD2 level due to the self-mixing effect (that is, phase noise and phase spur suppression effect at the mixer).
2. In real-life scenarios there is often a double-bounce effect of the radar signal reflected from the target, which leads to a ghost object at twice the distance of the actual object. This effect is often indistinguishable from the effect of HD2 itself.

**ANA#13B**
***TX1 to TX3 Phase Mismatch Variation over Temperature is Double that of TX2/TX1 and TX3/TX2 Combinations***


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**Revision(s)  
Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

TX3/TX1 combination exhibits a phase mismatch variation of  $\pm 6^\circ$  from  $-40^\circ\text{C}$  to  $105^\circ\text{C}$  whereas, TX2/TX1 and TX3/TX2 combinations exhibit a lower variation of  $\pm 3^\circ\text{C}$  over the same temperature range

**Workaround(s):**

In applications requiring high phase accuracy across TX channels, a background angle calibration or a 2-point calibration can be used to control phase variation over temperature.

<b>ANA#15</b>	<b><i>Excessive TX-RX Coupling or Reflection can Lead to Saturated RX Output</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	If there is excessing TX-RX coupling or chassis reflection, it can lead to a saturated RX output. This situation can occur if the RX input is stronger than -10dBm.
<b>Workaround(s):</b>	Improve TX-to-RX antenna isolation on PCB. Radome/chassis should give low reflection amplitude and should be as close as possible to the sensor, to reduce the IF frequency.



**ANA#16**

***LVDS Coupling to Clock System***

---

**Revision(s)  
Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

The digital activity in the High-Speed Serial Interfaces (HSI) state machine can couple to the clock system/FMCW synthesizer and can cause spurs in its clock output. The spur frequency is HSI rate dependent (for example, for a 600-MHz HSI clock rate, 6.25-MHz and 12.5-MHz spurs can be observed on TX/RX output, and for a 900-MHz HSI clock rate, 7-MHz and 14-MHz spurs can be observed on the TX/RX output). The spur levels are low (*near or below -65 dBc*).

**Workaround(s):**

The spur will not be present, when the LVDS is not used.

<b>ANA#17A</b>	<b><i>On-Board Supply Ringing Induced Spur</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, ES2.0 and ES3.0
<b>Description:</b>	Turning OFF and ON front-end modules can cause on-board supply ringing and slow the settling of the power supply. This supply ringing can manifest as a spur (~130KHz) in the FMCW synthesizer output spectrum.
<b>Workaround(s):</b>	<b>Workaround #1:</b> Disable inter-chirp duty cycling of the RX.  <i>or</i> <b>Workaround #2:</b> Design the power supply to damp out the ringing on the rails to the device.

**ANA#18B**

***Spurs Caused due to Digital Activity Coupling to XTAL***

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**Revision(s)  
Affected:**

IWR1443 ES1.0, ES2.0 and ES3.0

**Description:**

Digital filtering activity can potentially couple to XTAL pins and lead to spurs in the LO, which would also be seen in the Rx data. The spur in the Rx data would be seen at the spur frequency offset around a strong object. For example if the spur frequency is 500Khz and there is a strong object at 2Mhz , the Rx ADC spectrum could have a spike at 1.5Mhz or 2.5Mhz. Note that the Tx – Rx antenna coupling would also form a strong object close to DC. The spur frequency depends on the sampling rate ( $F_s$ ). The strongest of these spurs have been observed when  $F_s$  is close to 10, 12.5, 18, 18.75,20, 25, Msp. In these ranges, an IF spur can appear at  $F_s-10$  Mhz,  $2F_s-40$ MHz,  $4F_s-40$  MHz,  $4F_s-100$  MHz,  $8F_s-100$  MHz ,  $2F_s-37.5$  MHz,  $2F_s-36$  MHz. The spur is observable when the spur frequency falls within 1.5 MHz, beyond that it gets heavily filtered out. Please refer the device datasheet for max usable sampling rate.

**Workaround(s):**

**Workaround #1:**

Avoid sampling rates close to these numbers (10, 12.5, 18, 18.75, 20, 25 Msp) or use exactly these numbers (spur is at 0 Hz in the latter case).

**Workaround #2:**

Using external TCXO, instead of XTAL, with voltage swing between 1.4-1.8 Vpp can avoid these spurs.

<b>ANA#20</b>	<b><i>Occasional Failures Observed During Calibration of the Radar Subsystem</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	Rare occurrences of failures have been observed in the Dual-Clock Comparator (DCC) module, as a result the APLL or Synthesizer may report a failure.
<b>Workaround(s):</b>	<b>Workaround #1:</b> Any APLL calibration failure needs to be responded with a reset cycle. <i>or</i> <b>Workaround #2:</b> Any SYNTH calibration failure reported by the BSS will require an RFinIt.

**ANA#21A**

***Out of Band Radiated Spectral Emission***

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**Revision(s)  
Affected:**

IWR1443 ES1.0, ES2.0 and ES3.0

**Description:**

Out-of-band radiated spectral emissions are observed at 14.4-GHz and 28.8-GHz.

**Workaround(s):**

A grounded metallic shield around the device (excluding the antenna region) can be used to reduce the emission levels. Microwave absorber materials could also be placed on the device to reduce the emissions.

<b>ANA#22A</b>	<b><i>Overshoot and Undershoot During Inter-Chirp Idle Time</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, ES2.0 and ES3.0
<b>Description:</b>	At the end of the chirp , when the synthesizer starts to go back to the start frequency of the next chirp, there is some overshoot and undershoot. The undershoot/overshoot is proportional to the chirp bandwidth. Negative slope chirps have a worse undershoot than positive slope chirps.
<b>Workaround(s):</b>	To ensure the TX power amplifier is OFF during chirp idle time and not causing "on-air" emissions during the undershoot/overshoot period, keep the inter-chirp power savings ON.

**ANA#24A**

***40-MHz OSC CLKOUT Causing Spurs in 2D-FFT Spectrum***

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**Revision(s)  
Affected:**

IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

**Description:**

Harmonics of 40 MHz from osc-clkout can be coupled onto the synthesizer and can cause low amplitude spurs in the 2D-FFT spectrum. These spurs are at fixed doppler bin, across all range bins.

**Workaround(s):**

For single chip usecases, where OSC CLKOUT is not used , OSC CLKOUT output can be disabled.

<b>ANA#27</b>	<b><i>Digital Temperature Sensor Having Higher Error</i></b>
<b>Revision(s) Affected:</b>	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
<b>Description:</b>	Due to the single-ended nature of the digital temperature sensors, as compared to the differential design of analog temperature sensors (that is, TX, RX, and PM), it is vulnerable to noise and can have higher error than the analog temperature sensors.
<b>Workaround(s):</b>	Use only the analog temperature sensor values (TX and RX) in the algorithm. The digital temperature sensor value can be ignored.



## 7 Trademarks

All trademarks are the property of their respective owners.

## 8 Revision History

### Changes from October 31, 2018 to May 31, 2021 (from Revision B (October 2018) to Revision C (May 2021))

	Page
• <b>(Advisory to Silicon Variant / Revision Map):</b> Added ANA#10A, ANA#12A, ANA#13B, ANA#15 through ANA#18B, ANA#20, ANA#21A, ANA#22A, ANA#24A, ANA#27 advisories under Analog / Millimeter Wave, all silicon revisions.....	5
• <b>(Advisory to Silicon Variant / Revision Map):</b> Added MSS#20, MSS#22 through MSS#33, MSS#35, MSS#37B, MSS#38A through MSS#40 and MSS#43A through MSS#45 and removed MSS#2 advisories under Main Subsystem, all silicon revisions.....	5
• <b>(Advisory to Silicon Variant / Revision Map):</b> Updated/modified ANA#8A, ANA#11A, MSS#3A, MSS#4A, MSS#5A, MSS#7A and MSS#21A advisories under Analog / Millimeter Wave and Main Subsystem, all silicon revisions.....	5

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