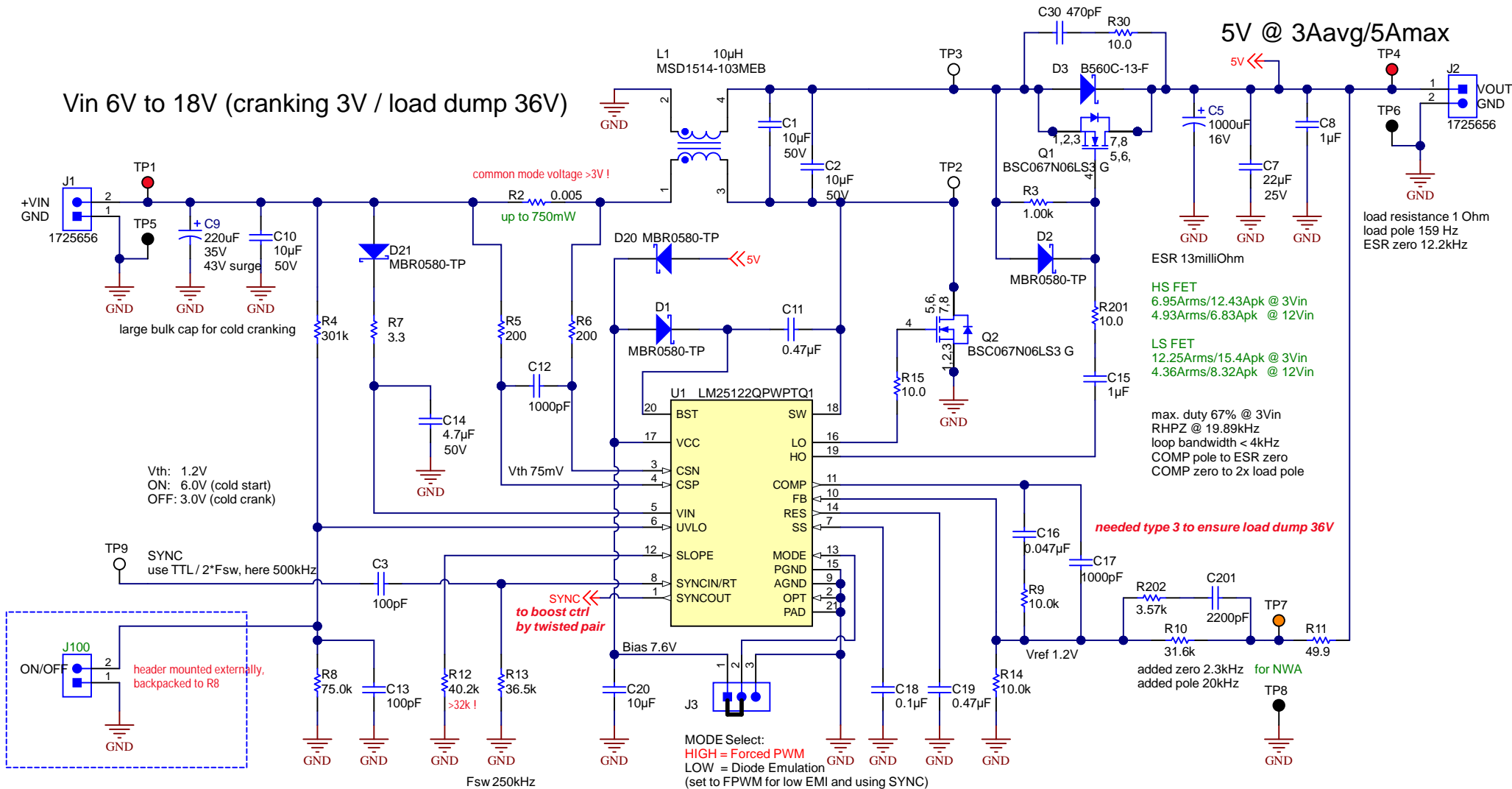


Vin 6V to 18V (cranking 3V / load dump 36V)

5V @ 3Aavg/5Amax



Vth: 1.2V
ON: 6.0V (cold start)
OFF: 3.0V (cold crank)

common mode voltage >3V!
up to 750mW

ESR 13milliOhm
HS FET
6.95Arms/12.43Apk @ 3Vin
4.93Arms/6.83Apk @ 12Vin

LS FET
12.25Arms/15.4Apk @ 3Vin
4.36Arms/8.32Apk @ 12Vin

max. duty 67% @ 3Vin
RHPZ @ 19.89kHz
loop bandwidth < 4kHz
COMP pole to ESR zero
COMP zero to 2x load pole

needed type 3 to ensure load dump 36V

SYNC
to boost ctrl
by twisted pair

MODE Select:
HIGH = Forced PWM
LOW = Diode Emulation
(set to FPWM for low EMI and using SYNC)

Fsw 250kHz

Revision History	
Revision	Notes
A	*** preliminary *** (cold start needs Vin > 6V)
B	used LL FETs to avoid charge pump of RevA
C	adjusted loop, optimized gate drive

- 1) automotive FETs IAUC41N06S5L 100 for short term cranking and output current <3Aavg - upper BSCs for prototyping only
- 2) R201, R202, C201 mounted externally; C31 OPEN

built on PCB 30232 A

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Orderable:	Designed for: Public Release	Mod. Date: 2/23/2022
TID #: N/A	Project Title: 25W sync SEPIC for 3V Cold Cranking	
Number: PMP31114	Rev: C	Sheet: 1 of 2
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Size: A4
Drawn By:	File: PMP31114RevC_sh1_SEPIC.SchDoc	
Engineer: B. Geck	Contact: http://www.ti.com/support	http://www.ti.com

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