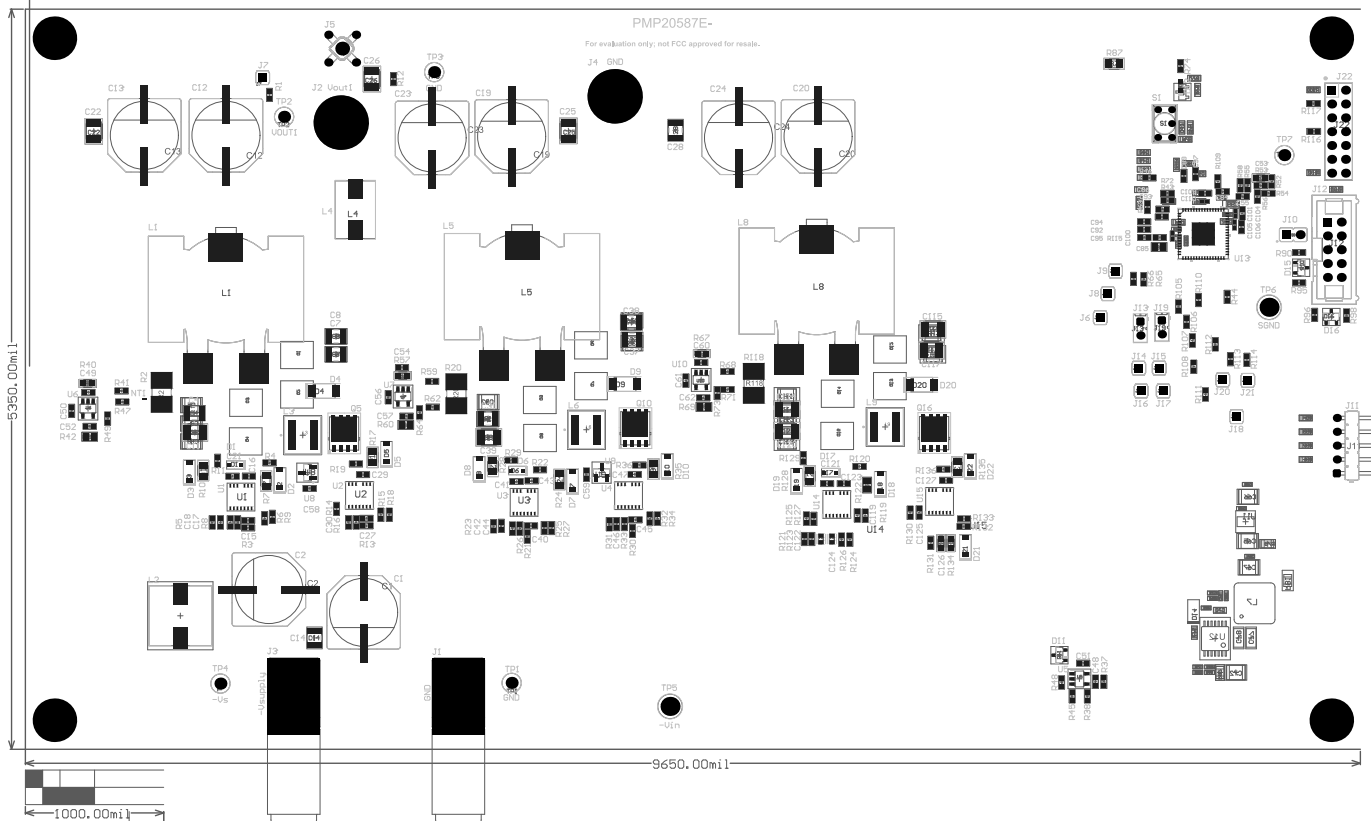
Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL: [ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED

ASSEMBLY VARIANT: 001

LAYER NAME = Assembly Bottom

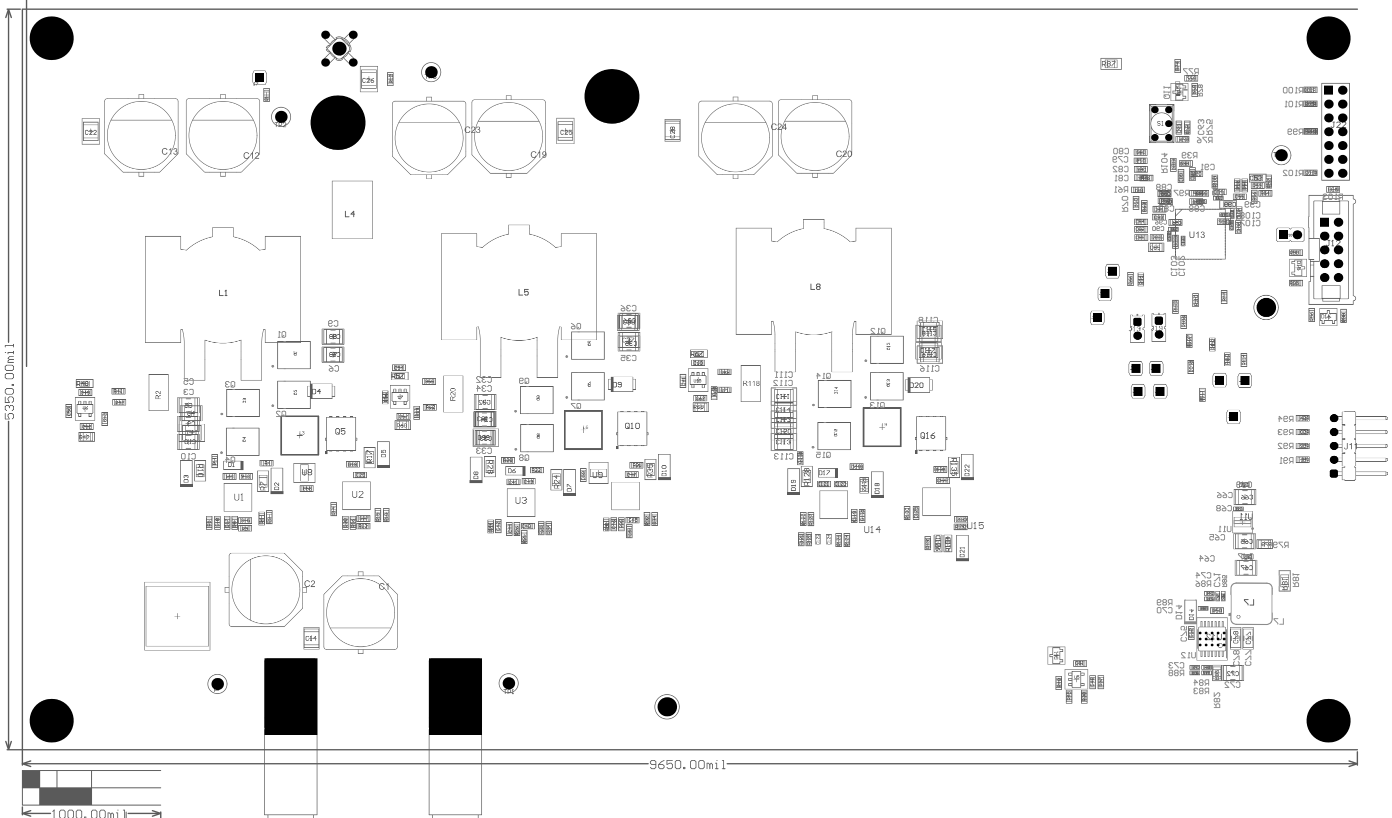
PLOT NAME: Assembly Bottom

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: ☐ FR-408 ☒ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2 ☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2 ☐ OTHER +/-

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG ☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE ☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

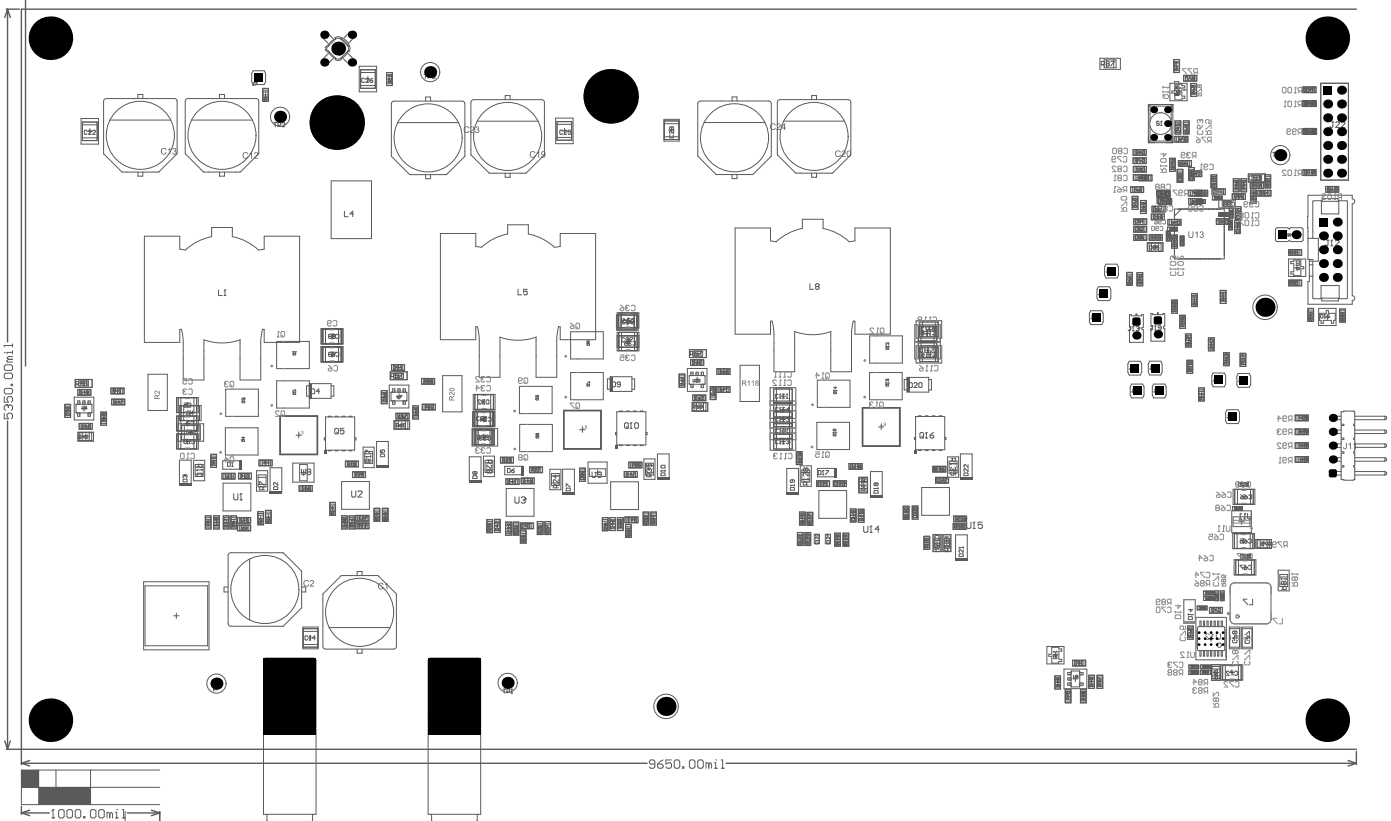
TEXAS INSTRUMENTS

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc
ENGINEER: Sean Xu & Sean Yu
LAYOUT BY: Sean Xu
SCALE: 0.72
ALTIUM DESIGNER VERSION: 22.1.2.22

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: 001
BOARD #: PMP20587 REV: E
LAYER NAME = Signal Layer 1
TID #: PMP20587
PLOT NAME = Signal Layer 1 Assembly Drawing
GENERATED : 12/15/2022 11:10:52 AM
TEXAS INSTRUMENTS

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL
MATERIAL:	
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER	
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER	
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
DRILLING:	
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES	
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER	
BOARD FINISH:	
SILKSCREEN: [X] TOP [X] BOTTOM	
SILKSCREEN COLOR: [X] WHITE [ ] OTHER	
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER	
[X] MATTE [ ] SEMI-GLOSS	
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG	
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER	
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE	
[ ] N.C. ROUTE [X] V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:	
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3	
[X] RoHS [ ] OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: [ ] YES	
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER	

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED

ASSEMBLY VARIANT: 001

LAYER NAME = Bottom

PLOT NAME: Layer 2

BOARD #: PMP20587 :# UNREV

TID #: PMP20587 :# DIT

TEXAS INSTRUMENTS

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PROJECT TITLE: UCD3138 Digital Inverting Buck Boost

DESIGNED FOR: Public Release

FILE NAME: PMP20587_REVE.PcbDoc

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
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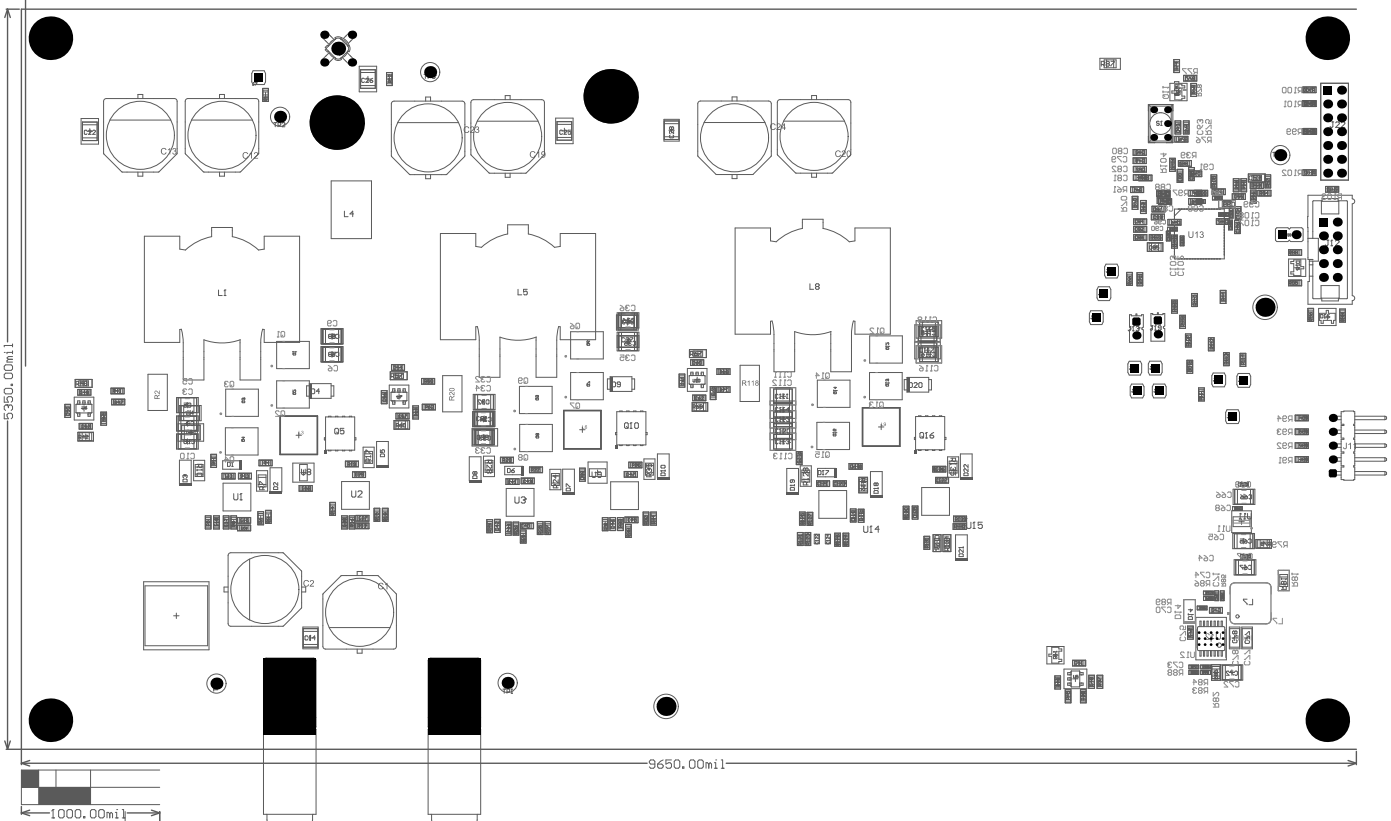
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER [X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE [ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED

LAYER NAME = Bottom

PLOT NAME: Layer 3

TEXAS INSTRUMENTS

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
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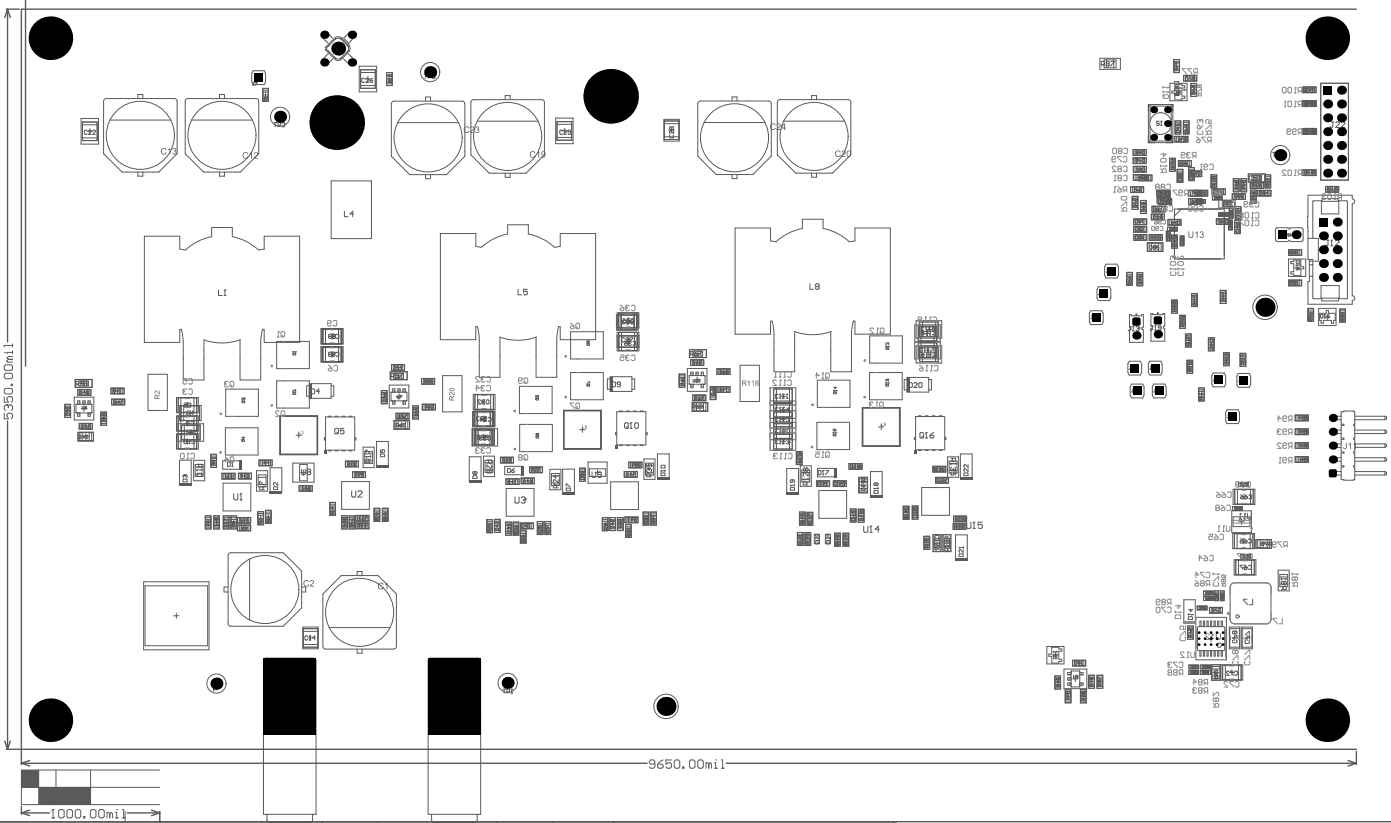
Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER [X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE [ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED

ASSEMBLY VARIANT: 001

LAYER NAME = Assembly Drawing Bottom

PLOT NAME: Assembly Layer 4 GENERATED :: 12/15/2020

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TEXAS INSTRUMENTS

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
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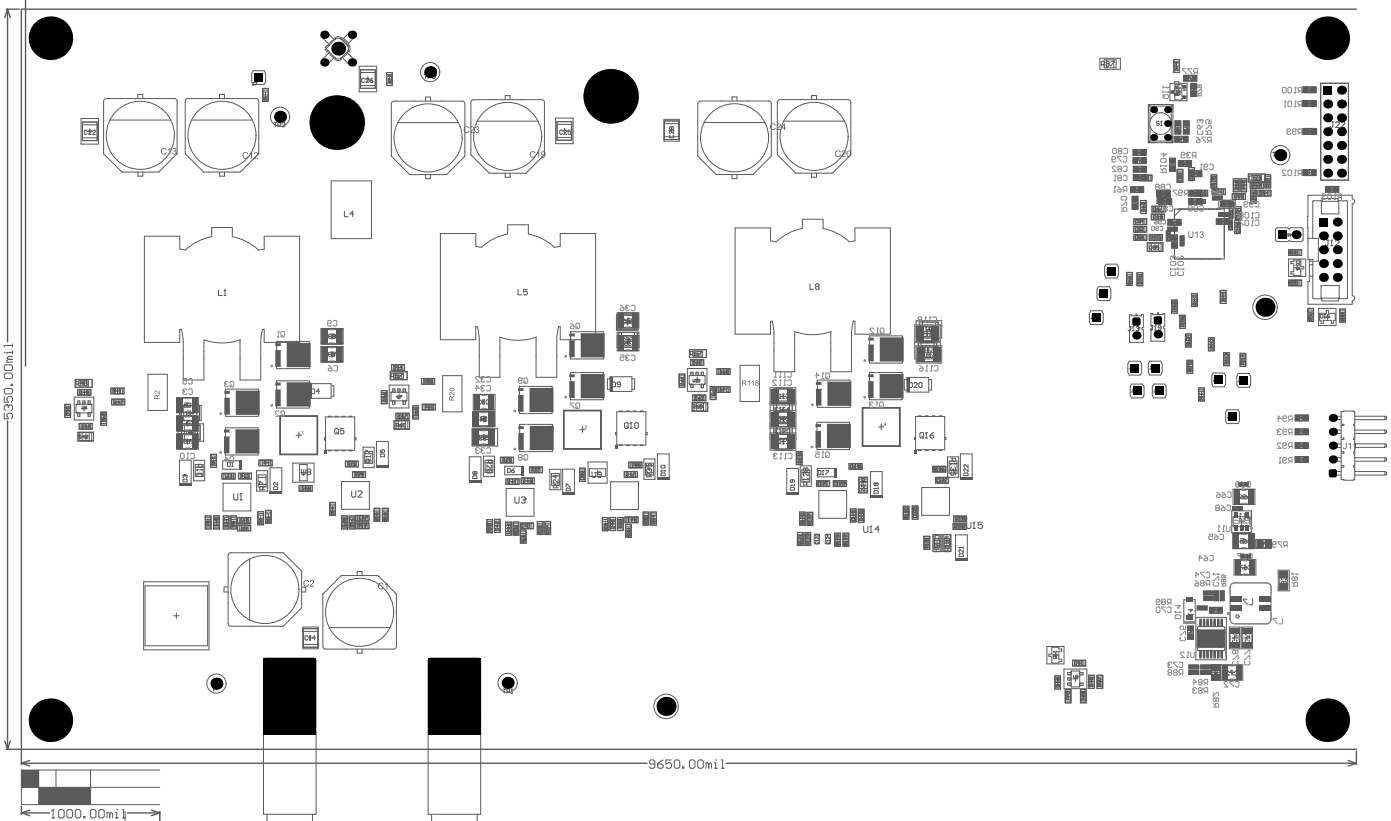
Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL
MATERIAL:	
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER	
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER	
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
DRILLING:	
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES	
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER	
BOARD FINISH:	
SILKSCREEN: [X] TOP [X] BOTTOM	
SILKSCREEN COLOR: [X] WHITE [ ] OTHER	
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER	
[X] MATTE [ ] SEMI-GLOSS	
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG	
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER	
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE	
[ ] N.C. ROUTE [X] V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:	
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3	
[X] RoHS [ ] OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: [ ] YES	
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER	

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: 001

LAYER NAME = Bottom

PLOT NAME: Layer Assembly Drawing GENERATED

TEXAS INSTRUMENTS

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost	
DESIGNED FOR: Public Release	
FILE NAME: PMP20587_REVE.PcbDoc	
ENGINEER: Sean Xu & Sean Yu	LAYOUT BY: Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

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